Applications Places System 12:29 AM

ISE Verilog Simulation - blinker_tb

```
Icarus Verilog + GTKWave driver for Xilinx ISE

Global simulation parameters can be tweaked by editing simulation settings/global_params
```

ISE Project Navigator (M.63c) - /afs/ir.stanford.edu/class/ee108a/groups/18/lab3/lab3.xise - [Design Summary]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Design Overview
Summary

Parser Messages - Errors, Warnings, and Infos

ProjectMgmt:806 - "/afs/ir.stanford.edu/class/ee108a/groups/18/lab3/blinker_
class/ee108a/groups/18/lab3/shifter_
e
ps/18/lab3/blinker_tb.v\" into library
e
ps/18/lab3/shifter_tb.v\" into library
e
ps/18/lab3/timer_tb.v\" into library w

GTKWave - simulation-output/blinker_tb.delgado4.ee108-4a/dump.lx2

File Edit Search Time Markers View Help

From: 0 sec To: 32 ns Marker: -- | Cursor: 5880 ps

SST

blinker_tb

Signals

bs_sim[0]
clk_sim[0]
out_sim[0]
rst_sim[0]

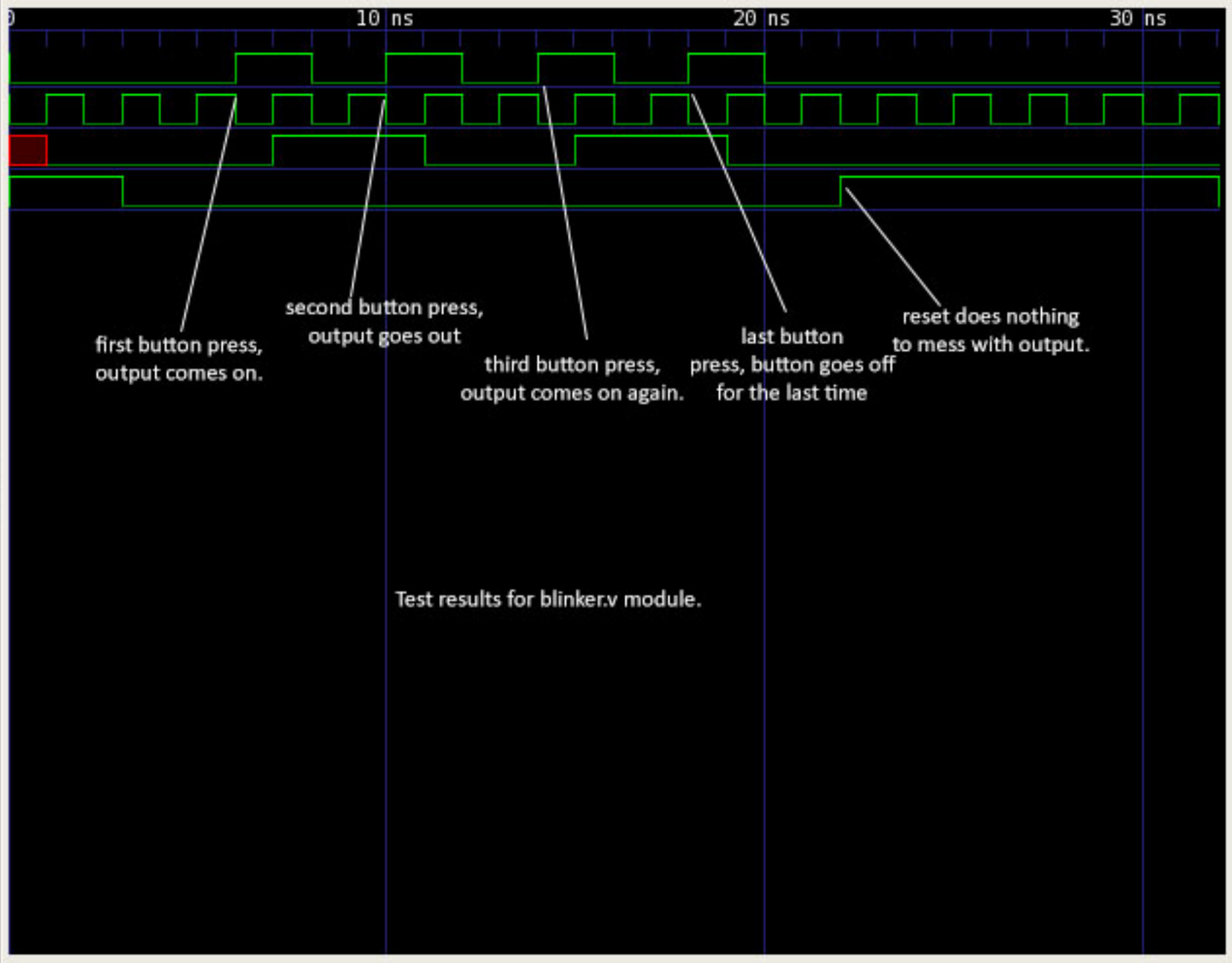
Filter:

Append Insert Replace

Signals

Time
bs_sim[0]
clk_sim[0]
out_sim[0]
rst_sim[0]

Waves




```
ModelSim GUI launched successfully
Process Simulate Behavioral Model setup completed successfully, the GUI will be up in a moment.
```

Console Errors Warnings Find in Files Results

Gnome-ter... ISE Project ... [CCNet - ee... EE108A: Pr... lab3 EE108A: Pr... programm... GTKWave - ... Starting Tak...

Applications Places System 4:34 PM

EE108A: Prelab + Lab 3

File Edit View Go Help

Previous Next 1 of 9 Fit Page Width

Thumbnails

GTKWave - simulation-output/lab3_top_tb.delgado4.rm128-13/dump.lx2

File Edit Search Time Markers View Help

From: 0 sec To: 15566 ns Marker: 150 ns | Cursor: 80 ns

SST

lab3_top_tb
dut
bicycle_fsm
fastBlink
blinker_instanc
shifter_instanc
timer_instanc

Signals

blinkerOut1[0]
blinkerOut2[0]
clk[0]
down_button[0]
heartBeat[0]
left1[0]
left2[0]
mux_output[0]
mux_sel[1:0]

Filter:

Append Insert Replace

Signals

Time
button[0]
clk[0]
leds[7:0]
light[0]
rst[0]
up_select[0]
down_select[0]
shifter_out[6:0]
shifter_out[6:0]
timer_out[0]
mux_sel[1:0]
heartBeat[0]

Waves

10 us

changing shifter countdown values when down/up is pressed

changing blink speed, according to up/down button presses (speed only changes only after current blink cycle)

timer outputs signal high after countdown complete

Waveform output for lab3_top module. Successfully responds according to project specifications.

o NOT

d shifters.
right

up and
ld be able
s, 1/2s or

4

5

These rates are stored independently. For example, you should be able to set Flash 1 to blink twice a second and Flash 2 to blink four times a second, and cycling through the states will not reset those blink rates. The rate control should be independent: pushing the up/down buttons in Flash 1 should only change the flash rate in state Flash 1, and pushing the up/down buttons in Flash 2 should only change the flash rate in state Flash 2.

Project architecture

The top-level module has been provided for you for this lab. Its inputs are up, button,

CCNet - ee10... Terminal ISE Verilog Si... GTKWave - si... Logfile viewer... Downloads EE108A: Prela... Starting Take ...

Applications Places System 3:29 PM

ISE Verilog Simulation - programmable_blinker_tb

ISE Verilog Simulation - programmable_blinker_tb

```
secs   794, out 1
secs   795, out 1
```

03:02 PM

...3.xise - [Design Summary]

GTKWave - simulation-output/programmable_blinker_tb.delgado4.rm128-13/dump.lx2

File Edit Search Time Markers View Help

From: 0 sec To: 6493 ns Marker: -- | Cursor: 50 ns

SST

programmable_blinker_tb

Signals

clk_sim[0]
fast_sim[0]
out_sim[0]
rst_sim[0]
secs[15:0]
sl_sim[0]
sr_sim[0]

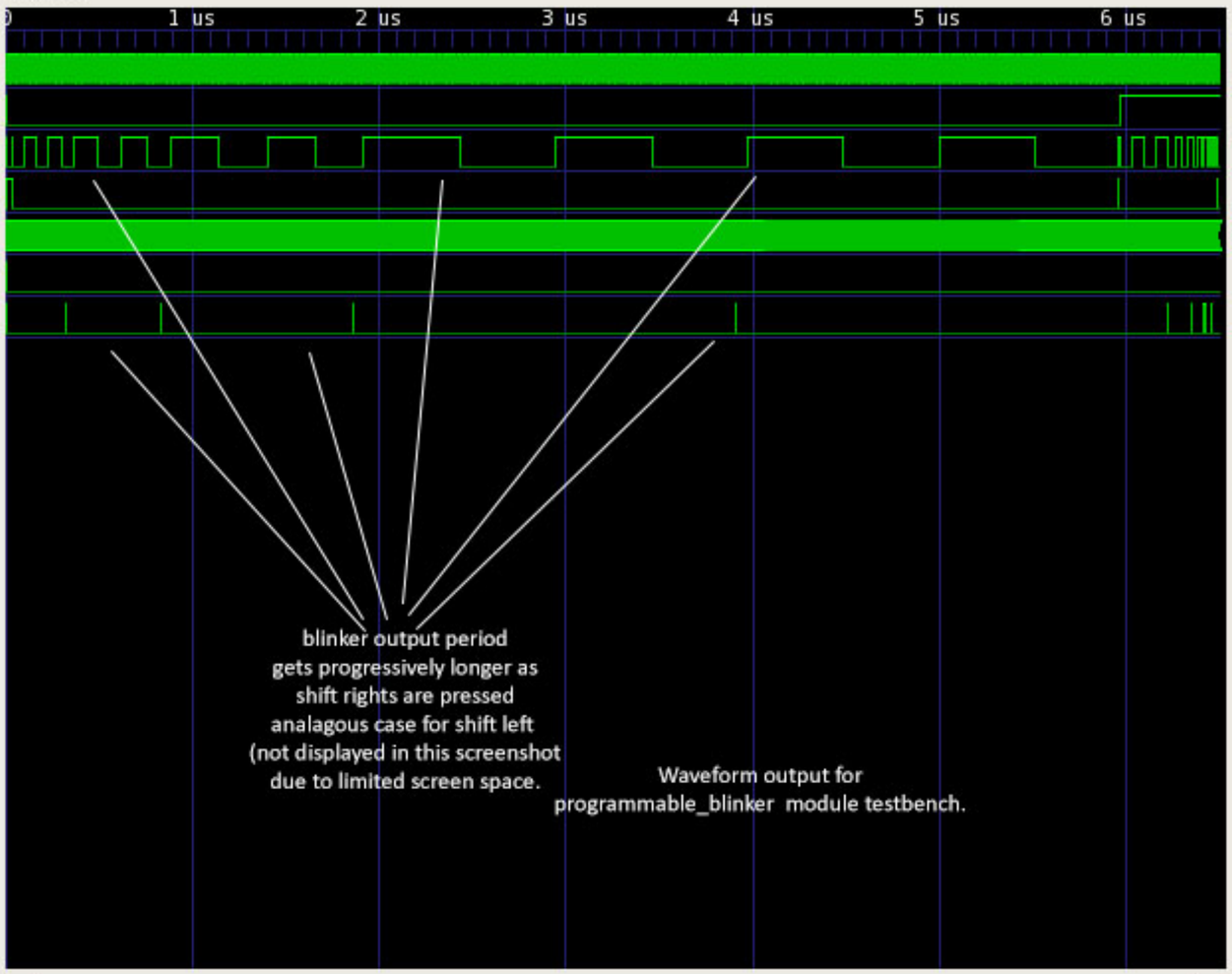
Filter:

Append Insert Replace

Signals

Time
clk_sim[0]
fast_sim[0]
out_sim[0]
rst_sim[0]
secs[15:0]
sl_sim[0]
sr_sim[0]

Waves



tus	
ors:	No Errors
tation State:	New
s:	
ings:	
ing Results:	
g Constraints:	
Timing Score:	

s	Warnings	Infos

[-]

Generated

Console

```
INFO: Automatic do files created successfully.

Launching Modelsim GUI...
Modelsim GUI launched successfully
Process Simulate Behavioral Model setup completed successfully, the GUI will be up in a moment.
```

Console Errors Warnings Find in Files Results

[ee108a -... Downloads Terminal ISE Projec... ISE Verilo... program... ISE Verilo... GTKWave... Logfile vi... Starting T...

Applications Places System 3:30 PM

ISE Verilog Simulation - programmable_blinker_tb

ISE Verilog Simulation - shifter_tb

Icarus Verilog + GTKWave driver for Xilinx ISE

03:02 PM

3.xise - [Design Summary]

GTKWave - simulation-output/shifter_tb.delgado4.rm128-13/dump.lx2

File Edit Search Time Markers View Help

From: 0 sec To: 207 ns Marker: -- | Cursor: 3700 ps

SST

shifter_tb

Signals

clk_sim[0]
fast_sim[0]
out_sim[6:0]
rst_sim[0]
sl_sim[0]
sr_sim[0]

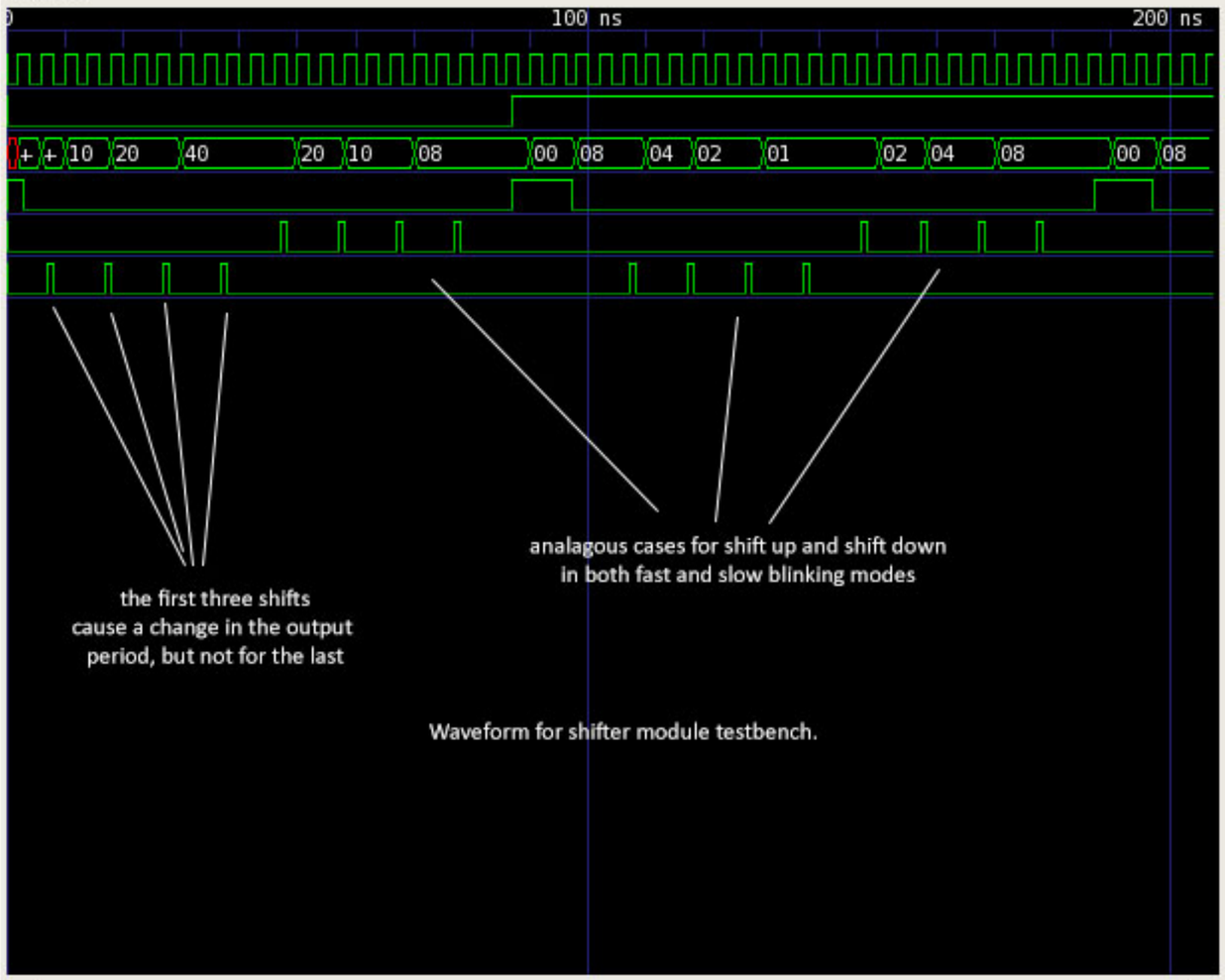
Filter:

Append Insert Replace

Signals

Time
clk_sim[0]
fast_sim[0]
out_sim[6:0]
rst_sim[0]
sl_sim[0]
sr_sim[0]

Waves



tus

rs:	No Errors
tation State:	New
s:	
ings:	
ing Results:	
g Constraints:	
Timing Score:	

[-]

s	Warnings	Infos

[-]

Generated

Start Design Files Design Summary

Console

INFO: Automatic do files created successfully.

Launching Modelsim GUI...
Modelsim GUI launched successfully
Process Simulate Behavioral Model setup completed successfully, the GUI will be up in a moment.

Console Errors Warnings Find in Files Results

[ee108a -... Downloads Terminal ISE Projec... ISE Verilo... program... ISE Verilo... GTKWave... Logfile vi... Starting T...

GTKWave - simulation-output/timer_tb.delgado4.ee108-4a/dump.lx2

File Edit Search Time Markers View Help

From: 0 sec To: 2356 ns Marker: 2356 ns | Cursor: 2145 ns

SST

timer_tb

Signals

clk_sim[0]
count_en_sim[0]
load_value_sim[8:0]
out_sim[0]
rst_sim[0]

Filter:

Append Insert Replace

Signals

Time
clk_sim[0] =0
count_en_sim[0] =0
load_value_sim[8:0] =100
out_sim[0] =1
rst_sim[0] =0

Waves

1 us 2 us

0+ 0+ 040 080 100

counting down from differing load_values, starting from the smallest, 4, then increasing corresponing to each increase in flashing period. A "1" signal is output when count-down is complete, and when countdown begins (reset signal). The waveform shows what we expect to see, with countdown times taking an increasing amount of time to com-plete.

Test results for the timer.v module.