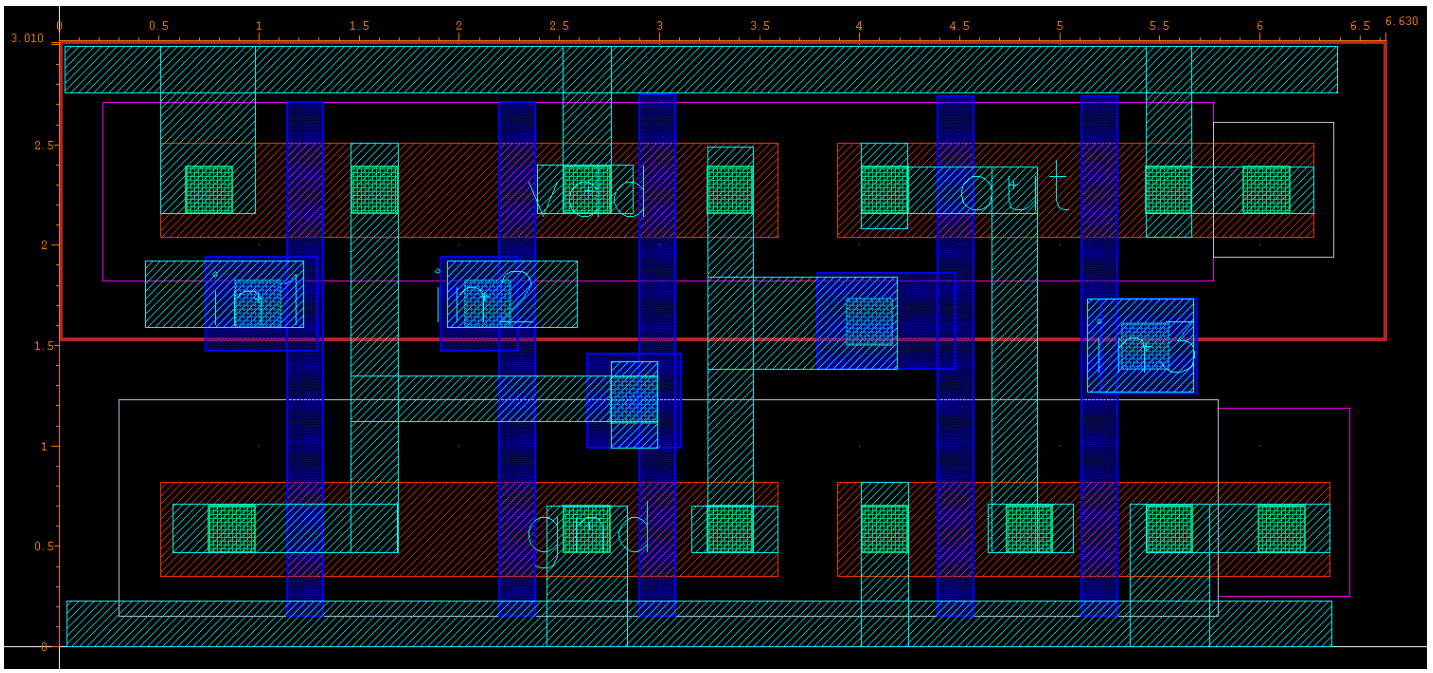
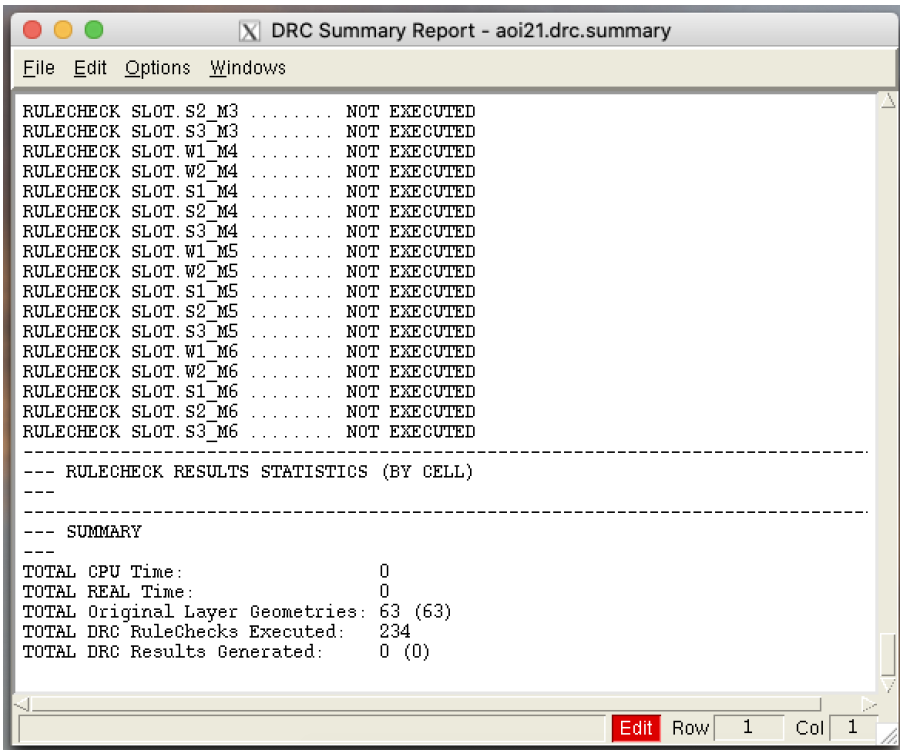
ID: 108042019
Name: 鄭佳凌

1. **Layout with rulers**

   area = 6.63μm*3.01μm = 19.9563 (μm)^2



2. **DRC summary report**



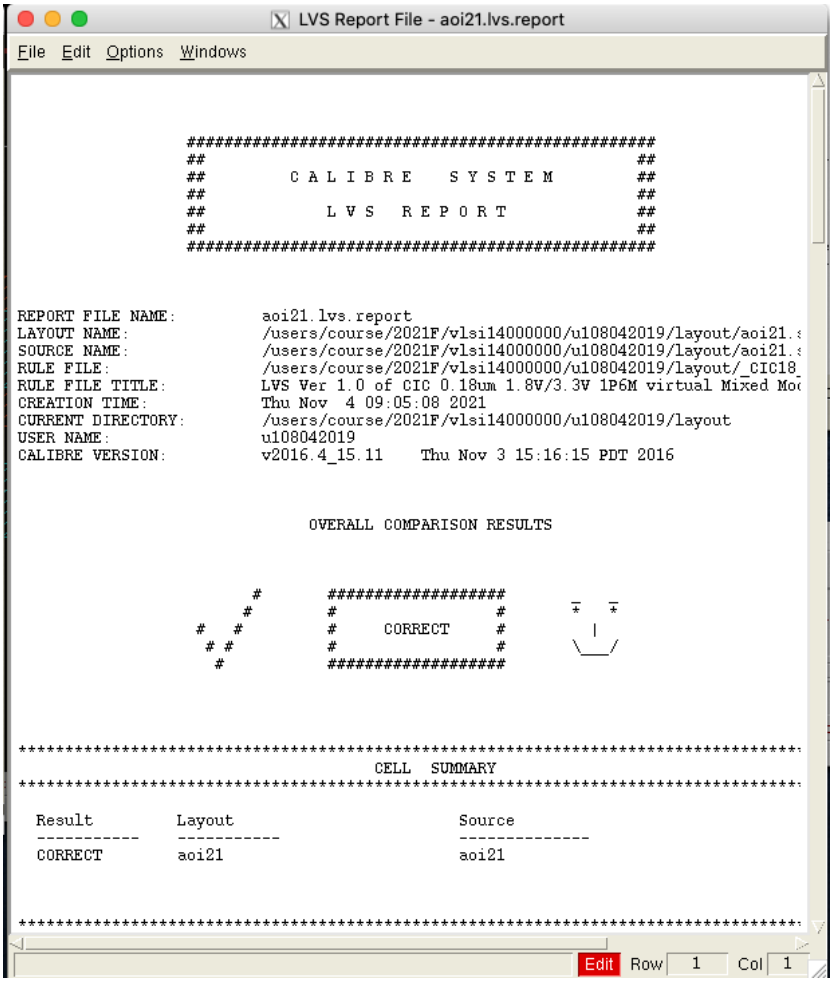
DRC Summary Report - aoi21.drc.summary

File Edit Options Windows

```
RULECHECK SLOT.S2_M3 ........ NOT EXECUTED
RULECHECK SLOT.S3_M3 ........ NOT EXECUTED
RULECHECK SLOT.W1_M4 ........ NOT EXECUTED
RULECHECK SLOT.W2_M4 ........ NOT EXECUTED
RULECHECK SLOT.S1_M4 ........ NOT EXECUTED
RULECHECK SLOT.S2_M4 ........ NOT EXECUTED
RULECHECK SLOT.S3_M4 ........ NOT EXECUTED
RULECHECK SLOT.W1_M5 ........ NOT EXECUTED
RULECHECK SLOT.W2_M5 ........ NOT EXECUTED
RULECHECK SLOT.S1_M5 ........ NOT EXECUTED
RULECHECK SLOT.S2_M5 ........ NOT EXECUTED
RULECHECK SLOT.S3_M5 ........ NOT EXECUTED
RULECHECK SLOT.W1_M6 ........ NOT EXECUTED
RULECHECK SLOT.W2_M6 ........ NOT EXECUTED
RULECHECK SLOT.S1_M6 ........ NOT EXECUTED
RULECHECK SLOT.S2_M6 ........ NOT EXECUTED
RULECHECK SLOT.S3_M6 ........ NOT EXECUTED
--------------------------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
--------------------------------------------------------------------------------
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 63 (63)
TOTAL DRC RuleChecks Executed:   234
TOTAL DRC Results Generated:     0 (0)
```

Edit Row 1 Col 1

3. LVS correct

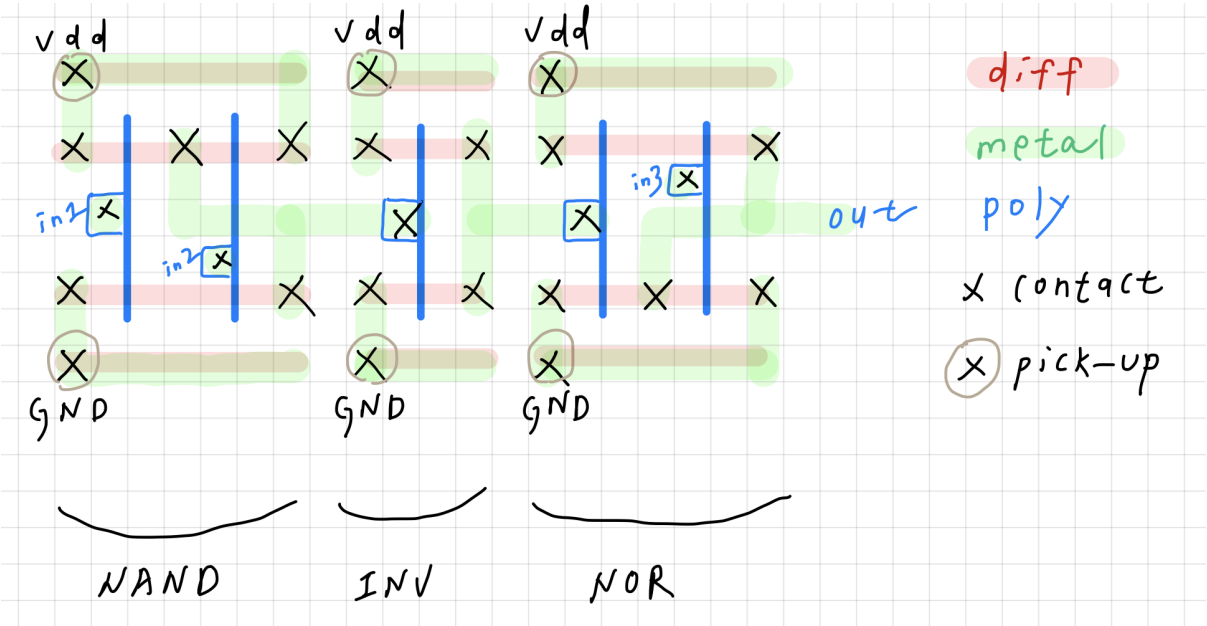


4. LVS schematic

mp : pmos, mn : nmos
inv : inverter
nand : nand gate
nor : nor gate
+r : the right one

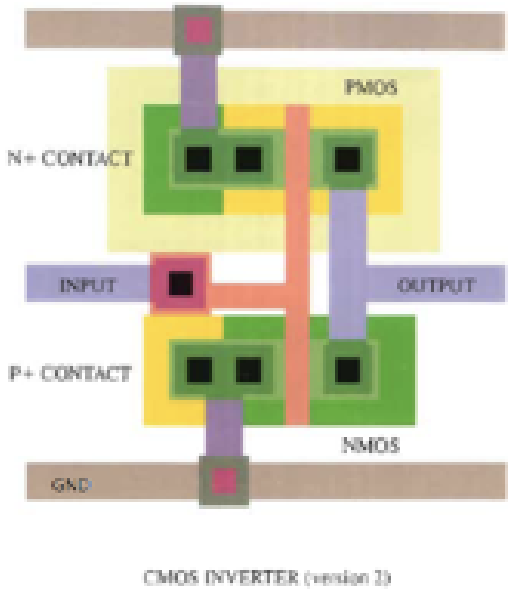
5. What did I did to enhance layout quality?

(1) Use stick diagrams to make cell placing and routing exploration.
Stick diagram as followed:
Version 0 (no optimization)

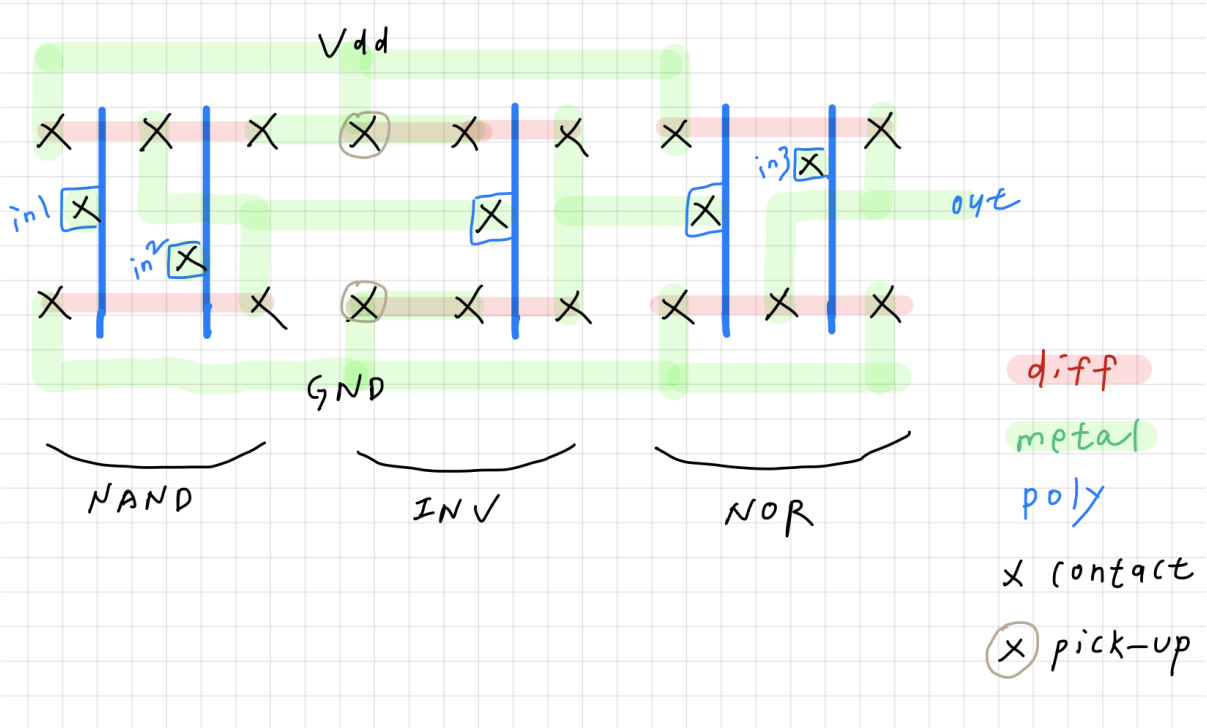


Version1 (optimize by re-locate pick-up)

Referenced from Textbook[1] and NTUT slide[2], the pick-up of both MOS in an inverter gate can be relocated. As a result, the inverter's pick-up can be relocated, and NAND's, NOR's pick-up can share the same power source.

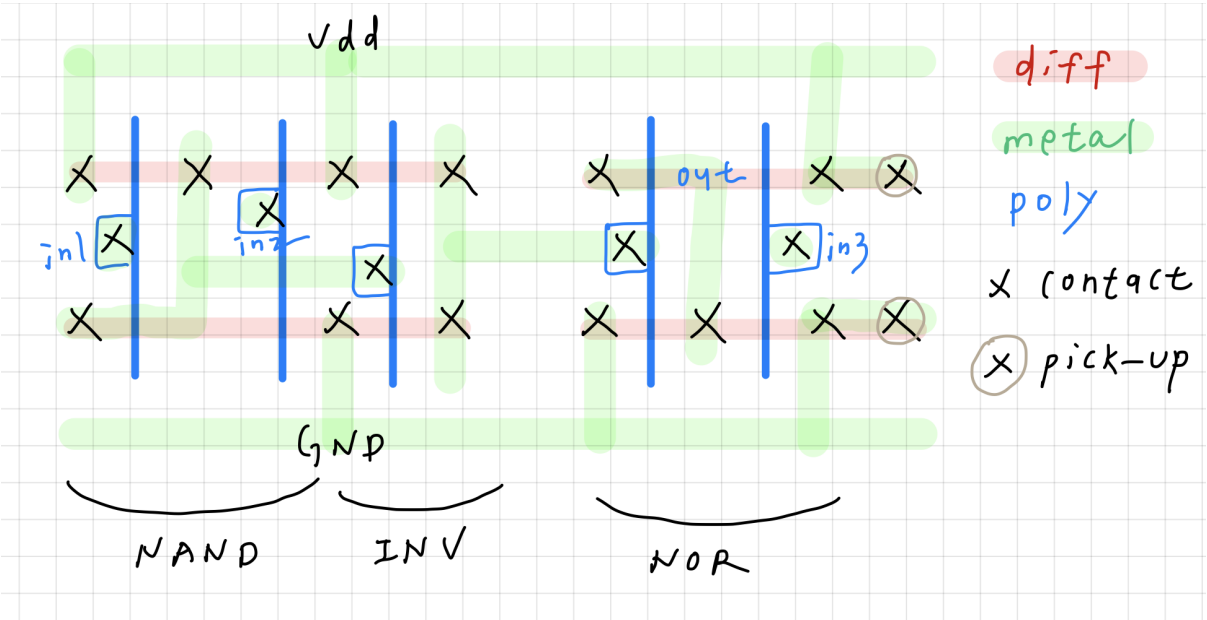


[1] CMOS Digital Integrated Circuits Analysis and Design, 4th analysis and design (Sung-Mo Kang) 2015
[2] https://myweb.ntut.edu.tw/~dkao/chap03.pdf p.18



(2) Version2 (optimize by sharing source with adjacent cell, and re-locate the pick-up)
Sharing source between NAND and inverter, and horizontally flip the output to satisfy the design. For pick-up, move them to the right most side because it can be shared by all of the gates. As for the NOR, horizontally flip the output.

This design needs to be handled very carefully because it includes a lot of rules. Especially around contact of every input/output contact. Since each contact would require metal and poly, the rules would be especially tight. Such as diff-poly clearance, metal-metal minimum width, contact-poly minimum extension, contact-metal minimum extension, and so on. Thus, each contact for IO should be separated.



(3) follow DRC

Run DRC frequently in order to check rules between each object. After seeing more rules, it is easier for me to decide the layout that can pass DRC and compact at the same time.

6. What I've learned & problems I've met

(1) my project progress

First, practice drawing an inverter introduced in course slides. During the practice, I tried the flow of layout and DRC/LVS. Since I want to know what information I can get from DRC, I frequently run DRC after I draw one or two objects. From the DRC report, I learned many of the design rules, which would eventually help me reduce my layout area. From LVS, I learned the real meaning of width on one MOS that I write in the schematic.

Second, I draw my second version of inverter, which reduces width by pick-up. By implementing this version, the width of MOS design can be smaller than before. Then I add NAND gate and NOR gate beside the inverter gate. However, rather than putting an poly-to-metal contact for every input, I use poly text to label inputs.

Third, I found out that the contacts between NAND and INVERTER gate can be shared. To implement this, the design of NAND itself needs to be modified. Also, the pick-ups can be moved to the right most, and the NOR would also need some modification. More importantly, I would need to fix my "input poly-to-metal contact" problem mentioned before. After the modification, the design of all MOS's width is almost fixed.

(2) problems

- I've met all the problems mentioned in the slides: Lock, LVS cell name difference, schematic MOS width & layout MOS width difference and thus occurs LVS property errors.
- Silly problems: wrong layer of label
- Virtuoso tool doesn't work properly ,X11 disconnect (then I would re-log in to the workstation until it works well)
- Reading DRC report : I understood the meaning of terms such as "space", "clearance", "extension".
- I was wondering how can I do to avoid repeating works of drawing one cell : we can create several cell and instance them (but I didn't use it in final layout)