1. Design Topic

Follow the same concept, please design a multi-modulus frequency divider with total 4 modes operation (÷16/17/18/19)

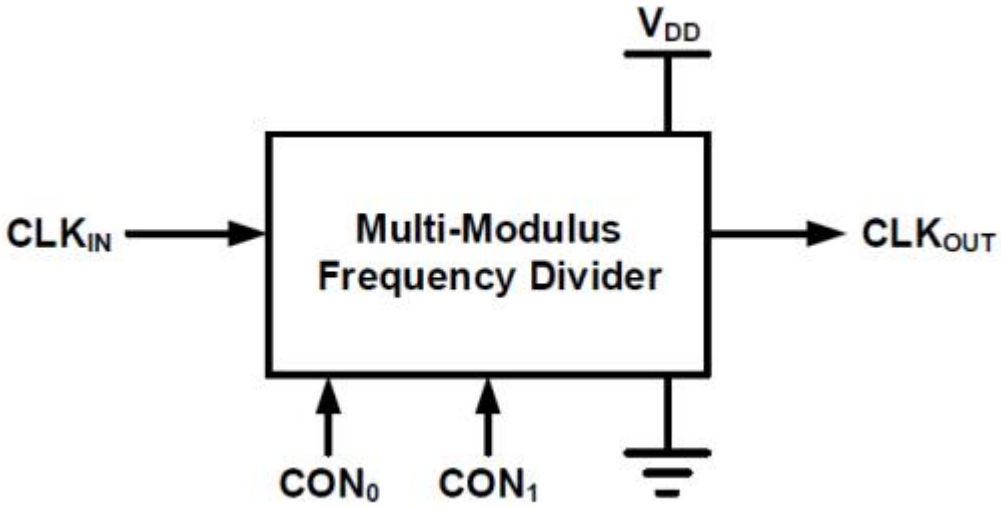

Fig. 1. The I/O description of the targeted design

2. Report

I. Block Diagram

(1) Draw top view of your system design and explain why you choose this architecture and how your design operated.

電路設計的想法:

首先，題目要求四種模式的除頻器，一開始的想法是分別設計四種(÷16/17/18/19)不同的除頻器電路，因此會需要解碼器來選擇指定的模式，最後需要多工器選擇要輸出的訊號。接下來我們發現÷16/17 可以使用簡單的邏輯閘整合成一個電路，所以建構出下一頁圖二的方塊圖。

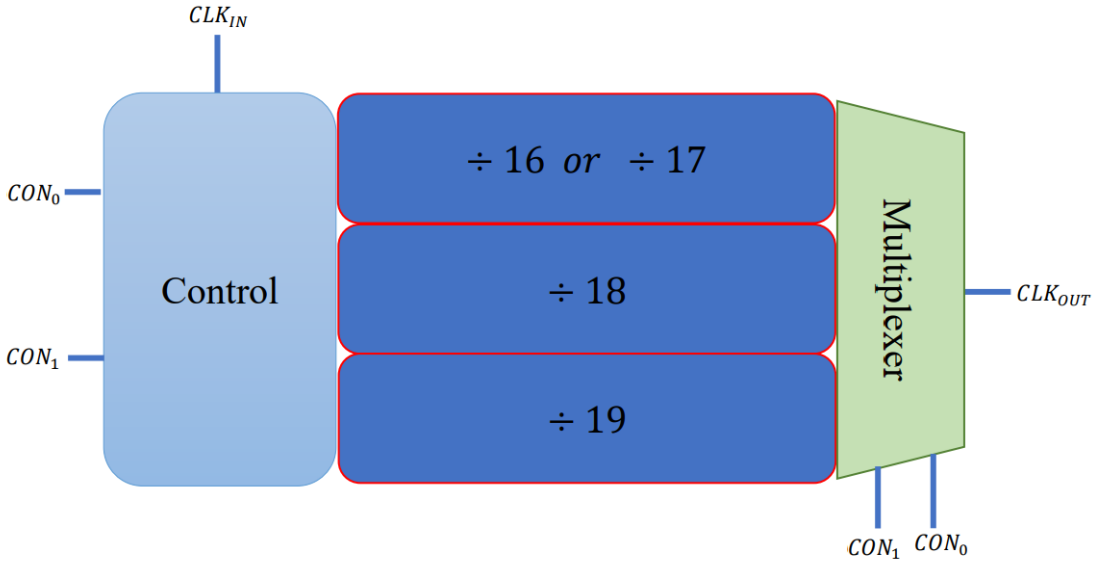

Fig. 2. Block diagram of our design

我們希望的運作方式如下，上圖左方的控制電路負責決定時脈的訊號要送到哪一個除頻器中，接著當除頻器啟動後，上圖的右方有一個多工器負責將除頻後的訊號送到輸出端。在一開始的設計中並沒有放入多工器，而是使用OR(NOR＋NOT)閘來實現，然而在HSPICE上的模擬結果並不符合我的預期，輸出端只有在÷19這個模式是正常運作，其餘的模式都沒有訊號，我認為是不同的輸出訊號互相干擾導致最後在輸出端的訊號不正確。

Table 1.

Control Signals		Mode
CON_1	CON_0	
0 V	0 V	÷16
0 V	1.8 V	÷17
1.8 V	0 V	÷18
1.8 V	1.8 V	÷19

(2) Draw sub-block in gate level and transistor level hierarchical and explain why you use them.

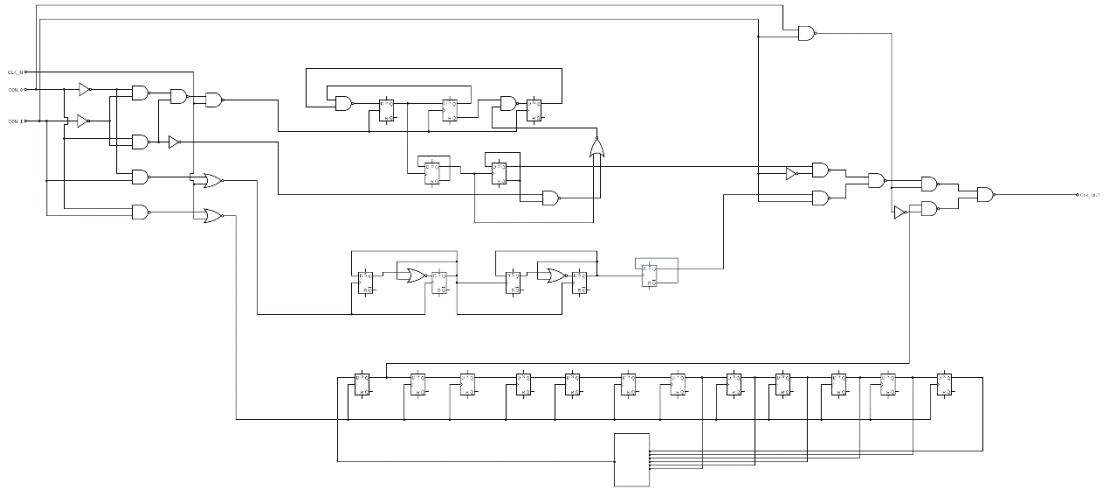

Fig. 3. Logic level circuit diagram of our design

Fig. 4. Transistor level circuit diagram of our design

電路運作方式解釋:

1. Divide by 16/17 frequency divider

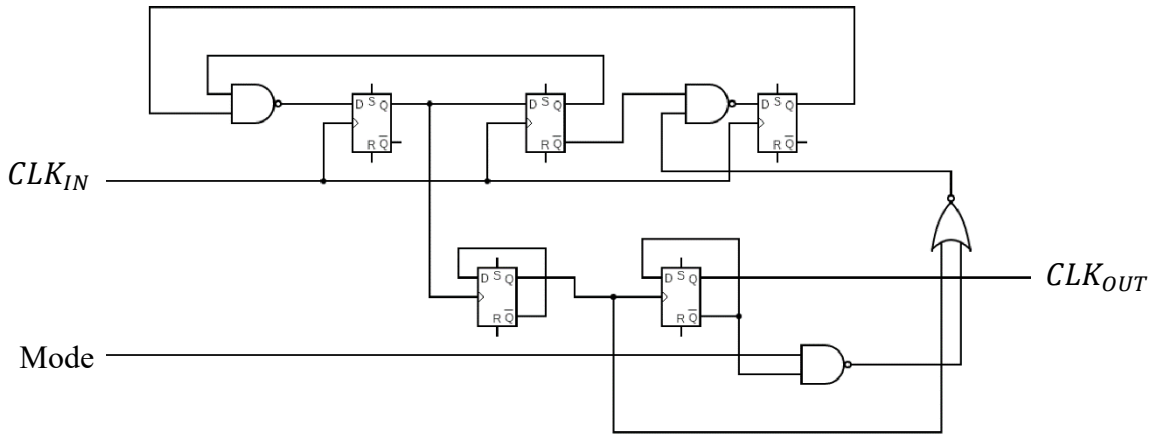

Fig. 5. Logic level circuit diagram of $\div 16/17$

上圖的電路是基於除 16 的電路作改良的雙模式除頻器，當 Mode 為 1 時，電路會將輸入訊號頻率除以 17，若 Mode 為 0 時，電路則會將輸入訊號頻率除以 16。

2. Divide by 18 frequency divider

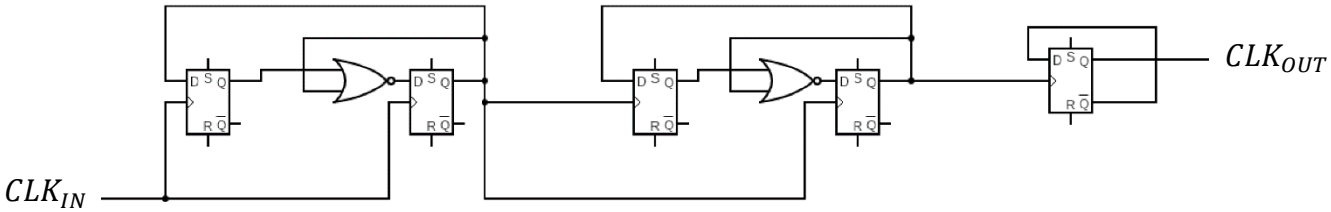

Fig. 6. Logic level circuit diagram of $\div 18$

上圖為個除 3 的電路相連最後再接上除 2 的電路，得到的就是除 18 的除頻器。

3. Divide by 19 frequency divider

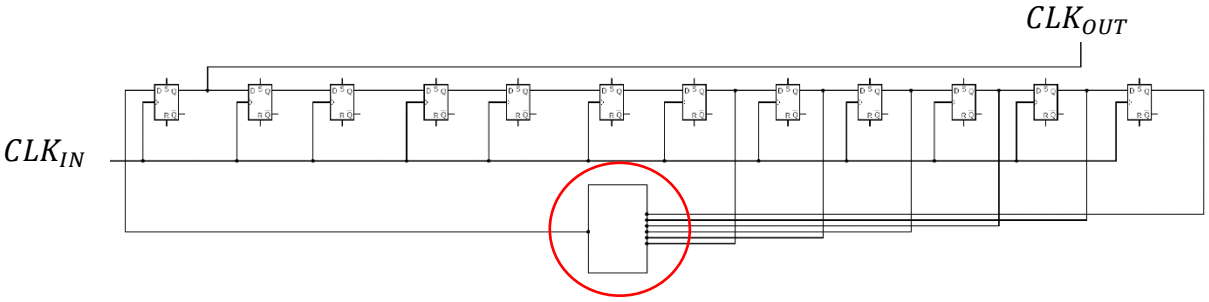

Fig. 7. Logic level circuit diagram of ÷ 19

上圖的電路架構是基於移位紀錄器(Shift Register)所設計的除 19 模式的電路。其中紅圈處的方框是一個 6 輸入的 NOR 閘，這是四個模式中最難設計的部分。

4. Control Block & Multiplexer

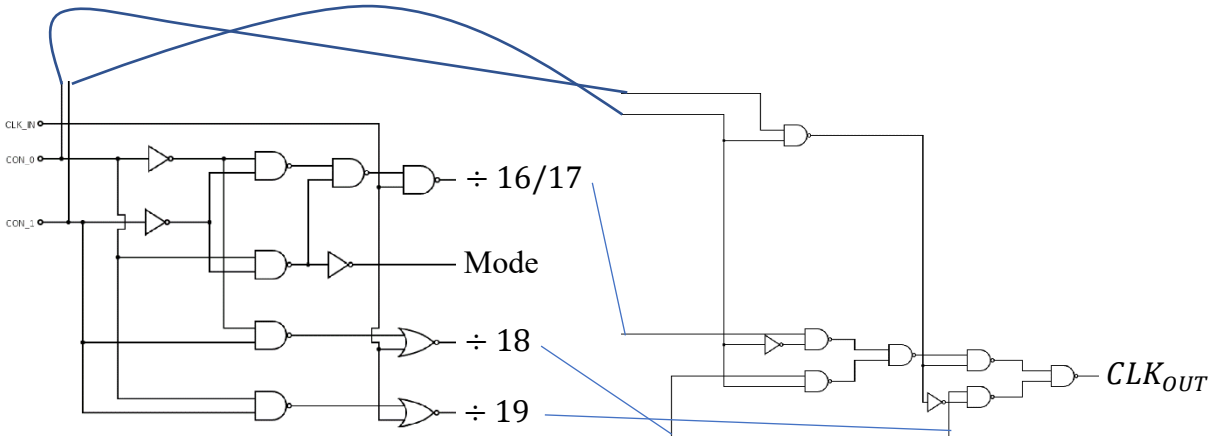

Fig. 8. Logic level circuit diagram of control block and multiplexer

上圖左方的電路是由 Decoder 加上一些邏輯閘所構成的控制電路，目的是讓不同的控制訊號選擇讓 CLK 啟動指定的電路。總共有 4 個模式，所以我使用的是 2-to-4 decoder。上圖右方的電路是個 3-to-1 multiplexer 由控制訊號CON_0、CON_1來選取要輸出的訊號。這個多工器是使用 2 個 2-to-1 multiplexer 來實現 3 選 1 的功能，並且在實作上比 4 選 1 的多工器更容易也更節省面積。

II. Layout

(1) Print-screen the whole design (with size & area) and sub-blocks.

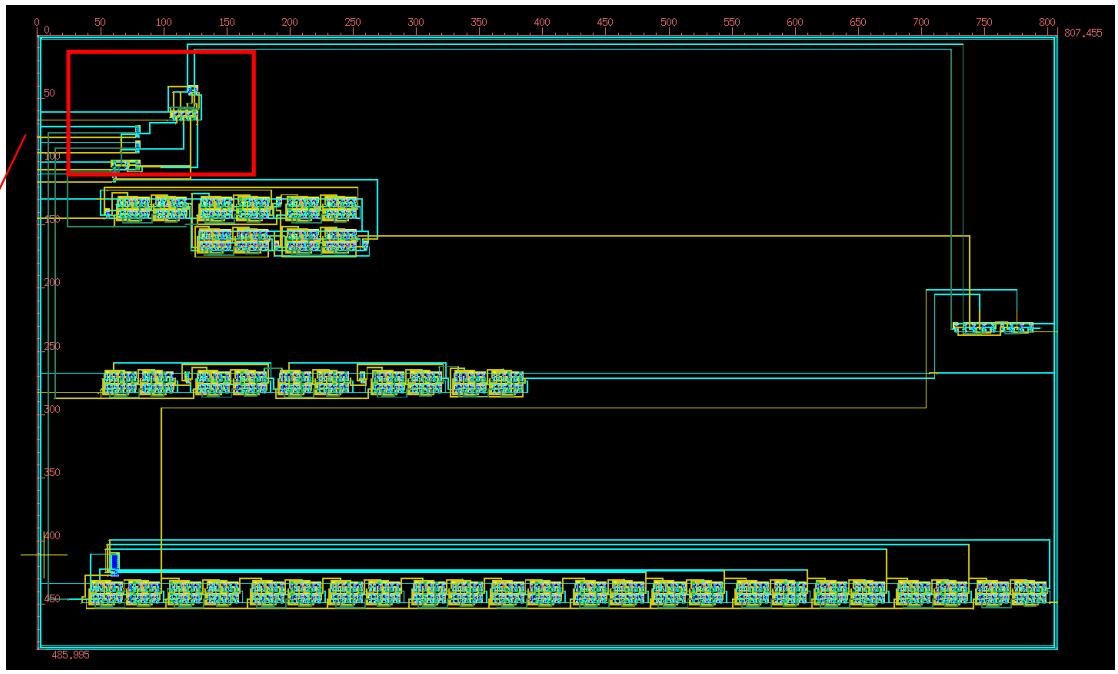

Fig. 9. Layout of the full circuit

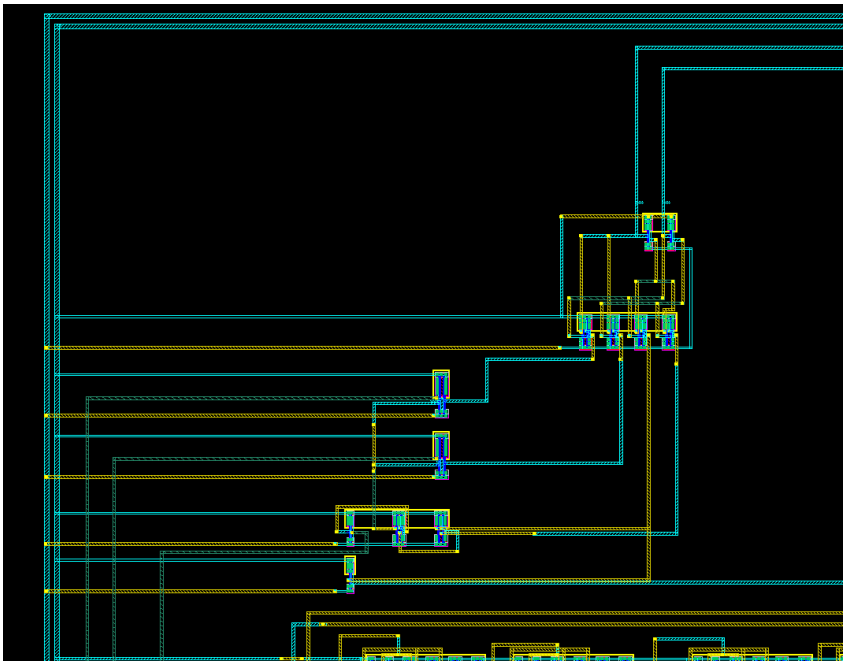

Fig. 10. Layout of the control block

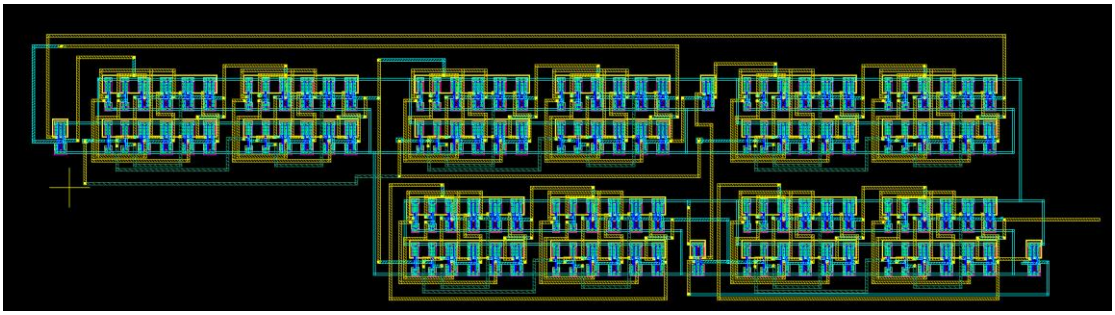

Fig. 11. Layout of the $\div 16/17$ frequency divider

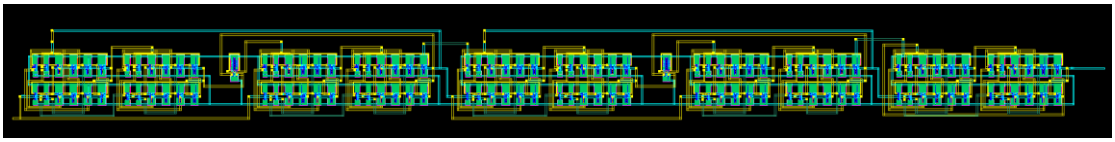

Fig. 12. Layout of the $\div 18$ frequency divider

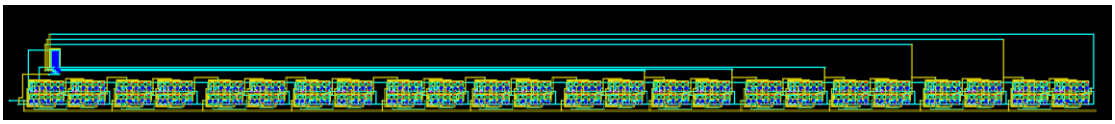

Fig. 13. Layout of the $\div 19$ frequency divider

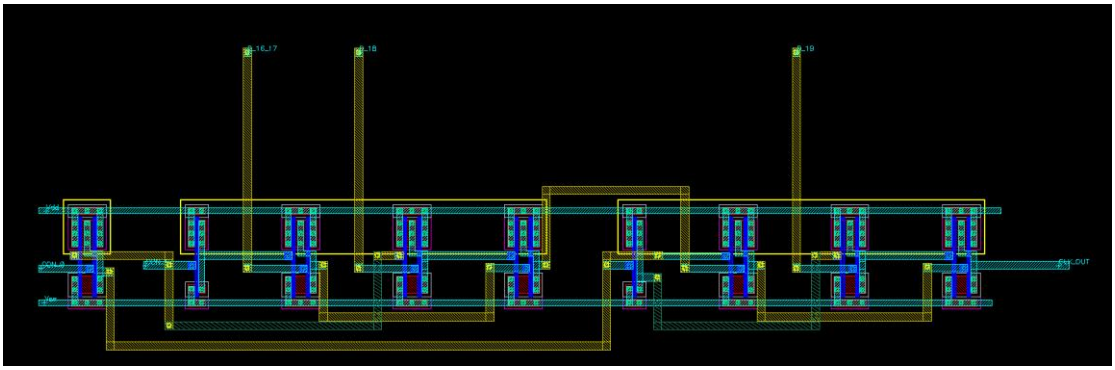

Fig. 14. Layout of the 3-to-1 multiplexer

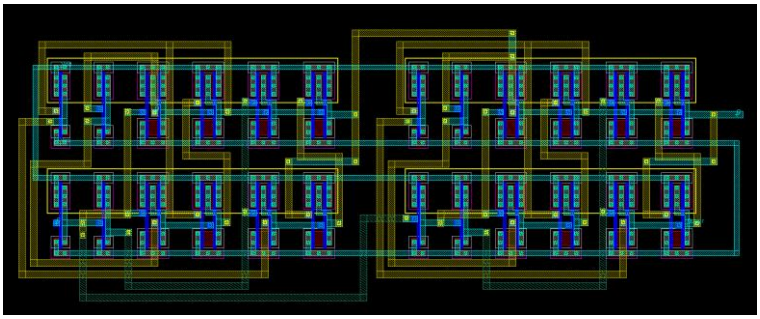

Fig. 15. Layout of the D type flip-flop

(2) DRC summary with no error (excluding the optional rules).

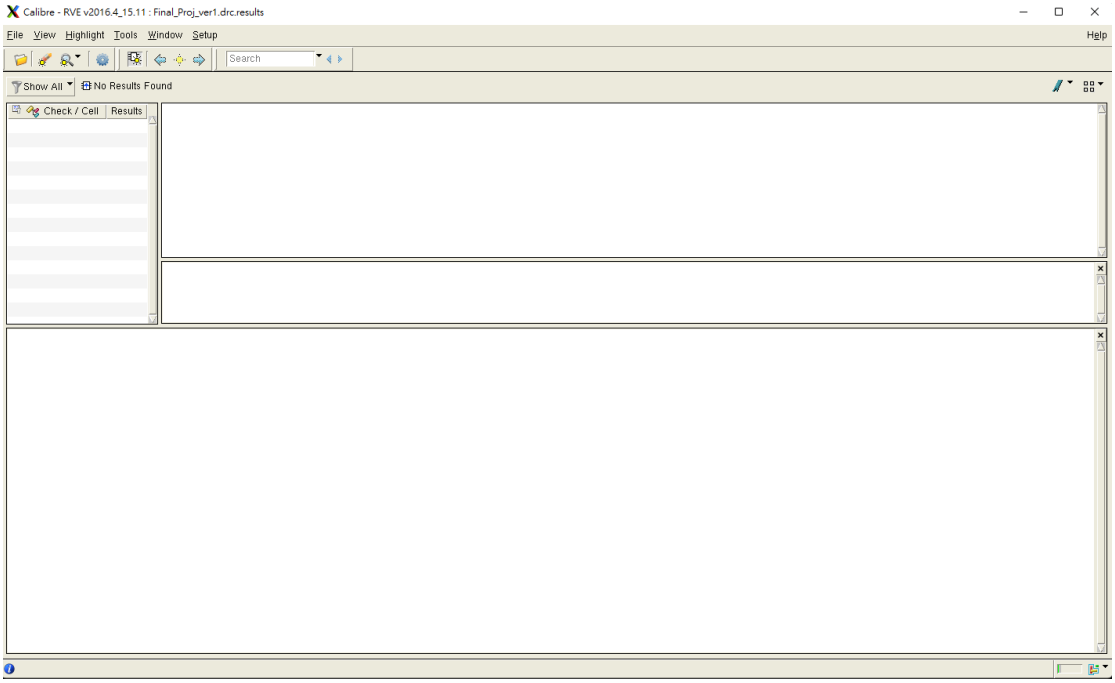

Fig. 16. DRC result (All violation is cleared)

(3) LVS report.

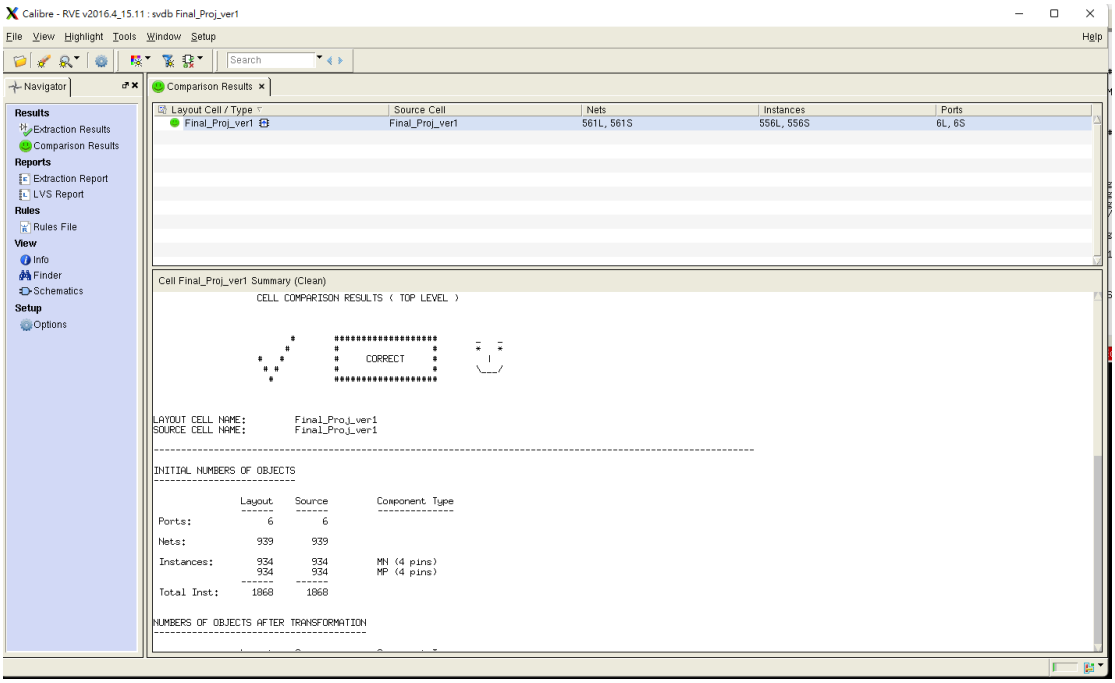

Fig. 17. LVS report

III. Simulation Results

(1) Pre-sim results & post-sim results, need to compare and explain the difference between them.

Corner specification: TT @25℃

◆ Divide by 16 simulation results ($f = 100\ MHz$)

Fig. 18. Pre-sim waveform

Fig. 19. Post-sim waveform

◆ Divide by 17 simulation results ($f = 100\ MHz$)

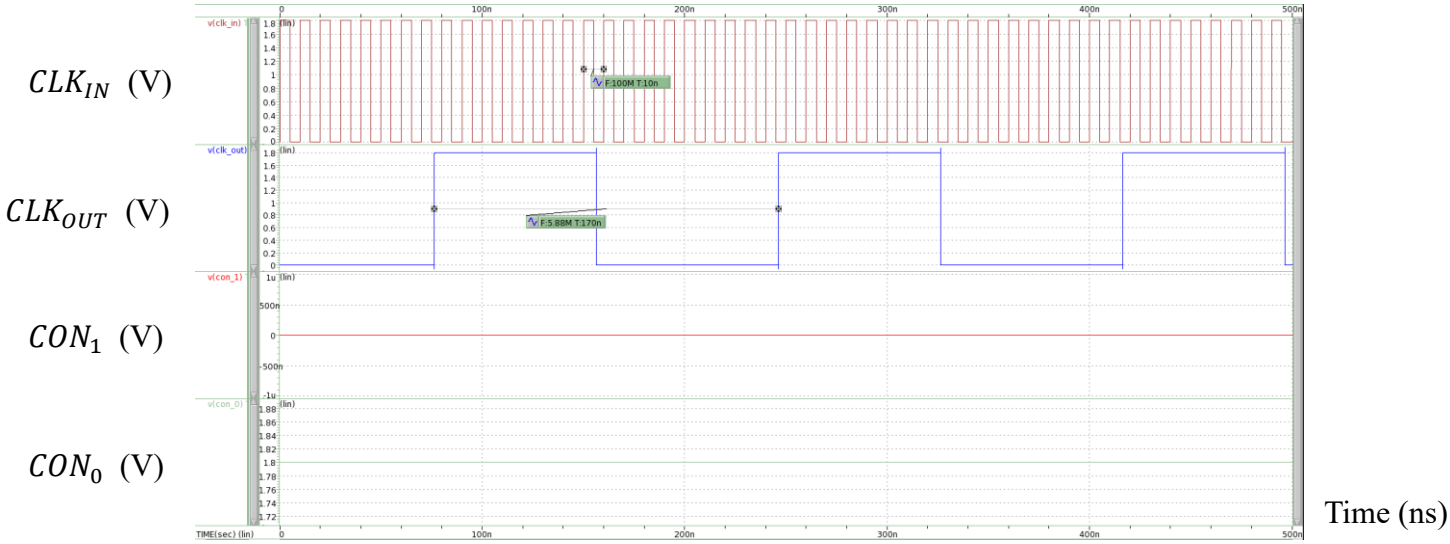

Fig. 20. Pre-sim waveform

Fig. 21. Post-sim waveform

◆ Divide by 18 simulation results ($f = 100\ MHz$)

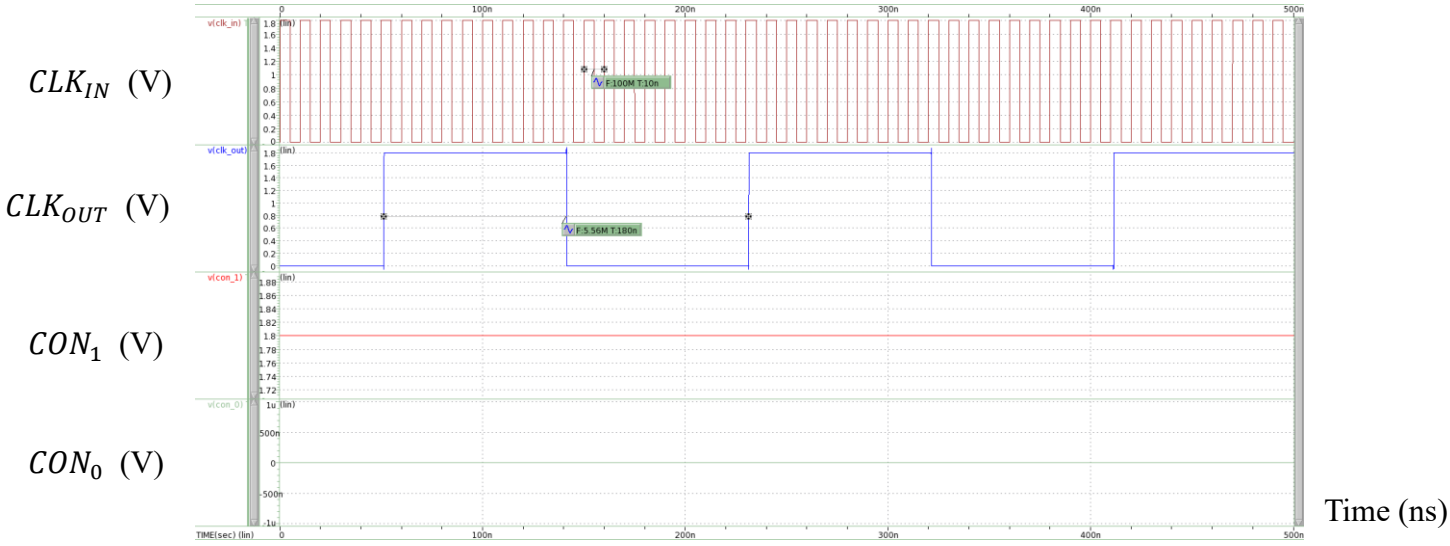

Fig. 22. Pre-sim waveform

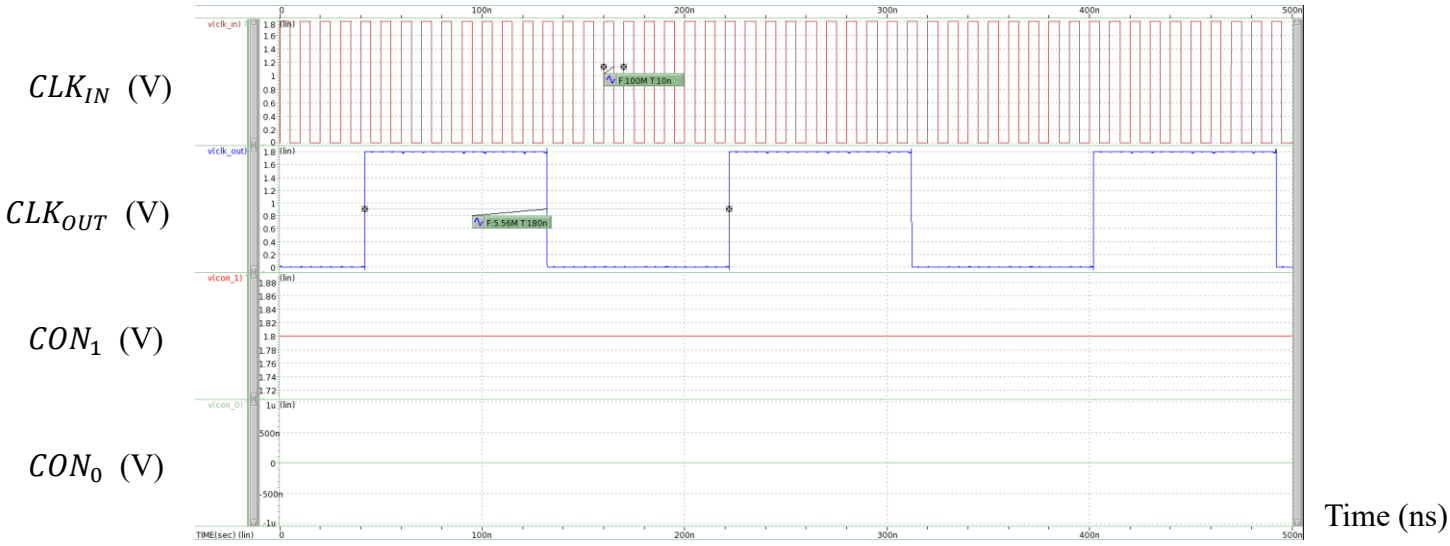

Fig. 23. Post-sim waveform

◆ Divide by 19 simulation results ($f = 100\ MHz$)

Fig. 24. Pre-sim waveform

Fig. 25. Post-sim waveform

Discussion:

在輸入時脈為 100MHz 的條件下，電路的運作皆為正確，在四種模式下的前模擬與後模擬的功能都正常，波形圖只顯示 TT corner 的模擬結果。另外可以在後模擬的波形圖中觀察到電位維持在 0 或 1.8 伏特時會有微小的波動，這是因為 Layout 中的寄生電阻電容造成 RC 充放電，所以才會有類似鋸齒狀的輸出波形。

(2) Waveforms (cursor is needed) and tables (filled with measured data) for all modulus modes.

Table 2.

Pre-Sim						
Corner	Temp. (℃)	f_{max} (MHz)	Power Consumption (mW)			
			÷ 16	÷ 17	÷ 18	÷ 19
TT	25	500	1.236	1.239	1.195	3.425
SS	125	151.15	0.552	0.531	0.533	1.327
FF	-40	500	1.279	1.286	1.252	3.511
SF	25	250	0.75	0.751	0.715	1.968
FS	25	333	0.811	0.829	0.797	2.317

Table 3.

Post-Sim								
Corner	Temp. (℃)	f_{max} (MHz)	Power Consumption (mW)				Area (mm^2)	FoM ($\frac{GHz}{W \cdot \mu m^2}$)
			÷ 16	÷ 17	÷ 18	÷ 19		
TT	25	250	0.729	0.736	0.719	2.019	0.39	0.00015
SS	125	100	0.35	0.353	0.35	0.994		
FF	-40	250	0.719	0.727	0.716	2.092		
SF	25	151.15	0.51	0.514	0.508	1.383		
FS	25	200	0.591	0.597	0.579	1.679		

Discussion:

模擬結果顯示此電路在所有的 corner 下皆能正常運作，但能正常運作的最高頻率(f_{max})會不太一樣。從表格中可知，TT corner 和 FF corner 的運作頻率都是比較高的，運作頻率最低的為 SS corner，那是因為 SS corner 的 carrier mobility 是最低的，溫度是最高的，溫度高會讓元件的運作頻率下降，影響電路的最高運作頻率。在整個模擬的過程中，我發現÷19模式的電路會是所有電路的運作速度之瓶頸，只要÷19的電路運作正常，其他模式都能夠正常運作，因此只要測試÷19模式的輸入時脈極限，就可以知道整個電路的輸入時脈極限，加快了模擬的效率與速度。

IV. Appendix

1. TT corner (Temperature = 25℃)

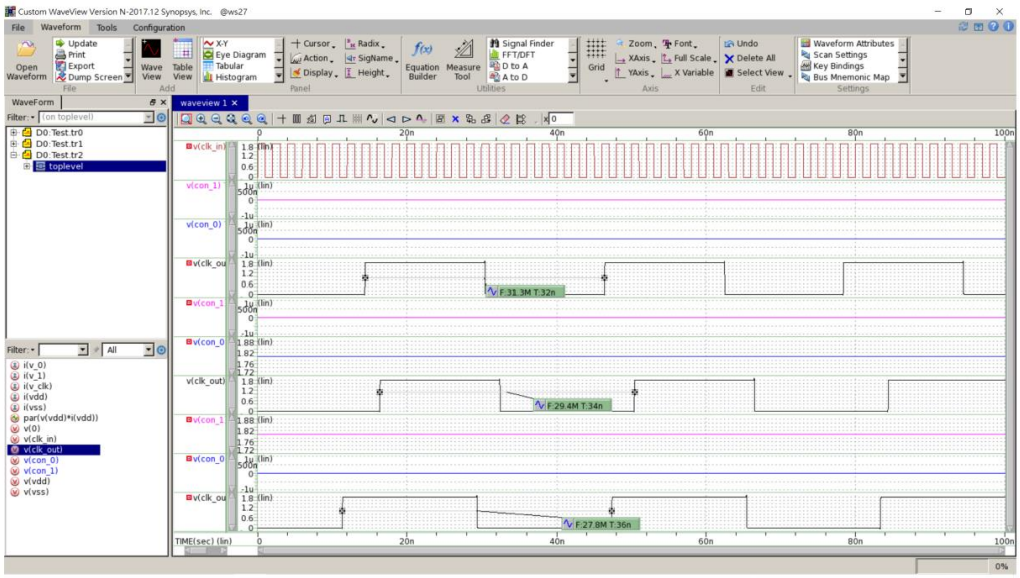

Fig. 26. Pre-sim waveform

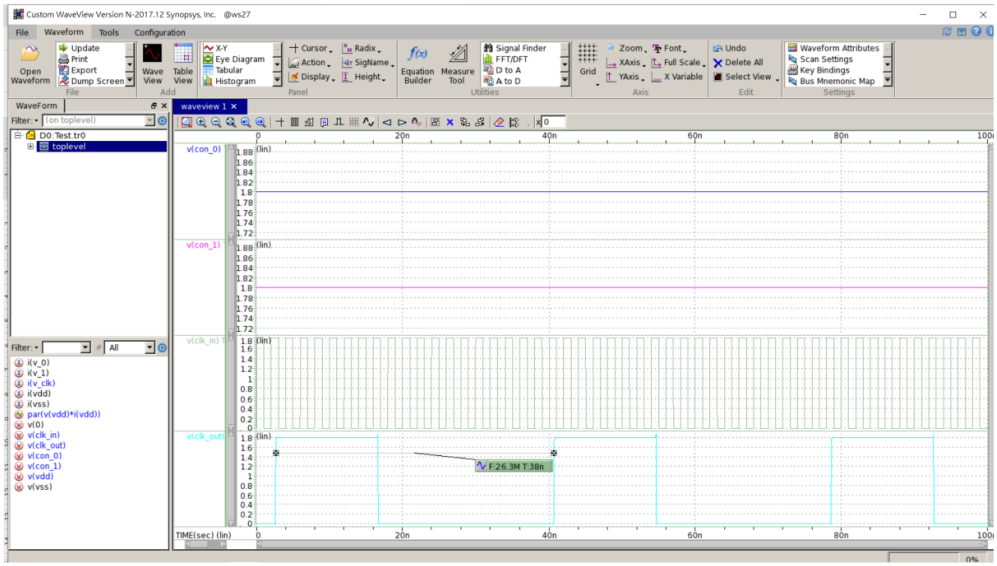

Fig. 27. Pre-sim waveform

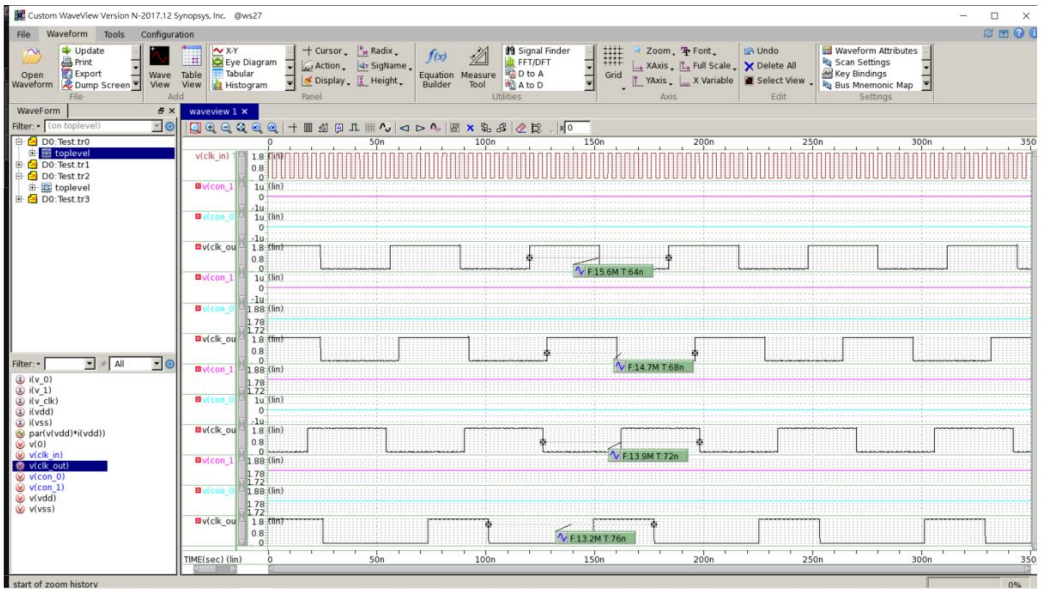

Fig. 28. Post-sim waveform

2. SS corner (Temperature = 125℃)

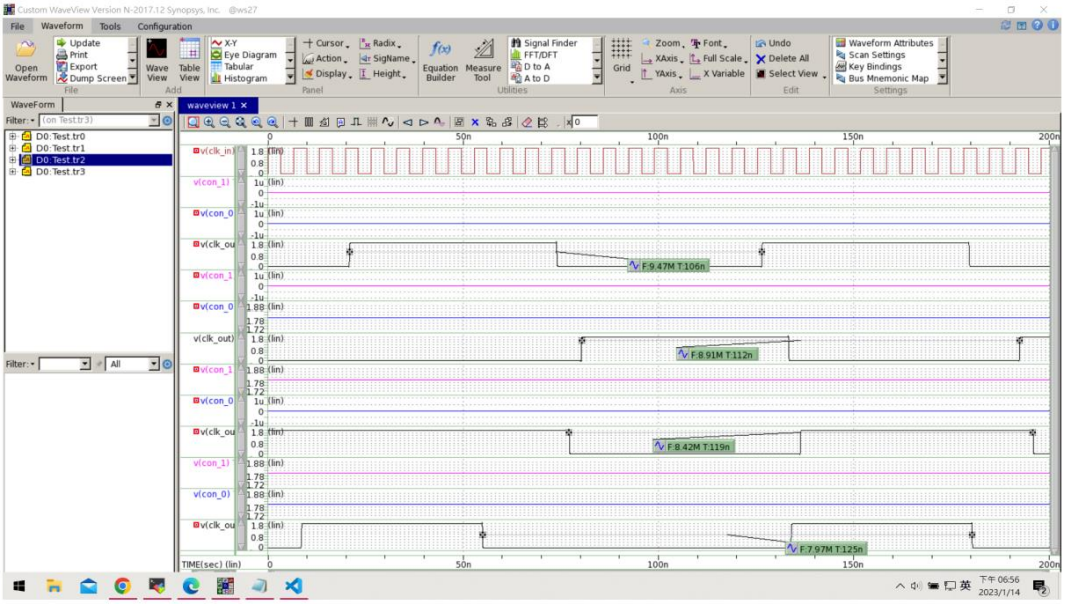

Fig. 29. Pre-sim waveform

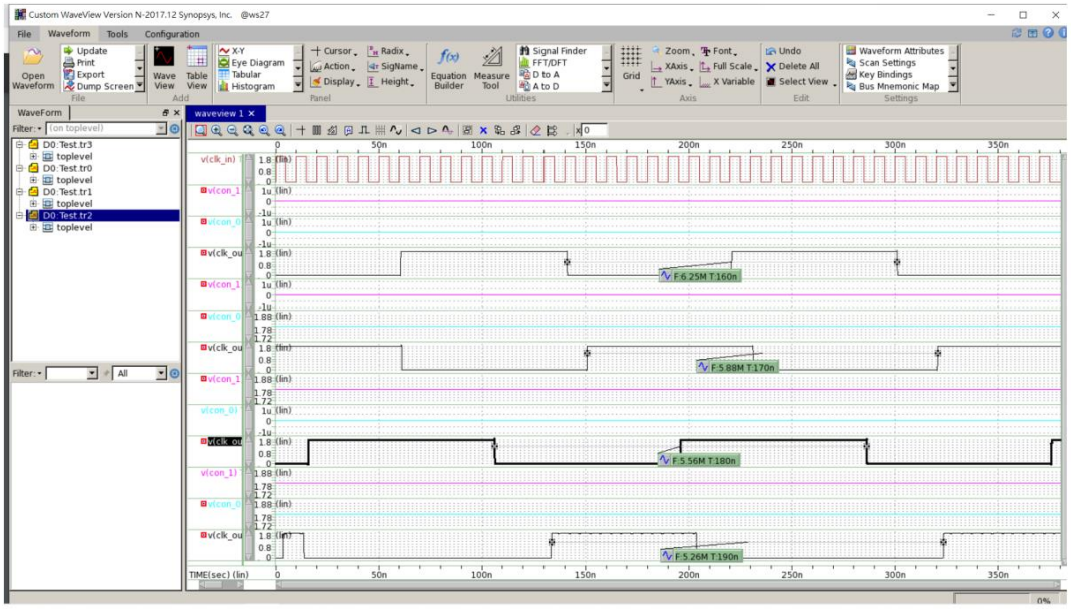

Fig. 30. Post-sim waveform

3. FF corner (Temperature = -40℃)

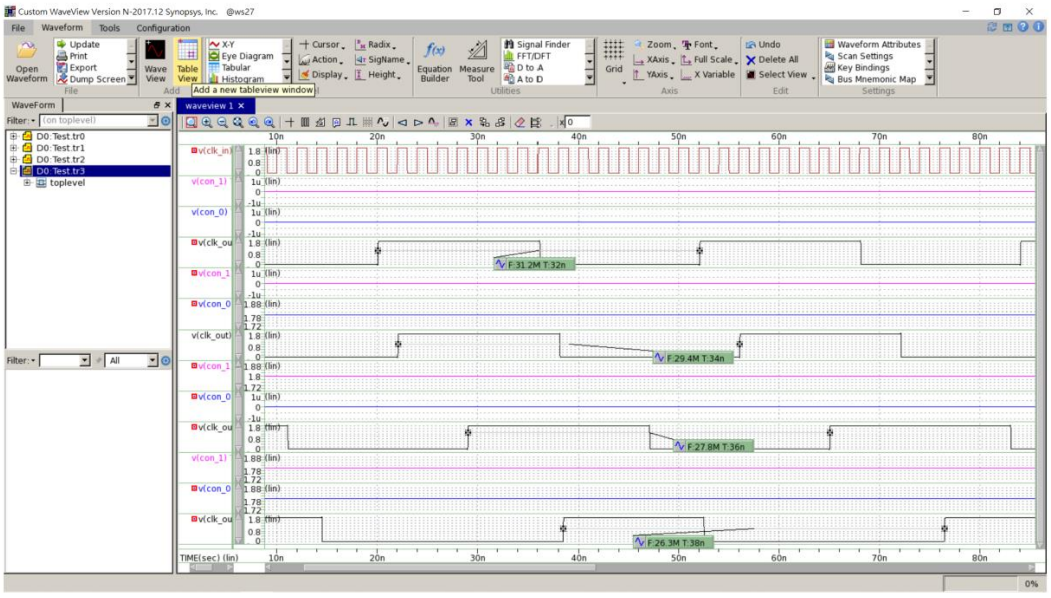

Fig. 31. Pre-sim waveform

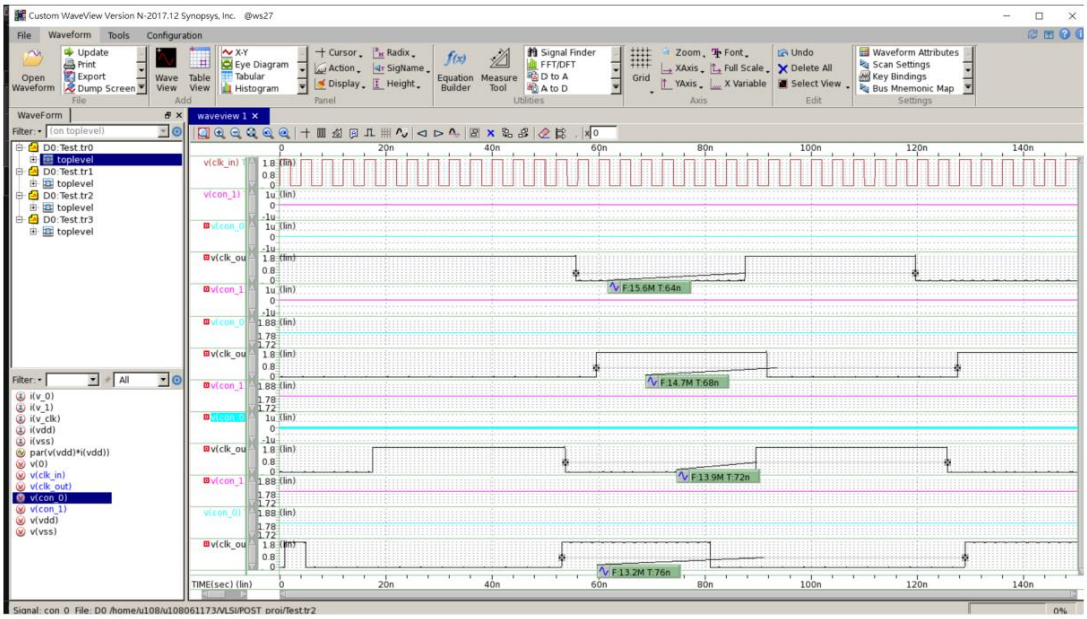

Fig. 32. Post-sim waveform

4. SF corner (Temperature = 25℃)

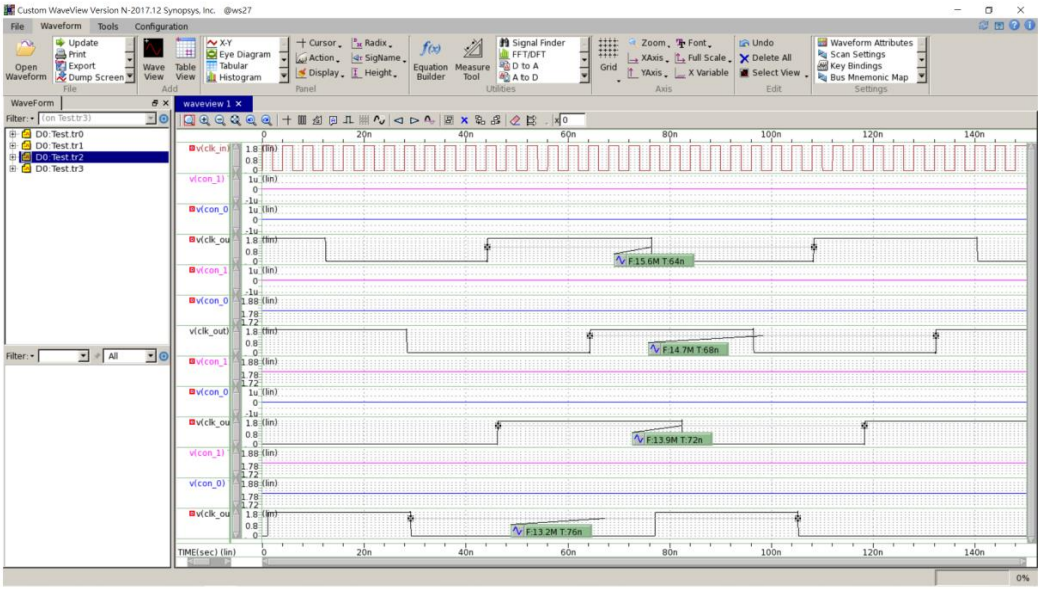

Fig. 33. Pre-sim waveform

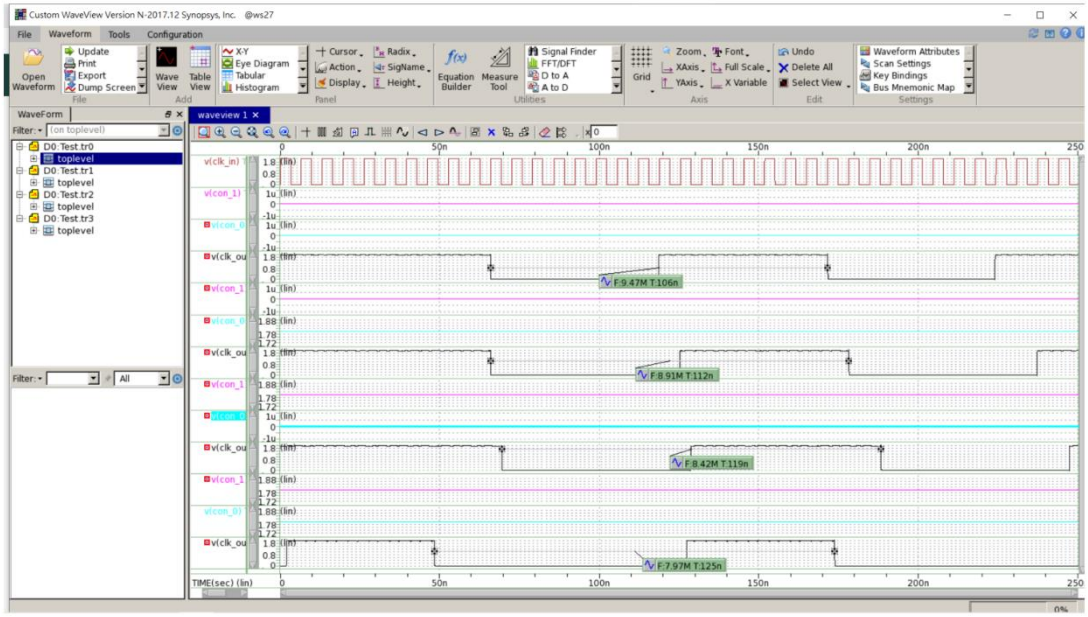

Fig. 34. Post-sim waveform

5. FS corner (Temperature = 25℃)

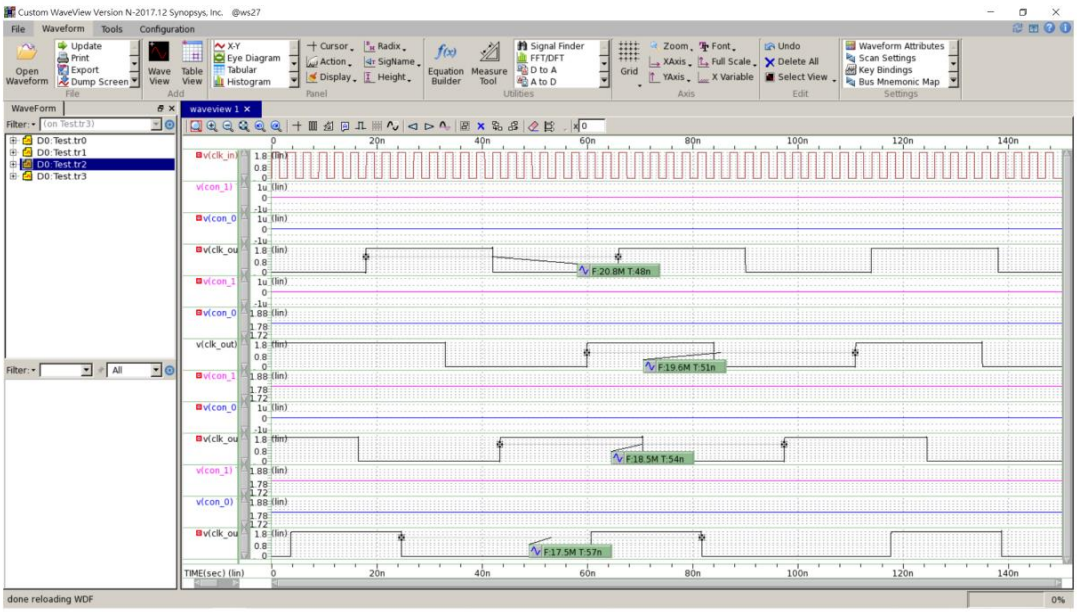

Fig. 35. Pre-sim waveform

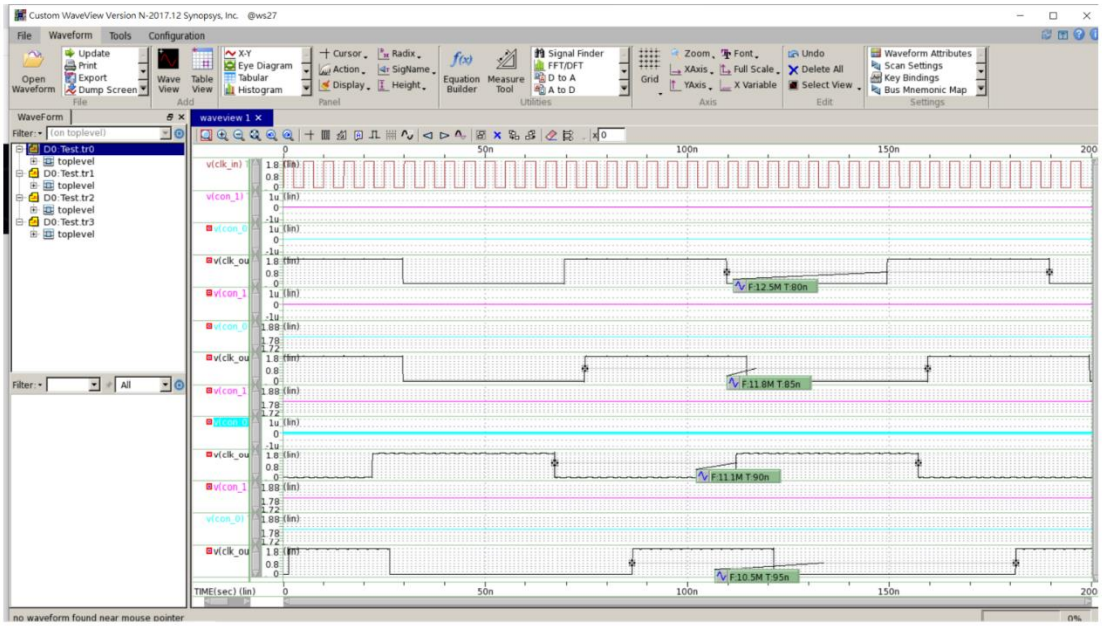

Fig. 36. Post-sim waveform

V. Reference

1. https://www.researchgate.net/figure/416-17-dual-modulus-prescaler-in-pulse-swallow-frequency-divider-f-is-the-output_fig8_224320943
2. https://www.jstage.jst.go.jp/article/elex/9/20/9_1611/_pdf