Lab 3: ATM Machine

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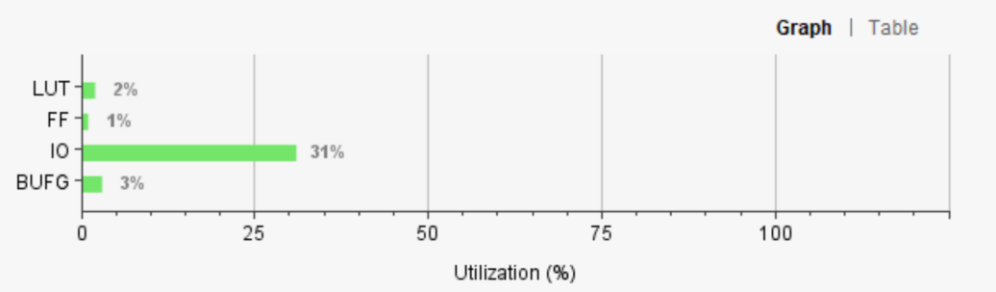
Summary and Lessons Learned

This lab taught me the importance of good design. When I first began working on this lab I realized that the design phase would have to be on of the longest parts of the lab. If the design of my datapath and controller were not very well thought out, then implementation was more challenging. I also learned the importance of writing a testbench before implementing my design on the board. I think it would have save me a lot of time to just write a testbench for my design and debug the circuit that way, but instead I did not write my testbench until I was half way through my design.

Resources



Max Frequency

Fmax = 10 ns – WNS = 10.75 ns

Testbenches

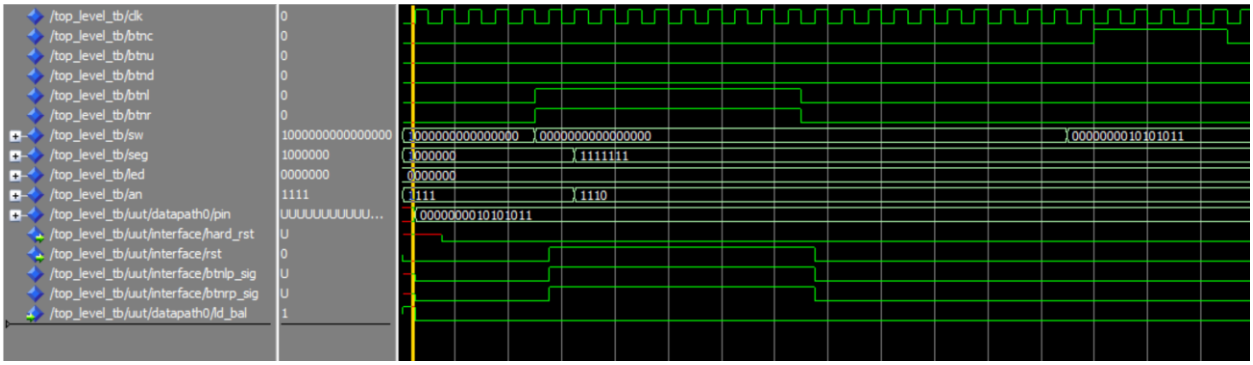


Figure 1: Reset test

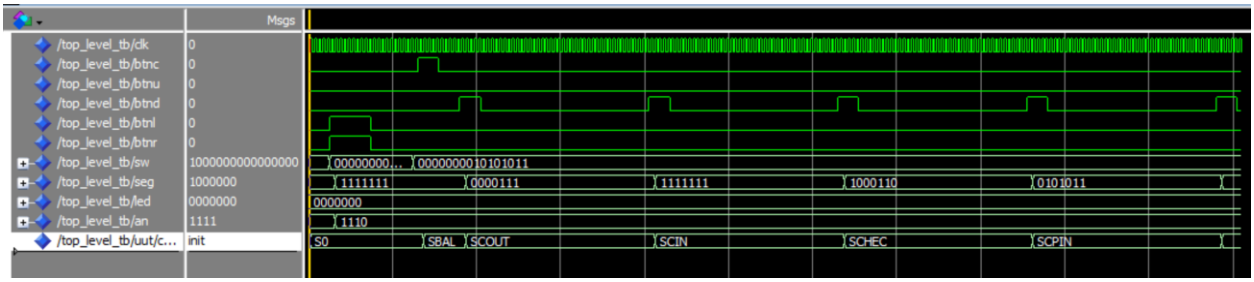


Figure 2: Menu test

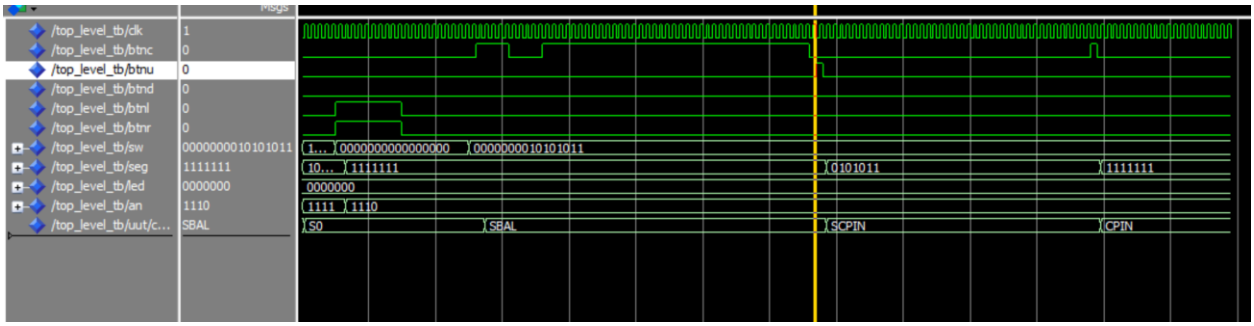


Figure 3: Menu test with btnu

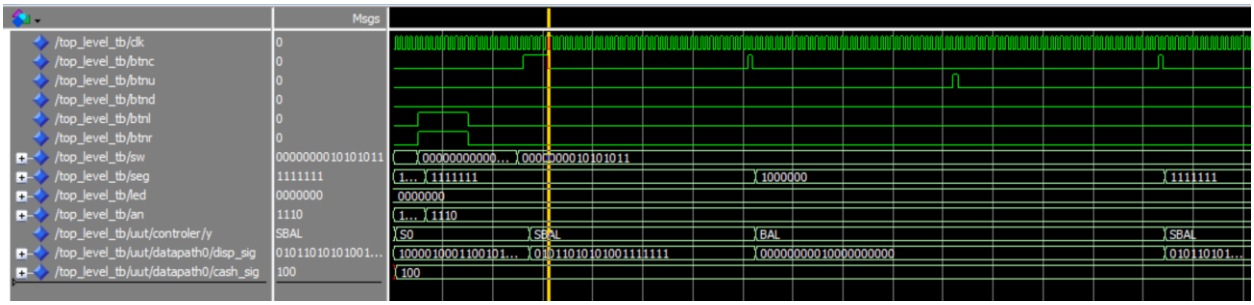


Figure 4: Balance test

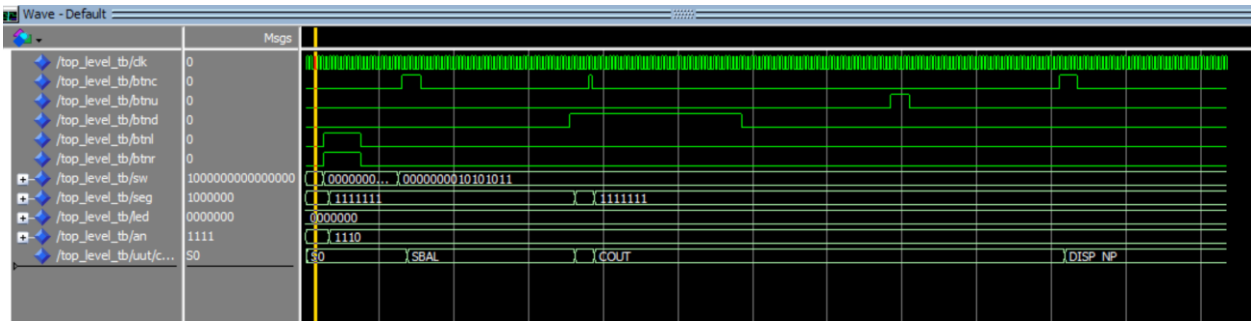


Figure 5: COUT test

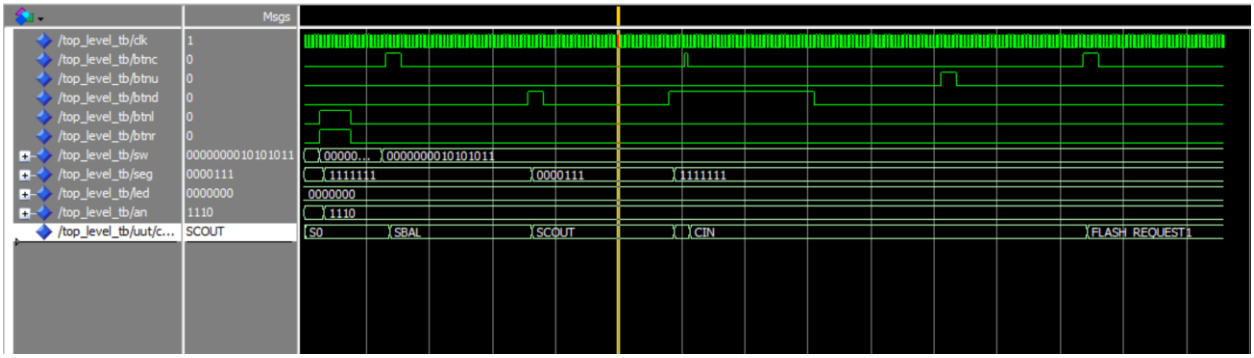


Figure 6: CIN test

Design

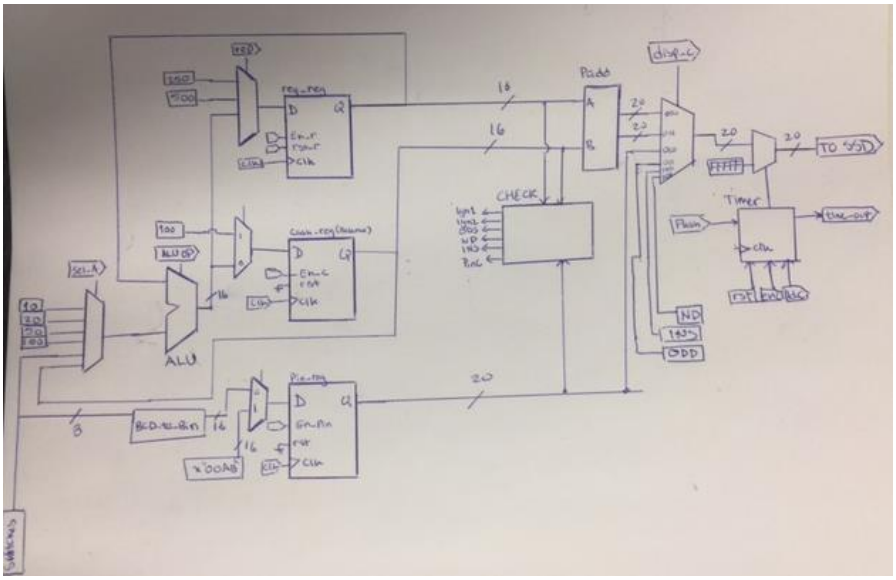


Figure 7: Datapath

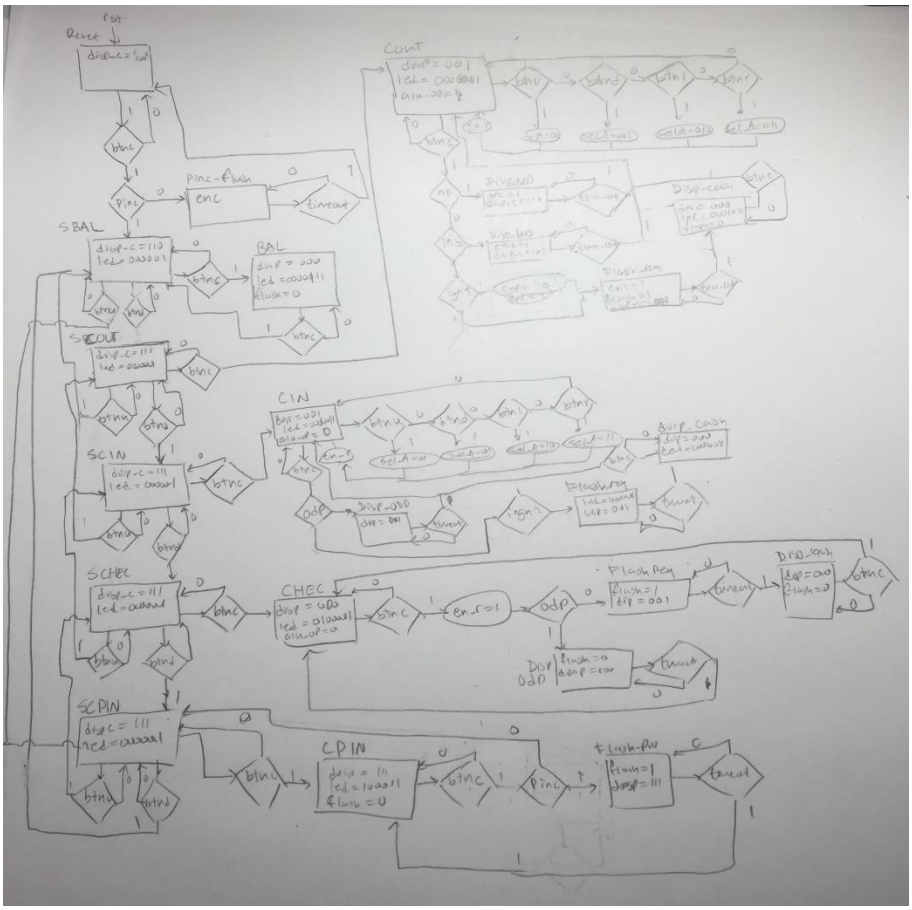


Figure 8: ASM.

RTL Diagram

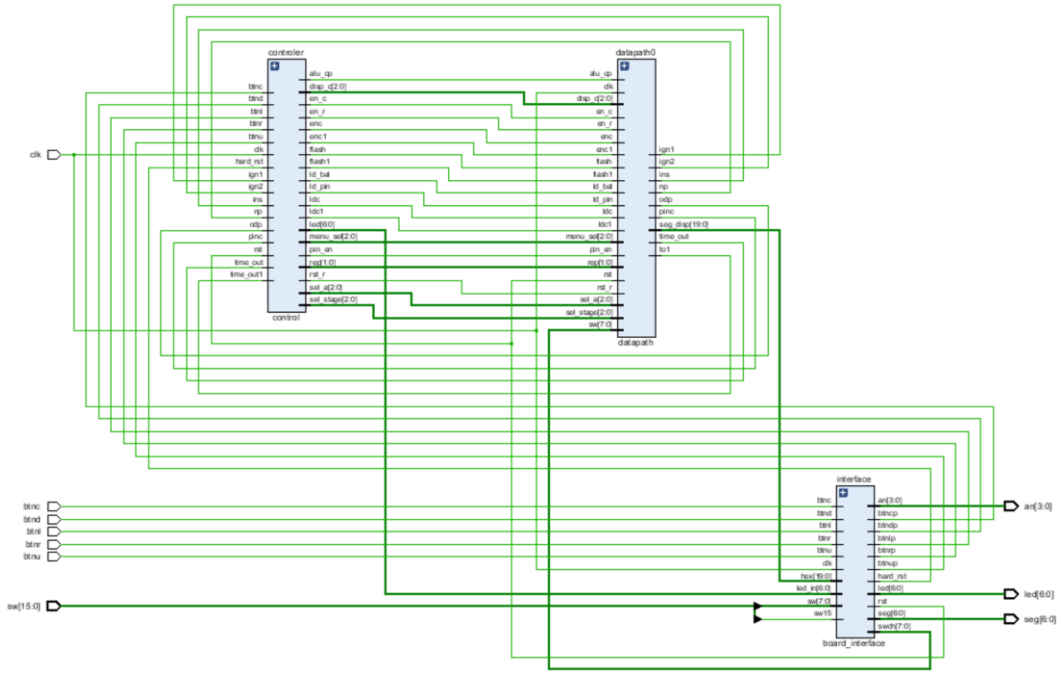


Figure 9: RTL top level

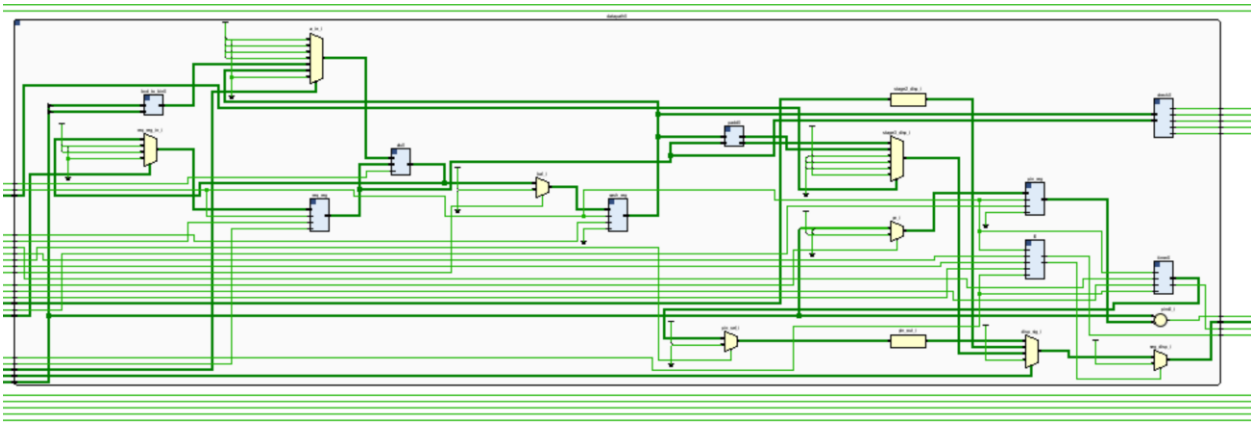


Figure 10: RTL Datapath

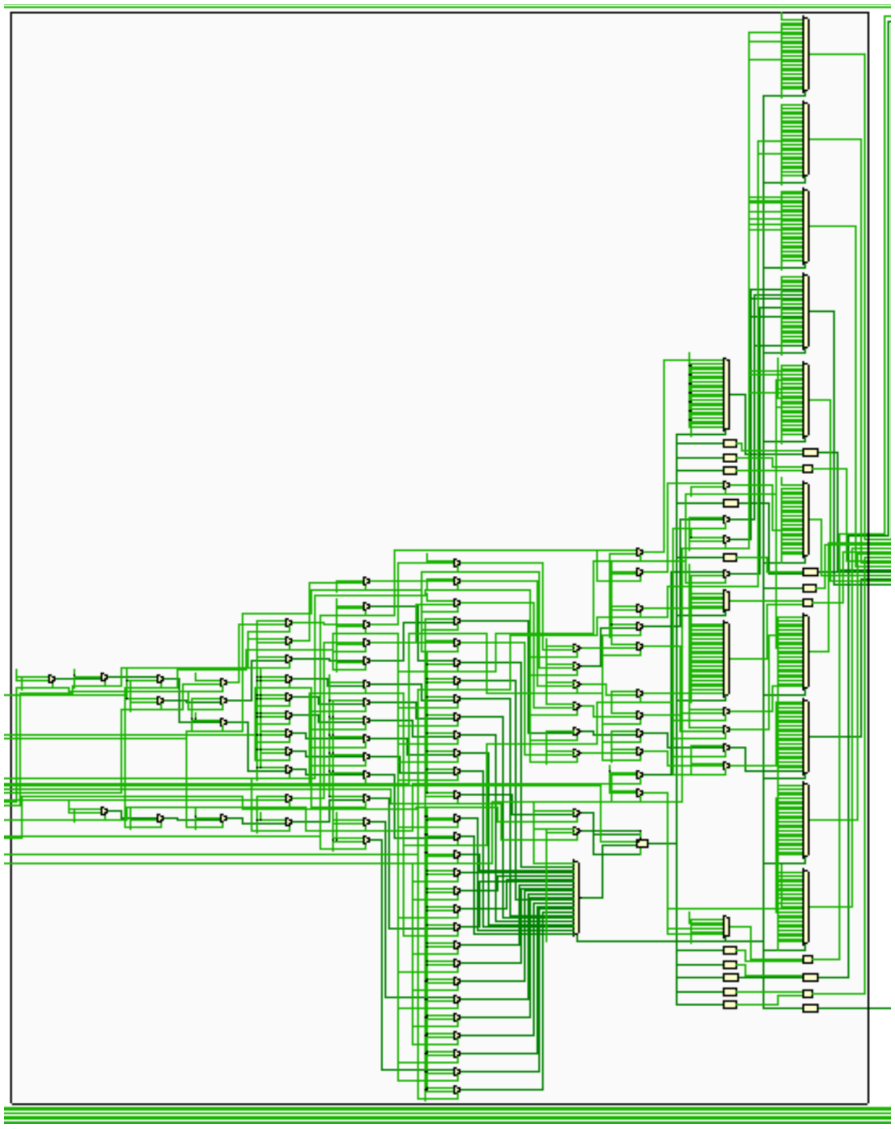


Figure 11: RTL Controller