Letter of Agreement on Collaboration in Research and Education

WHEREAS, **Telecommunications Systems Laboratory, Faculty of Electronics and Telecommunications, VNU-University of Engineering and Technology** (hereinafter referred to as "TSL-FET"), and **Cyber Information Security Lab in Department of Computer Science and Information Engineering, National Chung Cheng University** (hereinafter referred to as "CIS Lab") are mutually interested in cooperation in a joint project titled: "**Research and Development of a 6G-Enabled Reconfigurable Intelligent Surface (RIS)-Aided Integrated Sensing and Communication (ISAC) Platform and Hardware Prototyping for Smart Vehicles**". The two teams will apply for funding for the project in the field of Semiconductor to participate in the 2025 Protocol Science and Technology Mission under the Vietnam - Taiwan Science and Technology Cooperation Program. This program is according to Circular No. 10/2019/TT-BKHCN dated October 29, 2019, on the management of joint research projects under the Protocol. If the project is selected, the funding for the Taiwan research team will be provided by the Taiwan National Science and Technology Council – NSTC, Taiwan, while the Vietnamese Research team will be provided by the Ministry of Science and Technology (MOST) of Vietnam.

THEREFORE, TSL-FET and CIS Lab (hereinafter referred to as the "Parties") do hereby agree as follows:

Article 1. Objective

The purpose of this Letter of Agreement (LOA) is to establish the collaboration in education and research.

TSL-FET and CIS Lab shall together promote research cooperation with a view to contributing to the advancement of scientific research and technological development in wireless chips, Reconfigurable Intelligent Surfaces (RIS) panels, Integrated Sensing and Communications (ISAC) chipset control technology for smart vehicles, and high-frequency communications, all developed with a global perspective and for the benefit of the international community and two partners.

Article 2. Areas of Research Cooperation

2.1. TSL-FET and CIS Lab, recognizing the value of interchange and the benefits of collaboration, agree to the development of cooperative programs. The program will include the following areas:

- Exchange of academic and administrative staff;
- Performance of cooperative research, particularly in 6G RIS-aided ISAC systems;
- Share research equipment, prototypes, and related 6G testbeds;
- Education and training for technical staff, students; and

- Exchange of information on science and technology.

CIS Lab

- Develop chipset control software solutions for sensing detection, radar sensing application in automated vehicles, and evaluate their ability with 6G RIS panels and testbeds.
- Design the RIS-aided ISAC prototypes for automated vehicles
- Evaluation and improvement for enhancing communication-sensing capability
- Experimental tests for vehicles and vehicular networks,
- Deploy prototypes on vehicles, ground testing; and
- Share research equipment and related testbeds with the TSL-FET.

TSL-FET

- Conduct research on joint waveform design and RIS configuration in RIS-aided ISAC systems to improve both sensing and communication performance for 6G applications.
- Study channel estimation and the localization of users and targets within RIS-aided ISAC systems.
- Design a procedure to implement the proposed algorithms into the RIS-aided ISAC prototype.
- Research and design a controller for the ISAC BS to adjust the precoding matrix and optimize waveform design, based on an embedded system platform.
- Research and design a 1-bit Reconfigurable Intelligent Surface (RIS) for ISAC systems.
- Implement the joint waveform design and RIS configuration method on the designed RIS-assisted ISAC prototype.
- Perform experimental evaluations of the RIS-aided ISAC prototype, including tests involving vehicular scenarios.
- Share research equipment and related resources with the CIS Lab.

2.2. Research cooperation between TSL-FET and CIS Lab shall be carried out in areas of mutual interest on the basis of the research projects suggested by each Party.

Article 3. Implementation of Cooperation

During the conduct of research under this LOA, both parties shall implement the following forms of research cooperation:

- Dispatch of expert(s) for technical consultation;
- Training of researcher(s) in the field of wireless communications and chip designs;
- Exchange of nonproprietary technical information; and
- Share of research facilities.

Article 4. Research schedule and budget

Research schedule: From Jan 2026 to Dec 2028 (*See Research timetable in Appendix 1)*

Research budget: Total research budget for this period 420,000 USD

Of which:

- CISLab Lab: 150,000 USD (granted by the Taiwan National Science and Technology Council – NSTC, including the part of the original and add-on project)
- TSL-FET: 270,000 USD (State budget granted by Ministry of Science and Technology – MOST)

(See the details of budget estimation in Appendix 2)

Principle for cost sharing

The cost category will be borne by* CIS Lab *as following:

- Cost of CIS Lab staff in conducting research including salary, insurance, travel, etc.;
- Prototype production costs, ground testing costs;
- International collaborations, conferences, support the PhD students in Taiwan;
- Other cost.

The cost category will be borne by TSL-FET as following:

- Cost of TSL-FET's staff in conducting research including salary, insurance, travel, etc.;
- International collaborations, conferences, support CIS Lab members including PhD students in Vietnam;
- Other cost.

Article 5. Intellectual Property

The Parties share the rights to intellectual property of 50% for each side. The intellectual property registration must obey to Parties' laws and practices.

IN WITNESS WHEREOF, each Party hereto has caused this LOA to be executed in duplicate, each having equal authenticity, and retains one copy.

For and on behalf of TSL-FET

Date: / /2025

By: Assoc. Prof. Dr. Dinh Thi Thai Mai
Head of Telecommunications Systems Department

For and on behalf of CIS Lab

Date: 5 /14/2025

By: Assoc. Prof. Dr. Van-Linh Nguyen
Head of Cyber Information Security Lab

TRƯỜNG ĐẠI HỌC CÔNG NGHỆ

By: Prof. Chu Duc Trinh
Rector of the VNU University of Engineering and Technology

By: Prof. Shaw-Jenq Tsai
President of National Chung Cheng University, Taiwan

由於協議文件較晚才送達國立中正大學，
我校校長無法及時簽署。
完整簽署版將會放置於此連結：
http://ccucyberseclab.github.io/CCU-VNU-UET.pdf

Appendix 1. Research timetable

Activity	2026				2027				2028			
	QI	QII	QIII	QIV	QI	QII	QIII	QIV	QI	QII	QIII	QIV
Research in Vietnam												
Research and evaluation of the current status and development of RIS-aided ISAC Systems.	X	X	X									
Conduct research on joint waveform design and RIS configuration in RIS-aided ISAC systems to improve both sensing and communication performance for 6G applications	X	X	X	X								
Study channel estimation and the localization of users and targets within RIS-aided ISAC systems.		X	X	X	X							
Design a procedure and block diagram to implement the proposed algorithms into the RIS-aided ISAC prototype (*Taiwan visit*)				X	X	X	X					
Research and design a controller for the ISAC BS to adjust the precoding matrix and optimize waveform design, based on an embedded system platform.					X	X	X	X	X			
Research and design a 1-bit Reconfigurable Intelligent Surface (RIS) for ISAC systems.					X	X	X	X	X			
Implement the joint waveform design and RIS configuration method on the design RIS-assisted ISAC prototype and optimize a RIS-aided ISAC prototype (*Taiwan visit*)							X	X	X	X	X	X
Perform experimental evaluations of the RIS-aided ISAC prototype, including tests involving vehicular scenarios (*Taiwan visit*)								X	X	X	X	X
Research in Taiwan												
Study ISAC for automated vehicles (car roof, front, back optimal integration)	X	X	X									
Study RIS-aided sensing detection models in non-LOS areas	X	X	X	X								
Optimize FR1/FR2 ISAC with sensing enhancements for mobile targets		X	X	X	X	X						
Integrate FR1/FR2 ISAC for 6G V2X with sensing and localization Enhancements in non-LOS areas *(Vietnam visit)*					X	X	X	X				
Develop chipset control algorithms for ISAC to integrate for 6G V2X						X	X	X	X	X		
Design a 6G V2X ISAC hardware prototype with USRP and RIS testbeds								X	X	X		
Evaluation and improvement sensing and communication sensitivity									X	X	X	X
Structure optimization on 6G ISAC prototype design *(Vietnam visit)*										X	X	X
Ground testing of the hardware prototype with vehicles and 6G V2X										X	X	X

Appendix 2. Budget estimation

Unit: USD

No.	Description	Total	CIS Lab	TSL-FET	Remarks
1	Expenses calculated by direct labor rate	165,000	50,000	115,000	
2	6G testbed and RIS-aided ISAC prototypes/chip	164,000	60,000	99,000	
3	Small scale equipment	10,000	10,000	5,000	
4	Expenses to hire international & domestic experts	0	0	0	
5	Travel and visiting costs;	47,000	15,000	32,000	
6	Joint seminars and workshops	5,400	5,000	400	
7	Other expenses	28,600	10,000	18,600	
	Grand total (USD):	**420,000**	**150,000**	**270,000**	