APT8L08 Capacitive Touch Sensor Controller

DATASHEET

VER. 1.02

2015/06/25

1 Overview

1.1 Overview

APT8L08 is a 8-channel versatile capacitive touch sensing chip, embedded with multiple flexible and powerful configuration registers. For differential application, users can configure APT8L08 internal registers using an external MCU through an I^2C interface. The parameters such as sensitive and operating mode, etc. can be configured according to the specific application requirement.

1.2 Features

- Input Channels: 8 channels
- Communication Interface: I^2C, along with a dedicated interrupt output signal
- Noise Immunity: 120:1 (SNR)
- Sensitivity: Suitable for surface materials within 15mm in thickness. Then sensitivity of each channel can be adjusted individually.
- Self-adaptive adjustment technique: sensitivity automatically adjust along with environment variation (temperature / humidity)
- Low Operating Current:
    - Operating under 1MHz, IDD = 70uA@5V (typical)
    - Operating under 500KHz, IDD = 45uA@5V (typical)
    - Operating under 250KHz, IDD = 22uA@5V (typical)
    - Operating under 125KHz, IDD = 16uA@5V (typical)
    - Deep Sleep Mode, IDD = 1uA@5V (maximum)
- Event detect mode: Single key / multiple keys detection
- Operating Temperature Range: -40°C ~ +85 °C
- Operating Voltage Range: 2.2V ~ 5.5V
- Package Category:
  - QFN16（APT8L08NF)
  - SOP14（APT8L08SE)

1.3 Pin Assignment

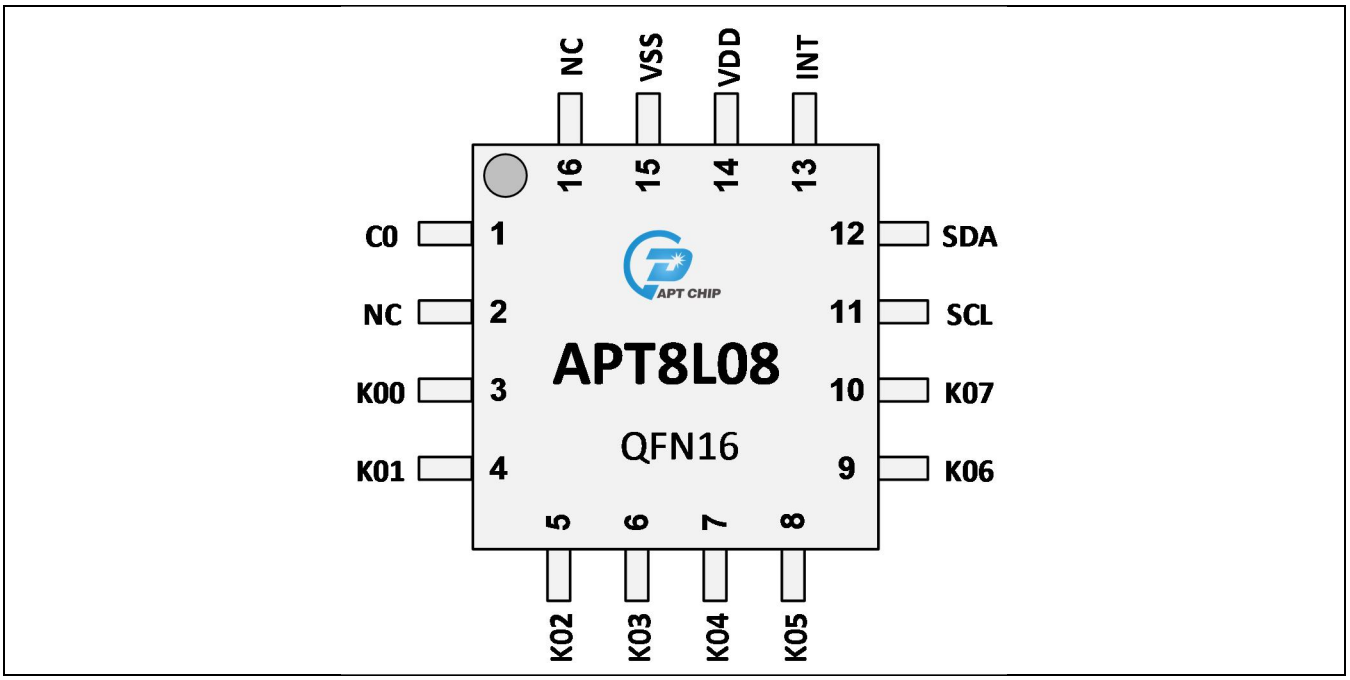


Figure 1-3-1 APT8L08 Pin Diagram (QFN16)

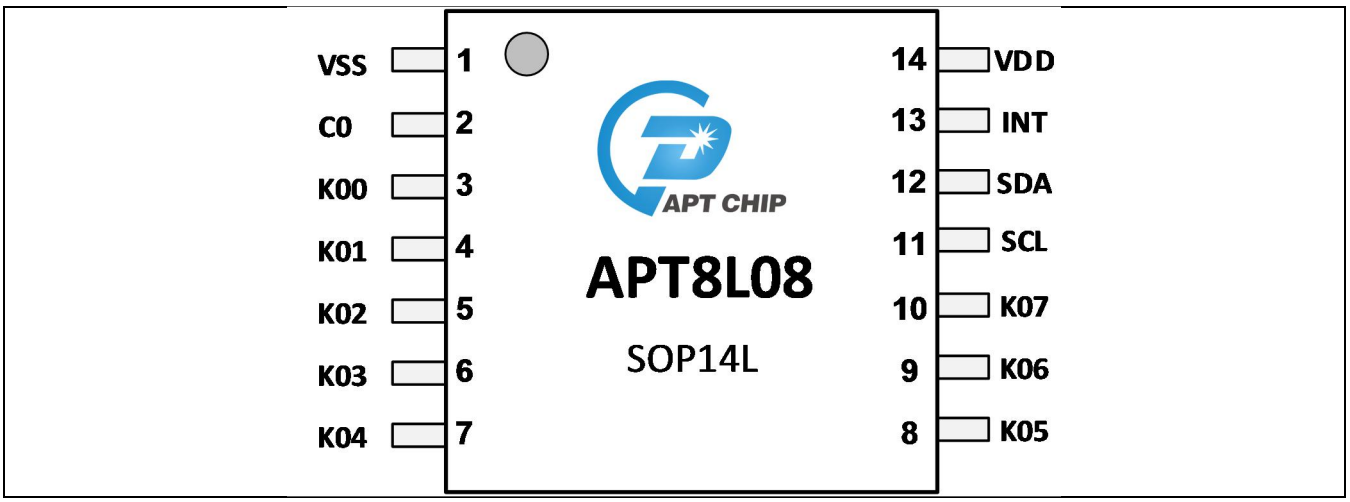


Figure 1-3-2 APT8L08 Pin Diagram (SOP14)

1.4 Pin Description

Table 1-4 APT8L08 Pin Description

Pin Name	Pin Type	Function	Circuit Type	QFN16 PIN NUM	SOP14 PIN NUM
C0	I/O	External cap, 10nF (103)	A	1	2
NC	-	NC	-	2,16	-
K0<7:0>	I/O	Touch sensor input (NC when it is not used)	A	3-10	3-10
INT	O	Interrupt output pin, active voltage level (L or H active) is configurable	D	13	13
SCL	I	I^2C clock pin	D	11	11
SDA	I /O	I^2C data pin	D	12	12
VDD	-	Power pin	P	14	14
VSS	-	Ground pin	P	15	1

2 Register Configuration

2.1 Registers List

Table 2-1 Register Table

Register Name	Address	R/W
SYSCON (System Control Register)	0x3A	R/W
MCON Register (Mode Control Register)	0x21	R/W
BUR (Baseline Update Register)	0x22	R/W
DMR (Development Mode Register)	0x2D, 0x2A	R/W
KDR0 (Key Disable Register)	0x23	R/W
GSR (Global Sensitivity Register)	0x20	R/W
KOR (Key Offset Register)	0x00 ~ 0x07	R/W
KVR0 (Key Value Register)	0x34	R

2.2 Registers Characterization

2.2.1 SYSCON (System Control Register)

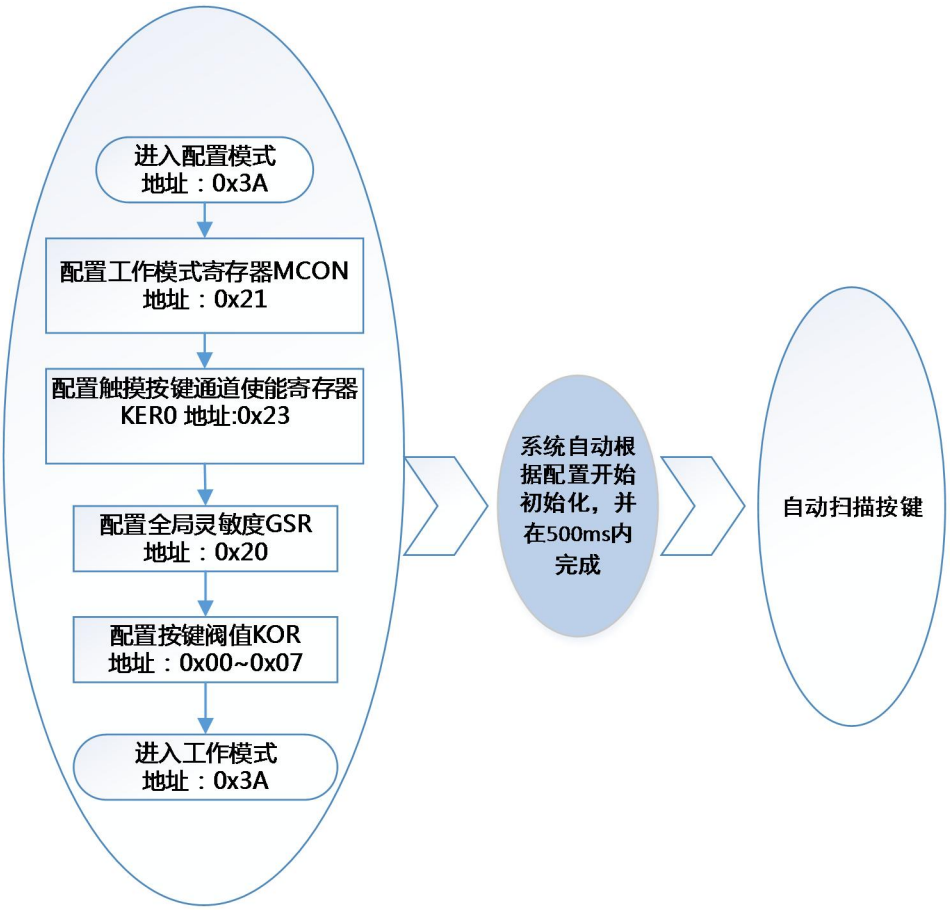
SYSCON (System Control Register) address is 0x3A, default value is 0x00, when SYSCON register is configured to 0x5A，system is configured as System Configuration Mode(Deep Sleep Mode)，system is halted, and power current will fall down (<1uA).

- SYSCON is configured to 0x5A: system transfer to Configuration Mode (Deep Sleep Mode).
- SYSCON is configured to 0x00: system transfer to Work Mode.

In order to configure chip Work Mode, sensitivity and other system initial registers, system much transfer to Configuration Mode. After configuration finish, system should be configured into Work Mode.

Table 2-2-1 System Configuration Flow Diagram

Note: After power on, the main control chip should wait for 500ms before the APT8L08 initial configuration. (It is proposal to do the read back check, to ensure data written successfully.)



2.2.2 MCON (Mode Control Register)

MCON (Mode Control Register) address is 0x21, default value is 0x01.

Table 2-2-2 MCON (Mode Control Register)

Bits	Function	Default	Value	Function
MCON<1:0>	Operating Frequency Selection	01	00	Operating Frequency：1MHz
			01	Operating Frequency：500KHz

			10	Operating Frequency：250KHz
			11	Operating Frequency：125KHz
MCON<2>	Touch Key Mode	0	0	**Single-Key Mode:** Touch key chip only recognize single-key. Multi-key operating is invalid. In this mode, large area overlying such as water or large objects covering the touch surface will be omitted efficiently.
			1	**Multi-Key Mode**: It can recognize all appropriate key simultaneously, and output all key values. In combined case, this bit should be configured to 1.
MCON<3>	Interrupt Output Mode	0	0	Recognized key operating being detected, output value change to '0'. It recover to '1', when key being released.
			1	Recognized key operating being detected, a pulse being generated on output pin 'INT'. Other conditions, 'INT' pin keep '0'status.
MCON<4>	RSVD	0	-	**Reserved, must configured to 1**
MCON<5>	RSVD	0	-	**Reserved, must configured to 0**
MCON<6>	RSVD	0	-	**Reserved, must configured to 1**
MCON<7>	RSVD	0	-	**Reserved, must configured to 0**

2.2.3 BUR （Baseline Update Register）

BUR (Baseline Update Register) address is 0x22, default value is 0x20. When configured to 0x00, baseline update speed-up. It can adjust the time of key invalid status when the key is pressed down while power-on. (It is recommended to keep the default value, only when you have such special case).

2.2.4 DMR （Development Mode Register）

There are two DMR registers. The DMR0 address is 0x2D, and default value is 0x00. The DMR1 address is 0x2A, and default value is 0x10. When the DMR0 is configured to 0x08 and the DMR1 is configured to 0xFF, it can enable the touch key recognizable by touch PCB PAD or springs directly without any surfacing material.

It is useful to configure like above case during product development. It must use default value when Mass-production. The default value can filter out strong interference.

2.2.5 KDR0 (Key Disable Register)

KDR0 （Key Disable Register） address is 0x23, and default value is 0x00. KDR0 is used as disable/enable control for 8-channels K00 ~ K07 correspondingly. In order to speed-up the response of touch-in-using channel, it is suggested to disable the channels that is not used.

When the bit is set as '1', the channel is disabled. When the bit is set as '0', the channel is enabled.

Table 2-2-5 KDR0 (Key Disable Register)

Register	**Register KER0 (Address : 0x23)**							
Bits	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Touch Channel	**K07**	**K06**	**K05**	**K04**	**K03**	**K02**	**K01**	**K00**

2.2.6 GSR (Global Sensitivity Register)

GSR (Global Sensitivity Register) address is 0x20. It is used to configure sensitivity for all touch key channels. High value means high sensitivity and long scanning period; and vice versa. GSR default value is 0x02, and must less than 0x0F.

2.2.7 KOR (Key Offset Register)

KOR00 ~ KOR07 address are 0x00-0x07. Each register has total 255 steps, and all registers default value is 0x04. The KOR is configured for sensitive adjustment. High register value means low sensitivity, and vice versa.

Table 2-2-7 KOR (Key Offset Registers) list

Register Name	KOR00	KOR01	KOR02	KOR03	KOR04	KOR05	KOR06	KOR07
Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
Default Value	0x04	0x04	0x04	0x04	0x04	0x04	0x04	0x04
Touch Key Channel	K00	K01	K02	K03	K04	K05	K06	K07

2.2.8 KVR0 (Key Value Register)

KVR0 (Key Value Register) address is 0x34, and default value is 0x00. The bit change to 1 when the corresponding key was pressed down.

Table 2-2-8-1 Key Value Register and Corresponding Touch Key Channel

Registers	**Register KVR0 Address:0x34**

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Channel	K07	K06	K05	K04	K03	K02	K01	K00

In Multi-key Mode, Key Value Register reflects the key status of each channel respectively. Please refer to the register MCON<2> for more information) .

Table 2-2-8-2 Example：KVR0(Key Value Register) in Multi-key Mode

Register	**Register KVR0 Address 0x34**									
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register Value	Description
Keys	K07	K06	K05	K04	K03	K02	K01	K00		
Single-key	0	0	0	0	0	0	0	1	0x01	press down K00
Multi-key	1	0	1	0	1	0	1	0	0xAA	press down K07,K05,K03,K01

3 IIC Communication Interface

3.1 Overview

APT8L08 can be operated as a slave device by using standard 7-bit IIC interface. The address is 0x56, only supports slave mode. APT8L08 can support transmit rate up to 400KHZ, 100KHz is suggested for stable transmission.

All registers in APT8L08 can be written directly. When read operation is required, it must configure the read address first, then read the data.

When a recognized touch operation is detected, main control chip can read the key value through IIC module. APT8L08 also provide interrupt pin to supply flexible communication method with main controller under different requirements.

3.2 Data Characterization

APT8L08 chip is embedded with a standard two-wire synchronous serial IIC interface working under Slave mode, transmitting & receiving data according to the requirement raised by external controller.

3.2.1 Write Operation (Only supports single-byte written)

START	7-bit address	Write bit (this bit 0)	ACK	Register Address	ACK	Data BYTE	ACK	STOP

3.2.2 Read Operation (Only supports single-byte read)

START	7-bit address	Write bit (this bit 0)	ACK	Register Address	ACK	START	7-bit address	Read R (this bit 1)	ACK	Data BYTE	NACK	STOP

4 Electrical Characteristics

4.1 Physical characteristic limitation

Table 4-1 physical characteristic limitation (T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{DD}		-0.3 to +6.5	V
Input Voltage	V_I	All ports	-0.3 to VDD + 0.3	V
Output Voltage	V_O	All output ports	-0.3 to VDD + 0.3	mA
I/O current high	V_{OH}	One I/O pin active	-10	mA
-		All I/O pins active	-40	mA
I/O current low	V_{OL}	One I/O pin active	+20(Peak)	mA
-		All I/O pins active	+60(Peak)	mA
Operating Temperature	T_A	-	--40 to +85	°C
Storage Temperature	T_{STG}	-	-65 to +150	°C

4.2 DC electrical characteristic

Table 4-2 DC electrical characteristics (T_A = -40°C ~ 85°C, V_{DD} = 2.2V to 5.5V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	-	-	2.2		5.5	V
Input high voltage	V_{IH1}	SCL,SDA,ADS	V_{DD}= 2.2 to 5.5 V	0.8 VDD	-	VDD	V
	V_{IH2}			VDD- 0.1			
Input low voltage	V_{IL1}	SCL,SDA,ADS	V_{DD}= 2.2 to 5.5 V	-	-	0.2 VDD	V
	V_{IL2}					0.1	
Output high voltage	V_{OH}	I_{OH} = – 10 mA INT	V_{DD}= 2.2 to 5.5 V	VDD-1.0	-	-	V
Output low voltage	V_{OL}	IOL = 20 mA SDA, K0, INT	V_{DD}=2.2 to 5.5 V	-	-	1.0	V
Input High leakage current	I_{LIH1}	SCL,SDA,ADS	V_{IN} = VDD	-	-	1	uA
Input Low leakage current	I_{LIL1}	SCL,SDA,ADS	V_{IN} = 0 V	-	-	-1	uA
Output high leakage current	I_{LOH}	INT	V_{OUT} = V_{DD}	-	-	1	uA
Output Low leakage current	I_{LOL}	INT, SCL,SDA	V_{OUT} = 0 V	-	-	-1	uA
Supply Current	I_{DD1}	Run Mode 1MHz clock	V_{DD}=2.2 to 5.5 V	-	50	70	uA
		Run Mode 500KHz clock		-	40	45	uA
		Run Mode 250KHz clock		-	22	25	uA
		Run Mode 125KHz clock		-	16	20	uA
	I_{DD2}	Stop Mode T_A = 25°C		-	0.4	1	uA

4.3 AC electrical characteristic

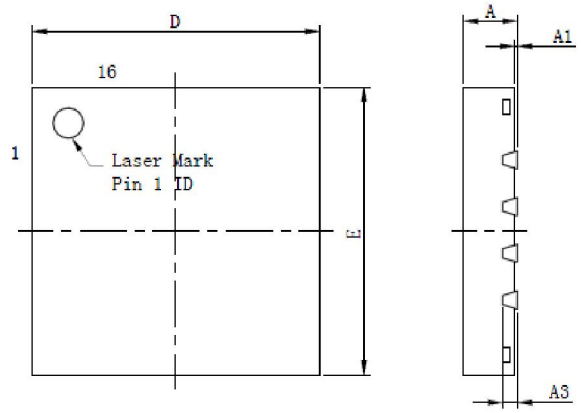
Table 4-3 AC electrical characteristics (T_A = -40°C ~ 85°C, V_{DD} = 2.2V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Cap	C_{IN}	f=1MHz; non-test pins must grounding			10	pF
Out Cap	C_{OUT}					
I/O pin Cap	C_{IO}					

5 Mechanical Data

APT8L08 is available in QFN16 and SOP14 package.

尺寸 / 标注	最小	标准	最大	尺寸 / 标注	最小	标准	最大
A	0.70	0.75	0.80	D1	2.20	2.30	2.40
A1	0.00	—	0.05	E1	2.20	2.30	2.40
A3	0.203REF			e	0.65TYP		
b	0.20	0.25	0.30	K	0.20	–	–
D	3.90	4.00	4.10	L	0.30	0.40	0.50
E	3.90	4.00	4.10				



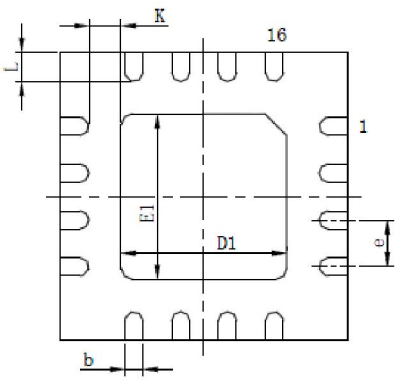
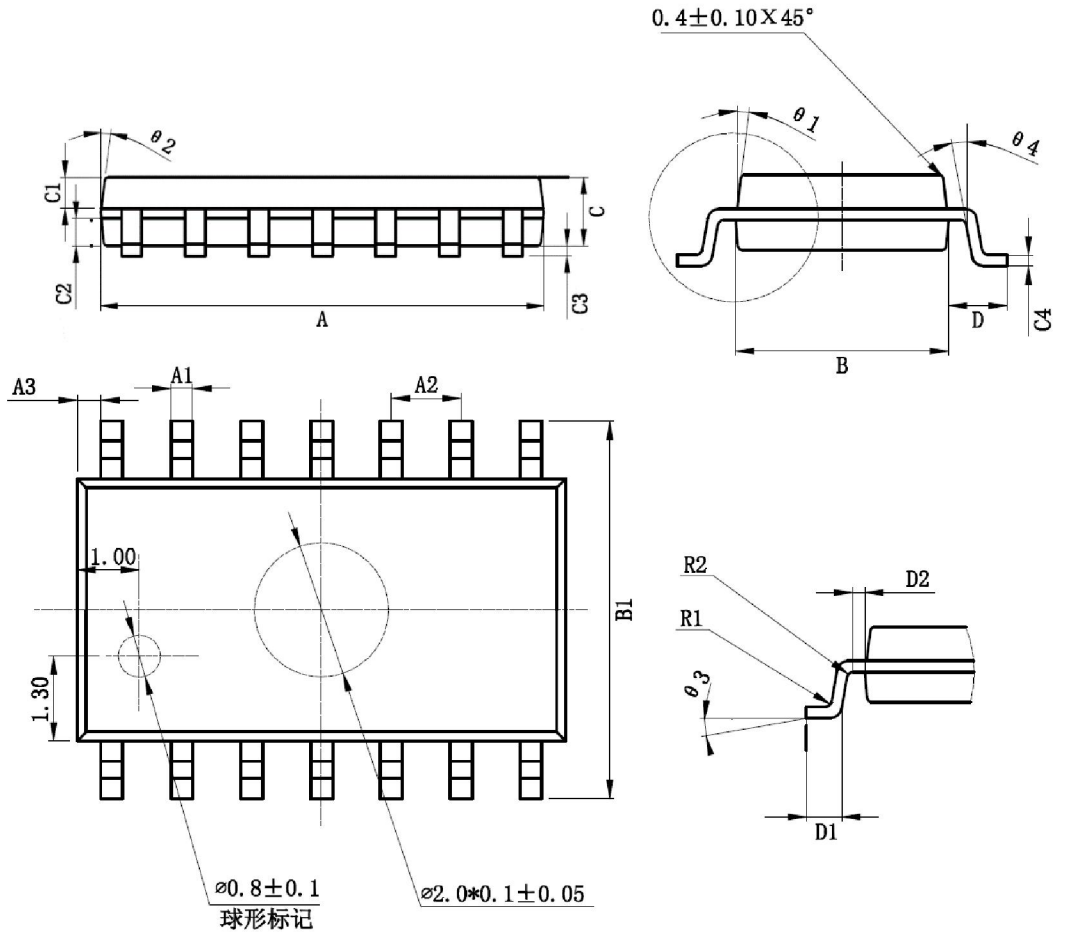


Figure 5-1 QFN16



尺寸 / 标注	最小(mm)	最大(mm)	尺寸 / 标注	最小(mm)	最大(mm)
A	8.55	8.75	C4	0.193	0.213
A1	0.356	0.456	D	0.95	1.15
A2	1.27TYP		D1	0.40	0.7
A3	0.312TYP		D2	0.20TYP	
B	3.80	4.00	R1	0.20TYP	
B1	5.80	6.20	R2	0.20TYP	
C	1.35	1.55	θ1	8° ~ 12° TYP4	
C1	0.60	0.70	θ2	8° ~ 12° TYP4	
C2	0.55	0.65	θ3	0° ~ 8°	
C3	0.10	0.25	θ4	4° ~ 12°	

Figure 5-2 SOP14

6 Reference Circuit

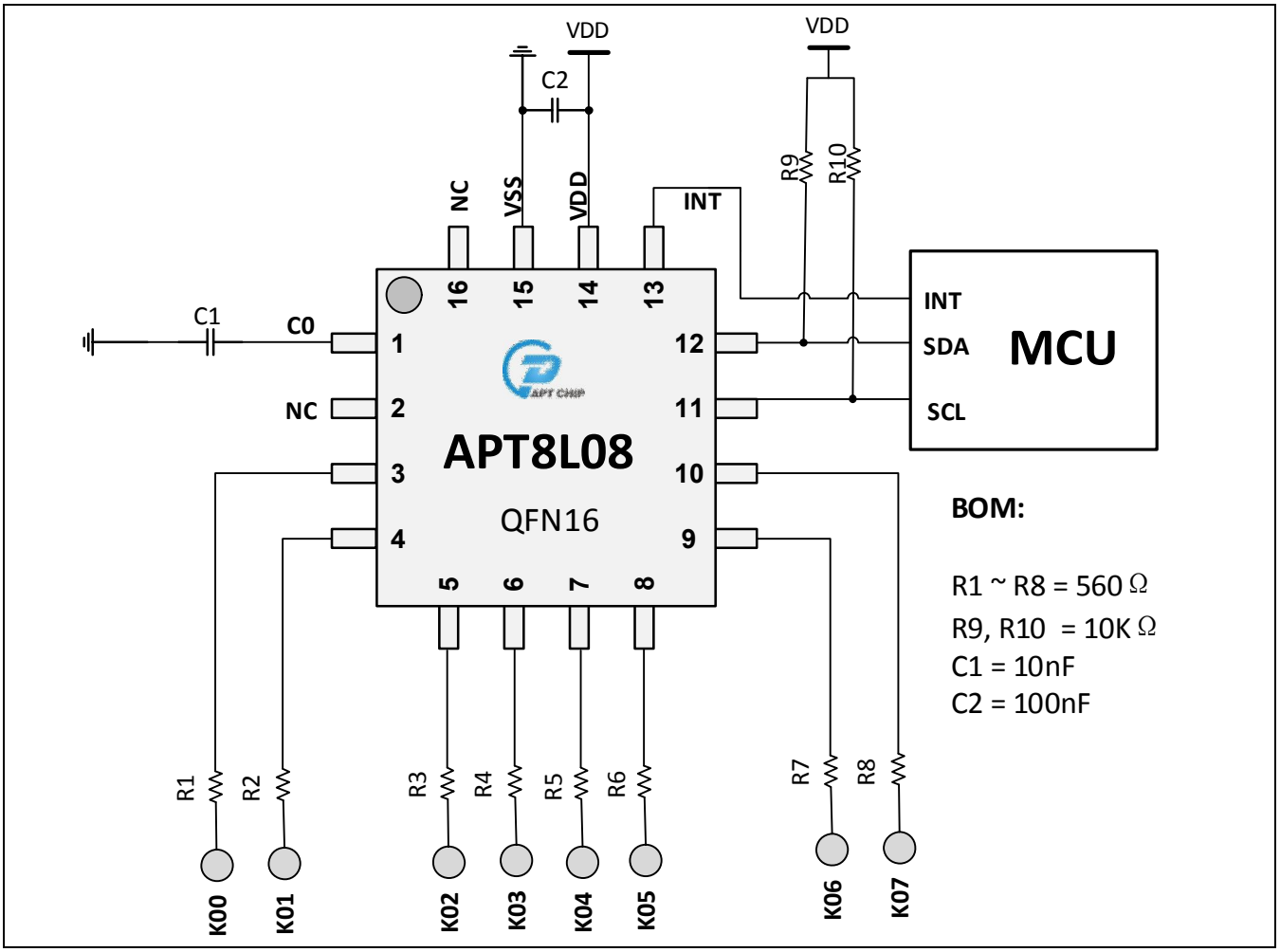


Figure 6-1 APT8L08 Reference Circuit