Calvin Deutschbein (they/them)

CONTACT INFORMATION

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ACADEMIC APPOINTMENTS

Assistant Professor of Computer Science, Willamette University — 2021 to present
School of Computing & Information Sciences, 2022-
College of Arts & Sciences, 2021-2022

Adjunct Professor, Elon University — 2020
Department of Computer Science

Instructor, The University of North Carolina at Chapel Hill — 2018
Department of Computer Science

Research Scholar, Semiconductor Research Corporation — 2018 to 2021
SRC Research Scholars Program

EDUCATION

The University of North Carolina at Chapel Hill, Chapel Hill, NC

Ph.D., Computer Science, August 2021

- Thesis: *Mining Secure Behavior of Hardware Designs*
- Advisor: Cynthia Sturton
- Area: Hardware Security

M.S., Computer Science, August 2017

- Thesis: *Multi-core Cyclic Executives for Safety-Critical Systems*
- Advisor: Sanjoy Baruah
- Area: Real-Time Systems

The University of Chicago, Chicago, IL

B.S., Computer Science, March 2015

- Thesis: *Performance and Energy Limits of a Processor-integrated FFT Accelerator*
- Advisor: Andrew A. Chien
- Area: Computer Architecture

B.A., Mathematics, March 2015

EXTERNAL RESEARCH FUNDING

National Science Foundation's Scholarships in Science, Technology, Engineering, and Mathematics — 2022 to 2028
- NSF Award # 2221694,
- Co-Principal Investigator 2024-, Senior Personnel 2022-2024
- Total Intended Award Amount: $1,499,246.00

Collaborative Research: SaTC: CORE: Medium: Hardware Security Insights: Analyzing Hardware Designs to Understand and Assess Security Weaknesses and Vulnerabilities — 2023 to 2027
- NSF Award # 2247756,
- Principal Investigator
- Total Intended Award Amount: $106,000.00

Refereed Journal Publications

[1] C. Deutschbein, A. Meza, F. Restuccia, R. Kastner, C. Sturton. Isadora: automated information-flow property generation for hardware security verification In: *Journal of Cryptographic Engineering*, November 2023. doi:10.1007/s13389-022-00306-w

[2] C. Deutschbein, A. Meza, F. Restuccia, R. Kastner, C. Sturton. Toward Hardware Security Property Generation at Scale In: *IEEE Security & Privacy*, April 2022. doi:10.1109/MSEC.2022.3155376

[3] R. Zhang, C. Deutschbein, P. Huang, C. Sturton. End-to-End Automated Exploit Generation for Processor Security Validation. *IEEE Design & Test Special Issue: Hardware Security Top Picks*. 2021. doi:10.1109/MDAT.2021.3063314

[4] C. Deutschbein, T. Fleming, A. Burns, S. Baruah. Multi-core Cyclic Executives for Safety-Critical Systems. *Science of Computer Programming*, March 2019. doi:10.1016/j.scico.2018.11.004

Refereed Conference Publications

[5] C. Deutschbein, J. Ostler, H, Raj. "vcd2df" – Leveraging Data Science Insights for Hardware Security Research In: *International Conference on Artificial Intelligence, Computer, Data Sciences and Applications (ACDSA)*, August 2025. doi:10.48550/arXiv.2505.06470

[6] C. Deutschbein, A. Stassinopoulos. "Test, Build, Deploy" – A CI/CD Framework for Open-Source Hardware Designs In: *International Conference on Electrical, Computer and Energy Technologies (ICECET)*, July 2025. doi:10.48550/arXiv.2503.19180

[7] S. Aftabjahani, M. Tehranipoor, F. Farahmandi, Farimah, B. Ahmed, R. Kastner, F. Restuccia, A. Meza, K. Ryan, N. Fern, J. van Woudenberg, R. Velegalati, C. Breunesse, C. Sturton, C. Deutschbein. Promising Directions for Automation of Security Assurance. In: *Special Session: CAD for Hardware Security at 2023 IEEE 41st VLSI Test Symposium (VTS)*, June 2023. doi:10.1109/VTS56346.2023.10140100

[8] C. Deutschbein, A. Meza, F. Restuccia, R. Kastner, C. Sturton. Isadora: Automated Information Flow Property Generation for Hardware Designs. In: *Proceedings of the 5th Workshop on Attacks and Solutions in Hardware Security (ASHES)*, November 2021. doi:10.1145/3474376.3487286

[9] C. Deutschbein, C. Sturton. Evaluating Security Specification Mining for a CISC Architecture. In: *Proceedings of the IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, December 2020. doi:10.1109/HOST45689.2020.9300291

[10] R. Zhang, C. Deutschbein, P. Huang, C. Sturton. End-to-End Automated Exploit Generation for Processor Security Validation. In: *MICRO-51: Proceedings of the 51st Annual IEEE/ACM International Symposium on Microarchitecture*, October 2018. doi:10.1109/MICRO.2018.00071

[11] C. Deutschbein, T. Fleming, A. Burns, S. Baruah. Multi-core Cyclic Executives for Safety-Critical Systems. In: *Proceedings of the Third International Symposium on Dependable Software Engineering: Theories, Repositorys, and Applications, SETTA 2017*, October 2017. doi:10.1016/j.scico.2018.11.004

[12] C. Deutschbein, S. Baruah. Preemptive Uniprocessor EDF Schedulability Analysis with Preemption Costs Considered. In: *Proceedings of the 2016 IEEE Real-Time Systems Symposium (RTSS)*, November 2016. doi:10.1109/RTSS.2016.047

[13] T. Thanh-Hoang, A. Shambayati, C. Deutschbein, H. Hoffmann, A. A. Chien Performance and energy limits of a processor-integrated FFT accelerator. In: *Proceedings of the 2014 IEEE High Performance Extreme Computing Conference (HPEC)*, September 2014. doi:10.1109/HPEC.2014.7040951

Invited Talks

[14] "Who ya gonna call?": Cybersecurity for the Spectre Era. Pacific University Mathematics, Computer Science, and Data Science Colloquium. 17 November, 2022.

[15] Isadora: Automated Information Flow Property Generation for Hardware Designs. 3rd Annual INTEL Side Channel Academic Program Workshop 2021. 11 November 2021.

[16] Isadora: Automated Information Flow Property Generation for Hardware Designs. Workshop on Secure RISC-V Architecture Design (secrisc-v'21). 7 November 2021.

[17] Creating Information Flow Specifications. Radix Presentation for Tortuga Logic. 20 August 2021.

[18] Extracting IF specifications from HW designs. University of Illinois–Urbana Champaign 20 July, 2021.

[19] "Who ya gonna call?": Cybersecurity for the Spectre Era. California State University Northridge Virtual Research Presentations: Computer Science and Cyber Security. 22 March, 2021.

Teaching Materials

Continuous Integration and Continuous Delivery Security
- WGU MS-SWE project
- External Subject Matter Expert - Content Design & Assessment Design

Network Architecture and Advanced Cloud Computing
- WGU MS-SWE project
- External Subject Matter Expert - Content Design & Assessment Design

chiTCP - A simple, testable TCP stack
- The UChicago χ-Projects,
- Contributor
- 14 stars / 26 watching / 11 forks on GitHub

Chair Service

Poster Session, Consortium for Computing Sciences in Colleges Northwestern Region (CCSC-NW 2024).

Inquiry-Based Learning for Computing-Based Sciences, Title III Grant Quantitative Reasoning (QR) Summer Learning Circles

Poster Session, Consortium for Computing Sciences in Colleges Northwestern Region (CCSC-NW 2023).

Coding and Automation Session, Northwest Scientific Association-American Association for the Advancement of Science Pacific Divison 2023

Program Committee Service

Hardware and Architectural Support for Security and Privacy (HASP 2025), co-located with MICRO 2025. https://haspworkshop.org/2025/committee.html

Consortium for Computing Sciences in Colleges Northwestern Region (CCSC-NW 2024). https://www.ccsc.org/northwest/2024/committee.html

Hardware and Architectural Support for Security and Privacy (HASP 2024), co-located with MICRO 2024. https://haspworkshop.org/2024/committee.html

Consortium for Computing Sciences in Colleges Northwestern Region (CCSC-NW 2023). https://www.ccsc.org/northwest/2023/committee.html

Hardware and Architectural Support for Security and Privacy (HASP 2023), co-located with MICRO 2023. https://haspworkshop.org/2023/committee.html

Real-time And intelliGent Edge computing workshop (RAGE 2023), co-located with CPS-IoT Week 2023. https://rage-workshop.github.io/2023/organizers/

Hardware and Architectural Support for Security and Privacy (HASP 2022), co-located with MICRO 2022. https://haspworkshop.org/2022/committee.html

Sixth Workshop on Attacks and Solutions in Hardware Security (ASHES 2022), co-located with ACM CCS 2022. http://ashesworkshop.org/committees-2022