1-3.3) Christopher Daffron CS 530 HW3

Pipeline 1)

Inst	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
LD F2,0(Rx)	IF	ID	EX	MEM	–	–	–	–	WB																							
DIVD F8,F2,F0		IF	ID	–	–	–	–	–	EX	–	–	–	–	–	–	–	–	–	–	–	–	MEM	WB									
ADDD F4,F0,F4			IF	–	–	–	–	–	IF	–	–	–	–	–	–	–	–	–	–	–	–	ID	EX	–	MEM	WB						
ADDI Rx,Rx,#8																						IF	ID	–	EX	MEM	WB					
SD F4,0(Ry)																							IF	–	–	ID	EX	MEM	–	WB		
BNZ R20,Loop																										IF	ID	–	EX	MEM	WB	

Pipeline 2)

Inst	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
MULTD F2,F6,F2		IF	–	–	–	–	–	–	ID	EX	–	–	–	–	–	MEM	WB																	
LD F4,0(Ry)									IF	ID	–	–	–	–	–	EX	MEM	–	–	–	–	WB												
ADDD F10,F8,F2										IF	–	–	–	–	–	–	–	–	–	–	–	–	ID	EX	–	MEM	WB						
ADDI Ry,Ry,#8																							IF	ID	–	EX	MEM	WB					
SUB R20,Ry,Rx																								IF	–	–	–	–	–	ID	EX	MEM	WB	

33 cycles per loop iteration

Assumption: Execution must be in order. No forwarding between separate pipelines

2-3.4) Instructions finishing out of order could be hazardous due to a WAW hazard and a WAR hazard.

WAW example: If ADDD F4,F0,F4 executed before LD F4,0(R7) then F4 would end up with the wrong value.

WAR example: If MULTD F2,F6,F2 executed before DIVD F8,F2,F0 then DIVD could read the wrong value.

3-3.11)

a)

Inst	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
LW R3,0(R0)	IF	ID	EX	MEM	–	–	WB														
LW R1, 0(R3)		IF	–	–	–	–	ID	EX	MEM	–	–	WB									
ADDI R1,R1,#1							IF	–	–	–	–	ID	EX	MEM	WB						
SUB R4,R3,R2												IF	ID	EX	MEM	WB					
SW R1,0(R3)													IF	–	ID	EX	MEM	–	–	WB	
BNZ R4, Loop														IF	ID	–	EX	–	MEM	WB	
LW R3,0(R0)																					IF

5 cycles

b) IF of second iteration LW starts in cycle 18, so 2 cycles are lost

c) IF of second iteration LW starts in cycle 16, so no cycles are lost

4-3.15a) Each iteration takes approx 10 cycles

Iteration	Instruction	Issues	Executes	Memory	CDB	Comments
1	LD F2,0(R1)	1	2	2	3	
1	MUL.D F4,F2,F0	2	4		19	Wait for F2
						Uses mult RS: 3-14
						Uses mult FU: 5-18
1	L.D F6,0(R2)	3	4	4	5	Uses ld buf: 4
1	ADD.D F6,F4,F6	4	20		30	Wait for F4
						Uses add RS: 5-20
						Uses add FU: 21-24
1	S.D F6,0(R2)	5	31	31		Wait for F6
						Uses SD buf 6-31
1	DADDIU R1,R1,#8	6	7		7	
1	DADDIU R2,R2,#8	7	8		9	

3.5a continued)

Iteration	Instruction	Issues	Executes	Memory	CDB	Comment
1	DSLTU R3,R1,R4	8	9		10	
1	BNEZ R3,foo	9	11			Wait for R3
2	L.D F2,0(R1)	10	12	12	13	Wait for BNEZ
						Uses ld buf 11-12
2	MUL.D F4,F2,F0	11	19		34	Wait for F2
						Wait for mult FU
						Uses mult RS 12-19
						Uses mult FU 20-33
2	L.D F6,0(R2)	12	13	13	14	Uses ld buf 13
2	ADD.D F6,F4,F6	13	35		43	Wait for F4
						Uses add RS 14-35
						Uses add FU 36-44
2	S.D F6,0(R2)	14	46	46		Wait for F6
						Uses SD buf 15-46
2	DADDIU R1,R1,#8	15	16		17	
2	DADDIU R2,R2,#8	16	17		18	
2	DSLTU R3,R1,R4	17	18		20	CDB conflict
2	BNEZ R3,foo	18	20			Wait for R3
3	L.D F2,0(R1)	19	21	21	22	Wait for BNEZ
						Uses LD buf 20-21
3	MUL.D F4,F2,F0	20	34		49	Wait for F2
						Wait for mult FU
						Uses mult RS 21-34
						Uses mult FU 35-48
3	L.D F6,0(R2)	21	22	22	23	Uses LD buf 22
3	ADD.D F6,F4,F6	22	50		60	Wait for F4
						Uses add RS 23-50
						Uses add FU 51-59
3	S.D F6,0(R2)	23	61	61		Wait for F6
						Uses SD buf 24-61
3	DADDIU R1,R1,#8	24	25		26	
3	DADDIU R2,R2,#8	25	26		27	
3	DSLTU R3,R1,R4	26	27		28	
3	BNEZ R3,foo	27	29			Wait for R3

3.15b)

Iteration	Instruction	Issues	Executes	Memory	CDB	Comments
1	L.D F2,0(R1)	1	2	2	3	Uses LD buf 2
1	MUL.D F4,F2,F0	1	4		19	Wait for F2 Uses mult RS 2-4 Uses mult FU 5
1	L.D F6,0(R2)	2	3	3	4	Uses LD buf 3
1	ADD.D F6,F4,F6	2	20		30	Wait for F6 Wait for F4 Uses add RS 3-20 Uses add FU 21
1	S.D F6,0(R2)	3	31	31		Wait for F6 Uses SD buf 4-31
1	DADDIU R1,R1,#8	3	4		5	
1	DADDIU R2,R2,#8	4	5		6	
1	DSLTU R3,R1,R4	4	6		7	INT FU busy Uses int RS 5-6
1	BNEZ R3,f0.	5	7			Wait for R3 INT FU busy Uses int RS 6-7
2	L.D F2,0(R1)	6	8	8	9	Wait for BNEZ
2	MUL.D F4,F2,F0	6	10		25	Wait for F2 Uses mult RS 7-10 Uses mult FU 11
2	L.D F6,0(R2)	7	9	9	10	INT FU busy Uses int RS 8-9
2	ADD.D F6,F4,F6	7	26		36	Wait for F6 Wait for F4 Uses add RS 8-26 Uses add FU 26
2	S.D F6,0(R2)	8	37	37		Wait for F6
2	DADDIU R1,R1,#8	8	10		11	INT FU busy Uses int RS 9-10
2	DADDIU R2,R2,#8	9	11		12	INT FU busy Uses int RS 10-11

Iteration	Instructions	Issues	Executes	Memory	CDB	Comments
2	DSLTU R3,R1,R4	9	12		13	Wait for R1 Uses int RS 10-12
2	BNEz R3,foo	10	14			Wait for R3
3	L.D F2,0(R1)	11	15	15	16	Wait for BNEz
3	MVL.D F4,F2,F0	11	17		32	Wait for F2 Uses mvl RS 12-17 Uses mvl FU 17
3	L.D F6,0(R2)	12	13	13	14	
3	ADD.D F6,F4,F6	12	33		43	Wait for F4 Wait for F6 Uses add RS 13-33 Uses add FU 33
3	S.D F6,0(R2)	13	44	44		Wait for F6 Uses int RS 14-44
3	DADDIU R1,R1,#8	15	16		17	All INT RS full Uses int RS 15-16
3	DADDIU R2,R2,#8	16	17		18	All INT RS full Uses int RS 16-17
3	DSLTU R3,R1,R4	17	18		19	All INT RS full Uses int RS 17-18
3	BNEz R3,foo	18	20			All INT RS full Wait for R3

Each iteration takes approx 6 cycles

5-3.16)

Instruction	Issues	Executes	Uses CDB
MUL.D F1,F2,F3	1	2	17
ADD R2,R2,R2	2	3	4
ADD R1,R1,R1	3	4	5
ADD R1,R1,R1	4	6	7
ADD R1,R1,R1	5	8	9
ADD R1,R1,R1	6	10	11
ADD R1,R1,R1	7	12	13
ADD R1,R1,R1	8	14	15
ADD R1,R1,R1	9	16	17 ← conflicts with MUL.D CDB access

6-(.1) a)

Reg	Src	Dest
R1	LD	DADDI
R1	DADDI	SD
R2	DADDI	DSUB
R4	DSUB	BNEZ

b)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
LD R1,0(R2)	F	D	E	M	W													
DADDI R1,R1,#1		F	-	-	D	E	M	W										
SD R1,0(R2)					F	-	-	D	E	M	W							
DADDI R2,R2,#4								F	D	E	M	W						
DSUB R4,R3,R2									F	-	-	D	E	M	W			
BNEZ R4,Loop												F	-	-	D	E	M	W
LD R1,0(R2)																		F

Assume PC not written until WB of branch.

Each loop instance takes 17 cycles

The loop iterates through $\frac{396}{4} = 99$ times

Total = (99)(17) = 1683 cycles

c)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
LD R1,0(R2)	F	D	E	m	W									
DADDI R1,R1,#1		F	D	-	E	m	W							
SD R1,0(R2)			F	-	D	E	m	W						
DADDI R2,R2,#4					F	D	E	m	W					
DSUB R4,R3,R2						F	D	E	m	W				
BNEZ R4,loop							F	-	D	E	m	W		
(bad inst)									F	-	-	-	-	
LD R1,0(R2)										F	D	E	m	W

Still 99 iterations

Now takes 9 cycles, except last which is now 8

Now takes $(99-1)(9)+8 = 890$

d)

	1	2	3	4	5	6	7	8	9	10	11	12	13
LD R1,0(R2)	F	D	E	m	W								
DADDI R1,R1,#1		F	D	-	E	m	W						
SD R1,0(R2)			F	-	D	E	m	W					
DADDI R2,R2,#4					F	D	E	m	W				
DSUB R4,R3,R2						F	D	E	m	W			
BNEZ R4,Loop							F	-	D	E	m	W	
LD R1,0(R2)									F	D	E	m	W

Still takes 99 iterations

Now takes 8 cycles, still takes 9 on last iteration

Now takes $(99-1)(8)+9 = 793$

7-C.7) a) 5 stage with data stalls = 6 cycles / 5 inst = $\frac{6}{5}$ CPI

12 stage with data stalls = 11 cycles / 8 inst = $\frac{11}{8}$ CPI

$$\text{Speedup} = \frac{\text{Exec Time}_5}{\text{Exec Time}_{12}} = \frac{I \times \text{CPI} \times \text{CCT}}{I \times \text{CPI} \times \text{CCT}} = \frac{(6/5) \times 1\text{ns}}{(11/8) \times 0.6\text{ns}} = 1.45$$

b) $\text{CPI}_5 = \frac{6}{5} + (0.20)(0.05)(2) = 1.22$ CPI

$\text{CPI}_{12} = \frac{11}{8} + (0.20)(0.05)(5) = 1.425$ CPI

8-C.12) a)

Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
L.D F2,0(R1)	IF	ID	EX	MEM	WB																		
MUL.D F4,F2,F0		IF	ID	–	M1	M2	M3	M4	M5	M6	M7	MEM	WB										
L.D F6,0(R2)			IF	–	ID	EX	MEM	WB															
ADD.D F6,F4,F6				IF	ID	–	–	–	–	–	A1	A2	A3	A4	MEM	WB							
S.D 0(R2),F6					IF	–	–	–	–	–	ID	–	–	–	EX	MEM	WB						
DADDIU R1,R1,#8											IF	–	–	–	ID	EX	MEM	WB					
DADDIU R2,R2,#8															IF	ID	EX	MEM	WB				
SGTIU R3,R1,done																IF	ID	EX	MEM	WB			
BEQZ R3,foo																	IF	–	ID	MEM	WB		

First instruction enters WB in cycle 5

Last instruction enters WB in cycle 23

Cycles/Iteration = 23 - 5 = 18 cycles