ECE551 – Digital Systems Design
Homework Assignment 2
Due January 27 by beginning of class

1. Download and follow the instructions in the "ModelSim Tutorial (for ada servers)" posted on Blackboard. You will also need to download the two associated VHDL files "counter.vhd" and "tcounter.vhd".

2. Zoom into the first 5 counts for your counter simulation and print screen. You may want to zoom into just the wave window so that the results are easy to read. **Copy the waveform image into a DOC, ODT or other document file as a deliverable for this homework.**

3. Follow the example of the counter VHDL files to write your own VHDL code implementing an 8-bit adder that adds two 8-bit std_logic_vector inputs. Be as creative you like. **Save the VHDL code as a deliverable for this assignment.**

4. A test bench "tcounter.vhd" was included in the tutorial. Study this and create your own test bench VHDL code for simulating your 8-bit adder. **Save the VHDL code as a deliverable for this assignment. Also report on the details for how you simulate and verify the functionality of your adder VHDL.**

5. Following the same steps as in the tutorial, use ModelSim to simulate your 8-bit adder. **Capture the waveform from your simulation and copy the image into your homework.**

   Deliverables:
   - Waveform from tutorial simulation
   - VHDL of 8-bit adder
   - VHDL of 8-bit adder test bench
   - Waveform from 8-bit adder simulation