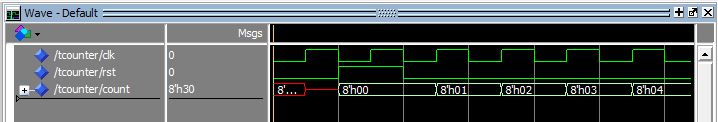
Christopher Daffron

ECE 551: Digital Systems Design

Homework 2

January 27, 2015

**Tutorial Waveform**

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**Adder VHDL**

See attachment

**Testbench VHDL**

See attachment

**Testbench Procedure**

I decided to test the adder by feeding the output back in as one of the inputs. I first got the process started by setting both of the inputs to be 1. Then, I waited for a positive clock edge to allow the adder to add them together. Then, on every falling clock edge, I set the first input to be the output of the counter. I ran the simulation for 500 ns and it added the values together correctly.

**Adder Waveform**

