Lab #1 Report

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2014.10.26



# Cache Simulator

For development of our cache simulator we decided to use Python. Neither of us has a large amount of experience with Python, so we thought it would be a good opportunity to try out a new language while working on the simulator. Python adds some nice functionality such as the **argparse** library. This library allows us to easily enforce the use of command-line arguments, as well as prompting the user with a help menu if an improper combination of arguments is passed to the program.

While we could have provided default values for the arguments required by the simulator, we opted to make all of the arguments explicit. From the command-line, a user can run the cache simulator with varying levels of cache, ranging from L1 up to L3. In addition, each level of cache has its own arguments to define how it will function. These arguments include the cache’s block size, number of lines in the cache, the cache’s associativity, as well as the hit time. For the purposes of our simulator, miss time and hit time are equal. In addition to the arguments passed for each individual cache, there are four more arguments that must be user-supplied. These arguments hold true for all levels of cache and include the word size used, write time to main memory, the cache write policy, and a filename of a cache trace file to be used. In addition to these arguments, there is a non-required debug flag that can be set from the command line to provide more verbose output from the program.

We used a data structure to hold each of the entries in the cache. Each instance of a cache entry has four parameters. Three of these parameters; valid bit, tag, and last access are needed for both of the write policies used, write-through and write-back. In addition the fourth parameter, dirty bit, is needed only for the write-back write policy. At the start of a cache simulation, the program parses the user-supplied arguments, error checks the word size, block size, and number of lines to make sure all are a power of two. In addition variables for each level of cache simulated are initialized. These include, but are not limited to, the number of sets in the cache, set size, index, cache start block, cache end block and block offset. In addition, each level of cache is initialized.

Our cache implementation is fairly linear in its approach. The input file is parsed line by line to retrieve the address and the mode to use, either read or write. First, the L1 cache is looped through and the valid bit of each block is checked. When the valid bit of a block is set to true, its tag is compared against the address from the parsed line. If there is a match and the request is a read, then a cache hit occurs and the access time is updated. If there is a match and the request is a write the access time is updated and the dirty bit is set if the write policy is write-back.

If the address is not found in L1, then the same procedure takes place in L2. In addition, if the address was found in L1 and the write policy is set to write-through, then the L2 cache is updated as needed. The same general program flow takes place in L3 if the address was not found in L1 or L2. Next the cache takes a main memory write penalty if the request is a write and the write policy is write-through.

After checking for, and not finding, the address in any level of cache the program places the address in cache starting with L3. The program loops through the range of L3 set addresses and if an empty block is found, which is denoted by the valid bit being set to zero, the address is placed in the cache. The valid bit and tag are set, last access is updated, and the dirty bit is cleared. If there are no blocks that are empty, the program then loops through the appropriate set addresses and finds the block with the oldest access time and places the address in that least recently used (LRU) block while also updating the access time and setting the valid bit and tag. If the write policy is write-back, and the replaced address had its dirty bit set, then there is a write to main memory. After placing the address in the L3 cache, the program then continues by doing the same in the lower levels of cache. The logic for L2 and L1 are slightly more complicated when the write policy is write-back. When this is the write-policy, replacing using LRU also requires a write to higher levels of cache when the cache line being replaced has the dirty bit set.

Finally, the cache simulator outputs all of the appropriate information about the simulation. Hit and miss numbers for each level of simulated cache are output as well as the hit and miss ratio and the average memory access time (AMAT). If the user has set the aforementioned debug flag when running the simulation, much more information is displayed for each individual cache request.

# Testing Methodology

Since the cache simulator has a lot of flexibility in terms of the parameters that a user can set, it was necessary to test the simulator with varying trace files. We created test files programmatically using Python. The program used to create the test files, makeTestCases.py, is included in the tar file that included this document. The created test files contain anywhere from 65,535 to 1,048,575 cache requests. Read, Write, and random Read/Write trace files were created using the following criteria:

* Continuous from 0 to 1,048,575
* Even values from 0 to 1,048,575
* Every fourth value from 0 to 1,048,575
* Every eighth value from 0 to 1,048,575
* Every sixteenth value from 0 to 1,048,575

In addition a file with 1,048,575 requests was created using pseudo-random values between 0 and 4,294,967,295 with the Read or Write value randomized as well. The first five types were created to test out varying levels of spatial locality, while the final trace file was created to test out a disparate data set.

Each of the 16 trace files was tested using varying amounts of associativity, levels of cache, block size, word size, and number of blocks. The same write time to main memory and hit/miss times were used for all tests. Results can be seen in Figure X.