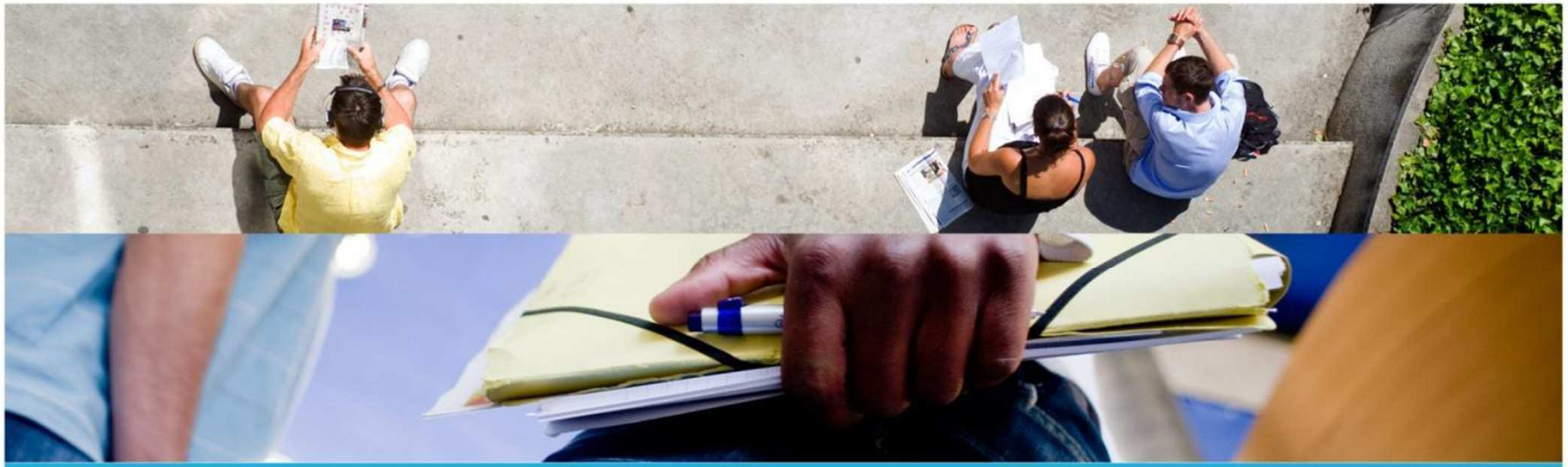


TC - 4ETI – CI : CAPTEURS INTELLIGENTS

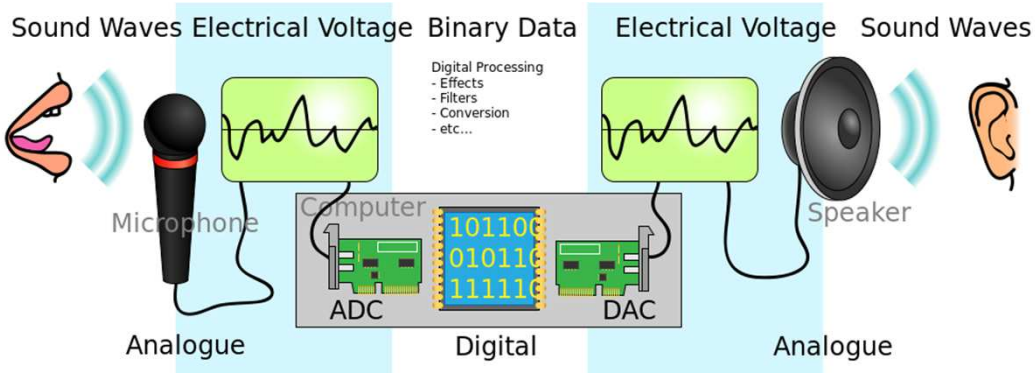
L. LABRAK

membre de UNIVERSITÉ DE LYON

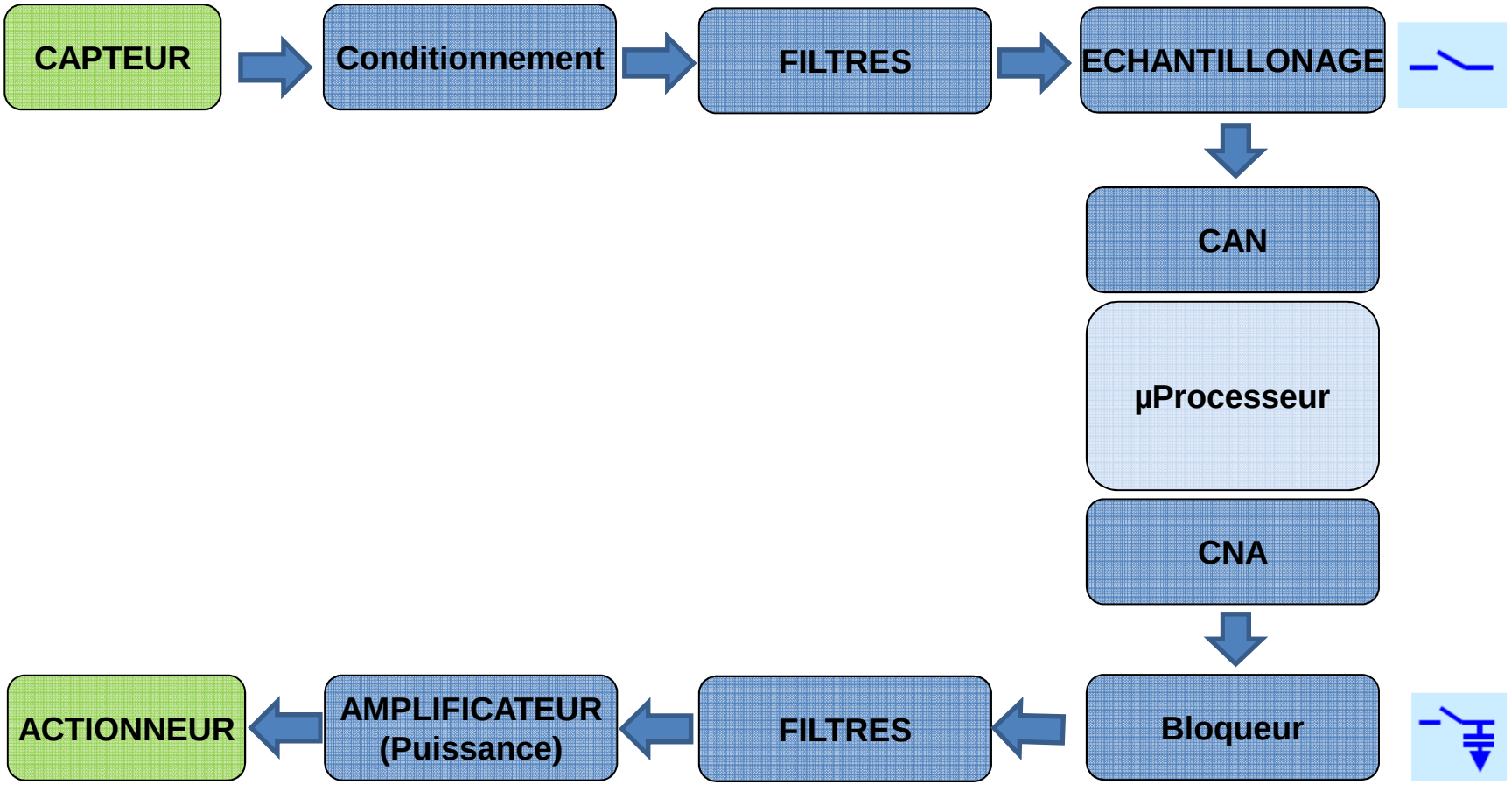
CPE LYON
ÉCOLE SUPÉRIEURE DE CHIMIE PHYSIQUE ÉLECTRONIQUE DE LYON

Section ETI :
Sciences du Numérique

CONVERSIONS DES SIGNAUX



La chaine d’acquisition

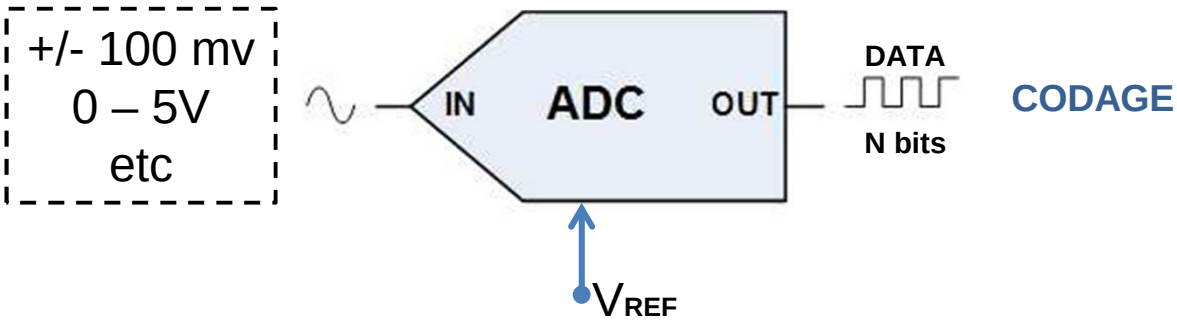


LES CAN (ou ADC)

CAN

Définitions

Entrée : simple ou différentielle



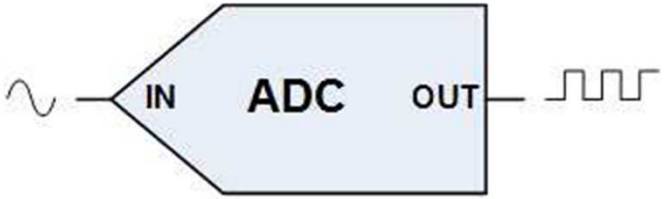
Q (Quantum) ou LSB (Last Significant Bit) => Résolution

$$1\ \mathrm{LSB} = \mathrm{FSR}/(2^n - 1)$$

Tension de pleine échelle (FSR) vs Tension de référence (V_{REF})

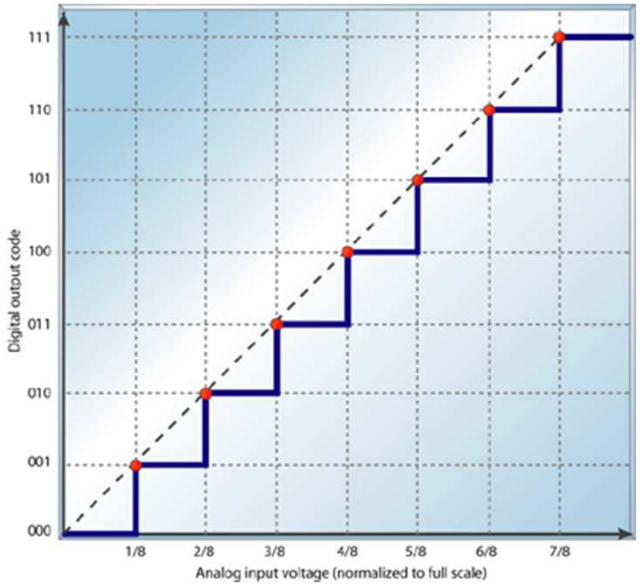
LES CAN (ou ADC)

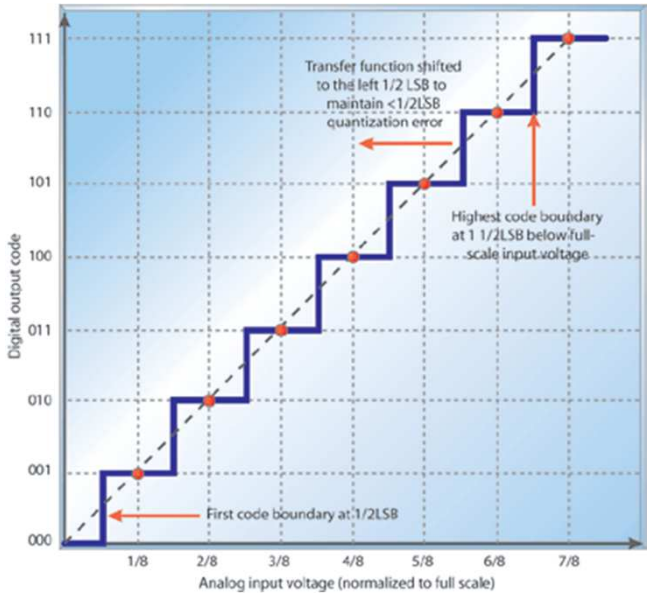
+/- 100 mv
0 – 5V
etc



CAN

Définitions





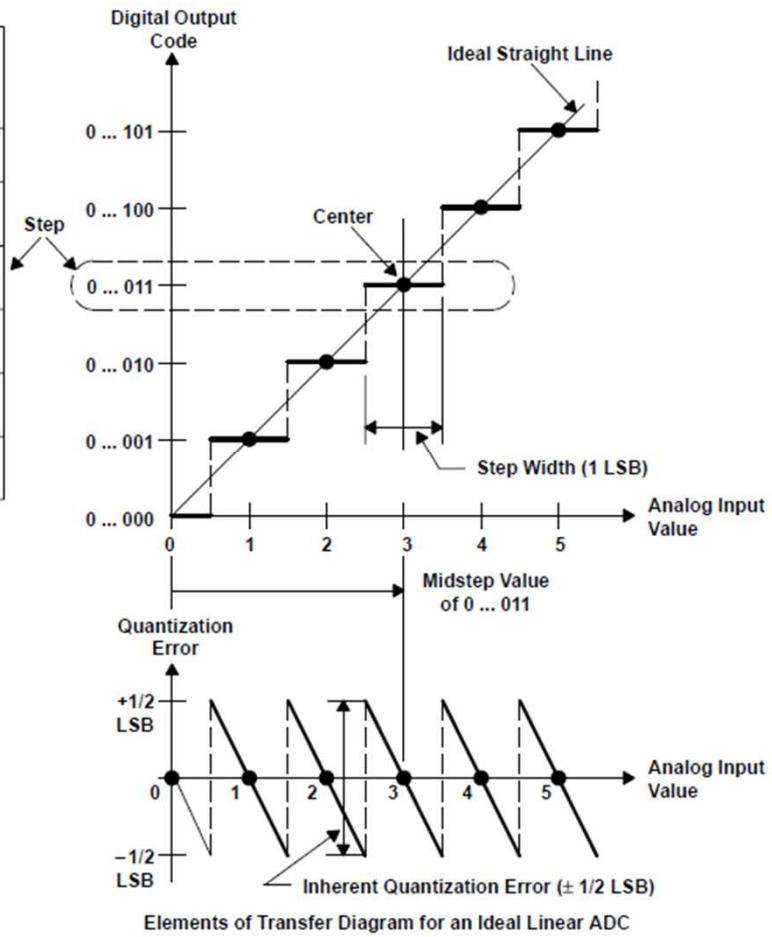
Caractéristique de transfert d'un CAN [1]

[1] Len Satller, Silicon labs, Application Notes

LES CAN (ou ADC)

CONVERSION CODE

RANGE OF ANALOG INPUT VALUES	DIGITAL OUTPUT CODE
4.5 • 5.5	0 ... 101
3.5 • 4.5	0 ... 100
2.5 • 3.5	0 ... 011
1.5 • 2.5	0 ... 010
0.5 • 1.5	0 ... 001
0 • 0.5	0 ... 000



Elements of Transfer Diagram for an Ideal Linear ADC

CAN

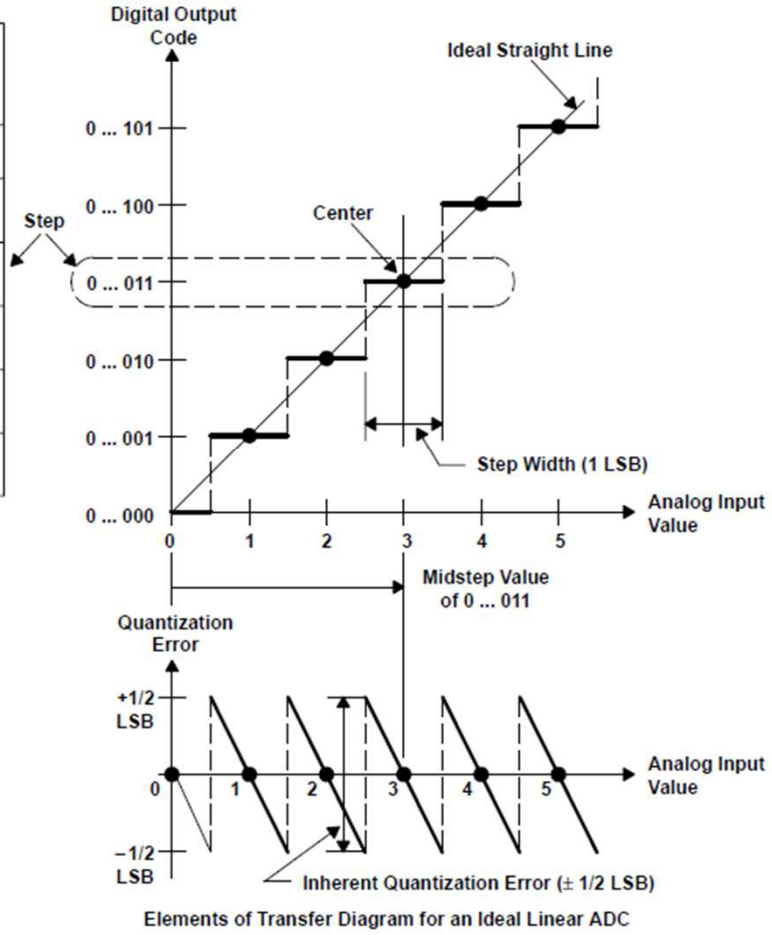
Erreur de quantification

Comment la réduire ?

LES CAN (ou ADC)

CONVERSION CODE

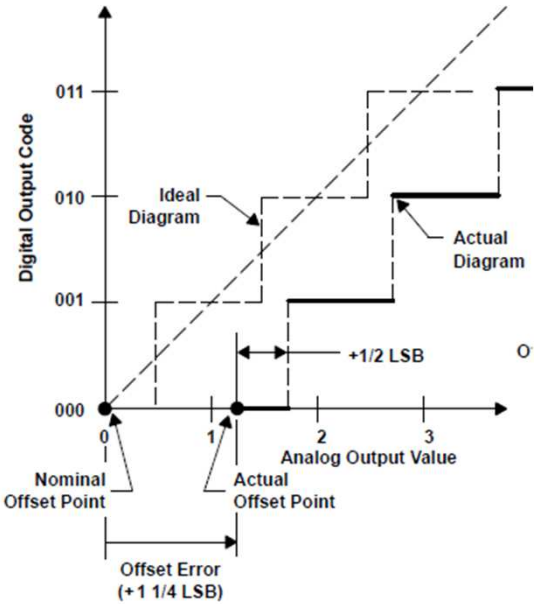
RANGE OF ANALOG INPUT VALUES	DIGITAL OUTPUT CODE
4.5 • 5.5	0 ... 101
3.5 • 4.5	0 ... 100
2.5 • 3.5	0 ... 011
1.5 • 2.5	0 ... 010
0.5 • 1.5	0 ... 001
0 • 0.5	0 ... 000



Elements of Transfer Diagram for an Ideal Linear ADC

CAN

Erreur de décalage



Constante sur toute la plage

LES CAN (ou ADC)

CONVERSION CODE

RANGE OF ANALOG INPUT VALUES	DIGITAL OUTPUT CODE
4.5 • 5.5	0 ... 101
3.5 • 4.5	0 ... 100
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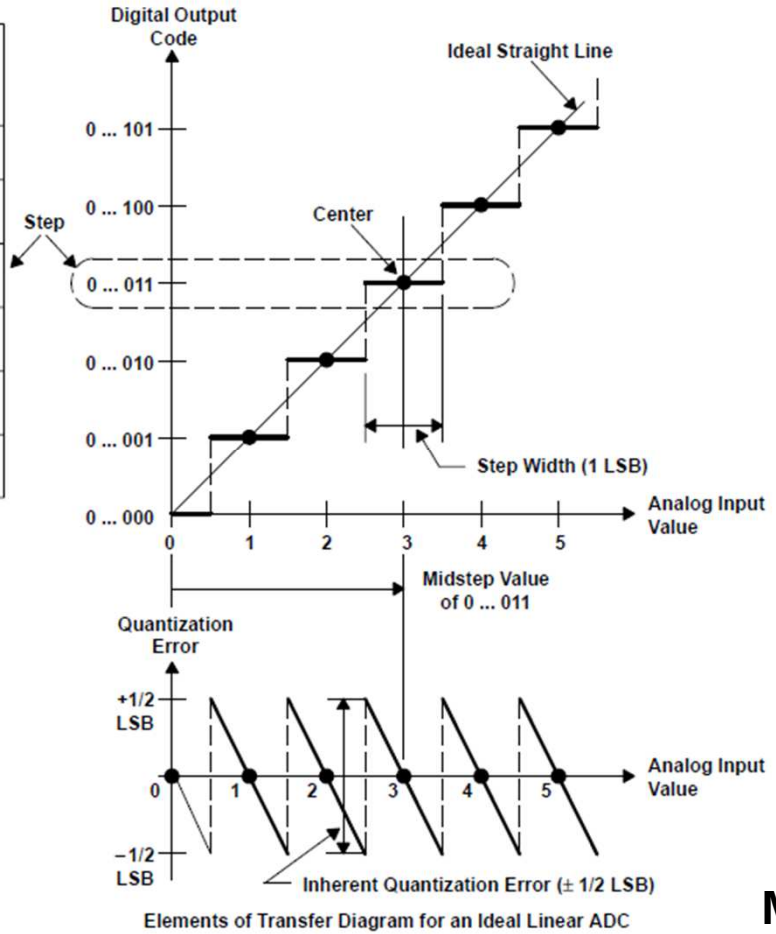
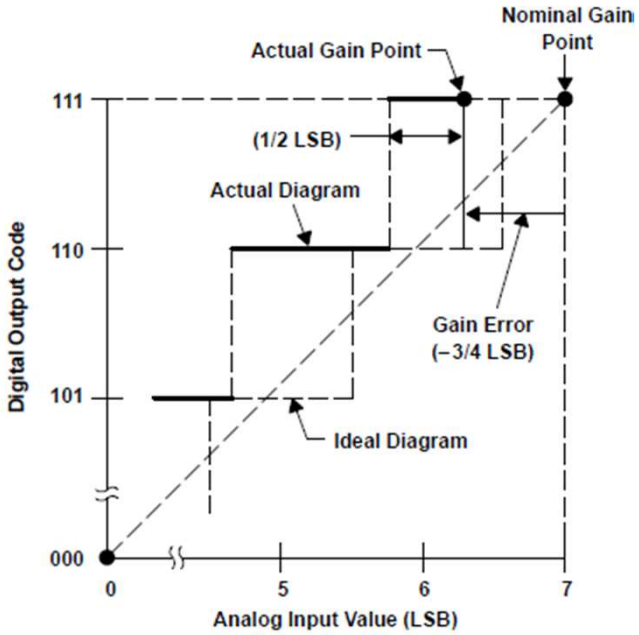


Elements of Transfer Diagram for an Ideal Linear ADC

CAN

Erreur de Gain



Mesurée sur la dernière transition

LES CAN (ou ADC)

CONVERSION CODE

RANGE OF ANALOG INPUT VALUES	DIGITAL OUTPUT CODE
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3.5 • 4.5	0 ... 100
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0.5 • 1.5	0 ... 001
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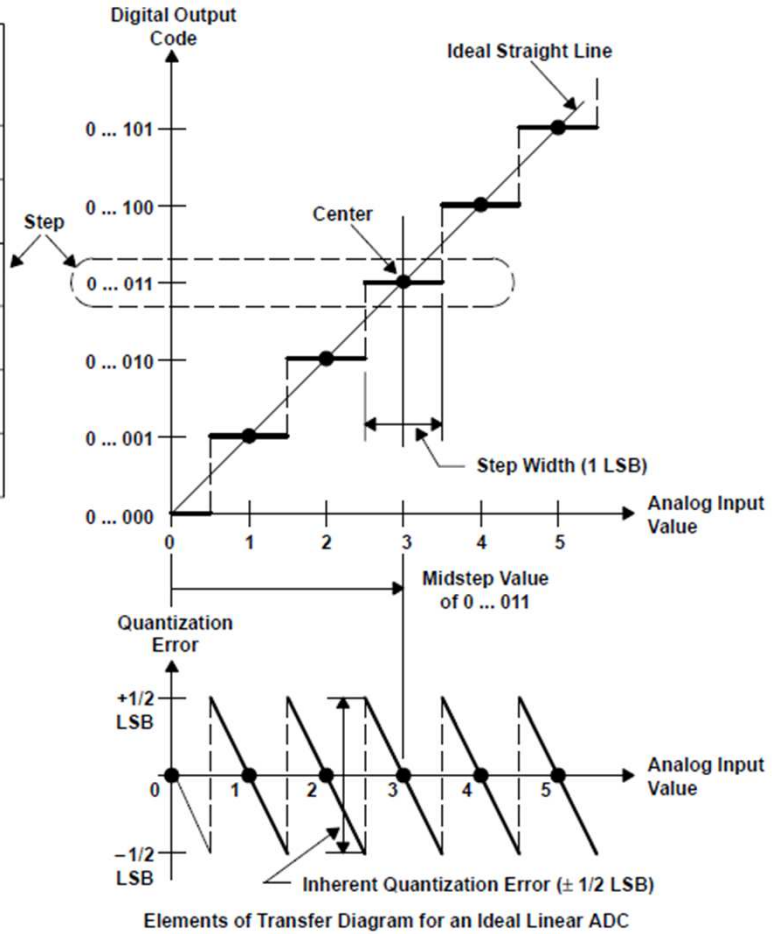
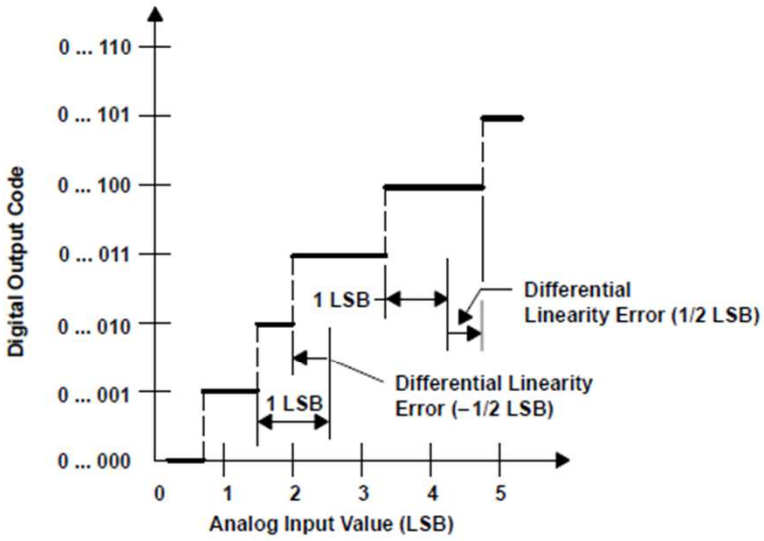


Elements of Transfer Diagram for an Ideal Linear ADC

CAN

DNL: Differential Non Linearity



Peut induire code manquant

LES CAN (ou ADC)

CAN

CONVERSION CODE

RANGE OF ANALOG INPUT VALUES	DIGITAL OUTPUT CODE
4.5 • 5.5	0 ... 101
3.5 • 4.5	0 ... 100
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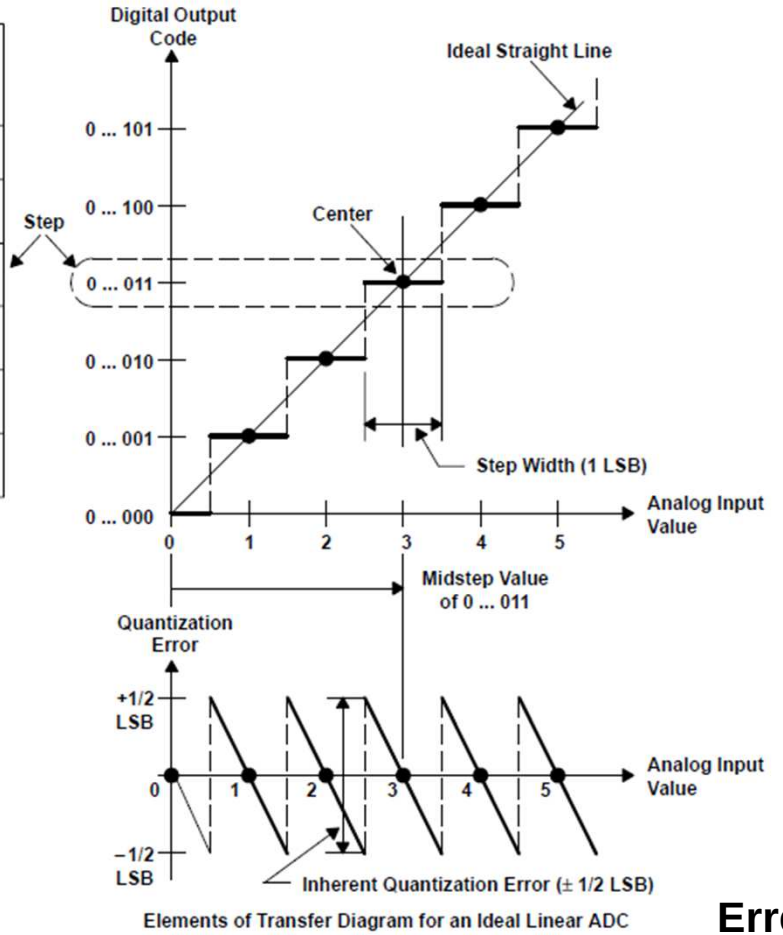
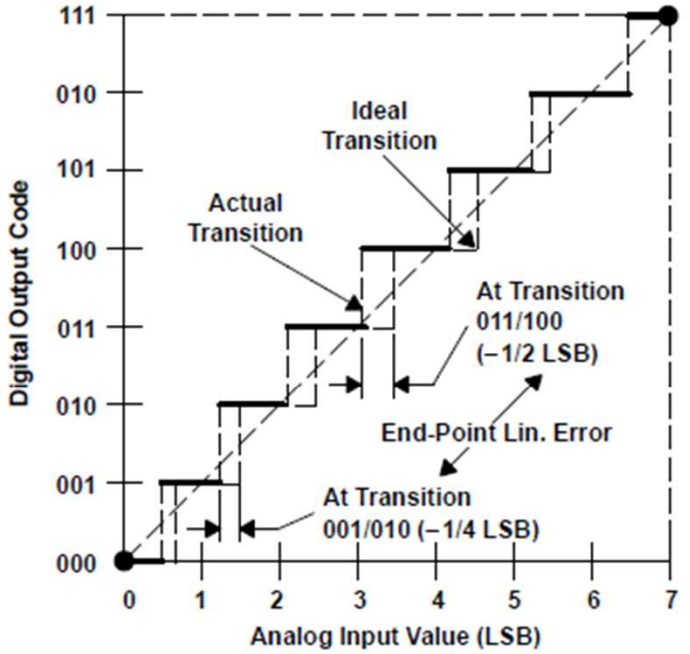
1.5 • 2.5	0 ... 010
0.5 • 1.5	0 ... 001
0 • 0.5	0 ... 000



Elements of Transfer Diagram for an Ideal Linear ADC

INL: Integral Non Linearity

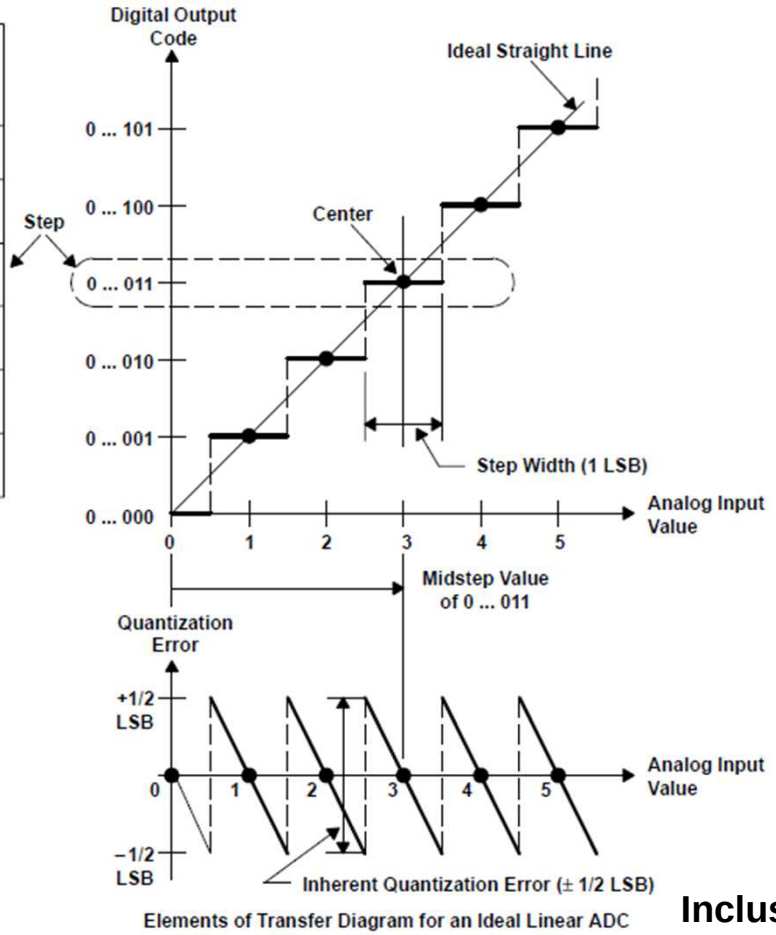


Erreur cumulative sur chaque transition

LES CAN (ou ADC)

CONVERSION CODE

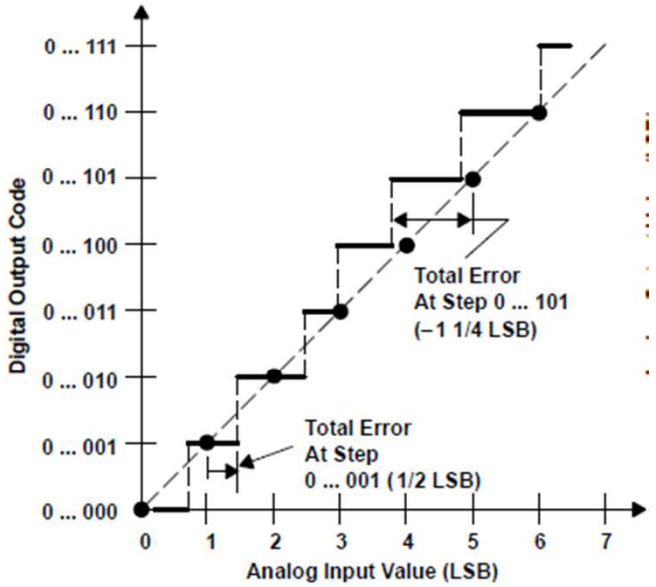
RANGE OF ANALOG INPUT VALUES	DIGITAL OUTPUT CODE
4.5 • 5.5	0 ... 101
3.5 • 4.5	0 ... 100
2.5 • 3.5	0 ... 011
1.5 • 2.5	0 ... 010
0.5 • 1.5	0 ... 001
0 • 0.5	0 ... 000



Elements of Transfer Diagram for an Ideal Linear ADC

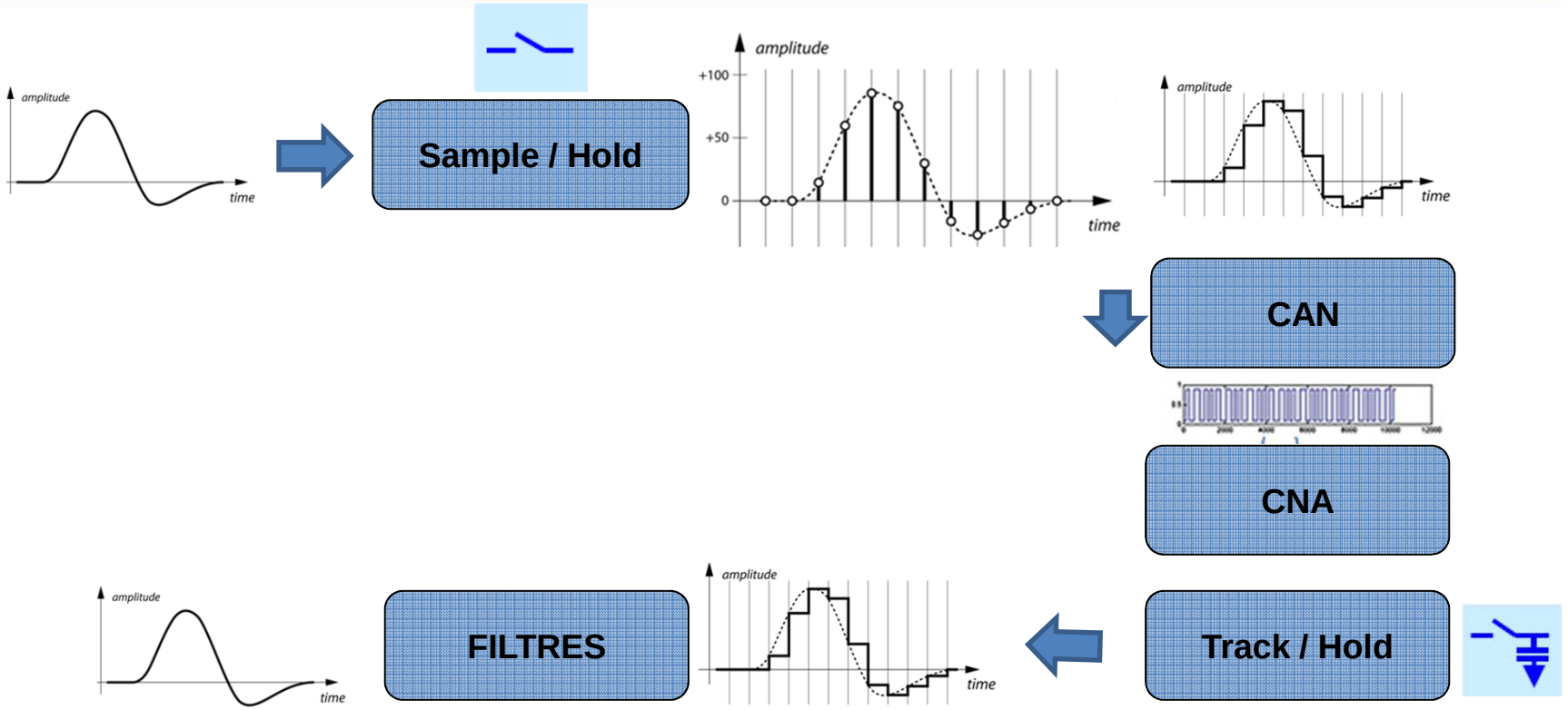
CAN

Total Error (Absolute Accuracy)



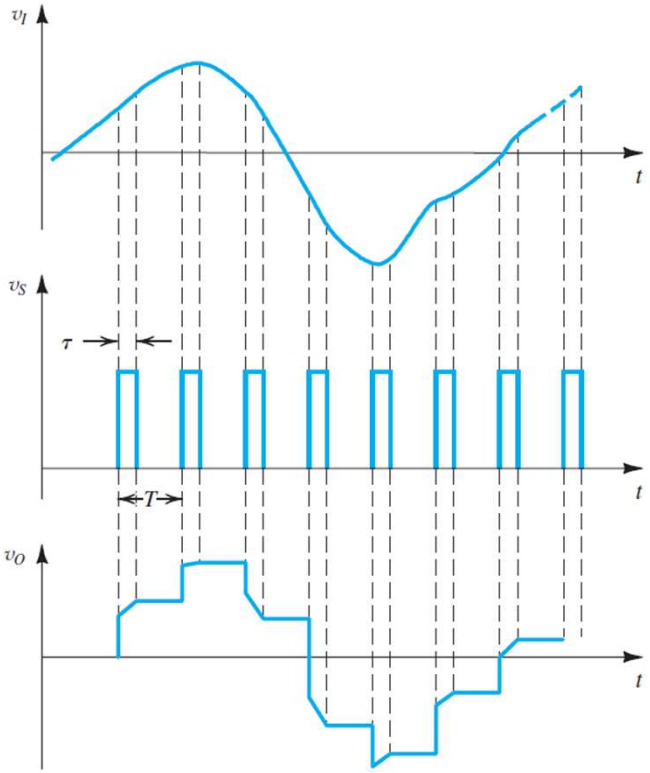
Inclus l'ensemble des défauts à chaque transition

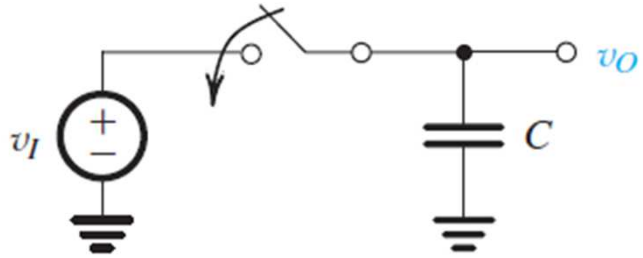
Retour sur l’échantillonage

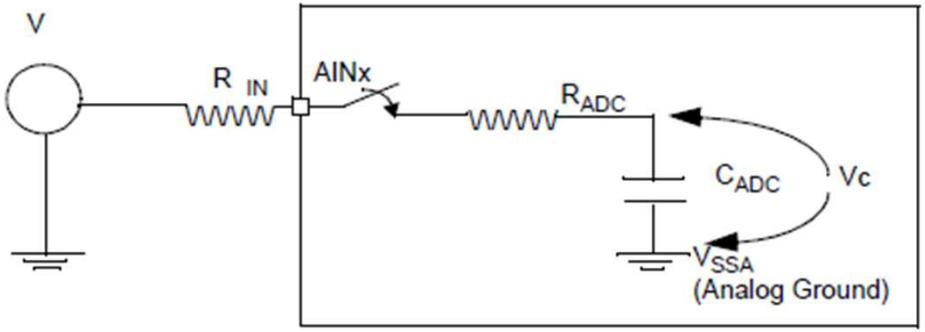


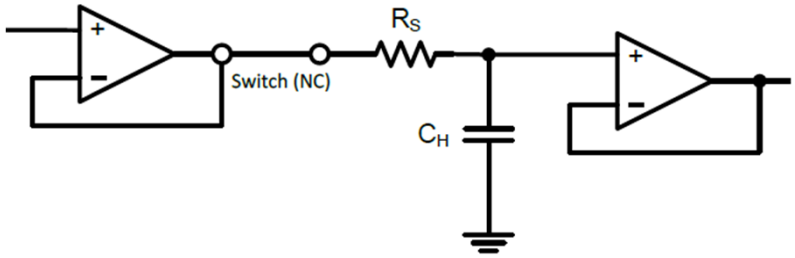
Retour sur l'échantillonnage

– Sample (Track) and Hold









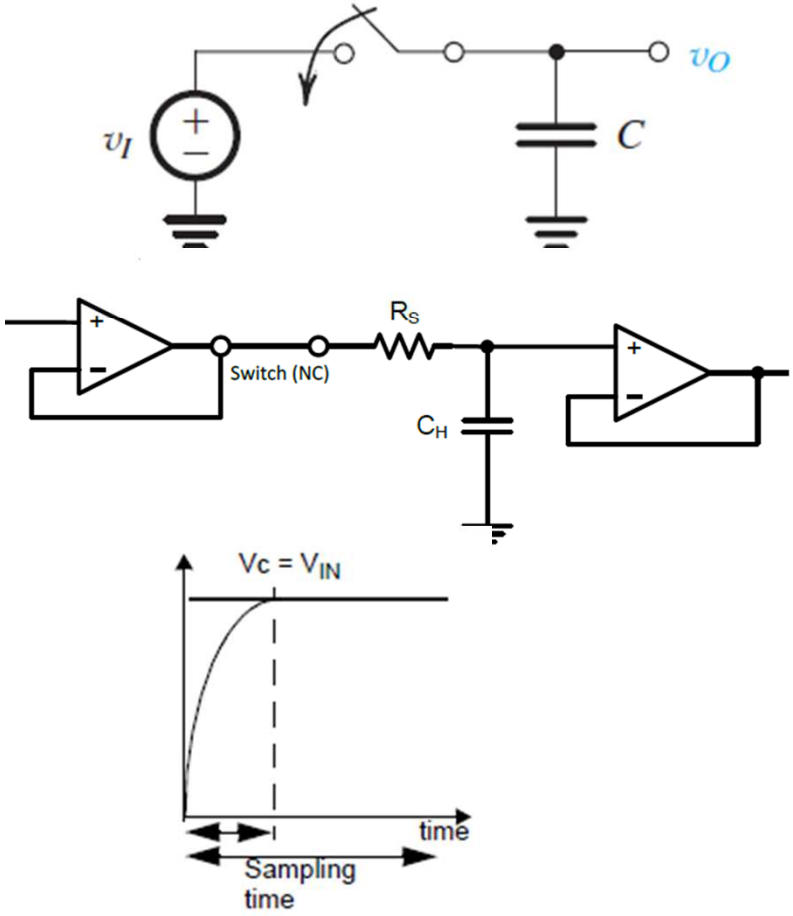
Retour sur l'échantillonnage

Acquisition Time (t_a):

Temps nécessaire à la capacité C_H pour se charger à la valeur de la tension V_{IN}

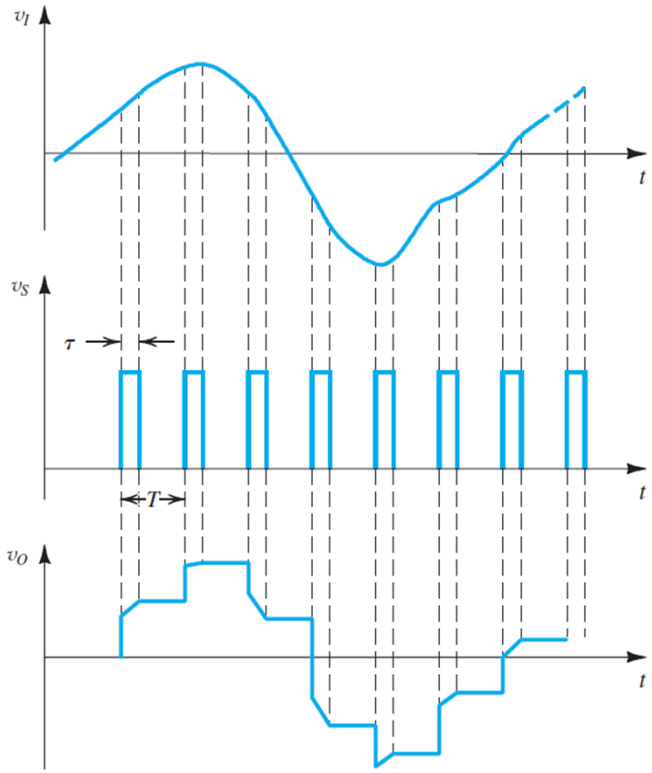
Il dépend de 3 facteurs:

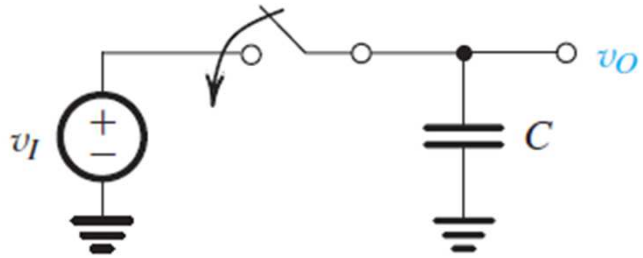
1. La constante de temps RC
2. Courant max de l'AOP
3. Slew rate de l'AOP

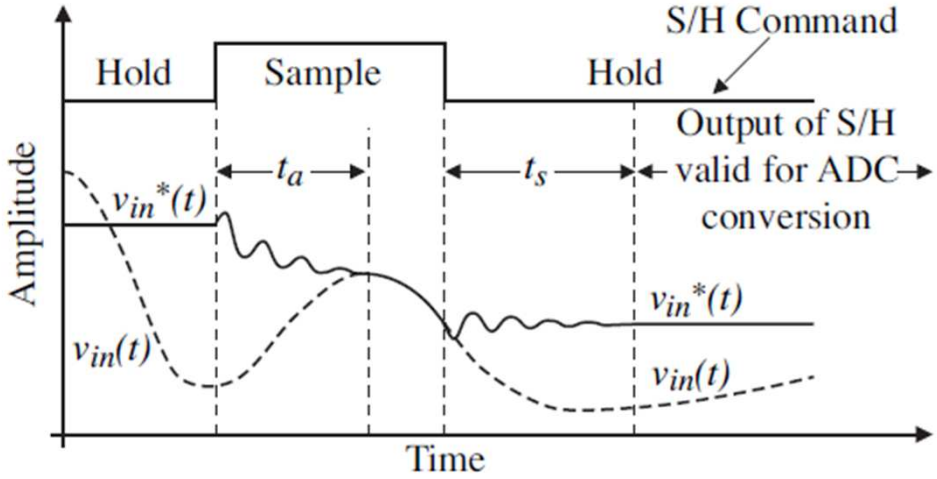


Retour sur l'échantillonage

– Sample and Hold







Retour sur l’échantillonage

Incertitude sur l’ouverture :

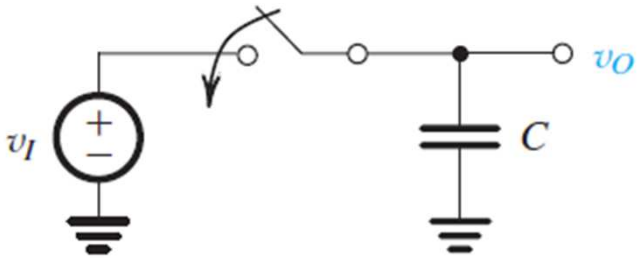
Variation du temps d’ouverture d’un échantillon à l’autre

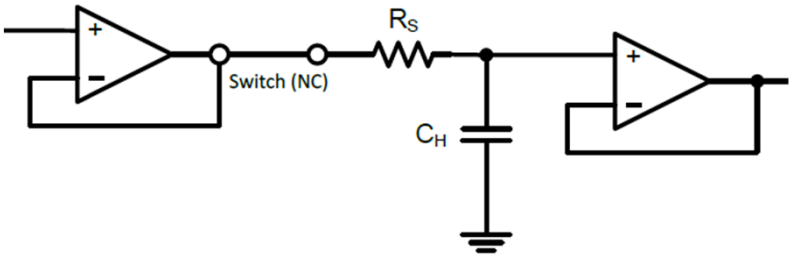
Temps d’établissement en mode bloqué :

Après application de la commande bloquage, il faut un certain temps pour atteindre le pourcentage d’erreur toléré 1%, 0.1%, 0.01%.

Offset :

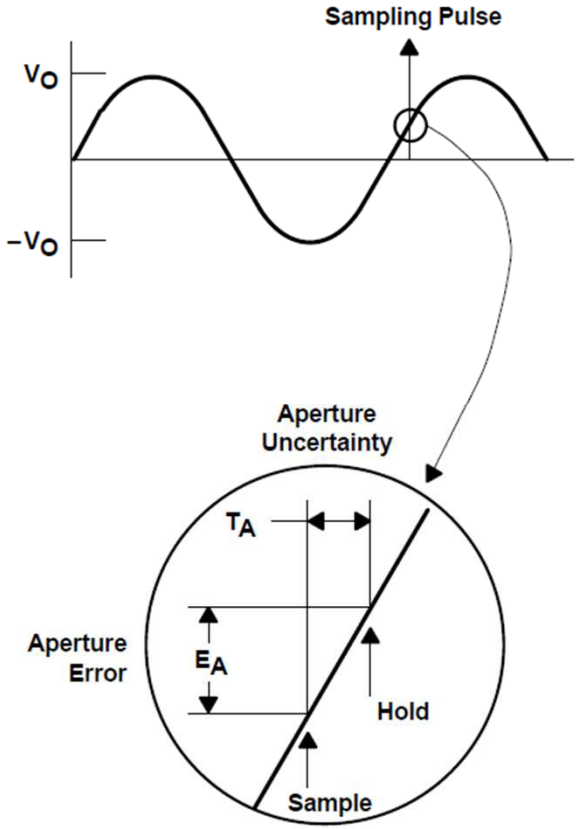
Au moment du passage du blocage à l’échantillonnage (et inversement) , il y a transfert de charge entre l’interrupteur (switch) et la capacité) => modification de la tension de sortie appelé pedestal error ou sample/hold offset

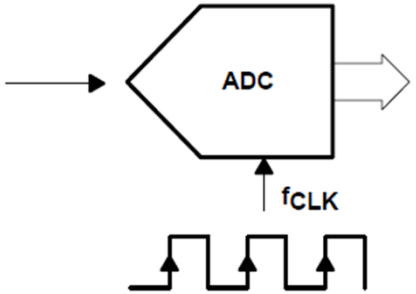




Retour sur l'échantillonnage

– Sample and Hold : variation max et fréquence





$$V = V_O \sin 2\pi f t$$

$$\frac{dV}{dt} = 2\pi f V_O \cos 2\pi f t$$

$$\left.\frac{dV}{dt}\right|_{max} = 2\pi f V_O$$

$$E_A = T_A \frac{dV}{dt} = 1/2\ LSB = \frac{2V_O}{2^{n+1}}$$

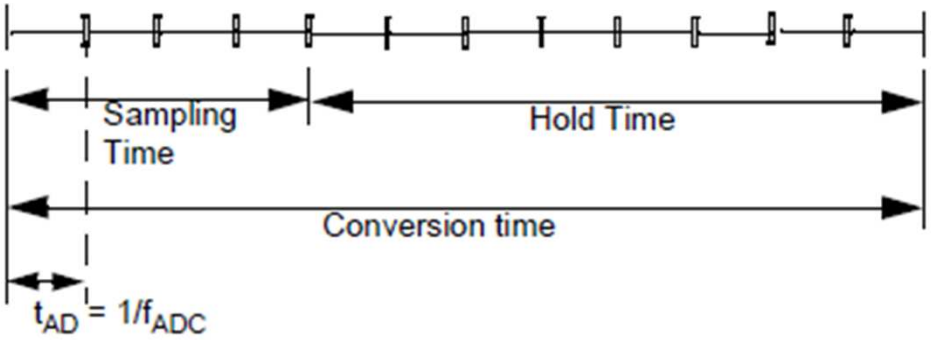
$$\frac{2V_O}{2^n + 1} = 2\pi f V_O T_A \Rightarrow$$

$$\boxed{f = \frac{1}{T_A \pi 2^n + 1}}$$

Performances dynamiques

– **Throughtput** et temps de conversion

- **100 MSPS** avec 13 clk => quelle est la fréquence d'horloge nécessaire?



- => 1/Throughput = NbrCycle* Tclk
- En déduire la fréquence max des signaux d'entrée

ADC0 du C8051F020

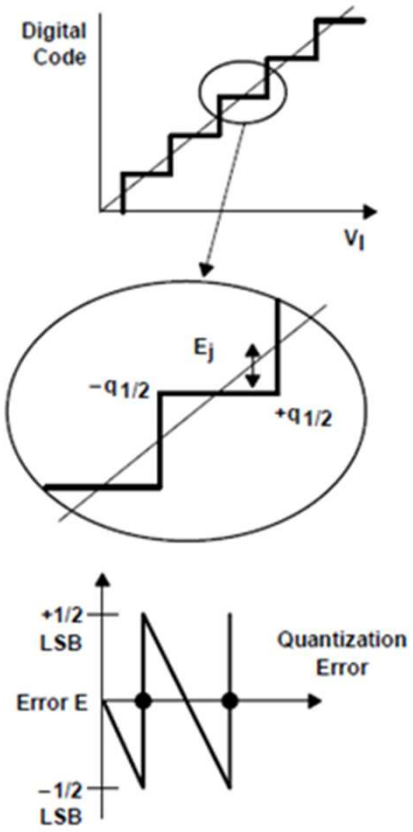
Table 5.1. 12-Bit ADC0 Electrical Characteristics (C8051F020/1)

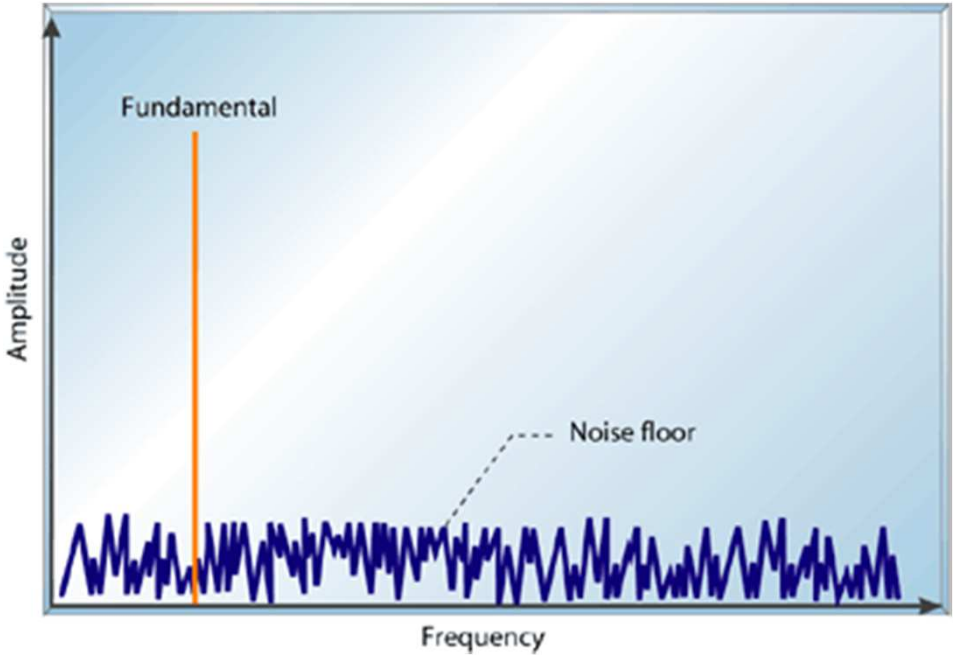
VDD = 3.0V, AV+ = 3.0V, VREF = 2.40V (REFBE=0), PGA Gain = 1, -40°C to +85°C unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY					
Resolution			12		bits
Integral Nonlinearity				±1	LSB
Differential Nonlinearity	Guaranteed Monotonic			±1	LSB
Offset Error			-3±1		LSB
Full Scale Error	Differential mode		-7±3		LSB
Offset Temperature Coefficient			±0.25		ppm/°C
DYNAMIC PERFORMANCE (10 kHz sine-wave input, 0 to 1 dB below Full Scale, 100 ksps					
Signal-to-Noise Plus Distortion		66			dB
Total Harmonic Distortion	Up to the 5th harmonic		-75		dB
Spurious-Free Dynamic Range			80		dB
CONVERSION RATE					
SAR Clock Frequency				2.5	MHz
Conversion Time in SAR Clocks		16			clocks
Track/Hold Acquisition Time		1.5			µs
Throughput Rate				100	ksps
ANALOG INPUTS					
Input Voltage Range	Single-ended operation	0		VREF	V
***Common-mode Voltage Range**	Differential operation	AGND		AV+	V
Input Capacitance			10		pF
TEMPERATURE SENSOR					
Nonlinearity		-1.0		+1.0	°C
Absolute Accuracy			±3		°C
Gain	PGA Gain = 1		2.86		mV/°C
Offset	PGA Gain = 1, Temp = 0°C		0.776		V
POWER SPECIFICATIONS					
Power Supply Current (AV+ supplied to ADC)	Operating Mode, 100 ksps		450	900	µA
Power Supply Rejection			±0.3		mV/V

Performances dynamiques

– Le SNR



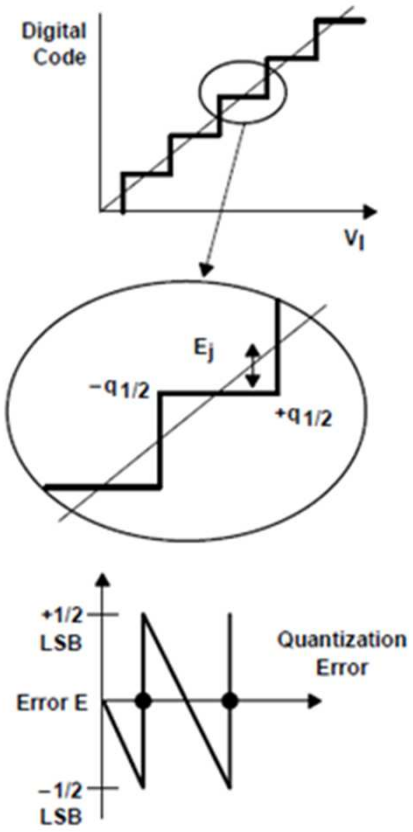


$$f_{eff} = \frac{1}{T}\int_0^T A^2 \sin^2 \omega t \, dt = \frac{A^2}{2}$$

$$E(\varepsilon^2) = \frac{1}{q}\int_{-q/2}^{+q/2} \varepsilon^2 d\varepsilon = \frac{q^2}{12}$$

Performances dynamiques

– Le SNR



Error at the jth step

$E_j = (V_j - V_I)$

The mean square error over the step

$$\overline{E}_j^2 = \frac{1}{q_1} \int_{-q/2}^{+q/2} E_j^2 \, dE = \frac{q^2}{12}$$

Assuming equal steps, the total error is

$\overline{N^2} = q^2/12$ (Mean square quantization noise)

For an input sine wave $F(t) = A \sin\omega t$, the signal power

$$\overline{F^2(t)} = \frac{1}{2\pi} \int_0^{2\pi} A^2 \sin^2\omega t \, d\omega t = \frac{A^2}{2}$$

and $$q = \frac{2A}{2^n} = \frac{A}{2^{n-1}}$$

$$SNR = 10 \text{ Log} \left(\frac{F^2}{n^2}\right) = 10 \text{ Log} \left(\frac{A^2/2}{A^2/3 \times 2^n}\right)$$

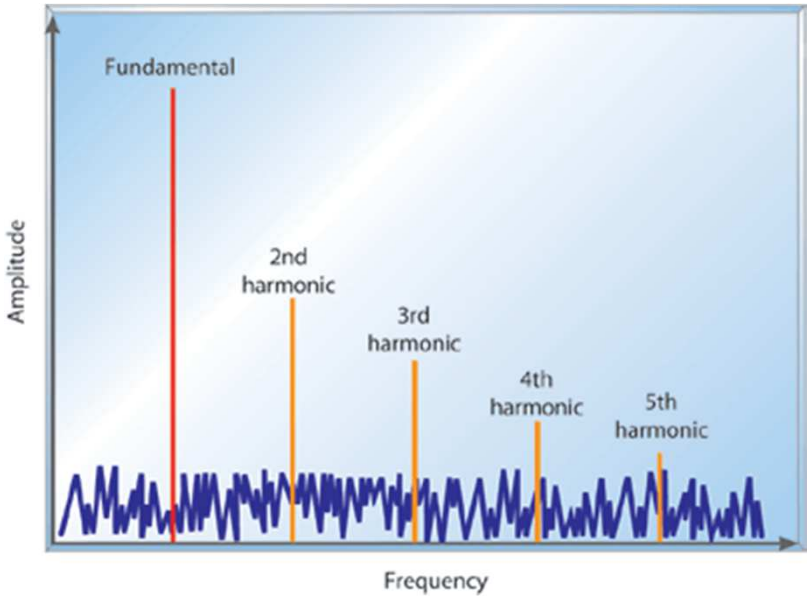
$$SNR = 6.02n + 1.76 \text{ dB}$$

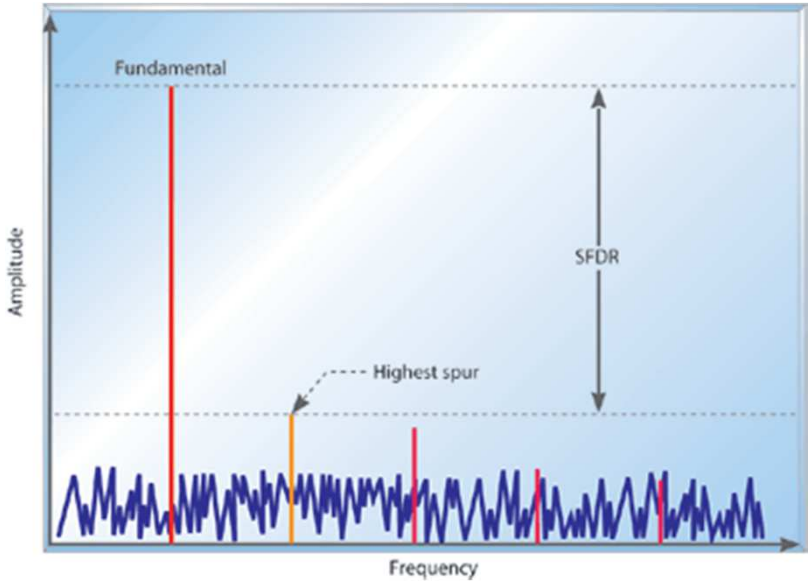
$$ENOB = \frac{SNR_{dB} - 1{,}76}{6{,}02}$$

Performances

– Dynamiques : THD – SINAD - SFDR

$$SNR = 20\log\left(\frac{S}{N}\right),$$





$$THD = 20\log\left(\frac{S}{D}\right) \qquad SINAD = 20\log\left(\frac{S}{N+D}\right)$$

ADC0 du C8051F020

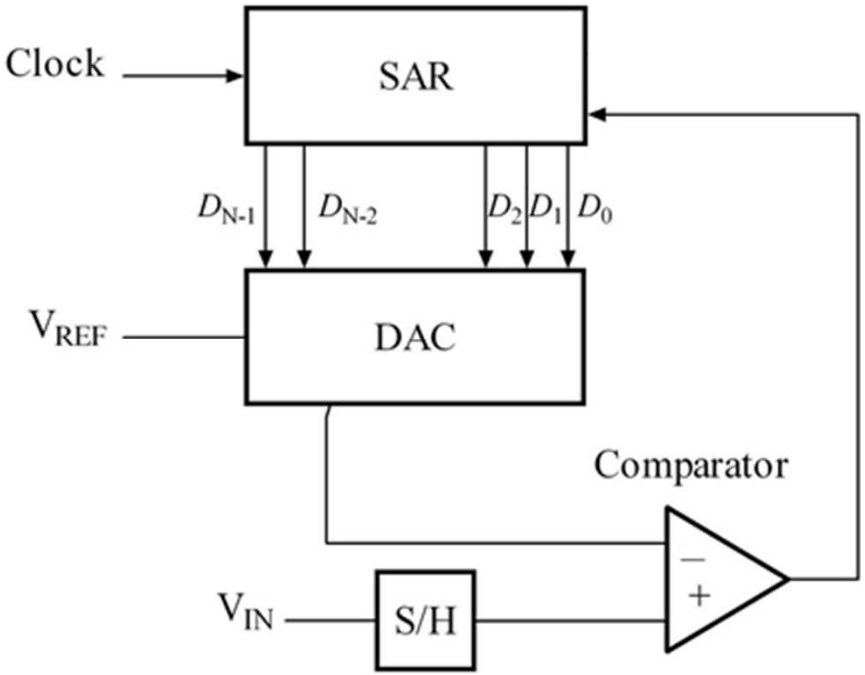
Table 5.1. 12-Bit ADC0 Electrical Characteristics (C8051F020/1)

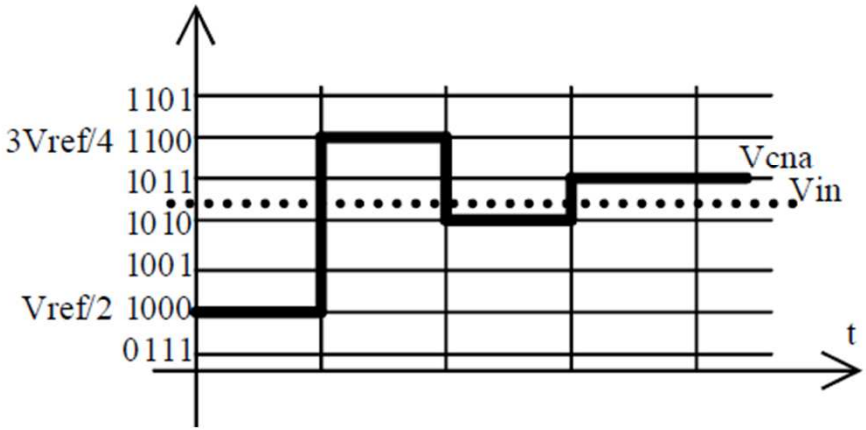
VDD = 3.0V, AV+ = 3.0V, VREF = 2.40V (REFBE=0), PGA Gain = 1, -40°C to +85°C unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY					
Resolution			12		bits
Integral Nonlinearity				±1	LSB
Differential Nonlinearity	Guaranteed Monotonic			±1	LSB
Offset Error			-3±1		LSB
Full Scale Error	Differential mode		-7±3		LSB
Offset Temperature Coefficient			±0.25		ppm/°C
DYNAMIC PERFORMANCE (10 kHz sine-wave input, 0 to 1 dB below Full Scale, 100 ksps					
Signal-to-Noise Plus Distortion		66			dB
Total Harmonic Distortion	Up to the 5th harmonic		-75		dB
Spurious-Free Dynamic Range			80		dB
CONVERSION RATE					
SAR Clock Frequency				2.5	MHz
Conversion Time in SAR Clocks		16			clocks
Track/Hold Acquisition Time		1.5			µs
Throughput Rate				100	ksps
ANALOG INPUTS					
Input Voltage Range	Single-ended operation	0		VREF	V
***Common-mode Voltage Range**	Differential operation	AGND		AV+	V
Input Capacitance			10		pF
TEMPERATURE SENSOR					
Nonlinearity		-1.0		+1.0	°C
Absolute Accuracy			±3		°C
Gain	PGA Gain = 1		2.86		mV/°C
Offset	PGA Gain = 1, Temp = 0°C		0.776		V
POWER SPECIFICATIONS					
Power Supply Current (AV+ supplied to ADC)	Operating Mode, 100 ksps		450	900	µA
Power Supply Rejection			±0.3		mV/V

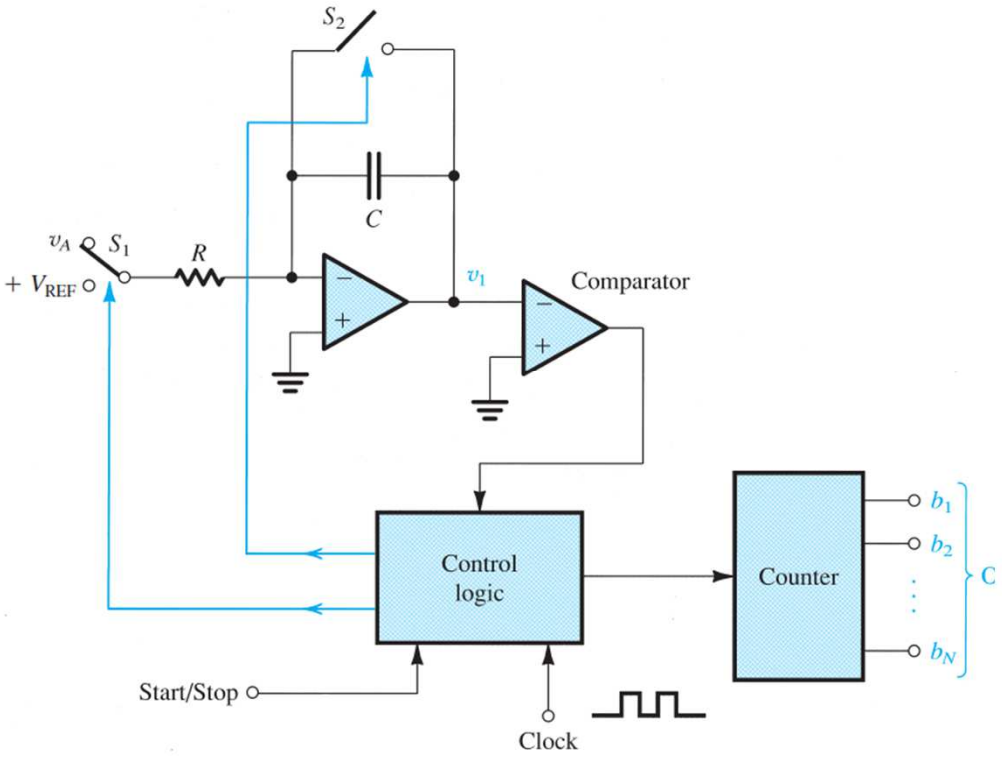
ARCHITECTURES : SAR

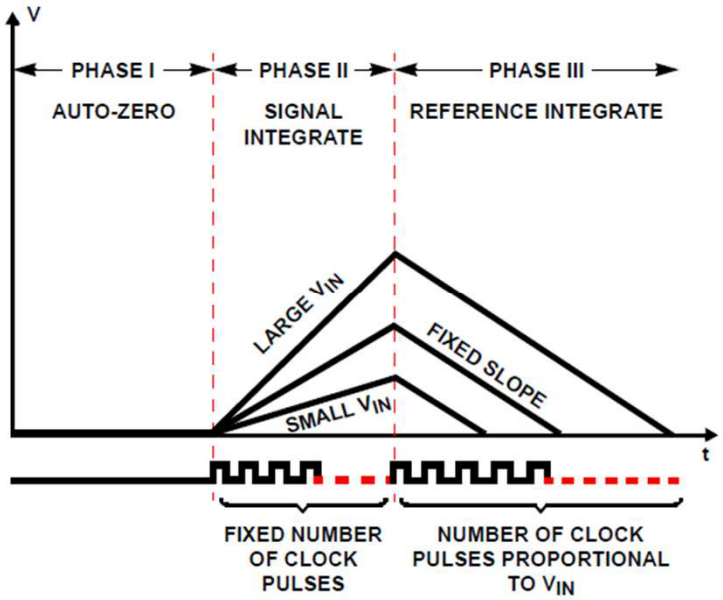
Registre à approximations successives



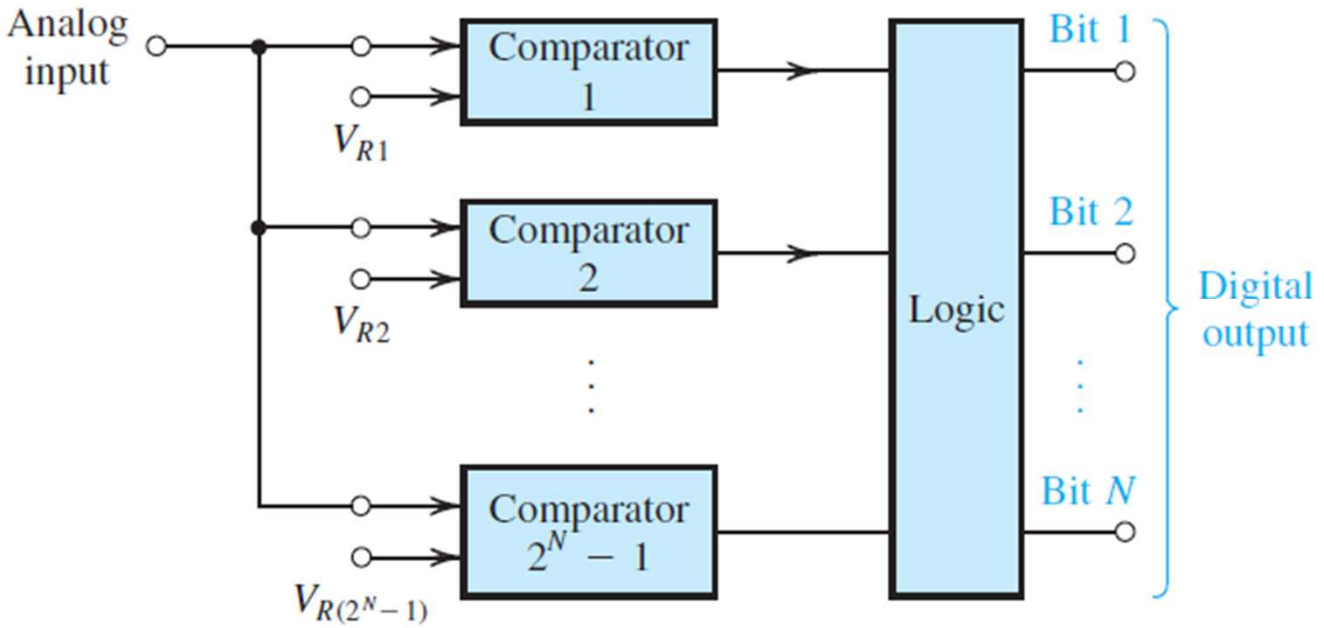


ARCHITECTURES : Double Rampe



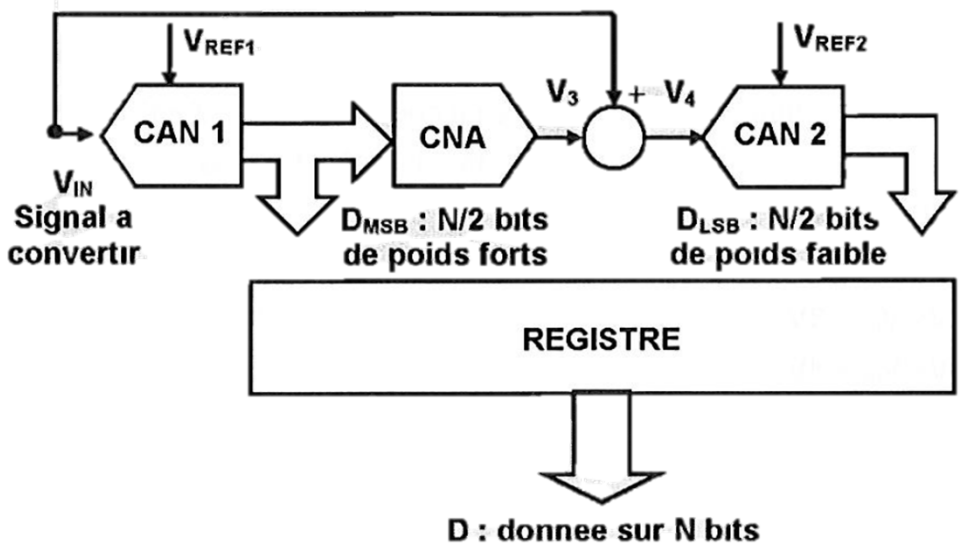


ARCHITECTURES : Flash et Semi-Flash



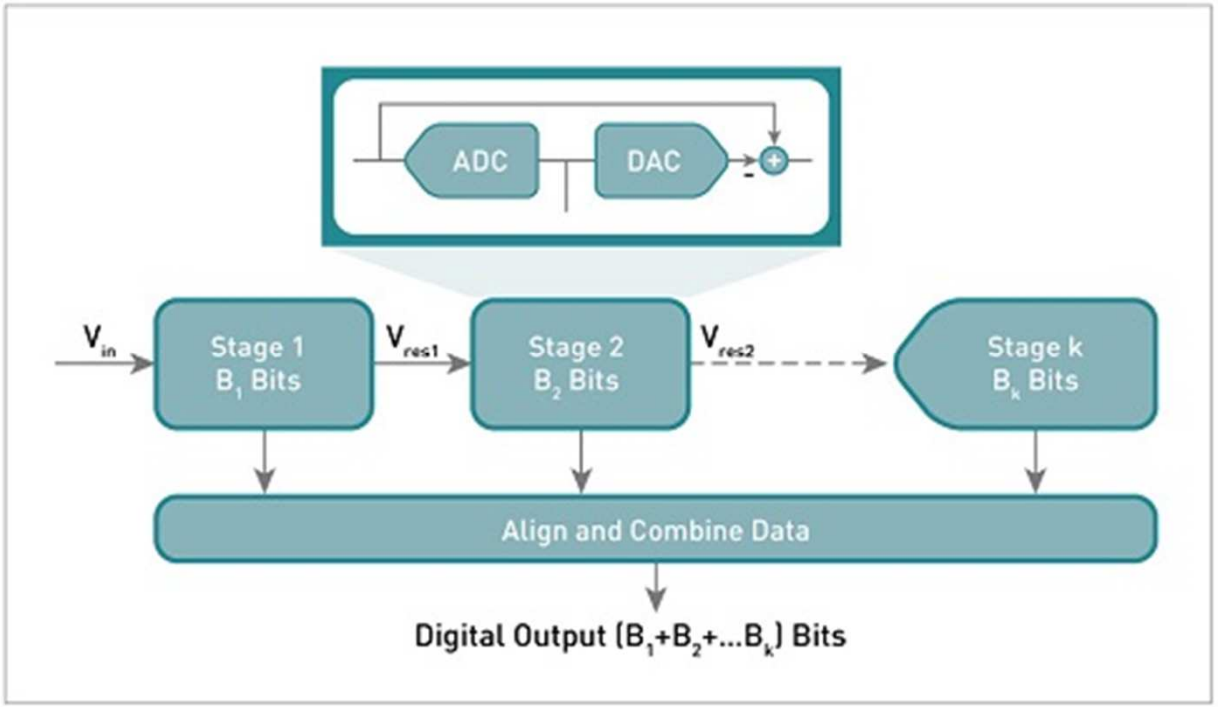
Le codeur détecte le nombre d'entrées au niveau 0 et code ce nombre sur N bits en sortie (A B C).

ARCHITECTURES : Flash et Semi-Flash

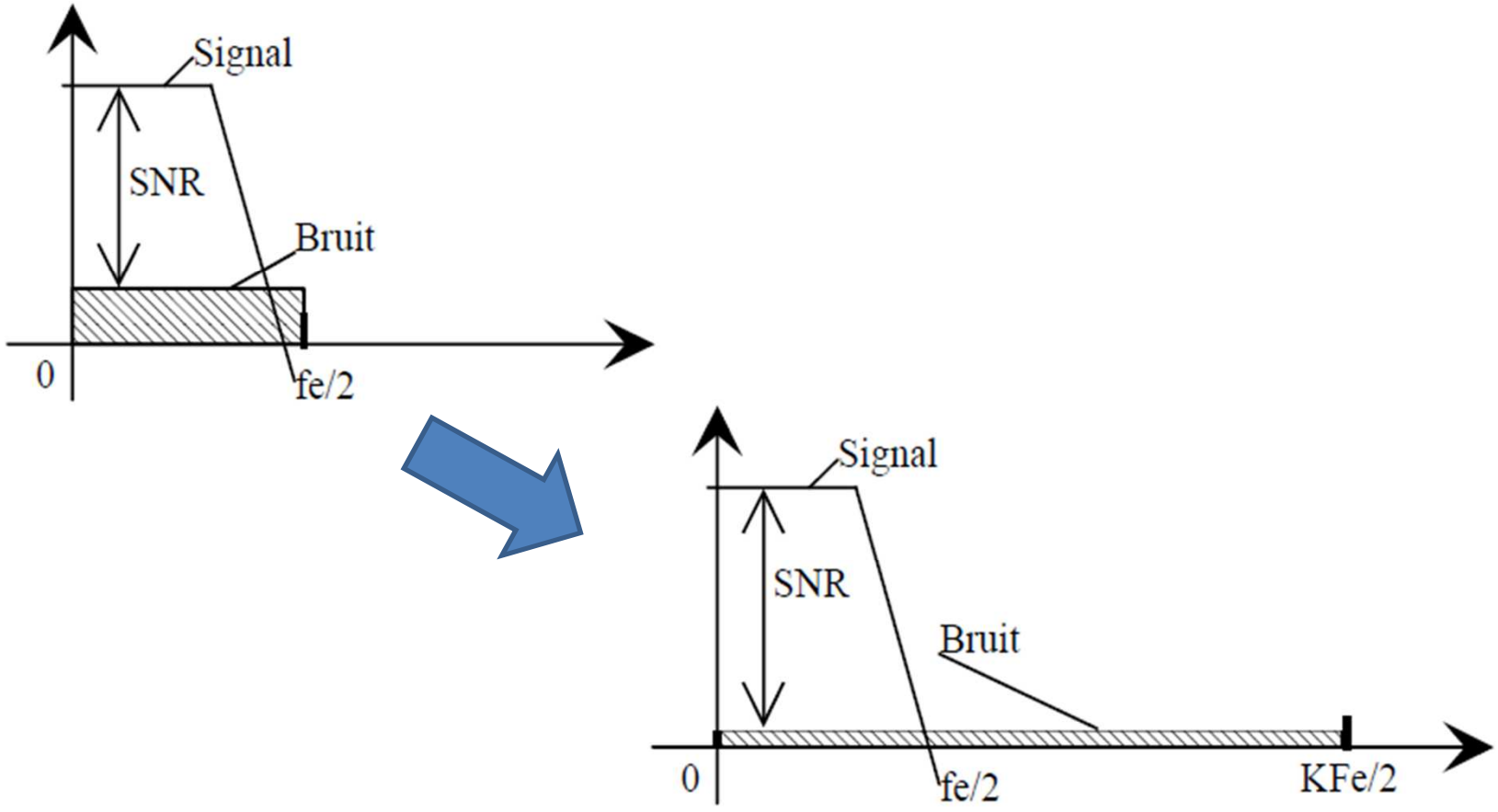


- Nous prenons le cas particulier $\mathbf{V_{IN} = 2.7\ V}$, calculer le nombre numérique $\mathbf{D_{MSB}}$ présent à la sortie du CAN1 (nous arrondirons à la valeur immédiatement inférieure).
- Calculer $\mathbf{V_3}$, la tension de sortie du CNA. En déduire $\mathbf{V_4}$, la tension d'entrée du CAN2.
- Calculer le nombre numérique $\mathbf{D_{LSB}}$ présent à la sortie du CAN2.
- En déduire la donnée **D**, résultat de la conversion à la sortie du registre.

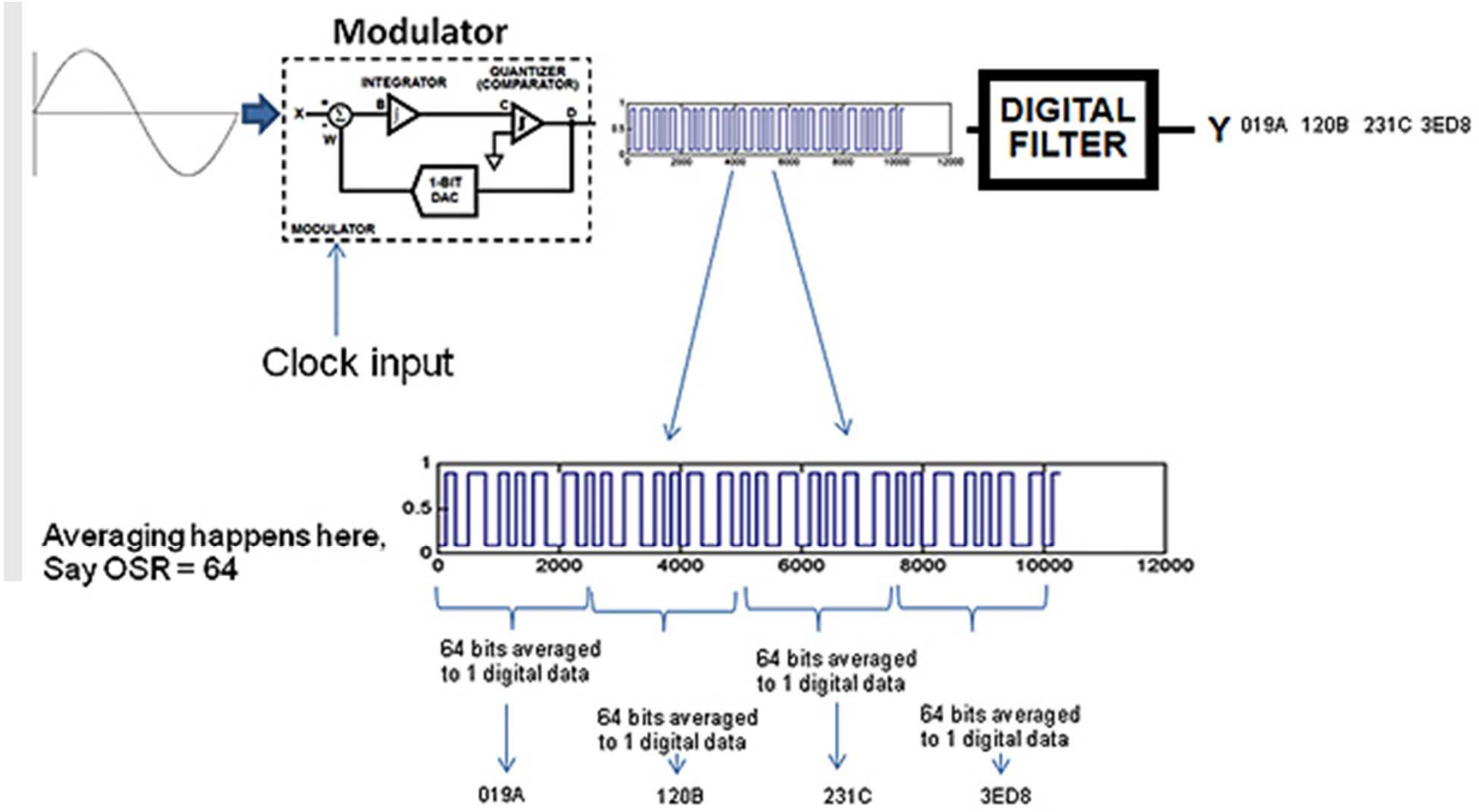
ARCHITECTURES : Pipeline



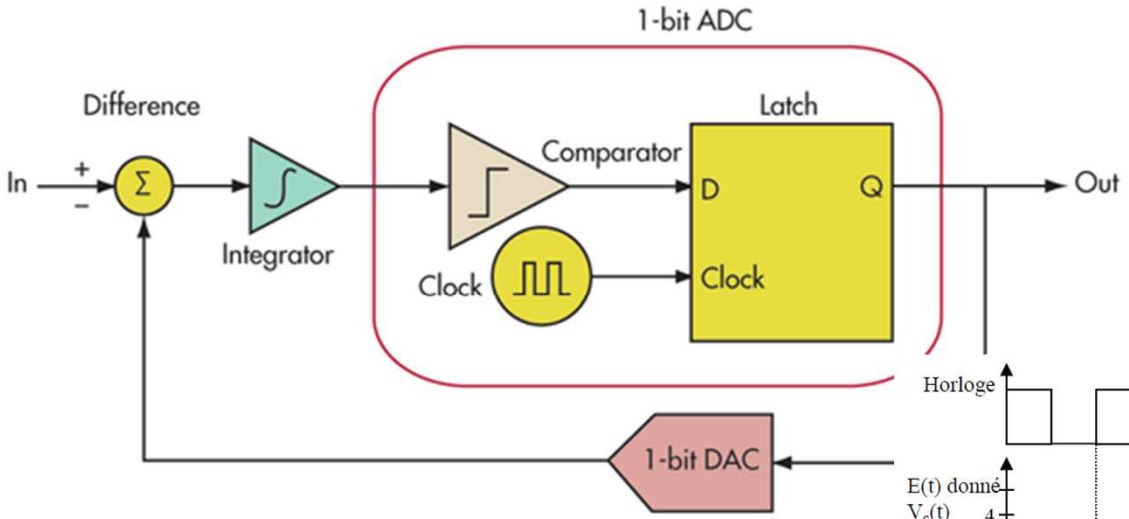
ARCHITECTURES : Sigma Delta

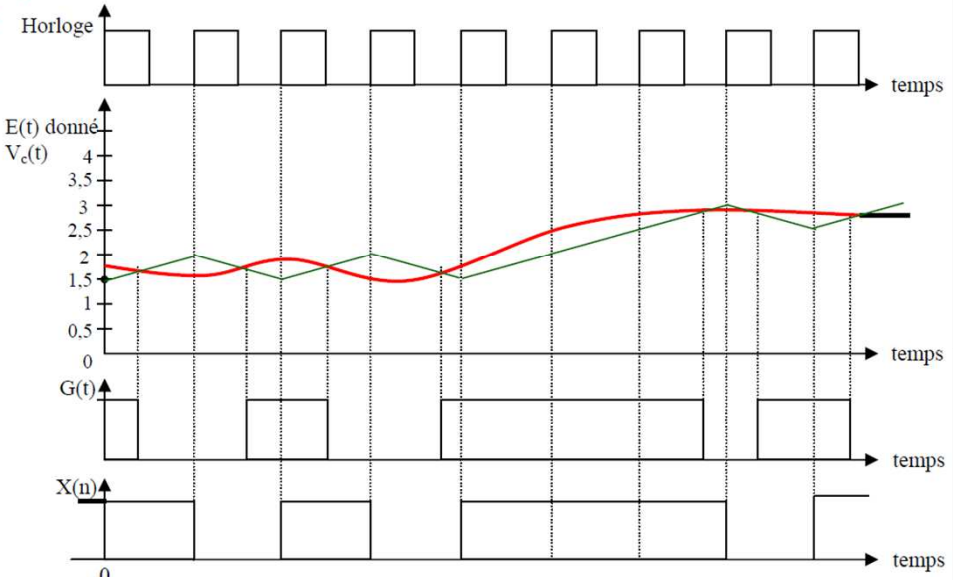


ARCHITECTURES : Sigma Delta

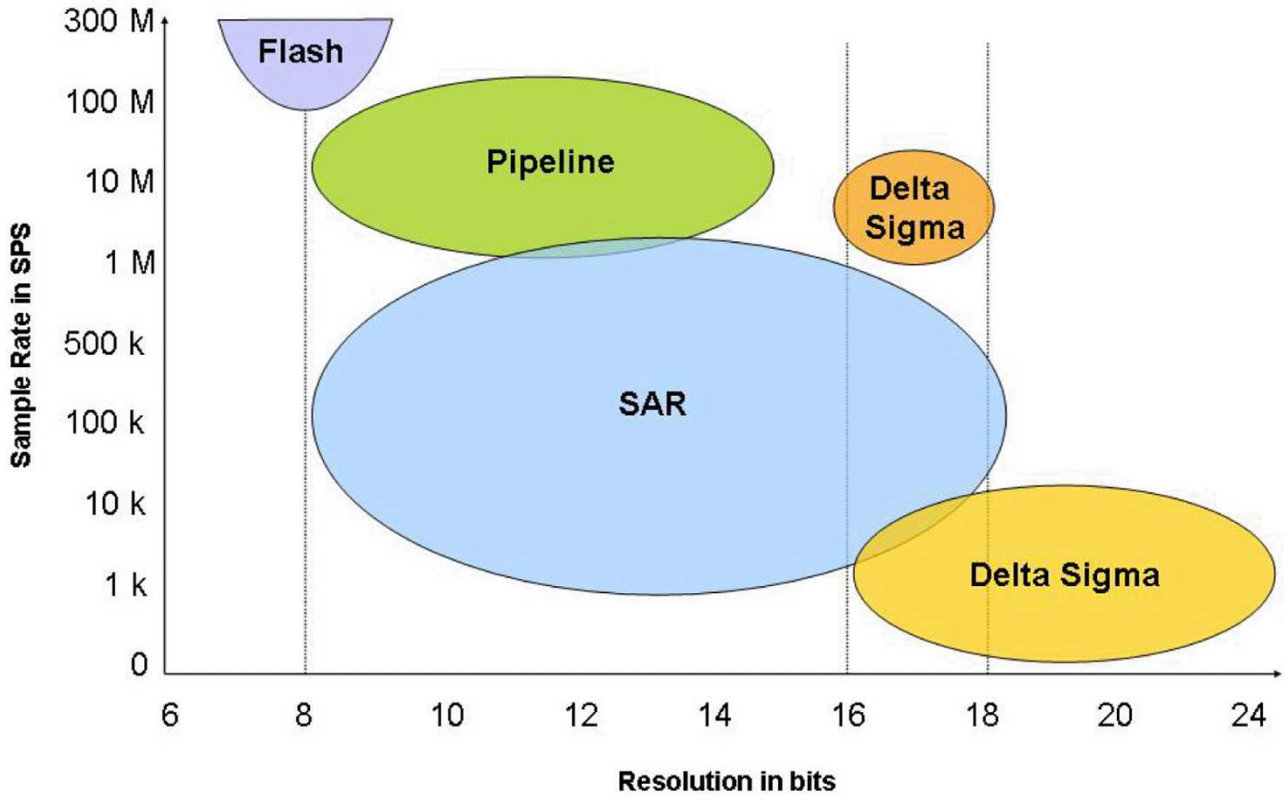


ARCHITECTURES : Sigma Delta

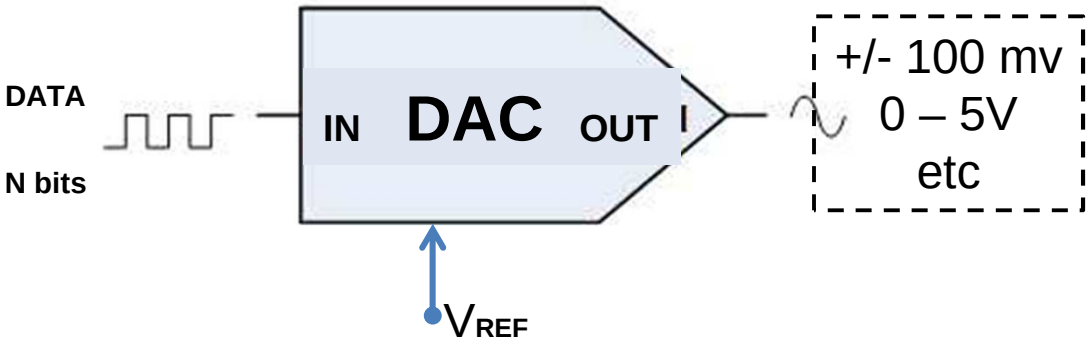




ARCHITECTURES : Comparaison



LES CNA (ou DAC)



CNA

Définitions

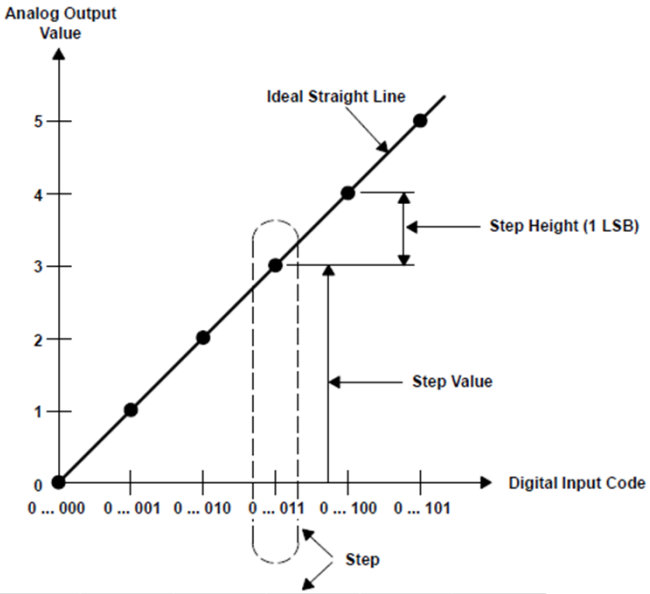
Q (Quantum) ou LSB (Last Significant Bit) => Résolution

$$1\ \mathrm{LSB} = \mathrm{FSR}/(2^{n} - 1)$$

Tension de pleine échelle (FSR) vs Tension de référence (V_{REF})

LES CNA (ou DAC)

CNA



CONVERSION CODE

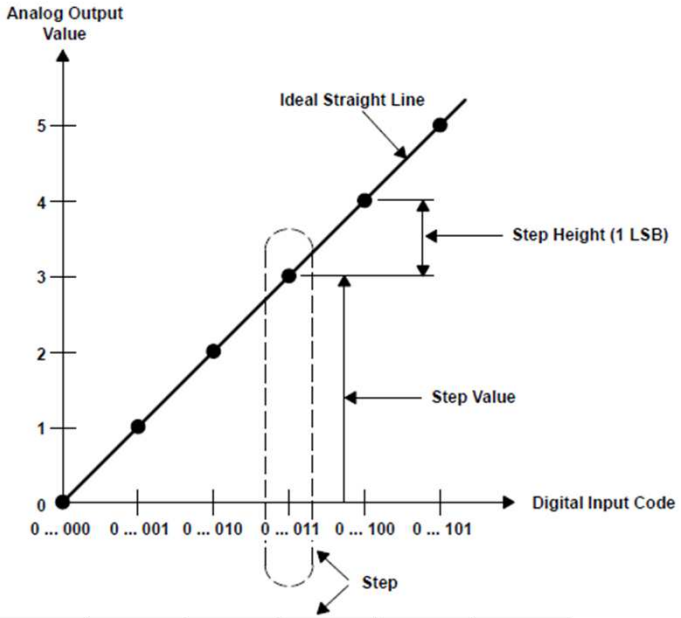
Digital Input Code	0 ... 000	0 ... 001	0 ... 010	0 ... 011	0 ... 100	0 ... 101
Analog Output Value	0	1	2	3	4	5

Elements of Transfer Diagram for an Ideal Linear DAC

LES CNA(ou DAC)

CNA

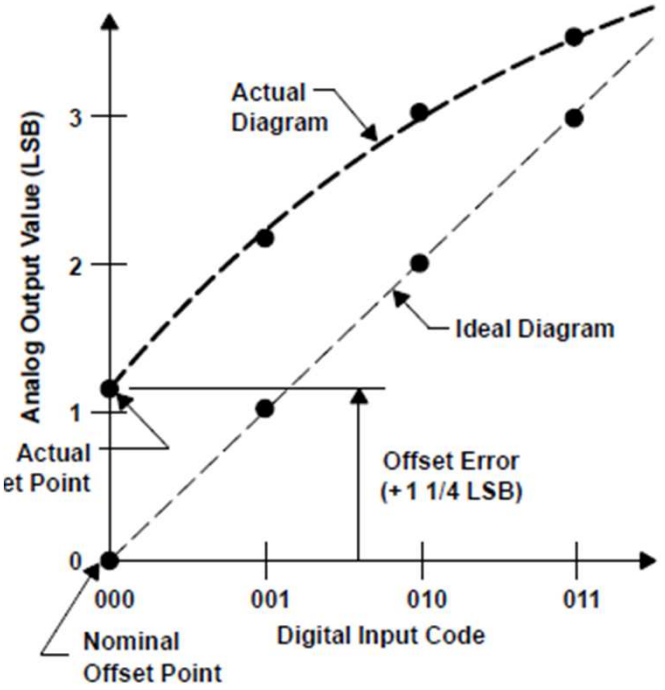
Erreur de décalage



CONVERSION CODE

Digital Input Code	0 ... 000	0 ... 001	0 ... 010	0 ... 011	0 ... 100	0 ... 101
Analog Output Value	0	1	2	3	4	5

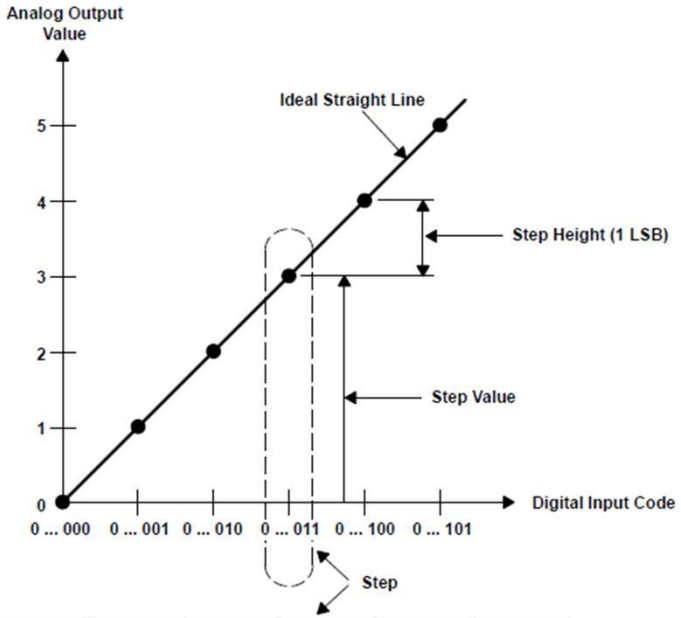
Elements of Transfer Diagram for an Ideal Linear DAC



LES CNA(ou DAC)

CNA

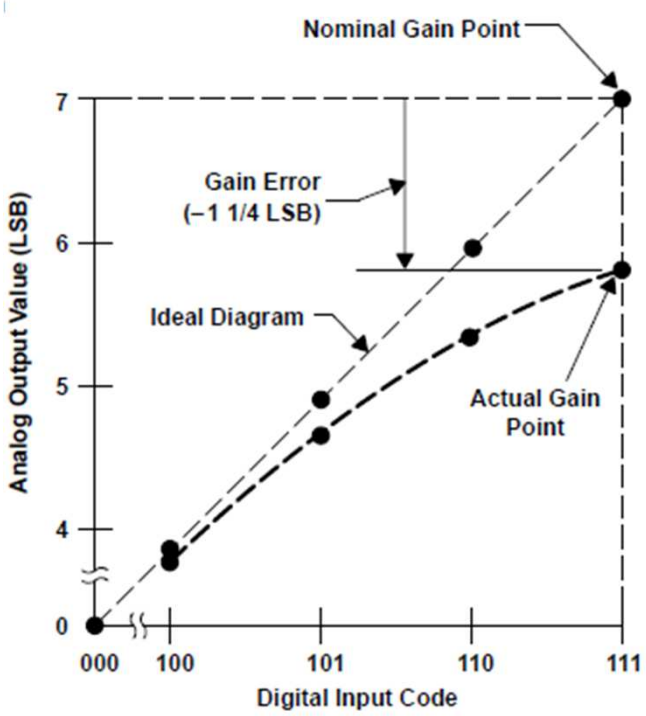
Erreur de Gain



CONVERSION CODE

Digital Input Code	0 ... 000	0 ... 001	0 ... 010	0 ... 011	0 ... 100	0 ... 101
Analog Output Value	0	1	2	3	4	5

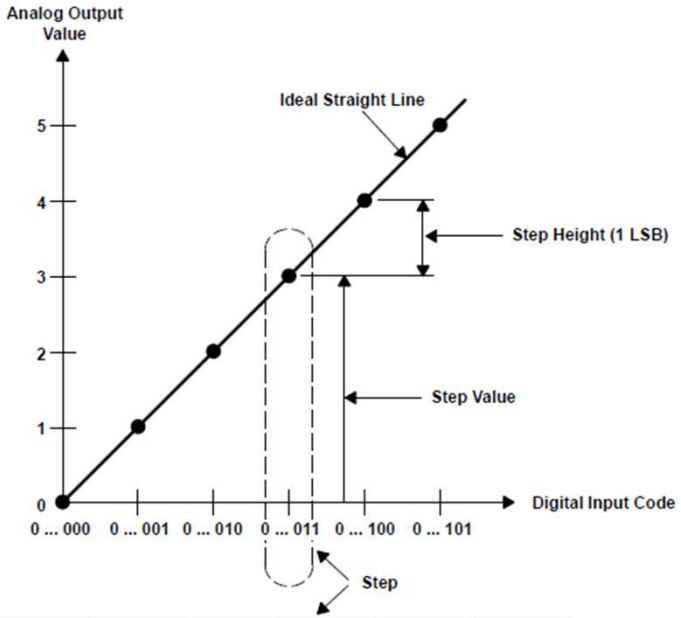
Elements of Transfer Diagram for an Ideal Linear DAC



LES CNA(ou DAC)

CNA

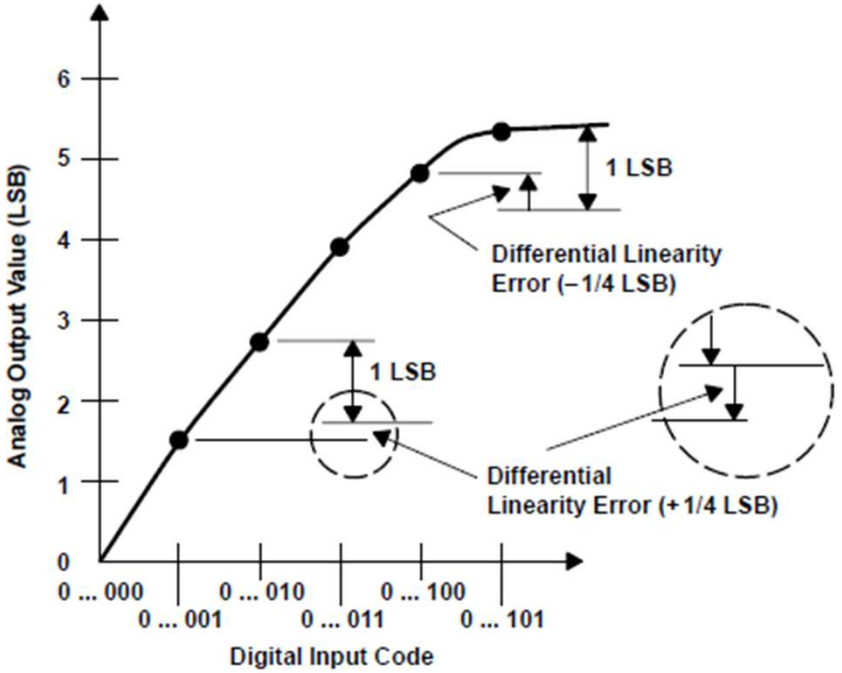
DNL: Differential Non Linearity



CONVERSION CODE

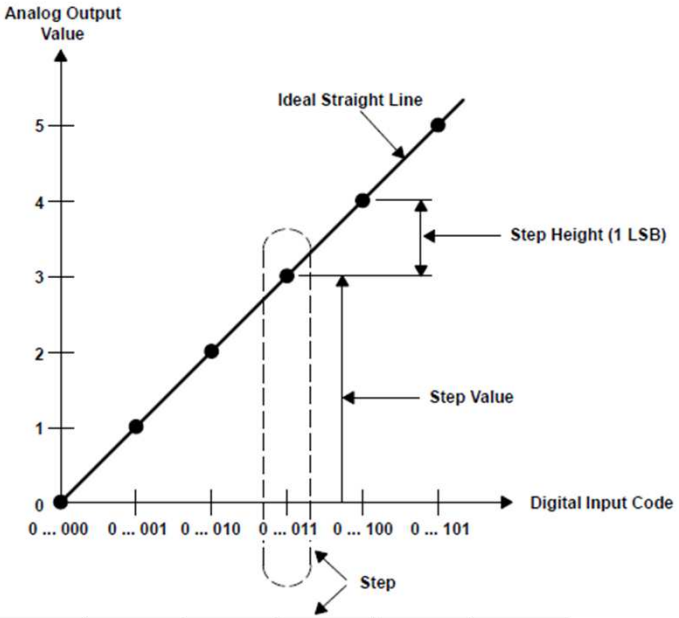
Digital Input Code	0 ... 000	0 ... 001	0 ... 010	0 ... 011	0 ... 100	0 ... 101
Analog Output Value	0	1	2	3	4	5

Elements of Transfer Diagram for an Ideal Linear DAC



LES CNA(ou DAC)

CNA

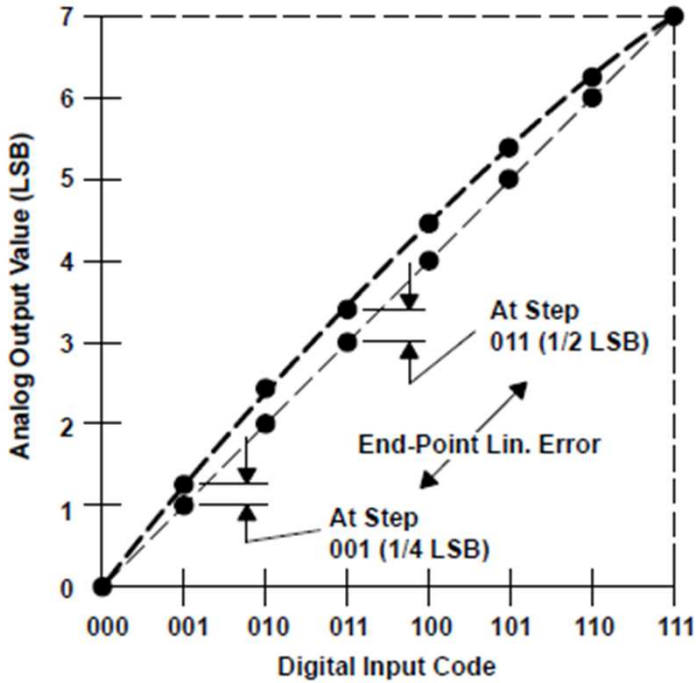


CONVERSION CODE

Digital Input Code	0 ... 000	0 ... 001	0 ... 010	0 ... 011	0 ... 100	0 ... 101
Analog Output Value	0	1	2	3	4	5

Elements of Transfer Diagram for an Ideal Linear DAC

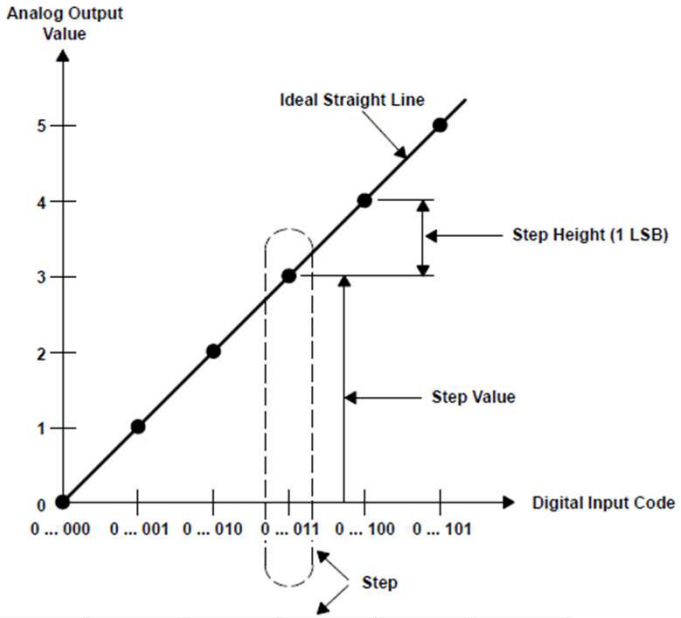
INL: Integral Non Linearity



LES CNA(ou DAC)

CNA

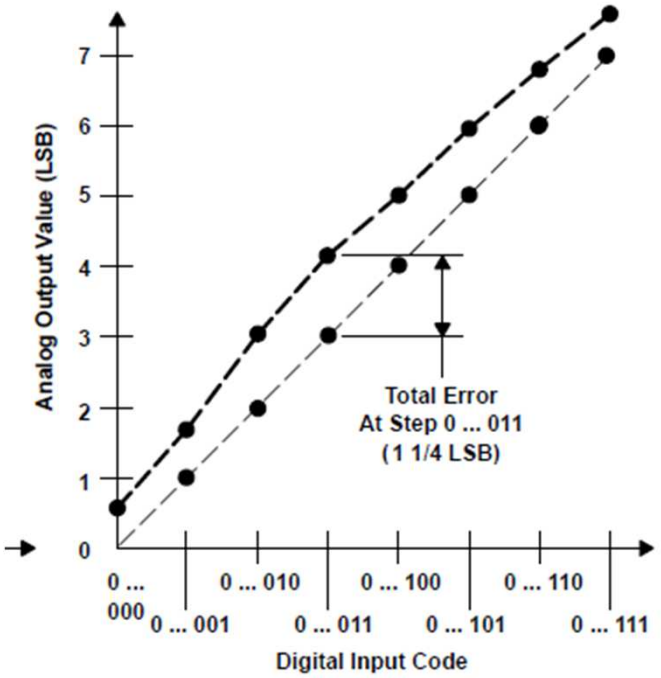
Total Error (Absolute Accuracy)



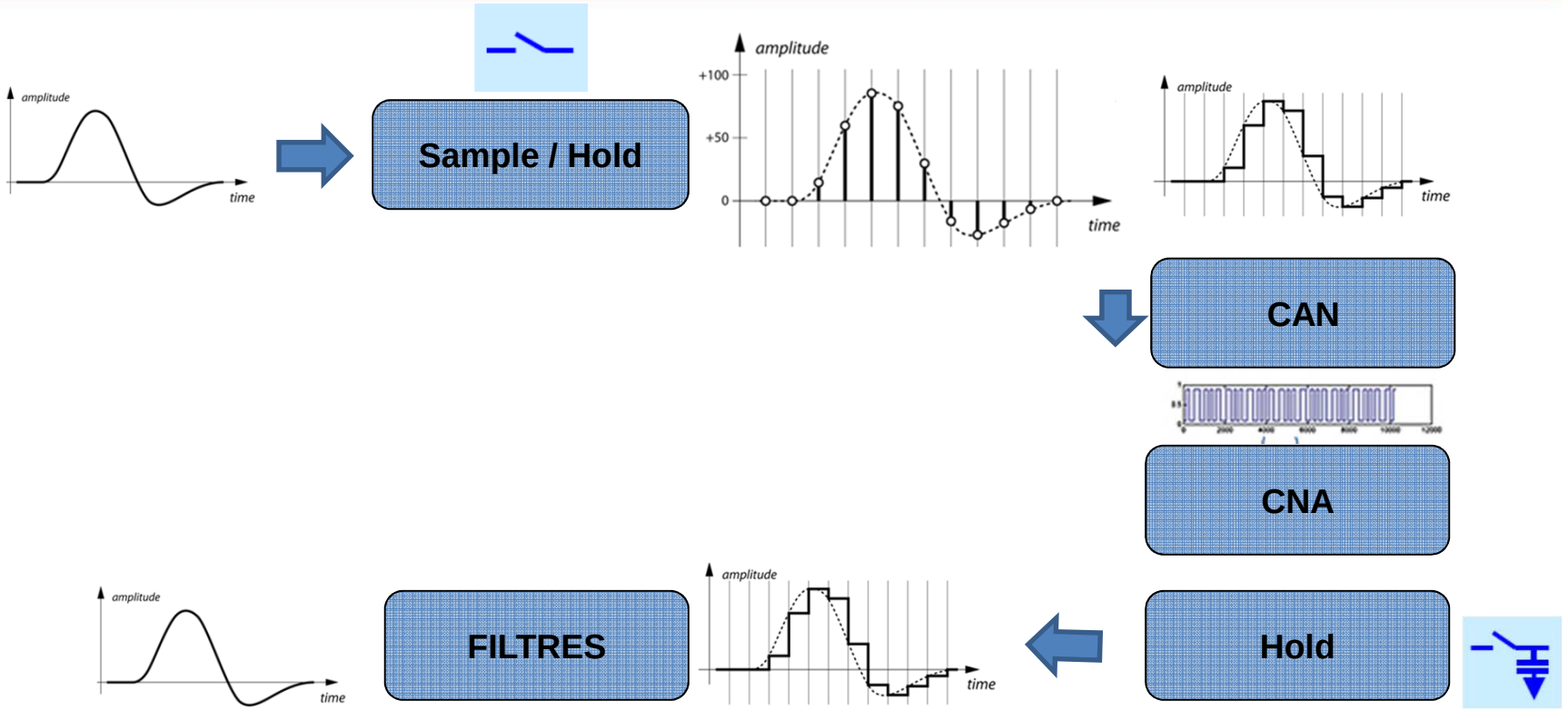
CONVERSION CODE

Digital Input Code	0 ... 000	0 ... 001	0 ... 010	0 ... 011	0 ... 100	0 ... 101
Analog Output Value	0	1	2	3	4	5

Elements of Transfer Diagram for an Ideal Linear DAC



Retour sur l’échantillonage



DAC du C8051F020

Table 8.1. DAC Electrical Characteristics

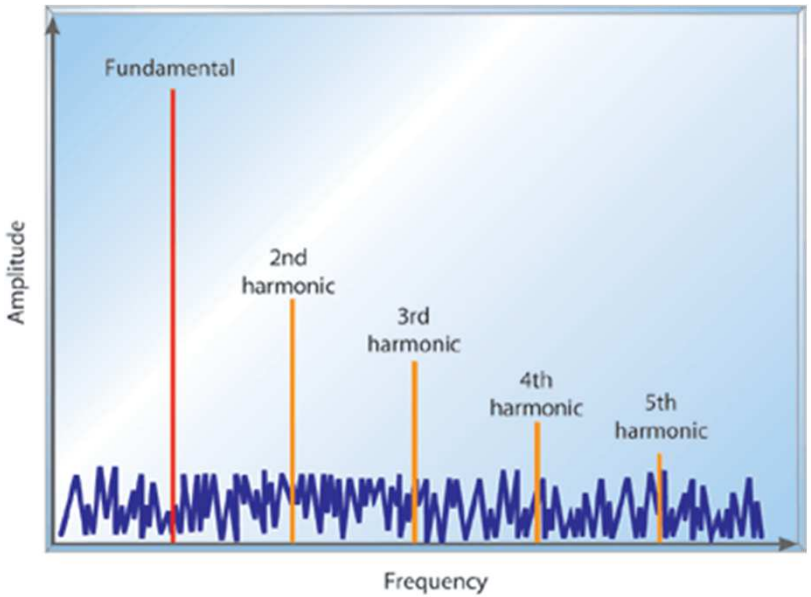
VDD = 3.0 V, AV+ = 3.0 V, VREF = 2.40 V (REFBE = 0), No Output Load unless otherwise specified

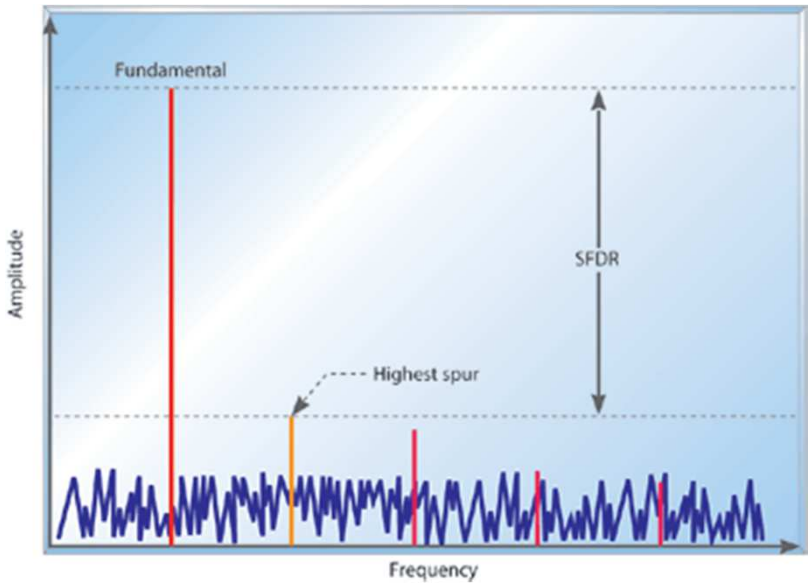
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE					
Resolution			12		bits
Integral Nonlinearity			±2		LSB
Differential Nonlinearity				±1	LSB
Output Noise	No Output Filter 100 kHz Output Filter 10 kHz Output Filter		250 128 41		µVrms
Offset Error	Data Word = 0x014		±3	±30	mV
Offset Tempco			6		ppm/°C
Gain Error			±20	±60	mV
Gain Error Tempco			10		ppm/°C
VDD Power Supply Rejection Ratio			-60		dB
Output Impedance in Shutdown Mode	DACnEN = 0		100		kΩ
Output Sink Current			300		µA
Output Short-Circuit Current	Data Word = 0xFFF		15		mA
DYNAMIC PERFORMANCE					
Voltage Output Slew Rate	Load = 40pF		0.44		V/µs
Output Settling Time to 1/2 LSB	Load = 40pF, Output swing from code 0xFFF to 0x014		10		µs
Output Voltage Swing		0		VREF-1LSB	V
Startup Time			10		µs
ANALOG OUTPUTS					
Load Regulation	I_L = 0.01mA to 0.3mA at code 0xFFF		60		ppm
POWER CONSUMPTION (each DAC)					
Power Supply Current (AV+ supplied to DAC)	Data Word = 0x7FF		110	400	µA

Performances

– Dynamiques : SNR - THD – SINAD - SFDR

$$SNR = 20\log\left(\frac{S}{N}\right),$$





$$THD = 20\log\left(\frac{S}{D}\right) \qquad SINAD = 20\log\left(\frac{S}{N+D}\right)$$

Performances

– Dynamiques : Settling time, Voltage swing

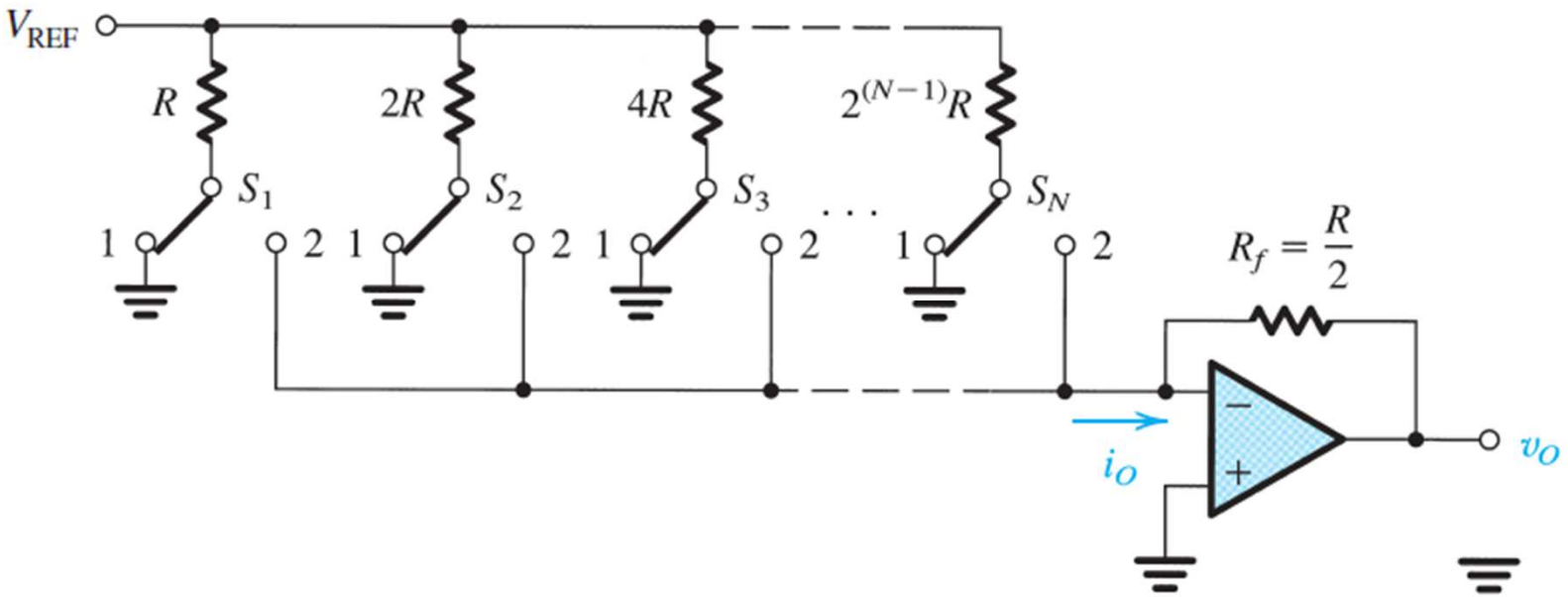
DAC du C8051F020

Table 8.1. DAC Electrical Characteristics

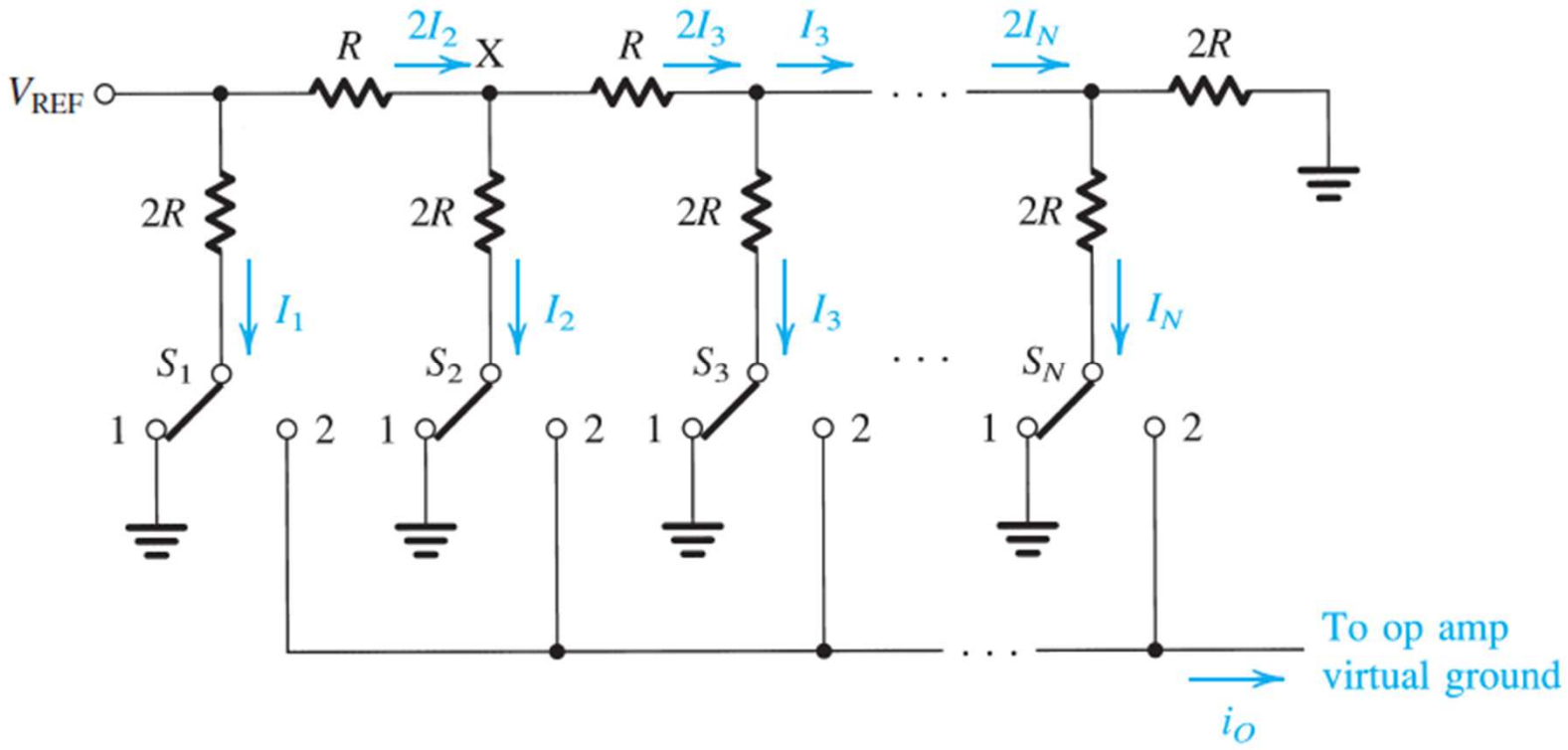
VDD = 3.0 V, AV+ = 3.0 V, VREF = 2.40 V (REFBE = 0), No Output Load unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE					
Resolution			12		bits
Integral Nonlinearity			±2		LSB
Differential Nonlinearity				±1	LSB
Output Noise	No Output Filter 100 kHz Output Filter 10 kHz Output Filter		250 128 41		µVrms
Offset Error	Data Word = 0x014		±3	±30	mV
Offset Tempco			6		ppm/°C
Gain Error			±20	±60	mV
Gain-Error Tempco			10		ppm/°C
VDD Power Supply Rejection Ratio			-60		dB
Output Impedance in Shutdown Mode	DACnEN = 0		100		kΩ
Output Sink Current			300		µA
Output Short-Circuit Current	Data Word = 0xFFF		15		mA
DYNAMIC PERFORMANCE					
Voltage Output Slew Rate	Load = 40pF		0.44		V/µs
Output Settling Time to 1/2 LSB	Load = 40pF, Output swing from code 0xFFF to 0x014		10		µs
Output Voltage Swing		0		VREF-1LSB	V
Startup Time			10		µs
ANALOG OUTPUTS					
Load Regulation	I_L = 0.01mA to 0.3mA at code 0xFFF		60		ppm
POWER CONSUMPTION (each DAC)					
Power Supply Current (AV+ supplied to DAC)	Data Word = 0x7FF		110	400	µA

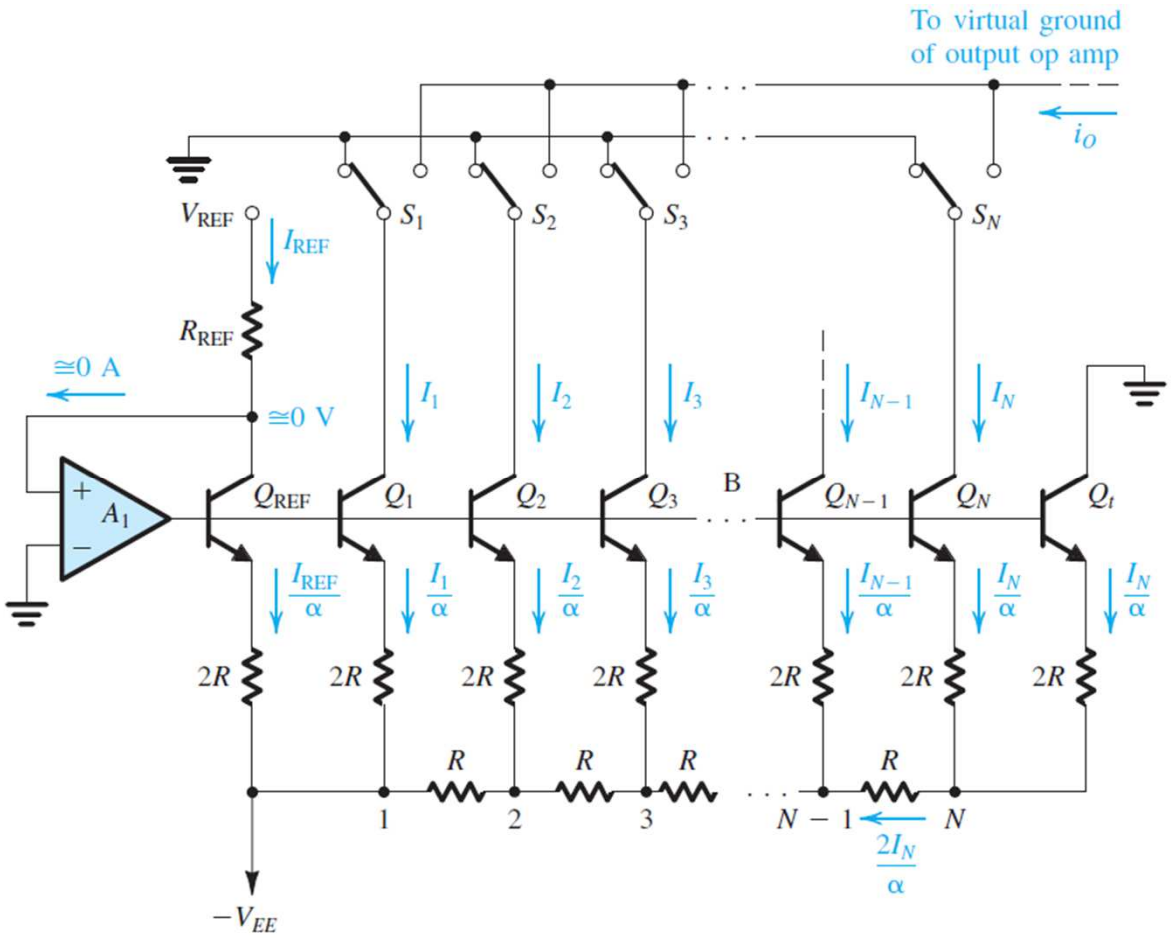
ARCHITECTURES : R pondérées



ARCHITECTURES : R-2R



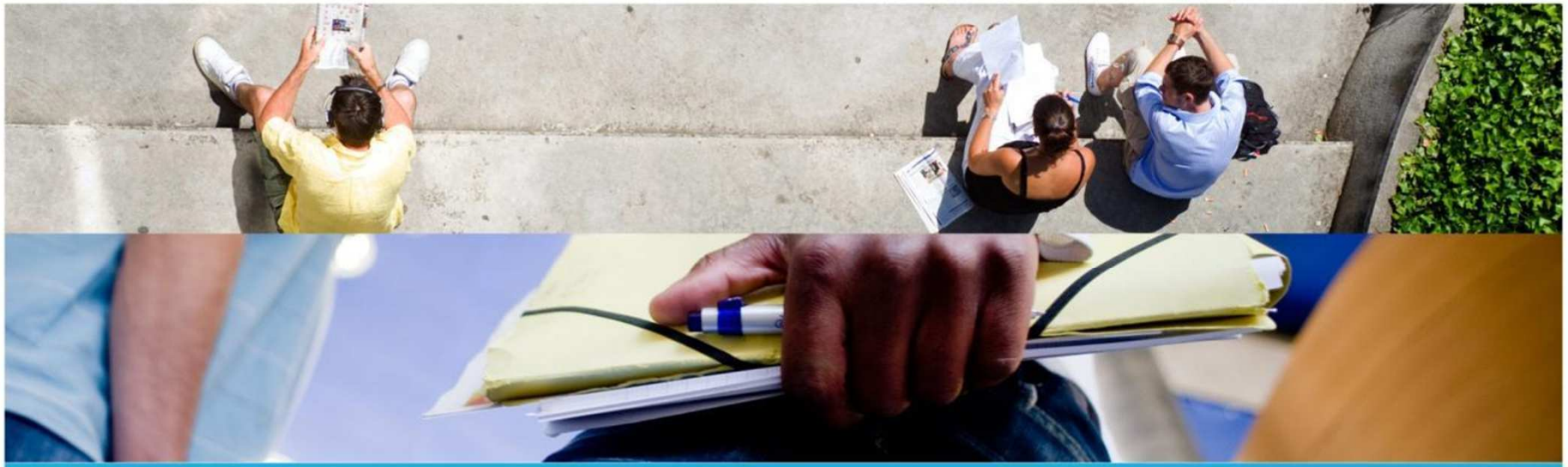
ARCHITECTURES : Courants pondérés



Références bibliographiques

[1] Len Satller, Silicon labs, Application Notes

[2] Understanding Data converters, Application report, Texas Instruments



MERCI DE VOTRE ATTENTION !

L. LABRAK

membre de UNIVERSITÉ DE LYON

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DE CHIMIE PHYSIQUE ÉLECTRONIQUE
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