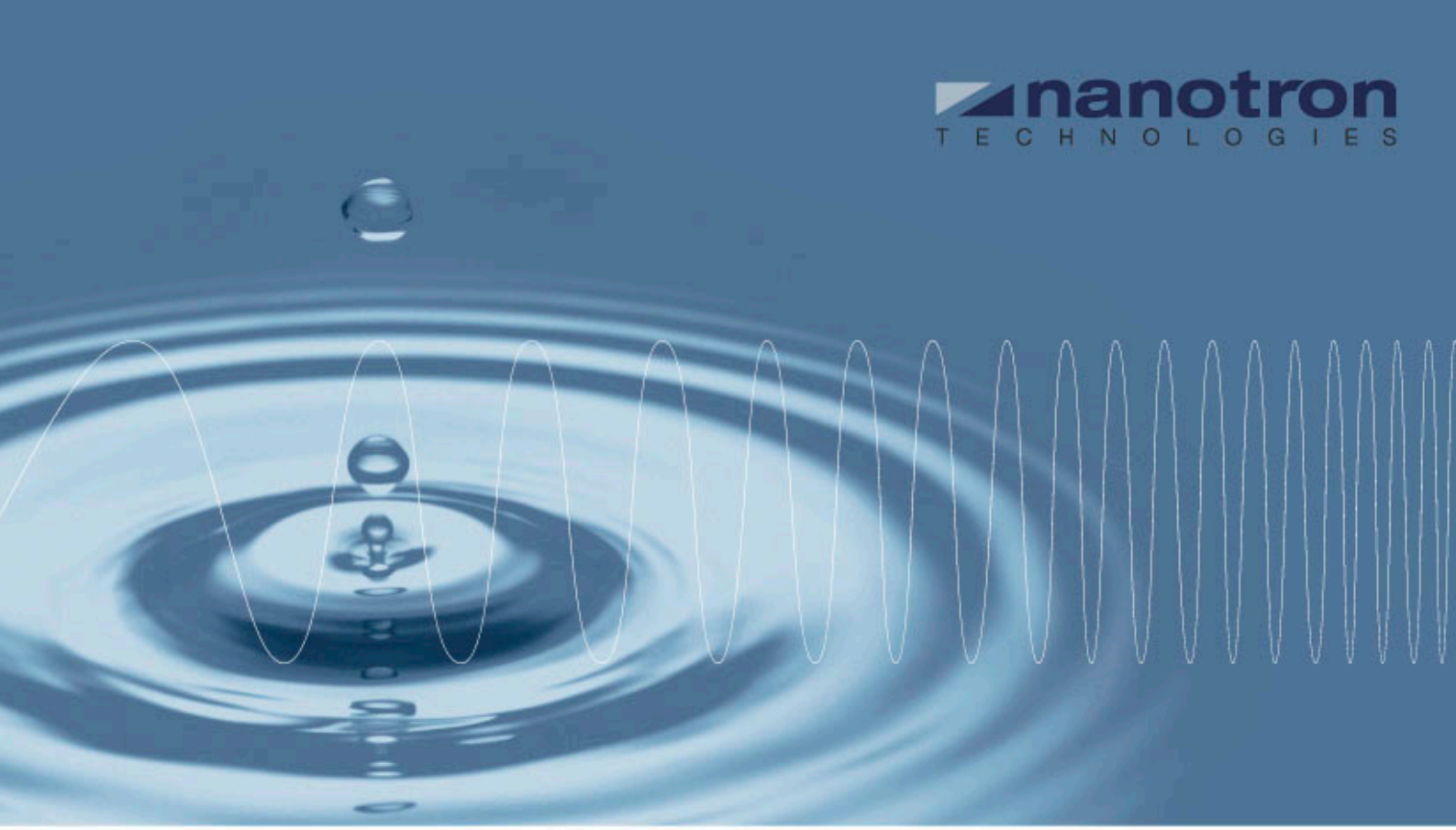

nanoLOC TRX Transceiver (NA5TR1)

User Guide

Version 1.01

NA-06-0230-0385-1.01

This document contains information on a pre-engineering chip. Specifications and information herein are subject to change without notice.

Chirp it.

Document Information

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CAUTION! Electrostatic Sensitive Device. Precaution should be used when handling the device in order to prevent permanent damage.

Table of Contents

1 Introduction

This User Guide provides programming guidelines and a detailed description of all user-programmable registers and baseband memory of the *nanoLOC TRX Transceiver* (NA5TR1).

1.1 Overview

This document consists of the following sections:

- *Introduction* on page 1 describes the conventions used in this document.
- *nanoLOC Chip Key Features* on page 6 provides a summary of the key features of the nanoLOC chip.
- *nanoLOC Architecture* on page 8 provides an overview of the digital and analogue parts of the chip.
- *nanoLOC Programming Interface (SPI)* on page 13 describes the SPI interface and how to use it to access the *nanoLOC TRX Transceiver*.
- *nanoLOC Clocks* on page 26 describes the clocks used in the nanoLOC chip.
- *Power Management* on page 32 provides a description of power management features of the transceiver.
- *nanoLOC Memory (Draft)* on page 38 describes the structure of the digital memory of the chip.
- *MACFrame and Baseband RAM Configuration (Draft)* on page 44 provides an overview of how to configure the baseband RAM and MACFrames.
- *Memory Map of Chip Registers 0x00 – 0x7F* on page 55 provides a memory map of the chip's registers as well as memory locations in BBRAM.
- *Chip Registers Description: 0x00 to 0x7F* on page 65 provides a detailed description of all end-user modifiable digital registers.
- *Memory Map of RAM Locations* on page 207 provides a memory map of the memory locations in BBRAM.
- *RAM Locations Descriptions: 0x80 to 0x3FF* on page 213 provides a detailed description of all memory locations in BBRAM based on buffer configuration mode.

1.2 Typographic Conventions

The following typographical conventions are used throughout this document.

Table 1: Document conventions

Convention	Description
Italics	Product names, trademarks, cross references, and document titles, and first occurrences of a special term. Also variables in equations.
`Courier`	Computer input, file names, signals, registers, and register field names.
SMALL CAPS	Application windows and dialogues.
Note	Denotes important supplementary information.
Warning	Alerts you that failure to take or avoid a specific action might result in physical harm to you and/or the hardware. The following icon is placed in the margin to highlight the warning. 

1.3 Chip Register and Memory Location Conventions

1.3.1 Registers and Fields

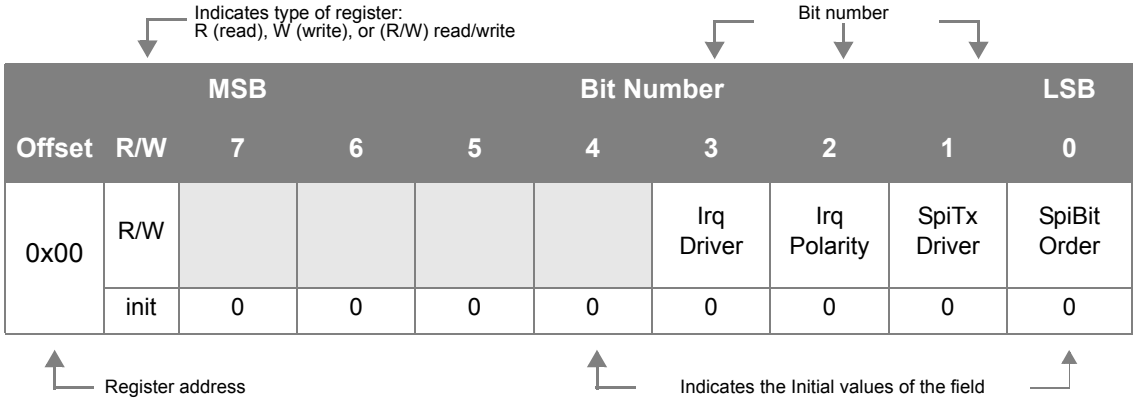
The following table describes chip registers and chip fields.

Table 2: Chip registers and fields

Item	Description
Registers and RAM Locations	The *nanoLOC TRX Transceiver* uses eight bit offset digital registers and RAM locations that can be set according to the requirements of the chip. Setting the chip may involve only a single register or a group of registers.
Fields	A field is a bit or a group of bits with a single purpose. Each field has a unique identifier, a Mnemonic, that has specific properties associated with it.

1.3.2 Register Diagram Conventions

Each register in the chip is graphically displayed as a row in a table that has the following conventions:



1.3.3 Reserved and Used Fields

All the fields are shown as either:

- Reserved fields (indicated by a dark hatched pattern)
- Used fields, with the name, or mnemonic, of the field shown (indicated by a white background spanning the range of the field)

1.3.4 Initial Value of Field

Below each used field is the initial value of the field.

1.3.5 Read Only, Write Only, or Read/Write Fields

Each register is indicated as either Read Only (RO), Write Only (WO), or Read/Write (R/W).

1.3.6 Field Description Tables

Following each register diagram is a table describing each used field in the register. The first column lists the bit numbers in ascending order, followed by the field's mnemonic, its properties (conventions are explained below), and a description that includes any usage rules and any special conditions or restrictions. A sample field description table is shown below.

Field Properties for Register 0x00

Bits	Mnemonic	Prop	Description
0	SpiBitOrder	R/W brst SPI	Select MSB or LSB Bit Order for SPI *Purpose:* Defines the bit order of the SPI. However, the byte order always remains the same. *Register Values/Settings:* • NA_SpiBitOrderLsbFirst_C(0x0) The first bit transmitted over the interface data lines is the LSB, while the last bit is the MSB. Each byte is, therefore, transmitted with LSB first. • NA_SpiBitOrderMsbFirst_C(0x1) The first bit transmitted over the interface data lines is the MSB, while the last bit is the LSB. Each byte is, therefore, transmitted with MSB first. • Default Value = 0x0 *Note:* After PowerUpReset or after wakeup from PowerDownModeFull, the SPI is configured as LSB first.

1.3.7 Property Column Conventions

The following conventions apply to the Properties (Prop.) column of the field description tables:

Table 3: Property column explanation

Convention	Description
r	This field supports read only mode.
w	This field supports write only mode.
r/w	This field supports both read and write mode.
brst	This field supports SPI burst access and can be a located within a block that is read from or written to in a burst.
strb	This field supports a strobe function where only a single write access is required for generating a command or action. The value `True` must be written to the location only once.
BbClk	To access this field, the baseband clock distribution must be enabled.
SPI	Register is running with the SPI clock.

1.3.8 Register Setting Values

In register settings, positive logic is used, which means:

- True = high level = 1
- False = low level = 0

Hexidecimal, decimal, and binary values are shown in the following examples:

Table 4: Hexidecimal, decimal, and binary examples

Value	Example
Hexidecimal value	0xABCD
Decimal value	1234
Binary value	0B1101

1.3.9 Setting the Value of Reserved Fields

A “0” must always be written to a field marked as Reserved.

Warning: Failure to write a “0” to a Reserved field may result in the *nanoLOC TRX Transceiver* having unexpected behavior.

2 nanoLOC Chip Key Features

2.1 About This Chapter

The nanoLOC TRX Transceiver (NA5TR1) includes most of the functionality of the nanoNET TRX Transceiver (NA1TR8), with a substantial number of changes and improvements. These include:

- Channelization provided
- Ranging capabilities added
- Digital Dispersive Delay Line incorporated in the chip
- Faster interface for Chirp Sequencer
- Standard set of default values set into chip
- Programmable pull registers provided

2.2 Channelization

Channelization is the subdividing of a single frequency band into many narrow frequency bands. The frequency band used by the nanoLOC chip is 2.4 GHz ISM band (2.400 GHz to 2.4835 GHz). However, within this band, a user can program the chip to use either the a 80 MHz channel, which uses the entire 2.4 GHz bandwidth, or use one of three 22 MHz bandwidths to increase coexistence with devices sharing the same ISM band.

The channelization of the nanoLOC chip is achieved by the use of FDMA (Frequency Division Multiple Access) to provide a 22 MHz band. This narrower band can be set to any frequency range in the ISM band through the use of FdmaEnable to enable FDMA and ENTER CROSS REFERENCE to set the starting frequency.

2.3 Ranging

The *nanoLOC TRX Transceiver* implements a ranging methodology called *Symmetrical Double-Sided Two-Way Ranging, or SDS-TWR*. In this approach to ranging, the timing values of four transmissions performed by two independent devices are needed to calculate the distance value. These four transmissions are:

1 A data packet sent from station A to station B.

2 An Ack packet sent from station B to station A.

3 A data packet sent from station B to station A.

4 An Ack packet sent from station A to station B.

Using algorithms, these four transmissions provide distance values which, along with the signal propagation delay of the Data and Ack packets and the processing delay of Ack packets, can be used to calculate the distance between two wireless devices.

2.4 Digital Dispersive Delay-Line

The nanoLOC TRX transceiver incorporates a Digital Dispersive Delay Line (DDDL), which in previous chips was an external component. RAM has been provided for storing reference values for I and Q, which are used to detecting incoming pulse generated by another nanoLOC chip.

The detectable pulses can be either an Upchirp (Linear frequency modulation, where frequency increases in time), a Downchirp (Linear frequency modulation, where frequency decreases in time), a Minus Folded Chirp (Upchirp and Downchirp overlaid), or a Plus Folded Chirp (Upchirp and Downchirp overlaid). An OffChirp is also possible, which is the absence of a chirp. These pulses have the same center frequency and the same bandwidth so that the difference occurs only in the phase information.

2.5 Chirp Sequencer

The nanoLOC chip provides a faster programming interface for setting up the Chirp Sequencer. Chirp Sequencer RAM memory *CSQ RAM) is provided for setting the I and Q values, which are used for calculating the Up and Down pulses.

2.6 Default Values

To nanoLOC TRX Transceiver has been set with values that most users of the chip would require for standard applications. These default values mean less initialization time, which reduces the amount of effort required to get an application to run with the chip.

2.7 Programmable Pull-Resistors

To lower the bill of material costs, the nanoLOC chip has programmable pull-resistors. The following pads can now be set as pull-up or pull-down:

- Four SPI pins: Spiclk, Spissn, Spirxd, and Spitxd
- Four other pins: PowerOnReset, Pamp, µCIrq, and µCReset
- Digital IO pad

3 nanoLOC Architecture

The nanoLOC TRX Transceiver has both a digital part and analog part in silicon. The digital part of the chip provides a programming interface for setting up the chip, a means of providing from an application data for transmission and providing an application with data that has been received. The analog part converts digital information provided by the digital part of the chip to generate a packet for transmission, while receiving packets from other nanoLOC chips and decoding these chirp pulses for use by the digital part.

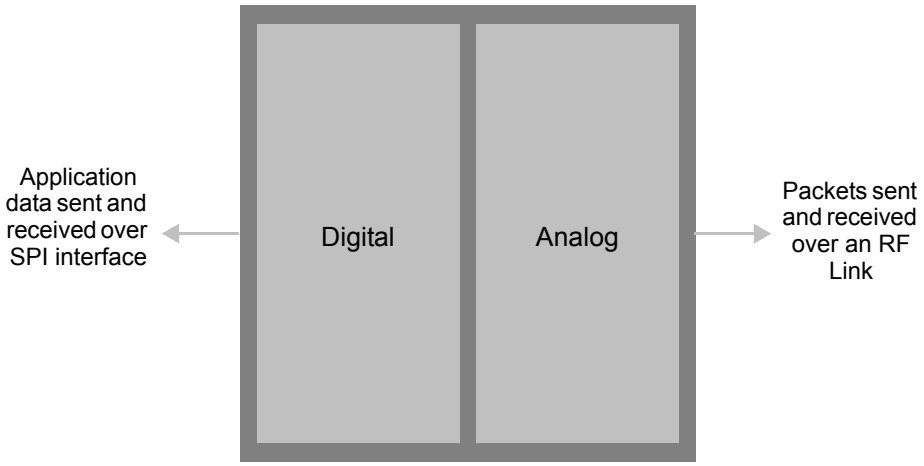


Figure 1: nanoLOC Architecture (simplified)

3.1 nanoLOC Digital Architecture

The digital architecture of the nanoLOC chip is structured to achieve maximum power savings by providing a minimum number of controls in a part of the chip that is always powered, while placing the remaining controls in a part that is powered up only during operating mode. The section of the digital part that is always powered is called the “ON part”, while the section powered only during operating mode is called the “PWD part”.

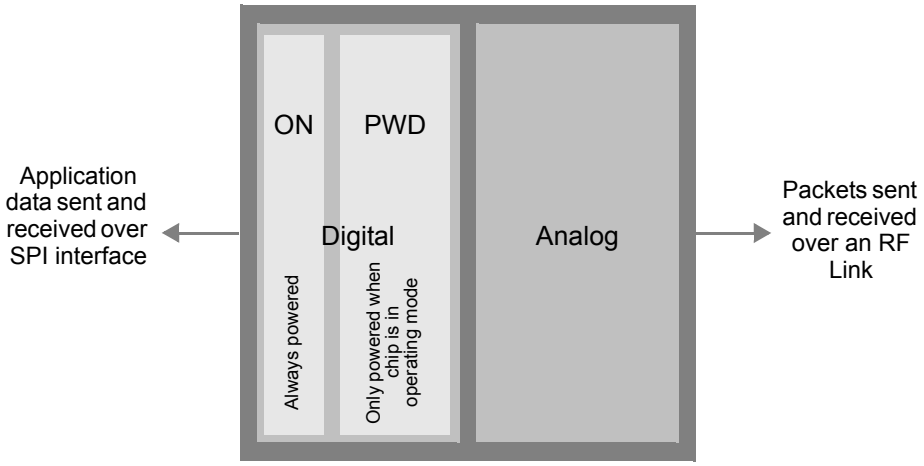


Figure 2: ON and PWD sections of the digital part

The ON part of the digital part is connected to the I/O pins, as these pins are needed for power managements.

The flow of signals within the chip can be illustrated as follows:

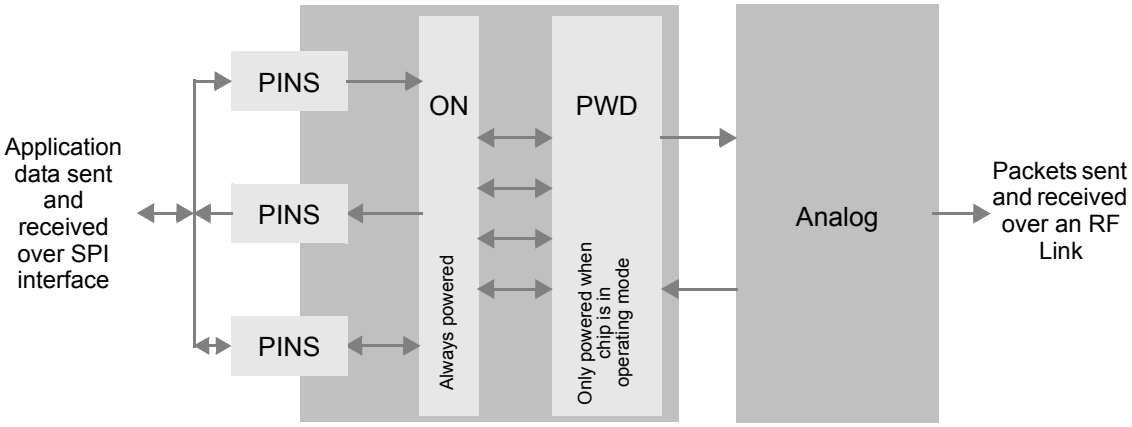


Figure 3: Signal flow in the nanoLOC chip

3.2 nanoLOC TRX Transceiver IO Pins

3.2.1 Digital Pins

The nanoLOC chip provides 15 digital pins for input/output, as described in the following sections.

- Seven Digital Input Pins:

Table 5: Digital input pins

Pin	Pin #	Direction	Description
Xtal32k	2	Input	Input for 32.768 kHz quartz oscillator.
Xtal32M	4	Input	Input for 32 MHz reference quartz oscillator.
PowerOnReset	24	Input	Power up reset line.
SpiClk	15	Input	The SPI Clock is generated by the microcontroller (master) and synchronizes data movement in and out of the device through the pins SpiRxD and SpiTxD.
SpiSSn	10	Input	SPI Slave Select (low active) is externally asserted before the microcontroller (master) can exchange data with the *nanoLOC chip*. Must be low before data transactions and must stay low for the duration of the transaction.
SpiRxD	16	Input	SPI Receive Data (MOSI).
[Test]	25	Input	Production Test Pin.

- Four Digital Output Pins

Table 6: Digital output pins

Pin	Pin #	Direction	Description
SpiTxD	14	Output	SPI Transmit Data (MISO).
Pamp	6	Output	External power amplifier control pin that allows the use of an external amplifier.
µCReset	9	Output	Reset for external microprocessor.
µCirq	8	Output	Interrupt request to external microprocessor.

- Four Bi-directional Digital Input/Output Pins

Table 7: Bi-directional digital I/O pins

Pin	Pin #	Direction	Description
D0	17	Input/Output	Digital Input or Output (programmable), line 0.
D1	18	Input/Output	Digital Input or Output (programmable), line 1.
D2	19	Input/Output	Digital Input or Output (programmable), line 2.
D3	20	Input/Output	Digital Input or Output (programmable), line 3. **Note**: 32.768 kHz clock operating on this pin after reset/power up.

3.2.2 Analog Pins

The nanoLOC chip provides one output analog pin:

Table 8: Analog pins

Pin	Pin #	Direction	Description
µCVcc	23	Output	Power supply for external microprocessor

3.2.3 Digital IO Pins (D0, D1, D2, D3) Configuration

The four Digital IO pins (D0, D1, D2, D3) run with the SPI Clock.

- Each Digital IO pin has 6 configuration bits, as described below:

Table 9: Digital I/O pin configuration

Field	Offset	Read/Write	Description
DioDirection	0x04	WO	Controls direction of Digital IO port, as either an input or an output pin.
DioOutValueAlarmEnable	0x04	WO	When a Digital IO port is configured as an input, this bit selects whether the signal level at this port or the occurrence of an alarm should be reported when reading this field.
DioAlarmStart	0x04	WO	This field starts the alarm, and is set after the digital IO port is configured to report the occurrence of an alarm.
DioAlarmPolarity	0x04	WO	When the digital IO port is configured as an input that should report the occurrence of an alarm, then this bit is used to select the edge which should trigger the alarm. When the digital IO port is configured as an output, then this bit selects whether the value programmed in DioOutValueAlarmEnable or the feature clock should be driven out of the digital IO port.
DioUsePullup	0x04	WO	When this bit is set to true, a pull-up resistor is connected to the corresponding digital IO pad.
DioUsePulldown	0x04	WO	When this bit is set to true, a pull-down resistor is connected to the corresponding digital IO pad only, but when DioUsePullup is false.

- Each Digital IO Pin has one write strobe, as described below:

Table 10: Digital I/O pin write strobe

Field	Offset	Read/Write	Description
DioPortWe	0x04	WO	Writes the settings of the 6 configuration bits described above to the digital IO controller:

- Each Digital IO Pin has one status bit, as described below:

Table 11: Digital I/O pin status

Field	Offset	Read/Write	Description
DioInValueAlarmStatus	0x04	RO	Each bit reports the signal level or the occurrence of an alarm at one of the four digital IO ports, where bit 0 belongs to DigIO 0, bit 1 belongs to DigIO 1, bit 2 belongs to DigIO 2, and bit 3 belongs to DigIO 3

3.2.4 IRQ Pin µCIRQ Configuration

Several fields are used to configure the IRQ pin µCIRQ and to set the source of the interrupt.

- The IRQ pins can be configured as either low or high active, as well as either push-pull or open-drain, as described below.:

Table 12: IRQ pin configuration

Field	Offset	Read/ Write	Default
IrqPolarity (high/low active)	0x00	RW	Defines the polarity of the IRQ signal as either high or low active. The default is low active.
IrqDriver (pushpull/opendrain)	0x00	RW	Switches between push-pull or open-drain for IRQ output driver. The default is open-drain.

- The transmitter interrupt, the receiver interrupt, the baseband timer interrupt, or the local oscillator interrupt can be enabled to drive the IRQ pin, as described below.:

Table 13: Interrupts driving the IRQ pin

Field	Offset	Read/Write	Description
TxIrqEnable	0x0F	RW	The transmitter interrupt can be enabled to drive the interrupt line. Default is disabled.
RxIrqEnable	0x0F	RW	The receiver interrupt can be enabled to drive the interrupt line. Default is disabled.
BbTimerIrqEnable	0x0F	RW	The baseband timer can be enabled to drive the interrupt line. Default is disabled.
LoIrqEnable	0x0F	RW	The Local Oscillator interrupt can be enabled to drive the interrupt line. Default is disabled.

4 nanoLOC Programming Interface (SPI)

This section provides guidelines and procedures on the following topics:

- SPI controller
- SPI signals and bus timing values
- SPI transfer format
- SPI protocol format
- Performing read and write operations

The *nanoLOC TRX Transceiver* is programmed through the use of a synchronous *Serial Peripheral Interface* (SPI) interface. This SPI interface is used to write control bits into the appropriate memory locations in the chip register and baseband locations. The SPI communicates between a master device, such as a microcontroller, and one or more slave devices, such as the nanoLOC chip and serial memory devices, connected via the SPI bus.

4.1 The SPI Controller

The SPI Controller directs SPI requests to the appropriate registers in the chip. However, because the SPI Controller is located in the PWD section, programming the chip is ONLY possible when the PWD section is powered. As can be seen from figure 4 below, all SPI requests are distributed through the SPI Controller, whether to registers and RAM locations in the PWD section or to registers and RAM locations in the ON section.

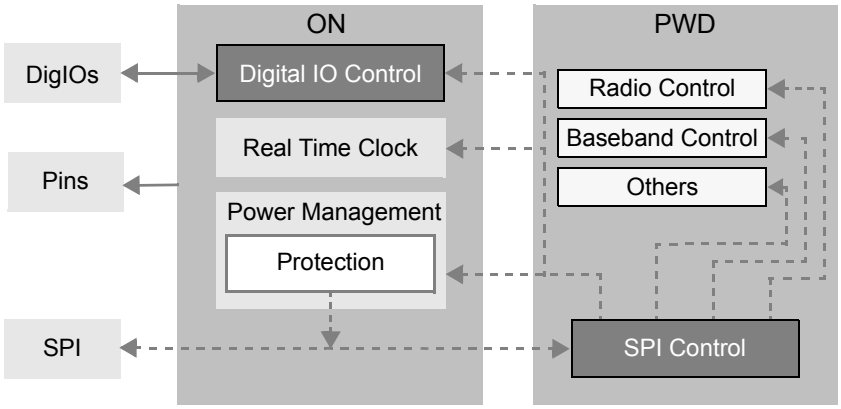


Figure 4: nanoLOC SPI Controller

Recall that during power down mode, the PWD section is completely powered down to reduce chip power consumption. However, the ON section retains a small amount of power to save specific chip settings related to the Digital IO pins, the Real Time Clock, and Power Management. The connections between a microcontroller and the SPI Controller is protected to enable the chip to wake-up quickly and to be fully operational in a very short time.

When the chip is brought into PowerUp mode, the connection between the microcontroller and the SPI Controller over the SPI bus is quickly reestablished. Then, depending on what Power Down Mode was set, the microcontroller then initializes the registers in the PWD section and (optionally) calibrates the Local Oscillator frequency.

Includes Mirror of On Part Registers

The SPI Controller contains a mirror of the registers in the ON part. This is done to save power due to less connections between ON and PWD, especially for those registers relating to Digital IO control. It is also mirrored to the SPI Controller because the registers in the Real Time Clock Controller and Power Management use the slower 32.786 kHz clock, whereas the SPI Controller runs with the much faster SPI Clock.

Includes Registers Required when Baseband Clock is Off

The SPI Controller also include those registers that must be accessible with the Baseband clock is off. These include:

- Pad controls

  For example, registers for the SPI direction (MSB/LSB)

- Clock controls

  For example, registers for enabling for BASEBAND clock

- Constants

  For example, the registers for the chip version and revision number

4.2 SPI Signals and Bus Timing Values

4.2.1 SPI Clock

All registers to which the SPI Controller write are run with SPI clock, with the exception of registers that are Read Only. For more details, see *SPI Signals: SpiClk, SpiSsn, SpiTxD, SpiRxD* on page 14.

4.2.2 Maximum SPI Transfer Rate

The maximum transfer rate for communication between the microcontroller (master device) and the *nanoLOC* chip (slave device) is 16 MBit/s.

4.2.3 SPI Signals: SpiClk, SpiSsn, SpiTxD, SpiRxD

The SPI interface works as a half-duplex channel and uses four signals:

- `SpiClk` (SPI Clock)

  This is a clock signal applied by the microcontroller (master device) that is used to transmit and receive data.

- `SpiSsn` (SPI Slave Select)

  This signal is used by the microcontroller (master device) to select the *nanoLOC* chip for communication, or other slave devices.

  Note: This signal is specific to only one slave.

- `SpiTxD` (Data Transmit)

  This signal is MISO (Master – Input; Slave – Output). With this signal, data is sent from a slave device (*nanoLOC chip* or other slave devices) to a master device (microcontroller).

  SpiTxD is programmable as either push-pull or open-drain pin. When more than one slave device is connected to the SPI bus, the SpiTxD pin should be set to open drain mode (in this mode an external pull up resistor is required).

- `SpiRxD` (Data Receive)

  This signal is MOSI (Master – Output; Slave – Input). With this signal, data is sent from a master device (microcontroller) to a slave device (*nanoLOC chip* or other slave devices).

4.2.4 SPI Interface Connections

Figure 5 below shows the connections between a microcontroller (master device) and the nanoLOC chip (slave device 1) and other slave devices (slave n). It also shows the direction of these connections:

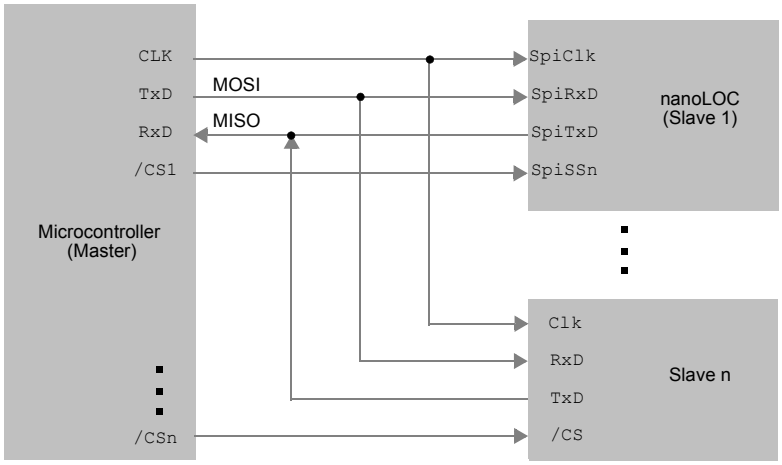


Figure 5: SPI interface connection

4.2.5 SPI Bus Timing Values

The following table lists the timing values for the SPI bus:

Table 14: SPI bus timing values

Parameter	Minimum	Maximum	Description
f_{max}	–	27 MHz	SpiClk
t_{LC}	18.5 ns	–	Low time SpiClk
t_{HC}	18.5 ns	–	High time SpiClk
t_{SS}	4 ns	–	SpiSsn Setup
t_{HS}	2 ns	-	SpiSsn Hold
t_{SRxD}	4 ns	–	SpiRxD Setup
t_{HRxD}	2 ns	–	SpiRxD Hold
t_{PDTxD}	–	18.5 ns	SpiTxD Propagation Delay Drive
t_{HTxD}	2.5 ns	–	SpiTxD Hold
t_{PTxDZ}	–	18.5 ns	SpiTxD Propagation Delay High Impedance

4.3 SPI Transfer Format

This section describes the bit ordering and the read and write timing of the SPI bus.

4.3.1 SPI Bit Ordering

SPI bit ordering of the *nanoLOC* chip is configurable, where either Least Significant Bit (LSB) First or Most Significant Bit (MSB) First can be selected.

For programming the SPI bus, the field SpiBitOrder is used, where:

- 1 = the first bit transmitted over the SPI is MSB
- 0 = the first bit transmitted over the SPI is LSB

The default bit ordering is LSB first.

4.3.2 Read Timing of the SPI Bus

The read timing of the SPI bus is as follows:

1 After receiving the last address bit, the *nanoLOC* chip begins to switch the data bits to `SpiTxD`.

2 On each falling edge of `SpiClk`, a new data bit is assigned.

3 The output starts driving with the first read data bit.

4 The timing of the `SpiRxD` pin that is used for length and address during read is identical to the timing of the `SpiRxD` pin that is used during writing.

The read timing of the SPI bus is shown in the following figure.

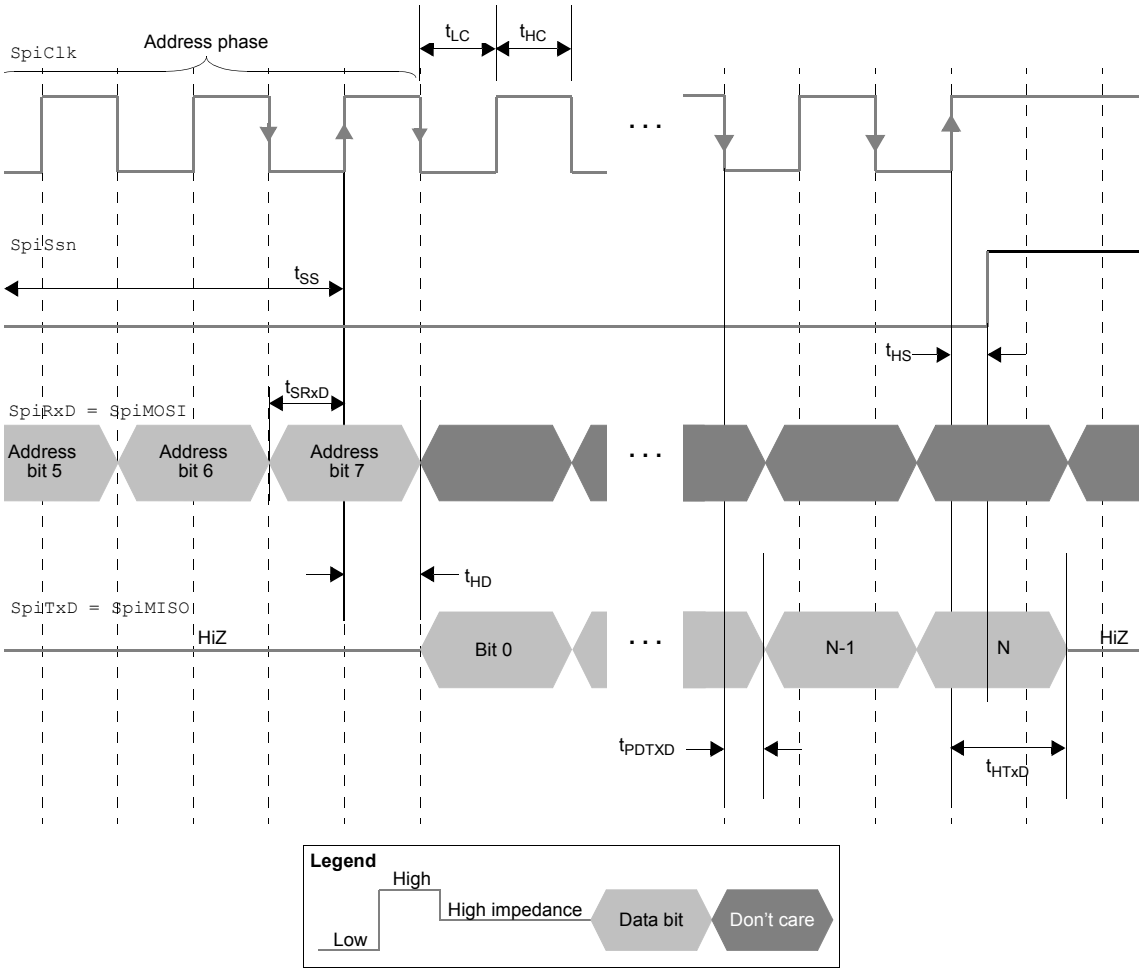


Figure 6: Read timing of the SPI bus

4.3.3 Write Timing of the SPI Bus

The write timing of the SPI bus is as follows:

1 On the first falling edge of the clock signal (`SpiClk`), with the master device SPI slave select (`SpiSsn`) being low, the first data bit is switched (sent) to `SpiRxD`.

2 As long as `SpiSsn` is activated, the *nanoLOC* chip latches one data bit onto each rising edge of the clock signal (`SpiClk`).

3 If several slave devices share the SPI bus, then the master device must control the communication with slave-dedicated chip selects (`SpiSsn(n)`).

4 To complete an operation to a specific SPI slave, the `SpiSsn` signal must be set to high after the last data bit has been transmitted.

The write timing of the SPI bus is shown in the following figure:

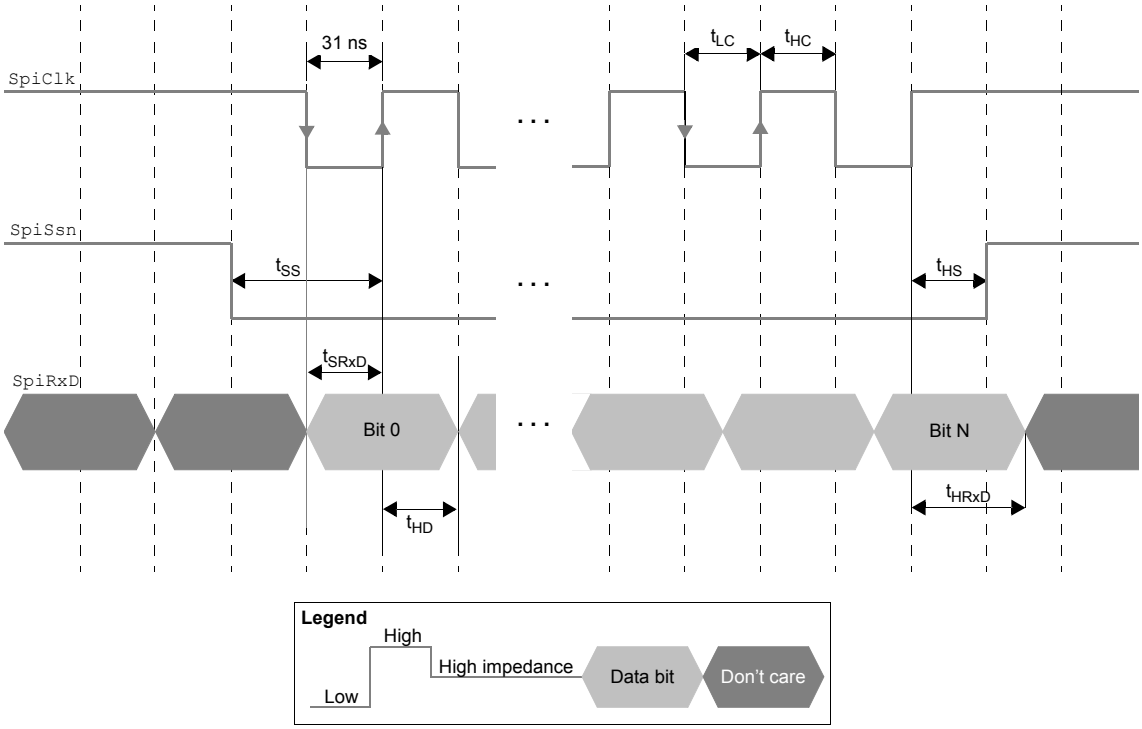


Figure 7: Write timing of the SPI bus

4.4 SPI TxD Output Driver

The SPI TxD Output Driver can be set as either push-pull or open-drain by using the field SpiTxDriver in register offset 0x00.

- When SpiTxDriver = 0, then the TxD output driver is set to open-drain.

  The pad is driven only when a logic 0 is sent from the nanoLOC chip to the SPI master. Otherwise, the output is in high-impedance state.

- When SpiTxDriver = 1, then the TxD output driver is set to push-pull.

  The pad is driven only when data is sent from nanoLOC to the SPI master. Otherwise, the output is in high-impedance state.

The default value is SpiTxDriver = false.

4.5 SPI Protocol Format

The SPI of the *nanoLOC* chip implements a burst capable address mode with automatic address increment. The SPI protocol has a variable data payload. The fields <Instruction> <Address> <N byte data> define the SPI protocol and is shown in the following figure.

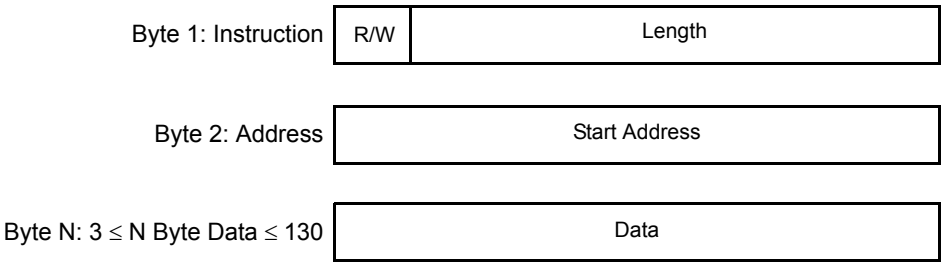


Figure 8: SPI transfer format

4.5.1 Bytes per transfer

For each SPI transfer, between 3 and 130 bytes (1-128 data bytes) can be sent per transfer.

4.5.2 Byte 1: Instruction

The <Instruction> field has a fixed length of one byte and contains the type of command (read[0] / write[1]) and number of data bytes:

MSB							LSB
7	6	5	4	3	2	1	0
Direction Bit	Data Bytes Size						

- Bit 7 is the “direction bit” and is used to differentiate between read or write access, where:
  - 1 = write access
  - 0 = read access
- Bits 0 to 6 provides the data byte size, that is the size of data that will be sequentially written to the *nanoLOC* chip or read from the *nanoLOC* chip in an access operation. The maximum length is 128 bytes, which is indicated by a 0x00 value.

4.5.3 Byte 2: Address

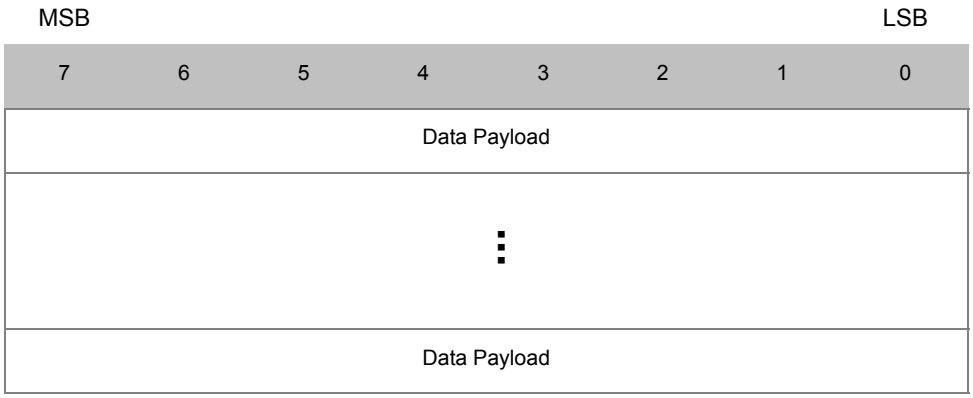
The <Address> field has a fixed length of one byte and contains the first address to be accessed, where additional data bytes are accessed at the following addresses.

MSB							LSB
7	6	5	4	3	2	1	0
Address Byte							

If the data payload is greater than one, the interface is used in burst mode with automatic address increment.

4.5.4 N Bytes: Data Payload

The <Data Payload> field has a size (N) and can vary from one to 128 bytes. It contains the data that is to be written to the target register(s) in the *nanoLOC* chip or read from the target register(s) in the *nanoLOC* chip.



4.6 Read and Write Operations

This section provides an overview of reading data from and writing data to the nanoLOC TRX Transceiver.

4.6.1 Read Operations

To read data from the *nanoLOC* chip, do the following:

1 In the <Instruction> field, set the direction bit to the value 0 (read data) and set the data size, where the maximum size is 128.

2 In the <Address> field, set the source address.

3 Send the <Instruction> and <Address> data to the slave device(s).

4 Read in the resultant data from the slave device(s).

The timing of a read operation is shown in the following figure:

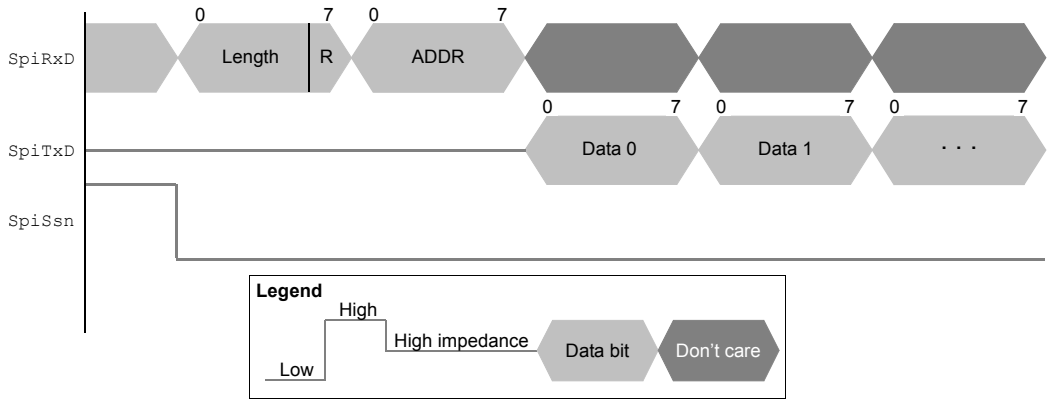


Figure 9: Read Access (LSB first)

Note: The SpiTxD pin is activated into push-pull or open-drain mode only if the data payload bytes are transmitted and if the slave device is selected through SpiSsn. Otherwise, the SpiTxD pin is always in the high impedance state.

4.6.2 Write Operations

To write data to the *nanoLOC* chip, do the following:

1 In the <Instruction> field, set the direction bit to the value 1 (write data) and set the data size, where the maximum size is 128.

2 In the <Address> field, set destination address.

3 In the <Data Payload> field, set the data that will be written to the slave device(s).

4 Send the <Instruction>, <Address>, and <Data Payload> data to the slave device(s).

The timing of a write operation is shown in the following figure:

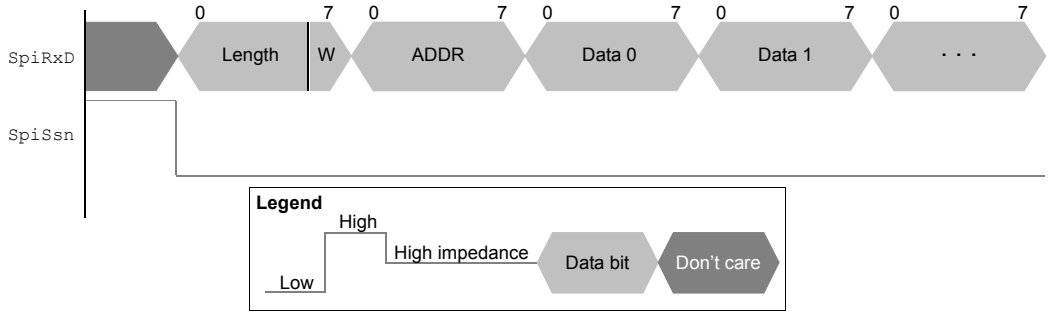


Figure 10: Write access (LSB first)

Note: During a write operation the SpiTxD pin is always in the high impedance state.

4.6.3 Write Access Example

This section shows a write access example where three bytes (0x11, 0x22 and 0x33) are written to three registers that start at the address location 0x23:

<0x83><0x23><0x11><0x22><0x33>

Instruction field | Address field | Data payload field

- **Instruction Field**

  First, the chip needs to know if this request is a read or write command, and how many bytes of data will be written to the register(s). In this example, the <Instruction> field has a value of <0x83>, which has a binary value of 10000011, as shown in the following diagram:

MSB LSB

7	6	5	4	3	2	1	0
1	0	0	0	0	0	1	1

Write Access | Number of Bytes = 3

The bit direction is set to write with three bytes of data to follow that are to be written.

- **Address Field**

  Next, the chip needs to know to where in the register these three bytes of data are to be written (that is, which offset address to point to). In this example, the <Address> field has a value of <0x23>, which has a binary value of 00100011, as shown in the following diagram:

MSB LSB

7	6	5	4	3	2	1	0
0	0	1	0	0	0	1	1

Address location is 0x23

The data bytes are be written beginning at the offset address 0x23.

- **N Data Fields (3 Bytes)**

  Finally, include the data to be written beginning at the offset address 0x23. In this example, the <Data Payload> field has the values 0x11, 0x22, and 0x33, which have the binary values 00010001, 00100010, and 00110011, respectively, as shown in the following diagram:

MSB LSB

7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1

The three values 00010001, 00100010, and 00110011 will be written to the chip registers beginning at offset address 0x23, that is offset addresses 0x23, 0x24, and 0x25.

4.6.4 Write Access Example Memory Map

Using the example of the previous write operation, the following illustrates the location of the three registers in the chip register where the data provided has been written.

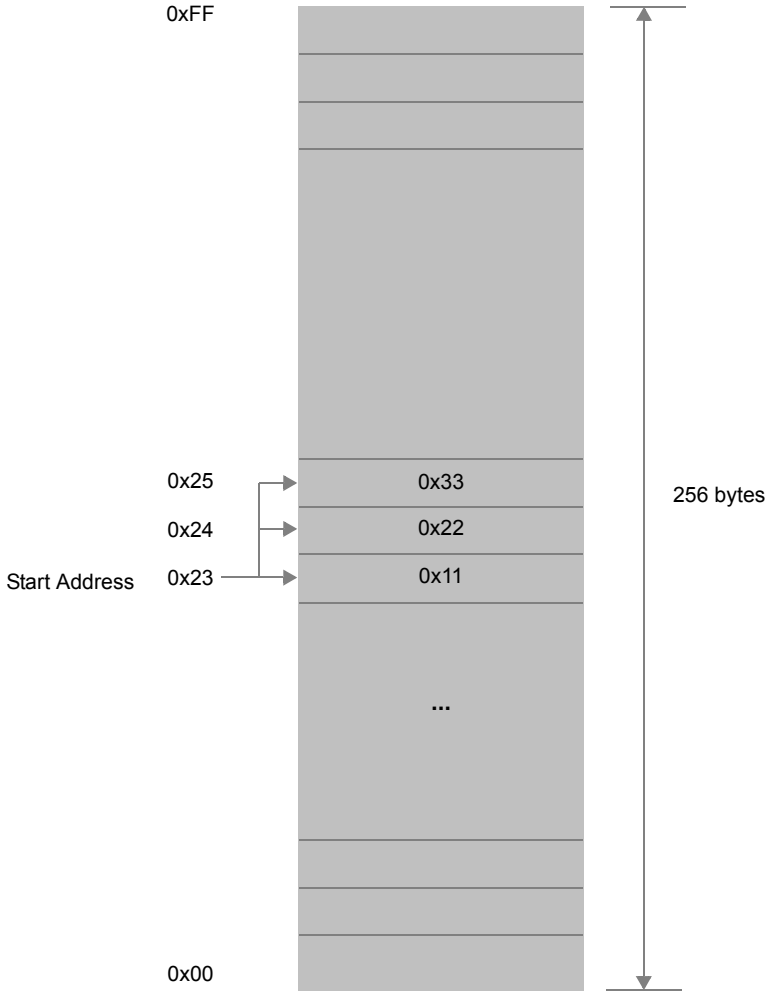


Figure 11: Write access example memory map

4.7 Programming Interface (SPI) Related Fields

4.7.1 Clock Control

Table 15: Clock control fields

Field	Offset	Read/Write	Default
EnableBbCrystal	0x08	RW	0x0
BypassBbCrystal	0x08	RW	0x0
EnableBbClock	0x08	RW	0x0
EnableFeatureClock	0x08	RW	0x0
FeatureClockFreq	0x08	RW	0x0

4.7.2 Reset Control

Table 16: Reset control fields

Field	Offset	Read/Write	Default
ResetBbClockGate	0x07	RW	reset clock gates
ResetBbRadioCtrl	0x07	RW	reset transceiver

4.7.3 Bit Order

Table 17: Bit order fields

Field	Offset	Read/Write	Default
SpiBitOrder (MSB/LSB first)	0x00	RW	LSB

4.7.4 Memory Control

Table 18: Memory control fields

Field	Offset	Read/Write	Default
RamIndex	0x0E	RW	select page in memory
DeviceSelect	0x0E	RW	select memory

4.7.5 Battery Management Fields

Table 19: Analog control fields

Field	Offset	Read/Write	Default
BattMgmtEnable	@0x03	RW	0x0
BattMgmtThreshold	@0x03	RW	0x0
BattMgmtCompare	@0x03	RO	0x0

4.7.6 Constants/Status Fields

Table 20:

Field	Offset	Read/Write	Default
Version	@0x01	RO	0x05
Revision	@0x02	RO	0x01
TxIrqStatus	@0x0F	RO	0x0
RxIrqStatus	@0x0F	RO	0x0
BbTimerIrqStatus	@0x0F	RO	0x0
LoIrqStatus	@0x0F	RO	0x0

5 nanoLOC Clocks

5.1 nanoLOC Clocking Structure

The nanoLOC chip provides four clocks for users:

- 32.786 kHz Clock

  This clock is used to run the Real Time Clock and Power Management. The modules in the digital part that use the 32.768 kHz clock are shown in figure 12 below with this shading .

- SPI Clock

  This clock is used for the SPI Controller and for the Digital IO Control, which is used for running the four digital IO pins. The frequency of the SPI clock is dependent on the frequency required by the microcontroller. The maximum frequency is 32 kHz. The modules in the digital part that use the SPI clock are shown in figure 12 below with this shading .

- Baseband Clock

  This clock is used for baseband control, radio control, and other baseband usages. The frequency of the baseband clock for the *nanoLOC* chip is 32 MHz. The baseband clock can be enabled or disabled by software. The modules in the digital part that use the baseband clock are shown in figure 12 below with this shading .

- CSQ (Chirp Sequencer) Clock

  This clock is used by the Chirp Sequencer (CSQ) Memory. The frequency of the CSQ clock is determined by dividing the LO frequency by 10. The CSQ clock can be enabled or disabled by software (enter cross reference here). The modules in the digital part that use the CDQ clock are shown in figure 12 below with this shading .

These clocks run these different modules which are in the ON and PWD sections of the digital part of the chip, as is shown in the following figure.

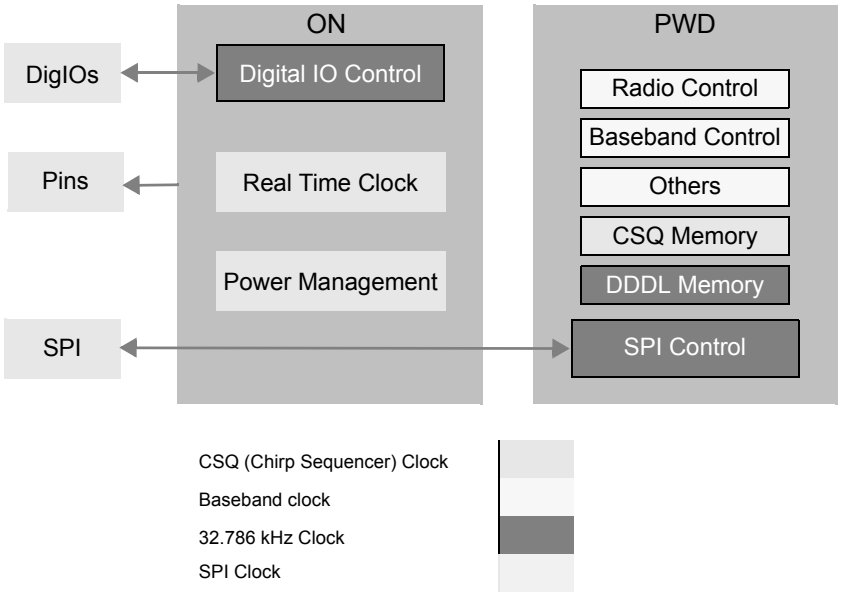


Figure 12: nanoLOC clock structure

5.2 32.786 kHz Clock (Real Time Clock)

The Real Time Clock runs at 32.768 kHz. It can be set or read through software using a 48 bit Real Time Clock value. As this clock is part of the ON section of the digital part of the chip, it is always powered (unless the chip is completely powered off) and can, therefore, be used for creating a wake-up time event.

The Real Time Clock is also used to generate a 4 kHz clock (the power management clock) for use by the Power Management module in the ON section. This slow clock is, like the Real Time Clock, always available during power down mode to protect the connections between the SPI and the SPI Controller.

5.2.1 Updating and Reading Real Time Clock Through Software

The 48 bit Real Time Clock is set and read through software. Since the Real Time Clock is updated every 30.517578125 µs, it is not directly accessible by the user. Therefore, a buffer in RAM is used, RamRtcReg, to hold the value of the internal Real time Clock after it has been read, or to hold a value that will be written to the Real Time Clock.

To update the Real Time Clock, do the following

1 Write a 48 bit value for the Real Time Clock to the buffer RamRtcReg.

2 Write this buffer to the Real Time Clock using the write command RtcCmdWr.

To read the value of the Real Time Clock, do the following:

1 Read the Real Time Clock using the read command RtcCmdRd to place the 48 bit value of the Real Time Clock in the buffer RamRtcReg .

2 Read out the buffer RamRtcReg.

5.2.2 Updating and Reading the Real Time Clock Through the TimeB Packet

The Real Time Clock can also be updated from received TimeB packets that have been sent from a base station or other stations in a network. This updating can be performed automatically or manually. If automatically, then when a TimeB packet is received, the RTC value in the packet is automatically written to the Real Time Clock. If manually, then when a TimeB packet is received, the RTC value in the packet must be manually updated as described above in *Updating and Reading Real Time Clock Through Software* on page 27.

To automatically update the Real Time Clock through from the RTC value in a TimeB packet, do the following:

- Set RtcTimeBAutoMode = NA_RtcTimeBAutoModeOn_BC_C to enable auto mode for TimeB packets.

  This causes the RTC values in received TimeB packets to be automatically stored in the Real Time Clock.

To manually update the Real Time Clock through the RTC value in a TimeB packet, do the following:

- Set RtcTimeBAutoMode = NA_RtcTimeBAutoModeOff_BC_C to enable manual mode for TimeB packets.

  This causes the 48 bit RTC value in received TimeB packets to be stored in the Real Time Clock buffer RamRtcReg, where it can then be written to the Real Time Clock using the write command RtcCmdWr.

5.2.3 RTC and TimeB Related Fields

The following lists the fields used for updating the Real Time Clock with TimeB packets.

Table 21: RTC and TimeB packets

Field	Offset	Read/Write	Description
RtcTimeBAutoMode	0x62	WO	When set to 1, the RTC value is transferred in TimeB packets
RtcTimeBRxAdj	0x61	WO	Adjusts the RTC value for receiver delay.
RtcTimeBTxAdj	0x60	WO	Adjusts the RTC value for transmitter delay
RamRtcTx	0xE0	RW	The 48 bit RTC value that is to be transmitted (loaded/written) in a TimeB packet
RamRtcRx	0xE8	RW	The 48 bit RTC value that has been received in a TimeB packet
RtcCmdWr	0x62	WO	Writes the 48 bit RTC value.
RtcCmdRd	0x62	WO	Reads the 48 bit RTC value
RamRtcReg	0xF0	RW	48 bit RTC value read from the RTC by software or written to the RTC by software

5.2.4 Using the Real Time Clock as a Wake-Up Event

The Real Time Clock can be used to create a wake-up time event at a predefined time. The field EnableWakeUpRtc enables the Real Time Clock to be used as a wake-up event.

Note: RtcWakeUpTime can only be accessed through WakeUpTimeByte and WakeUpTimeWe.

The wake-up time is a 24 bit value split into 3 bytes. The field WakeUpTimeByte is used to set each of the three segments of the wake-up time (the segment to write is selected using the a byte-selector field WakeUpTimeWe). This wake-up time value is then compared to bits 31 to 8 of the Real Time Clock. When these values match, a wake-up event is then triggered. This process is shown in the following figure.

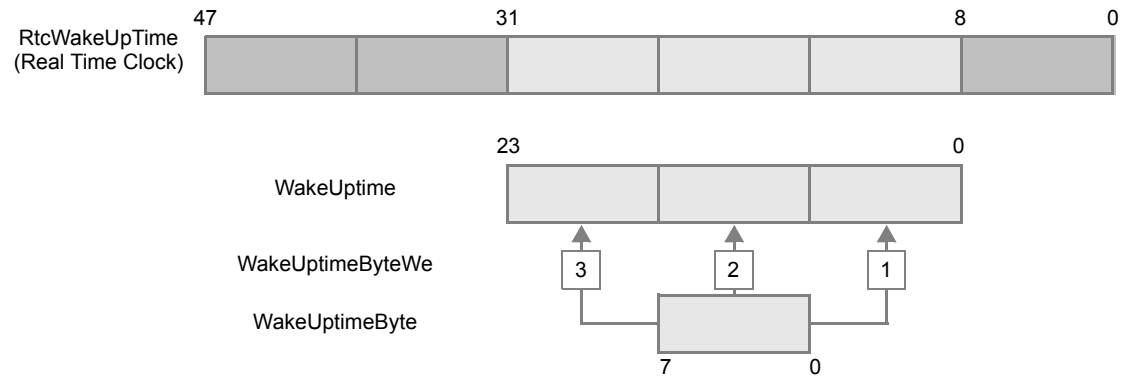


Figure 13: Using Real Time Clock as wake-up event

5.2.5 RTC and Wake-Up Time Related Fields

The following fields are used for using the Real Time Clock as a wake-up time event.

Table 22: Wake-up time fields

Field	Offset	Read/Write	Description
WakeUpTimeByte	0x01	WO	Stores a one byte value for the wake-up time, which is programed to the wake-up time RtcWakeUpTime using WakeUpTimeWe.
WakeUpTimeWe	0x02	WO	Loads the value of RtcWakeUpTimeByte to the appropriate byte of the wake-up time in the wake-up time circuitry.
EnableWakeUpRtc	0x06	RW	Enable Real Time Clock as Wake-Up Source

5.3 SPI Clock

The SPI Clock is an externally delivered clock provided to the chip through an SPI signal from a master device, such as a microcontroller. The frequency of the SPI clock is dependent on the frequency of the master device. The maximum frequency of the SPI clock, however, is 32 kHz. It is provided as one of the four signals of the SPI interface: `SpiClk`.

Digital IO Pins

The SPI Clock is used to run the SPI Controller. As the Digital IO Control is run by the SPI Controller, the SPI Clock is also used to run the four digital IO pins: D0, D1, D2, D3.

SPI Clock and Writing to Chip Registers

The SPI Clock also runs all registers that are written by the SPI Controller. This is indicated in the properties column of the register description. Registers that are Read Only, however, do not use the SPI Clock.

5.4 Baseband Clock

The baseband clock distribution obtains its frequency from the internal quartz oscillator. In the *nanoLOC* chip, the frequency provided by this oscillator is 32 MHz. This clock is used for baseband control, radio control, and other baseband usages. The baseband clock can be enabled and disabled by software.

Baseband Clock and Power Down Mode

As the baseband clock is entirely within the PWD section, when the chip goes into Power Down mode, then the PWD section is also powered off. Therefore, the baseband clock and all modules run by the baseband clock are also powered off. Furthermore, the contents of all chip registers are also lost.

Switching Off the Baseband Clock To Reduce Chip Power Consumption

To reduce chip power consumption, but without losing the contents of chip registers, the baseband clock distribution can be stopped and the quartz oscillator circuitry can be powered down. The chip provides a means of doing so without introducing clipping or glitches on the clock signal.

Three fields, EnableBbClock, ResetBbClockGate, and EnableBbCrystal are used to switch off the baseband clock and to power down the quartz oscillator. Subsequently, when the quartz oscillator is powered up and the baseband clock distribution is switched on, the SPI Controller does not need to be reinitialized, thereby saving the contents of the chip registers. The following block diagram shows the baseband clock and baseband quartz oscillator circuitry.

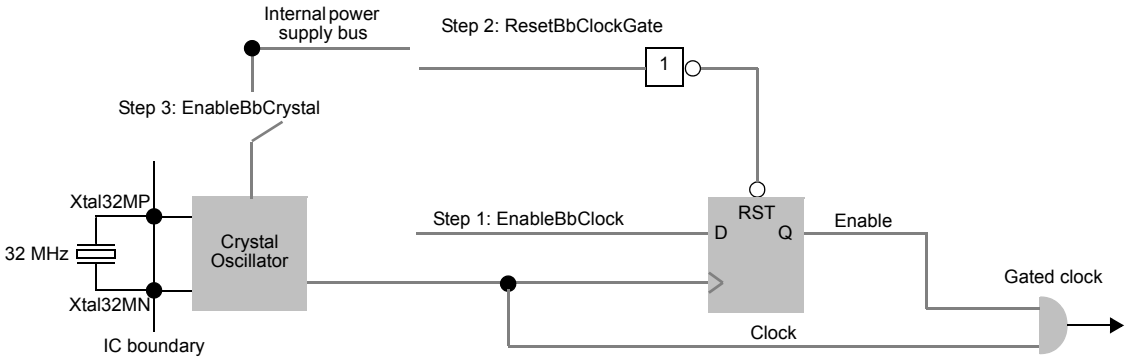


Figure 14: Switching on/off the baseband clock

ResetBbClockGate

To keep the clock switcher in a stable state during warm-up and shut down of the quartz oscillator, ResetBbClockGate is used.

5.4.1 Stopping the Baseband Clock Distribution

To stop the baseband clock distribution, do the following:

1 Switch the baseband clock distribution off using of EnableBbClock = False.

2 Enable active reset of the baseband clock circuitry using ResetBbClockGate = True.

3 Power off the internal baseband quartz oscillator using EnableBbCrystal = False.

5.4.2 Starting the Baseband Clock Distribution

To enable the baseband clock distribution, do the following:

1 Switch the baseband clock distribution on using of EnableBbClock = True.

2 Enable inactive reset of the baseband clock circuitry using ResetBbClockGate = False.

3 Power on the internal baseband quartz oscillator using EnableBbCrystal = True.

5.4.3 Baseband Clock Related Fields

Table 23: Wake-up time fields

Field	Offset	Read/Write	Description
ResetBbClockGate	0x07	RW	*Purpose:* Resets the baseband clock distribution circuitry.
ResetBbRadioCtrl	0x07	RW	*Purpose:* Resets the digital baseband and radio control circuitries supplied by the baseband clock.
EnableBbCrystal	0x08	RW	*Purpose:* Powers on the internal baseband quartz oscillator.
EnableBbClock	0x08	RW	*Purpose:* Enable the baseband clock distribution.

5.5 Chirp Sequencer Clock

The Chirp Sequencer Clock (CSQ) is required for programming the Chirp Sequencer RAM memory. The frequency of the CSQ clock is determined by dividing the LO frequency by 10. The CSQ clock can be enabled or disabled by software using EnableCsqClock .

5.5.1 Chirp Sequencer Clock Related Fields

Table 24: Wake-up time fields

Field	Offset	Read/Write	Description
EnableCsqClock	0x42	RW	Enables the Chirp Sequencer (CSQ) clock.

6 Power Management

The *nanoLOC TRX Transceiver* has been designed to efficiently use the power required to operate it. Modules required during transmission and reception, such as baseband memory, CSQ memory, the SPI Controller, and other modules, are located in the PWD section, which can be powered down when not in use. The minimum required modules to keep the chip operational, such as the Digital IO Control, the Real Time Clock, and Power Management, are located in the ON section, which maintains a connection with the microcontroller using minimal power.

Unless the power source, such as a battery, is completely disconnected from the chip, the ON part remains powered at all times. This ensures the functions of the ON section are maintained during all power down modes. The PWD part, however, can be completely powered off or only the baseband clock distribution and quartz oscillator circuitry can be powered off, depending on usage requirements.

6.1 Power Management Module

The Power Management module located within the ON section is provided with a clock frequency of 4 kHz by the 32.768 kHz Real Time Clock.

The figure below shows the connections between the pins and the ON and PWD sections as dashed lines. The Power Management module protects several connections during power down of the PWD section, as shown by the light lines.

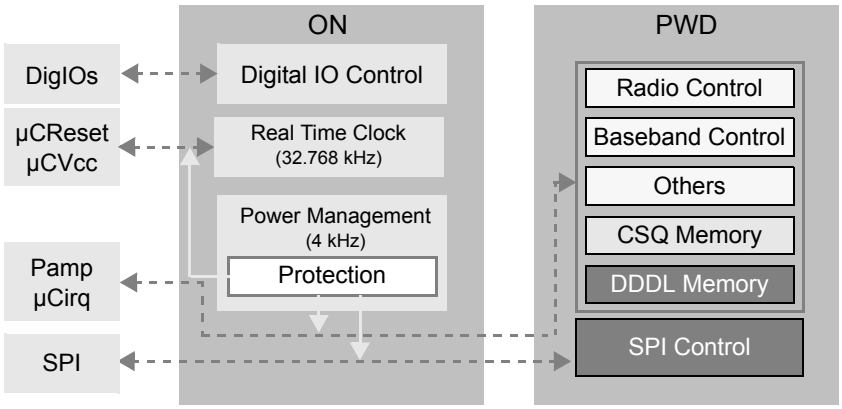


Figure 15: Power Management Module

The Power Management module is responsible for maintaining the pull-up and pull-down states of the SPI interface during all Power Down modes. This includes the pins: SpiClk, SpiSSn, SpiRxD, and SpiTxD.

This module is also responsible for maintaining the pull-up and pull-down states of several additional input/output pins, including:

- PowerOnReset, an input pin which provides a signal to is the power up reset line.
- Pamp, an output pin which is used to control an external power amplifier.
- µCReset, an output pin which resets an external microcontroller.
- µCIRQ, an output pin which sends interrupt requests to an external microcontroller.

The Digital IO pins are always powered as they can be programmed to provide a wake-up event to bring the PWD section back to powered up state.

6.2 Power Management State Model

The power management states model of the *nanoLOC* chip is shown below.

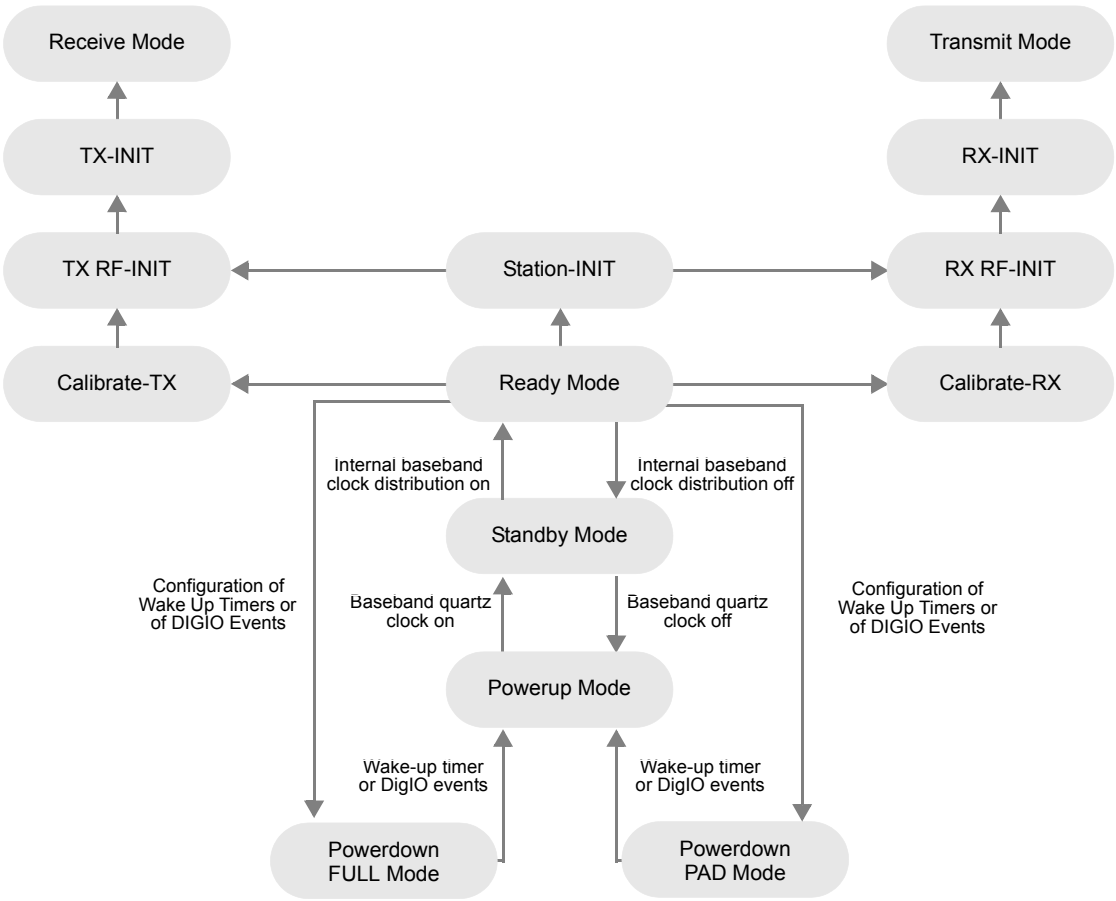


Figure 16: Power management state model

6.3 PowerDownModeFull

In PowerDownModeFull, the chip consumes less power, but after power up, the chip will need to be reconfigured. The chip's pins and registers are powered off. Reconfiguration of the transceiver registers is required after wake-up, but the leakage current is the lowest possible in this mode.

The chip is in the following state during PowerDownModeFull:

- External microcontroller is powered down.
- PWD section is completely powered down, which means all register settings are lost.
- ON section is powered, but all pins, except Digital IO pins, are powered off.
- Real Time Clock is running.
- Wake-up timer is running.
- Digital IO Control is running and Digital IO pins are still running.
- Power Management module is running.

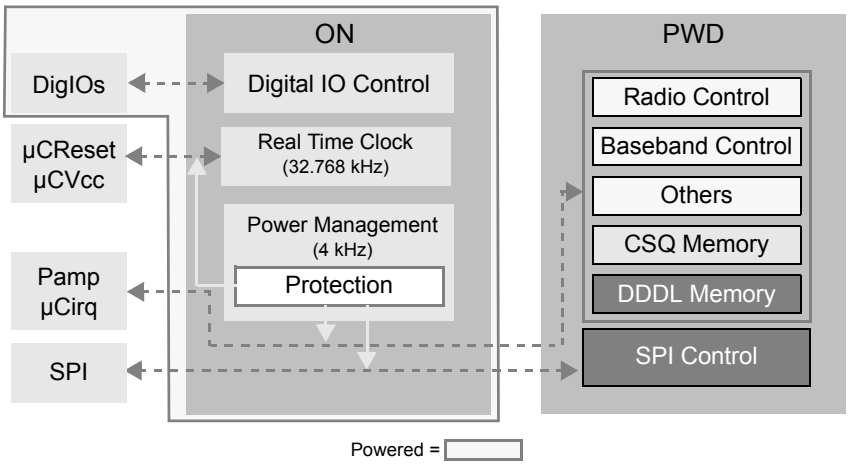


Figure 17: PowerDownModeFull showing powered sections

6.3.1 Setting PowerDownModeFull

To set PowerdownModeFull, do the following:

1 Set PowerDownMode = NA_PowerDownModeFull_C (0x0).

2 Set PowerDown = 1, to go to the power down mode set above.

6.3.2 Current Consumption During PowerDownModeFull

The current consumption[1] during PowerDownModeFull is from 1.0 to 2.0 µA.

6.3.3 Bringing the Chip Out of PowerDownModeFull

Either an internal wake-up timer or an external event on a Digital IO pin brings the chip out of PowerDownModeFull. The chip then goes into PowerUp Mode.

The activation time into PowerUp state from PowerDownModeFull is programmable using the field PowerUpTime in a range between 1 and 32 ms + boot time of the external microcontroller.

After the chip is in PowerUp mode, the external microcontroller can then initialize and (optionally) calibrate the chip. .

6.4 PowerDownModePad

In PowerDownModePad, the chip consumes more power, but after power up, the chip does not need to be reconfigured. All output pads are disabled and all bi-directional pads are switched to input, but all transceiver registers are still powered. Reconfiguration of the transceiver registers is not required, but leakage current is higher.

The chip is in the following state during PowerDownModePad:

- External microcontroller is powered down.
- PWD section remains powered, which means all register settings are maintained.

1. Current consumption values are typical values only and are values without an external µC and where DIGIO-pads are tri-state or inputs and no external pull-up resistors soldered on pads.

- ON section is powered, but all output pins are powered off. .
- Real Time Clock is running.
- Wake-up timer is running.
- Digital IO Control is running, but Digital IO pins are switched to input pins.
- Power Management module remains powered.

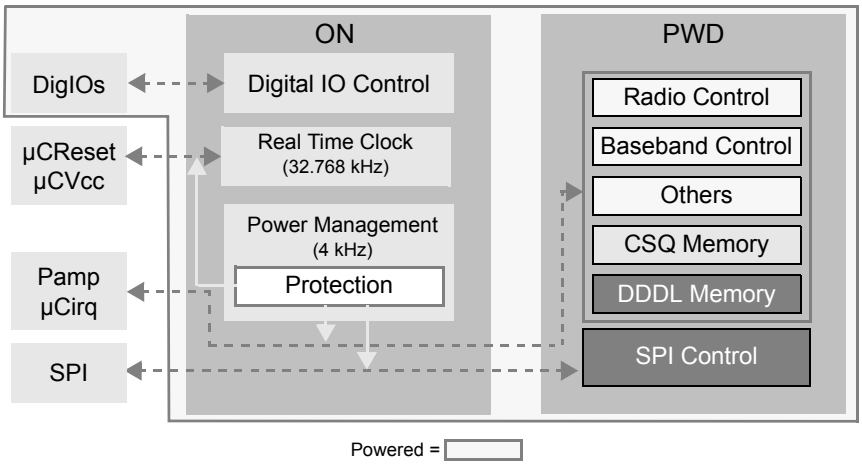


Figure 18: PowerDownModePad showing powered sections

6.4.1 Current Consumption During PowerDownModePad

The current consumption during PowerDownModePad is approximately 75 µA.

6.4.2 Bringing the Chip Out of PowerDownModePad

Either an internal wake-up timer or an external event on a Digital IO pin brings the chip out of PowerDownModePad. The chip then goes into PowerUp Mode, after which it goes into Standby mode.

The activation time into PowerUp state from PowerDownModePad is programmable using the field PowerUpTime in a range between 1 and 32 ms + boot time of the external microcontroller.

After the chip is in PowerUp mode, the external microcontroller can then initialize and (optionally) calibrate the chip.

6.5 Waking Up after PowerDown Modes

The chip is brought to PowerUp mode by a wake-up source. This is either a Real Time Clock wake-up event or an alarm event (a rising or falling edge) at one of the digital IOs configured as a wake-up source. The following lists the fields used to set a wake-up event.

Table 25: RTC and TimeB packets

Field	Offset	Read/Write	Description
EnableWakeUpRtc	0x06	R/W	Enable the Real Time Clock as a wake-up source. Default is disabled.
EnableWakeUpDio	0x06	R.W	Enable a digital IO pin as a wake-up source. Default is disabled.

6.6 PowerUp Mode

An internal wake-up timer or an external event on a Digital IO pin brings the chip to PowerUp mode from either PowerDownModeFull or PowerDownModePad. When the chip is brought to Powerup mode, the following occurs:

1 The external microcontroller is powered.

2 From PowerDownModeFull, all pins are enabled and the PWD section is powered up.

3 From PowerDownModePad, all output pins are enabled and the Digital IO pins become bi-directional.

4 The internal baseband quartz oscillator is powered on, then the baseband clock distribution is switched off.

5 The internal baseband modules are initialized with default settings, and can now be programmed via the SPI interface.

6 A microcontroller can now initiate packet transmission and reception.

6.6.1 Current Consumption in PowerUp Mode

The current consumption during Powerup Mode is from 140 to 300 µA.

6.6.2 Bringing the Chip to Standby Mode

To bring the chip into Standby mode, all blocks are powered, except the baseband distribution remains switched off. Activation time to bring the chip into Standby mode from PowerUp mode is approximately 5 ms, depending on the speed of the baseband quartz oscillator.

6.7 Standby Mode

In Standby mode only the baseband clock distribution is switched off. All other blocks of the chip are fully powered.

6.7.1 Current Consumption in Standby Mode

The current consumption during Standby Mode is from 140 to 300 µA.

6.7.2 Bringing the Chip to Ready Mode

To bring the chip into Ready mode, the baseband clock distribution is switched on. Activation time to bring the chip into Standby mode from PowerUp mode is 6 µs @ 4 Mbit/s SPI (without reconfiguration).

6.8 Ready Mode

In Ready mode, the baseband clock distribution is switched on, and the microcontroller can immediately initiate a packet transmission or reception.

6.8.1 Current Consumption in Ready Mode

The current consumption during Ready Mode is from 8 to 10 µA.

6.9 Completely Powering Off the Chip

When the chip is completely powered off, that is, the power source is disconnected from the chip, both the ON and PWD sections are powered off and all chip settings are lost. The connection between the microcontroller (master device) and the chip (slave device) are lost and the Local Oscillator will require recalibration.

7 nanoLOC Memory (Draft)

The *nanoLOC* chip provides four memory spaces: a 128 byte register, a 512 byte baseband RAM, a Chirp Sequencer (CSQ) RAM, and a Correlator memory. Access is through a 256 byte Device Window divided into a 128 byte RAM block and a 128 byte Register block. Using selectors, RAM memory is swapped into the RAM block for read and write operations. The memory of the *nanoLOC* chip is illustrated below.

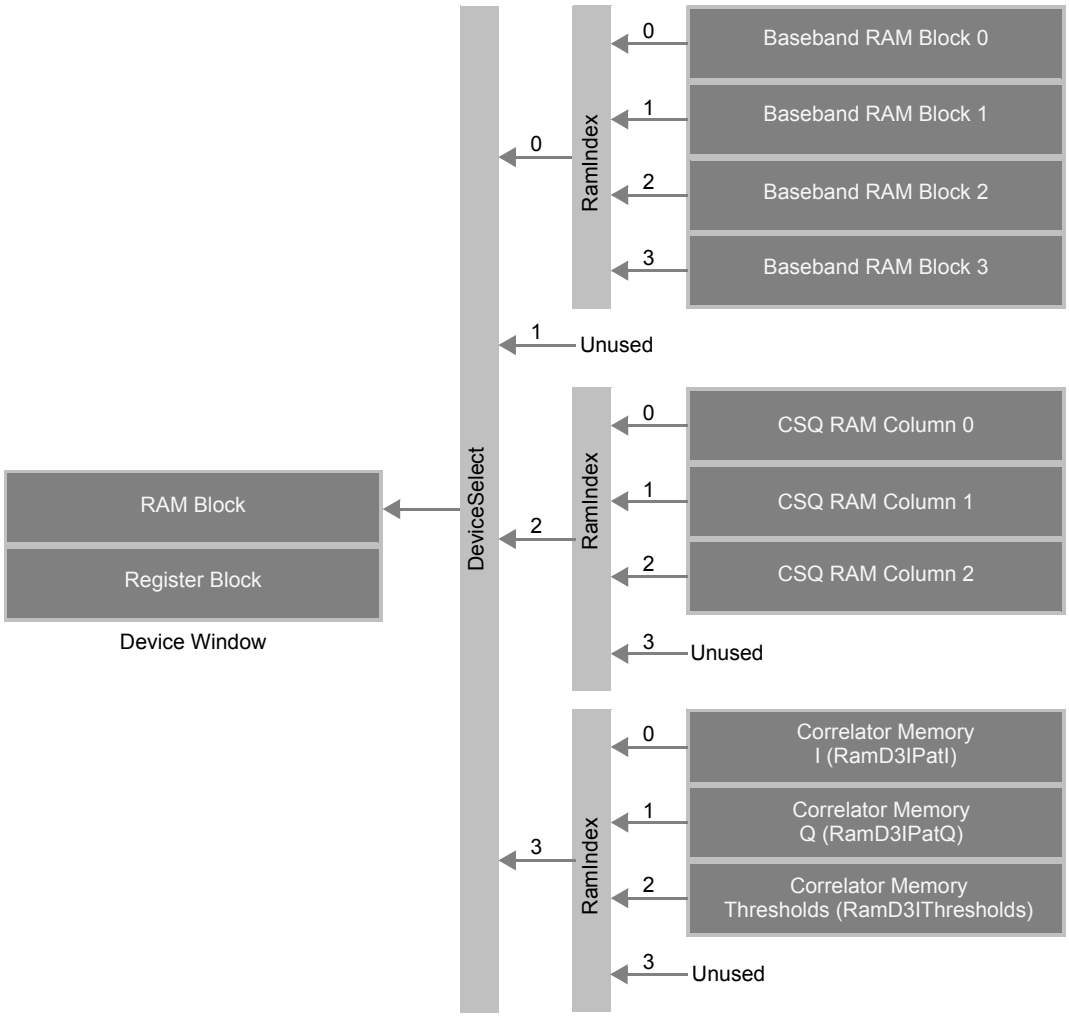


Figure 19: nanoLOC Memory

7.1 Device Window

The Device Window is equivalent to the SPI address range. It is divided into the following two segments:

- 128 byte register block (address locations – 0x00 and 0x7F).
- 128 byte baseband RAM block (address locations – 0x80 and 0xFF).

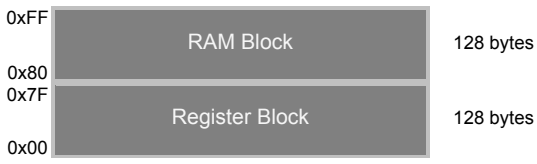


Figure 20: 256 byte Device Window

All chip registers are accessible through the 128 byte register block. However, the baseband RAM has a total address space of 512 bytes, while the Chirp Sequencer RAM and the Correlator memory are both larger than 128 bytes. Therefore, to access these RAM memory locations, a 128 byte segment of RAM must be swapped into the Device Window for read or write activities using selectors. For more details about using the Device Window, see *Memory Access Through SPI* on page 40.

7.1.1 Device Window Related Fields

The following fields are used for the Device Window.

Table 26: Device Window related fields

Field	Offset	Read/Write	Description
RamIndex	0x0E	RW	Selects one page of the selected memory type, which is selected using DeviceSelect, to be mapped into accessible SPI address space. When addresses are greater than 0xFF, the higher bits have to be written to this field.
DeviceSelect	0x0E	RW	Selects either the baseband RAM, the chirp sequencer RAM or the correlator memory to be mapped into the accessible SPI address space. Register access to locations < 0x80 are not influenced by index settings.

7.2 Register Space

The *nanoLOC* chip provides a 128 byte register space for chip configuration settings. The address space for the register is from 0x00 to 0xFF. However, the register is mapped to three other locations within the 1024 byte memory space of the baseband RAM. These additional offsets include 0x100, 0x200, and 0x300, which are logically equivalent to the memory locations between 0x00 and 0x7F. This mapping is illustrated in the figure below.

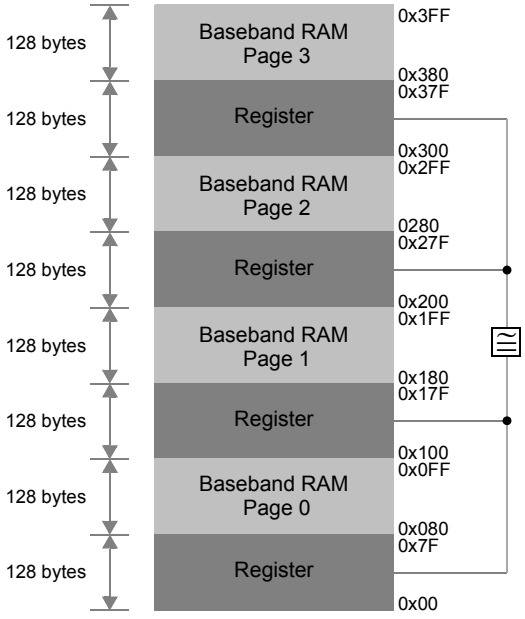


Figure 21: Register mapping in the 1024 byte baseband RAM memory space.

7.3 Baseband RAM Locations

The *nanoLOC* chip contains a 1024 byte baseband RAM memory space. The baseband RAM consists of four 128 byte pages, each with a mapped 128 byte register space. It is used to store both received and ready to transmit MACFrames, station addresses, encryption keys, related control values, and snapshot values of the Real Time Clock (RTC).

Since the entire 512 bytes of the baseband RAM does not fit into the 128 byte RAM block of the Device Window, it is segmented into four parts of 128 bytes each, as shown below.

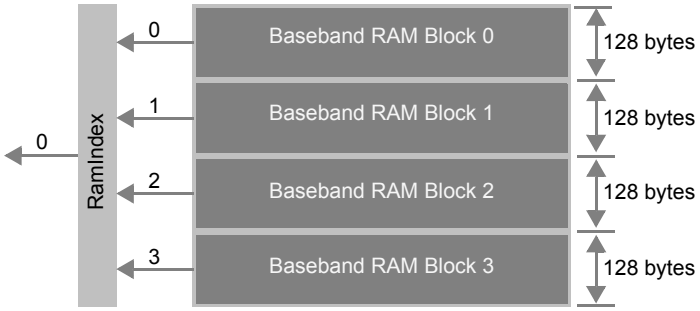


Figure 22: 512 byte Baseband RAM blocks

One of the RAM blocks is swapped into the Device Window RAM block by using DeviceSelect and RamIndex fields, where DeviceSelect = 0 and RamIndex = [0 ... 3].

The baseband RAM is a dual port SRAM with a size of 512 locations by 8 bits, where one port is used for software accesses via the SPI Interface, while the other port is used for the digital baseband controller.

Both ports can be used concurrently as synchronization between data transactions (read and write operations) and baseband controller accesses is not required. Furthermore, software can directly write to or read from the memory without waiting on arbitration flags. The software needs, however, to regard the baseband controller flags of transmit and receive operations. These flags indicate that there is data in memory that is ready to be read out or that the memory is ready to be written to with new data. The embedding of the baseband memory is shown in the following figure.

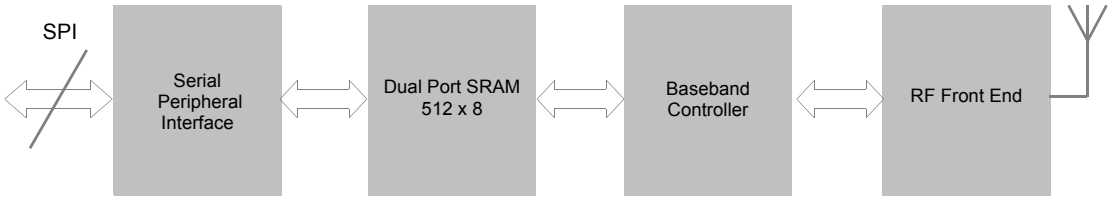


Figure 23: Embedding of the baseband memory

7.4 Memory Access Through SPI

Either SPI single byte operations or SPI burst transfers can be used for chip memory accesses. The lower 7 bits of a given memory location are identical with the start address in the selected segment. SPI burst transfers are limited to 128 bytes (which is the segment size). .

Note: A wraparound SPI burst transfer leads to unpredictable behavior. A wraparound SPI burst is when the number of bytes to be accessed is greater than the number of bytes from the start address to the end of the segment.

7.4.1 SPI Address Format

The address format used to select registers and baseband RAM is a 10 bit value consisting of a 2 bit page selector, a 1 bit RAM block selector, and a 7 bit offset address, as shown below.

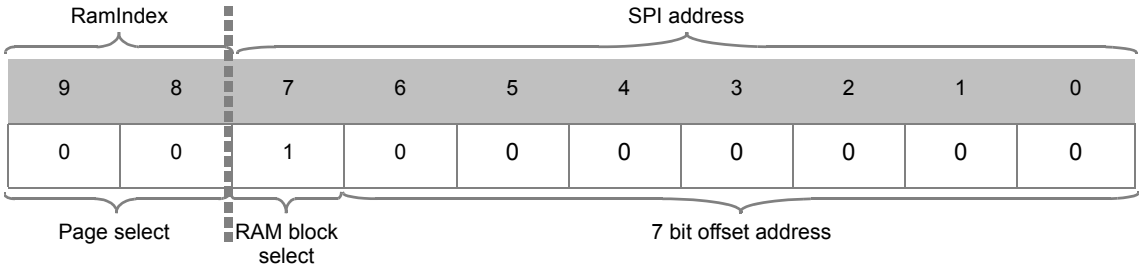


Figure 24: Baseband memory address format

The bits in the SPI address format are described below.

Table 27: SPI Address formats

Bits	Description
RamIndex (Page selector)	This 2 bit page selector (bits 9 and 8) is derived from the RamIndex field. It indicates which page of the baseband RAM to swap into the RAM block of the Device Window. The RamIndex register has to be programmed as an extra SPI access. Note that It is not used for Register access.
SPI Address[7] (RAM block selector)	This is a 1 bit selector where: • 0 = address is in the register • 1 = address is in baseband RAM location
SPI Address[6:0] (Offset address)	This is a 7 bit selector that give the offset of the address location. • If bit 7 was set to 0, then this address is in the Register. • If bit 7 was set to 1, then this address is a baseband RAM location in the segment of RAM selected by the 2 bit RamIndex field.

7.4.2 Accessing a Register Address Location

To access a memory location in the register, it is not necessary to select a baseband RAM segment because the RamIndex field is not used for register access. Consequently, only one SPI transfer is required. Set the SPI address as follows:

- SPI Address[7] = 0 (RAM block select bit is set to 0)
- SPI Address[6:0] = offset address in register

The following figure shows the address format for selecting the register 0x3E.

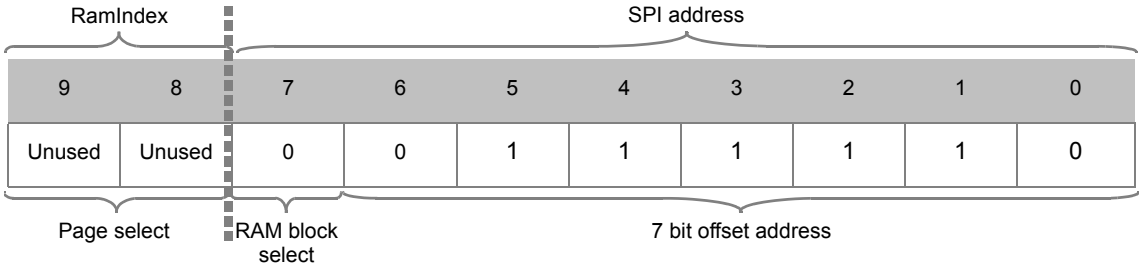


Figure 25: Register access address format example

7.4.3 Accessing a Baseband RAM Address Location

To access a location in baseband RAM, at least two SPI write transfers are required:

1 On the first SPI write transfer, select baseband RAM by writing a DeviceSelect value (register 0x0E):
   - For baseband RAM (DeviceSelect=0)

   Note: For CSQ RAM (DeviceSelect=2) and for Correlator Memory (DeviceSelect=3).

2 Also on the first SPI write transfer, select a RAM block by writing the RamIndex value (register 0x0E):
   - RamIndex[9:8] = baseband RAM page number.

3 On the second SPI write transfer, select the baseband RAM location to accessed:
   - Addr[7]= 1 (RAM block select bit is set to 1)
   - Addr[6:0] = offset address in BBRAM

The following figure shows an SPI write transfer to address the memory location at offset 0xBE:

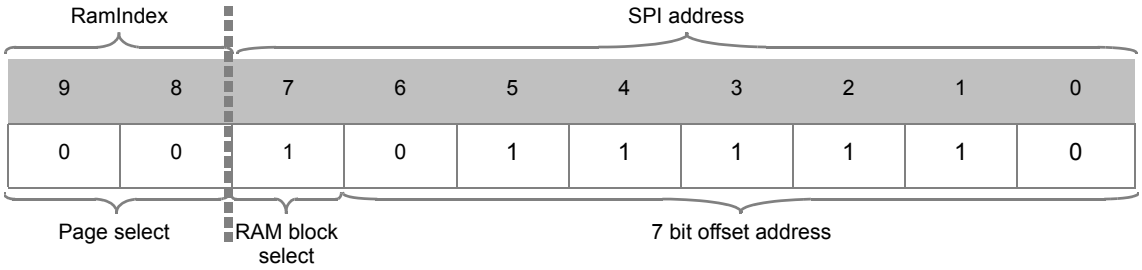


Figure 26: Example baseband memory address format

RAM block 0 is selected by setting bits 8 and 9 to 00, the baseband RAM is selected by setting bit 7 to 1, and the offset location 0x0BE is addressed by setting bits 6 to 0 to 0111110.

Baseband RAM memory access can be illustrated as follows.

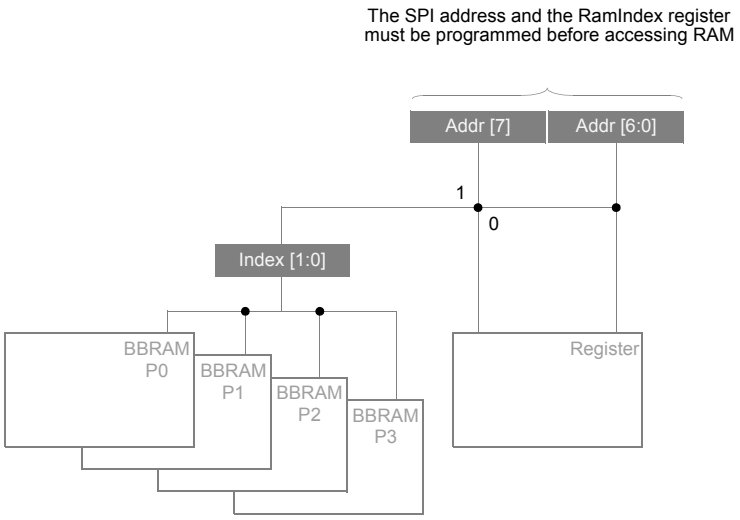


Figure 27: Baseband RAM Memory access

7.4.4 Setting a Shadow Variable for the RAM Access Register

When bit 7 of the 10 bit memory address is 1, the RamIndex field must be set with the two highest bits of this address (shifting right by 8 positions). The lower 8 bits are directly used in the next SPI access, which writes this data.

To reduce the overhead caused by writing the RamIndex field for each memory access, it is recommended that an RamIndex shadow variable be maintained in software. This variable can be used to back up the last value of the RamIndex field. If address locations in the same segment are accessed sequentially, write operations to the RamIndex field can be eliminated by comparing the RamIndex value with the shadow variable.

8 MACFrame and Baseband RAM Configuration (Draft)

The nanoLOC chip provides settings for configuring the MACFrame in either Auto mode or Transparent mode. In Auto mode, the chip is responsible for processing MACFrame settings, such as addressing, etc., while in Transparent mode, software is responsible for processing MACFrame settings and the MACFrame data is “transparent” to the chip.

Related to MACFrame configuration is the Baseband RAM configuration. The nanoLOC chip provides settings for configuring the baseband RAM in either simplex or duplex mode. In simplex mode, a single data buffer is used for packets to be transmitted as well as for received packets, while in duplex mode, two buffers are used with one for packets to be transmitted and one for received packets.

These two configuration settings can be combined into four possible combinations:

- Auto MACFRame mode/simplex baseband RAM mode
- Auto MACFRame mode/duplex baseband RAM mode
- Transparent MACFrame mode/simplex baseband RAM mode
- Transparent MACFrame mode/duplex baseband RAM mode

8.1 MACFrame Configuration

A transmitted or received packet contains a Preamble, a SyncWord, the MACFrame, and a Tail. The Preamble, the SyncWord, and the Tail are used by the chip to help process the received packet, as shown below.

Figure 28: nanoLOC packet

The MACFrame, however, contains the raw data which will be used by upper layers, including the MAC layer, as shown below.

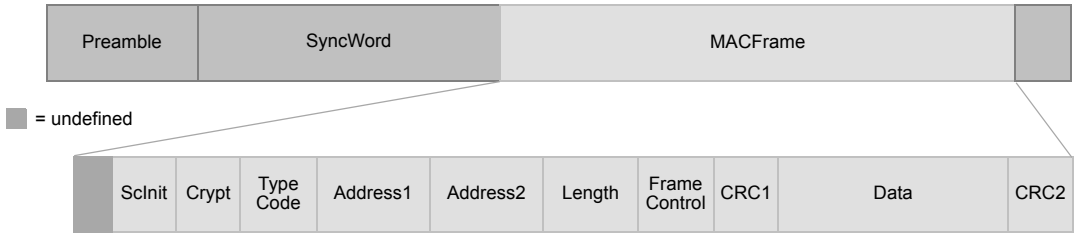


Figure 29: MACFrame contents

The nanoLOC chip provides the option of automatically processing the MACFrame in the chip (Auto mode) or sending the entire MACFrame up to software to permit software to process the MACFrame (Transparent mode).

8.1.1 MACFrame Auto Mode

In Auto mode, the upper half of the Baseband RAM (two segments totalling 256 bytes) is used for data, as either a TX or a RX buffer. The other two segments totalling 256 bytes are reserved for :

- MAC frame header data
- Station addresses

- Encryption keys and related control values
- Real Time Clock snapshots

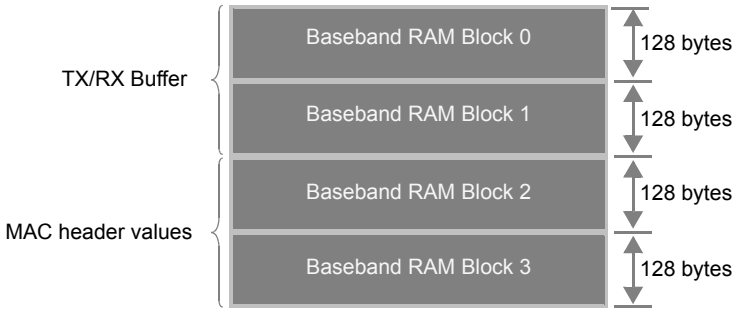


Figure 30: Baseband RAM in Auto mode

In Auto mode for TX, the digital part of the chip builds the MAC header for the MACFrame using values stored in chip buffers and registers and adds the data stored in a specific chip buffer. The Preamble, SyncWord and Tail are added and the packet is transmitted.

In Auto mode for RX, the MACFrame is extracted from the packet and the data is stored in specific buffers, while the MAC header is stored in other memory locations for further processing.

To set Auto mode for the MACFrame, do the following:

- Set TxRxBbBufferMode0 = NA_TxRxBufferMode0Auto_BC_C (0x0)

8.1.2 MACFrame Transparent Mode

In this mode, the complete Baseband RAM (all four segments totalling 512 bytes) is used for data, as either a TX or a RX buffer.

• Default Value = 0x0

Note: Buffer size and configuration depend on the combination of TxRxBbBufferMode0 and TxRxBbBufferMode1.

• NA_TxRxBufferMode0Transparent_BC_C (0x1)

8.2 Baseband RAM Modes

The baseband can be configured in two different modes:

- Auto Mode
- Transparent Mode

These two modes are selectable by using the register `TxRxMode` (0x39).**Auto Mode**

Transparent Mode

If the baseband is configured in Transparent mode, the complete MACframe has to be built by software. The hardware handles the complete MACframe as data, which also means that, for example, no addresses or CRCs are calculated or checked. The complete received frame (RX) is stored to one buffer, or the complete frame to be transmitted (TX) is taken from one buffer.

With this mode, it is possible to build other MACframe formats.

8.3 Buffer Configuration

There are four buffer configuration modes for BBRAM:

- Auto/Duplex
- Auto/Simplex
- Transparent/Duplex
- Transparent/Simplex

These four modes are selectable using the following registers:

- `TxRxBbBufferMode0` – for Auto or Transparent mode .
- `TxRxBbBufferMode1` – for Duplex or Simplex mode.

Note: The configuration of the baseband determines which of these four modes are usable.

Warning: Be aware that Auto mode and Transparent mode for the buffer is different than Auto mode and Transparent mode for the baseband.

8.3.1 TxRxBbBufferMode0 – Auto or Transparent

The register `TxRxBbBufferMode0` determines use of BBRAM, as follows:

- Only the upper half of BBRAM is used to store received data or to provide data to be transmitted. In this case, `TxRxBbBufferMode0 = Auto`.
- The entire BBRAM is used to store received data and to provide data to be transmitted. In this case, `TxRxBbBufferMode0 = Transparent`.

When baseband is configured as Auto mode, baseband stores MACframe information from a received packet, such as addresses, or it provides MACframe information, such as addresses, to build a packet for a transmission. As the memory locations for addresses are placed in the lower half of the BBRAM in Auto mode, only half of the BBRAM can be used for data. Consequently, the buffer must also be configured as Auto mode.

When baseband is configured as Transparent mode, the complete MACframe is handled as data. In this mode, no memory is needed to store or get header information. In this case, the user determines how much of the BBRAM should be used to store data. Consequently, when the baseband is configured as Transparent mode, the buffer can be configured as either Auto mode or Transparent mode.

8.3.2 TxRxBbBufferMode1 – Duplex or Simplex

The register `TxRxBbBufferMode1` determines the configuration of buffers, as follows:

- Separate buffers are provided for receive and transmit data.
  In this case, set `TxRxBbBufferMode1 = Duplex`.
- One buffer is used for both receive and transmit data.
  In this case, set `TxRxBbBufferMode1 = Simplex`.

This configuration can be used independent of the baseband mode.

8.3.3 Explanation of Buffer Settings

Auto/Duplex

- Only half of the BBRAM is used for data (256 bytes in total)
- Separate data buffers for RX and TX (128 bytes each)
- RX data buffer consists of two blocks (64 bytes each), where:
  - Start address of lower block for RX = `RamRxBuffer_0`
  - Start address of upper block for RX = `RamRxBuffer_0 + 0x040`
  - Start address of lower block for TX = `RamTxBuffer_0`
  - Start address for upper block for TX = `RamTxBuffer_0 + 0x040`
- TX data buffer consists of two blocks (64 bytes each), where:
  - Start address of lower block for TX = `RamTxBuffer_0`
  - Start address for upper block for TX = `RamTxBuffer_0 + 0x040`

The memory map of Auto/Duplex buffer configuration is shown in the following figure.

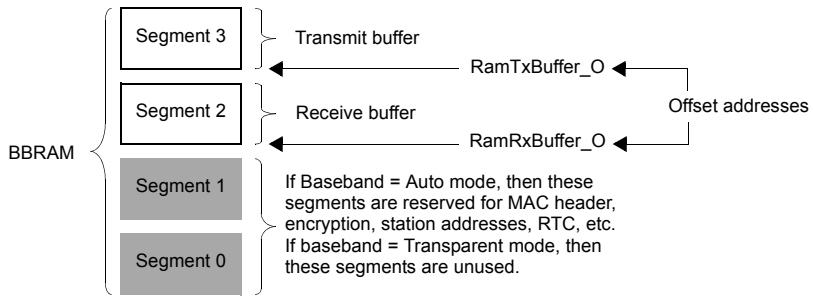


Figure 31: Auto/Duplex buffer configuration

Auto/Simplex

- Only half of the BBRAM is used for data (256 bytes in total)
- Only one data buffer for RX and TX (256 bytes in total)
- Data buffer consists of two blocks (128 bytes each), where:
  - Start address of lower block for RX and TX = `RamTxRxBuffer_0`
  - Start address of upper block for RX and TX = `RamTxRxBuffer_0 + 0x100`

The memory map of Auto/Simplex buffer configuration is shown in the following figure.

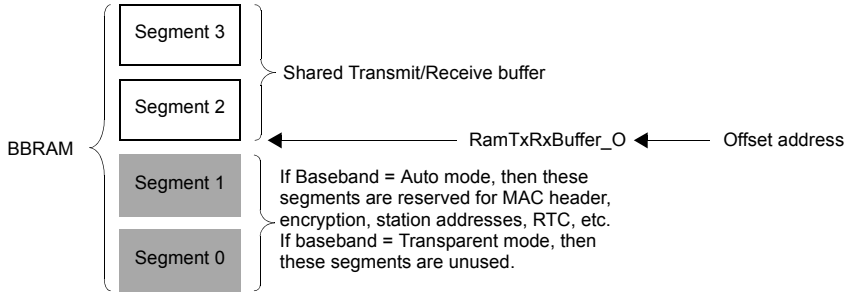


Figure 32: Auto/Simplex buffer configuration

Transparent/Duplex

- Complete BBRAM is used for data (512 bytes in total)
- Separate buffers for RX and TX (256 bytes each)
- RX data buffer consists of two blocks (128 bytes each), where:
  - Start address of lower block for RX = `RamRxTransBuffer_0`
  - Start address of upper block for RX = `RamRxTransBuffer_0 + 0x100`
- TX data buffer consists of two blocks (128 bytes each), where:
  - Start address of lower block for TX = `RamTxTransBuffer_0`
  - Start address of upper block for TX = `RamTxTransBuffer_0 + 0x100`

The memory map of Auto/Simplex buffer configuration is shown in the following figure.

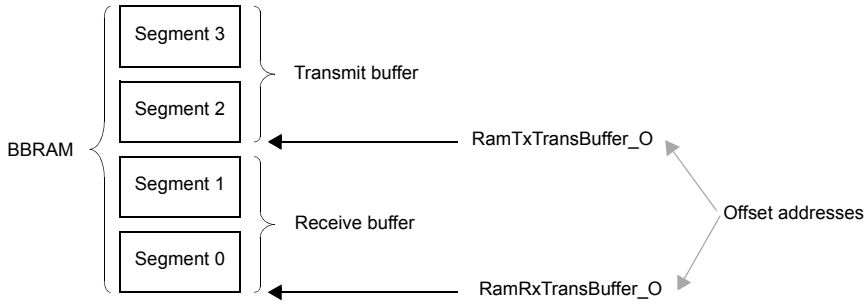


Figure 33: Transparent/Duplex buffer configuration

Transparent/Simplex

- Complete BBRAM is used for data (512 bytes in total)
- Only one data buffer for RX and TX (512 bytes in total)
- Data buffer consists of two blocks (256 bytes each) where,
  - Start address of lower half of the lower block for RX and TX = `RamTxRxTransBuffer_0`
  - Start address of upper half of the lower block for RX and TX = `RamTxRxTransBuffer_0 + 0x100`

- Start address of lower half of the upper block for RX and TX
  = `RamTxRxTransBuffer_0 + 0x200`
- Start address of upper half of the upper block for RX and TX
  = `RamTxRxTransBuffer_0 + 0x300`

Warning: It is important to be aware that each of the two blocks are spread over two segments.

The memory map of Auto/Simplex buffer configuration is shown in the following figure.

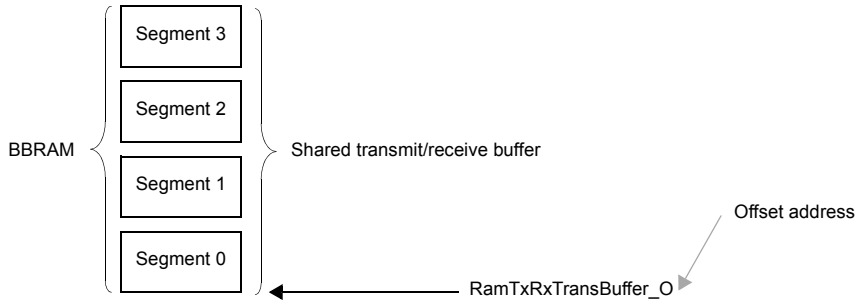


Figure 34: Transparent/Duplex buffer configuration

8.4 Buffer Access Synchronization

To avoid underrun or overflow exceptions of ready to be transmitted data or received data, the delivery or consumption of data by an external microcontroller must be synchronized to the transmit or receive data rate. Consequently, each transmit and receive buffer is divided into two parts of equal length – an upper part and a lower part. Additionally, each buffer has a flag and a command to control the data traffic to and from the buffers. The size of the buffer depends on the selected Buffer Configuration mode. An example buffer is illustrated below:

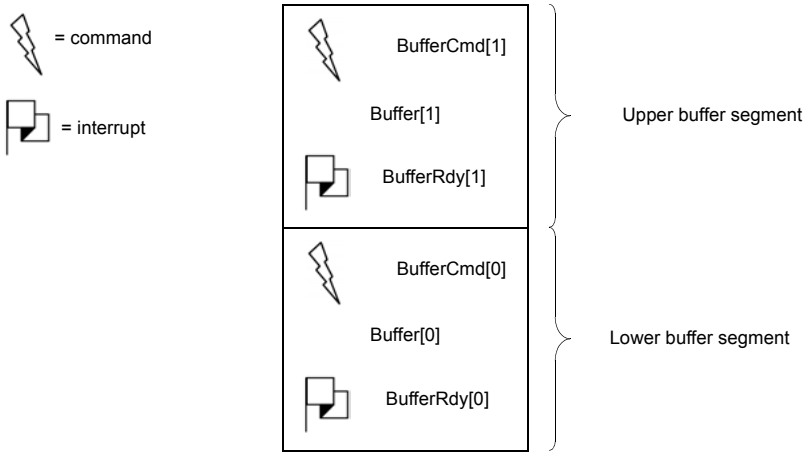


Figure 35: Example buffer showing upper and lower parts with flags and commands

8.5 Flags and Commands for Buffer Access Synchronization

A flag-command pair is provided for each buffer segment (lower and upper) and for each direction (transmit and receive).

8.5.1 Flags

Flags indicate to the software that buffers are ready for a data transfer and are not accessed by the transceiver baseband. Usually flags are enabled as interrupts so that the software can react to a triggered flag as quickly as possible.

Receive Flags

Table 28: Receive Flags

Flag	Description
RxBufferRdy[0]	Indicates to the software that RxBuffer[0] (lower segment) has been filled up with data by a receive operation.
RxBufferRdy[1]	Indicates to the software that RxBuffer[1] (upper segment) has been filled up with data by a receive operation.
RxOverflow	Indicates to the software that a buffer part has been accessed by the receiver, but was not ready to store data (which means that a receive buffer command was not issued in time).

Transmit Flags

Table 29: Receive Flags

Flag	Description
TxBufferRdy[0]	Indicates to the software that TxBuffer[0] (lower segment) has been emptied by a transmit operation and is ready to store new data.
TxBufferRdy[1]	Indicates to the software that TxBuffer[1] (upper segment) has been emptied by a transmit operation and is ready to store new data.
TxUnderrun	Flag which indicates to the software that a buffer part has been accessed by the transmitter but was not ready for transmission (means that a transmit buffer command was not issued in time).

8.5.2 Commands

Commands are issued after a data transaction and indicate to the transceiver baseband that data are ready for transmission or buffers are ready to store received data.

Receive Commands

Table 30: Receive Commands

Command	Description
RxBufferCmd[0]	Indicates to the transceiver that RxBuffer[0] (lower segment) has been emptied and the buffer is now ready to store data of a receive operation.
RxBufferCmd[1]	Indicates to the transceiver that RxBuffer[1] (upper segment) has been emptied and the buffer is now ready to store data of a receive operation.

Transmit Commands

Table 31: Receive Commands

Command	Description
TxBufferCmd[0]	Indicates to the transceiver that TxBuffer[0] (lower segment) has been filled up and data is now ready for transmission.
TxBufferCmd[1]	Indicates to the transceiver that TxBuffer[1] (upper segment) has been filled up and data is now ready for transmission.

The following diagram shows the flags and commands for buffer access synchronization.

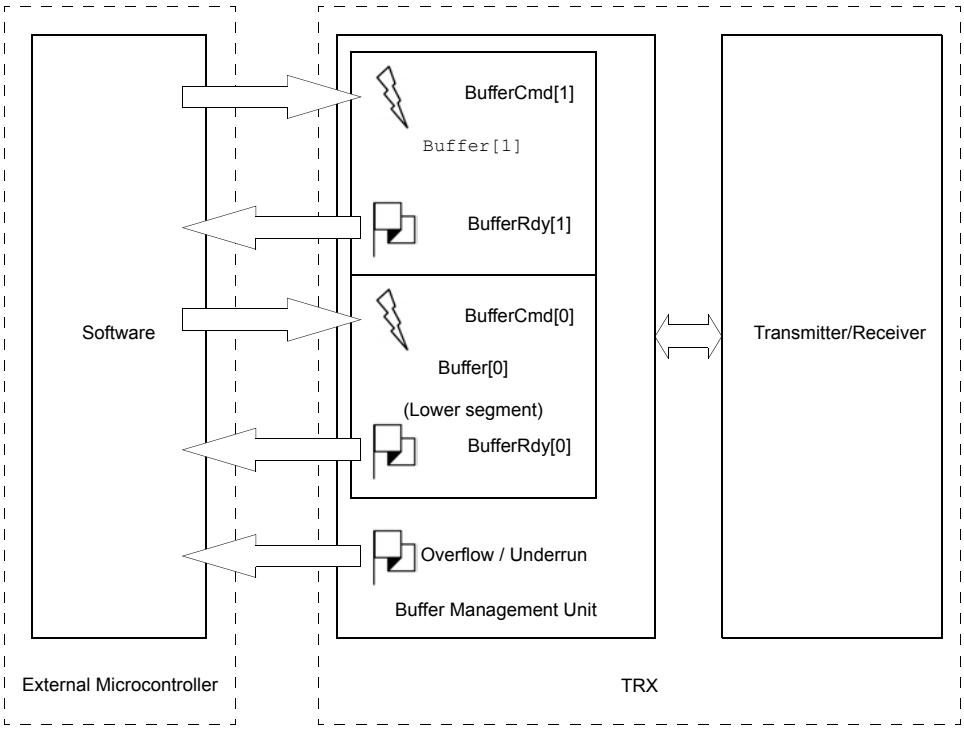


Figure 36: Flags and commands for buffer access synchronization

Note: Flags and commands are always related to their buffer segments, independent of buffer size. Also, transmit buffer overflows are severe software errors and are not implemented.

8.6 Transmit Buffer Control Timing

Before a packet is transmitted, the external microcontroller software can fill up both transmit buffer segments. After each data transaction, the corresponding buffer command is issued. The software then initiates the transmission of a packet. Data for transmission is taken from the transmit buffers, but always beginning with the lower buffer segment (`Buffer[0]`). The buffer ready flag indicates that a buffer segment has been emptied and the software can fill it up again. When the number of MACFrame (payload) data bytes is not an integer number of the buffer segment size, the buffer ready flag is also triggered when the last byte of the frame has been taken from a buffer segment. In this case, it is not required to fill this buffer part up completely, but it is mandatory to issue the buffer command.

A typical transmit buffer control timing is illustrated below.

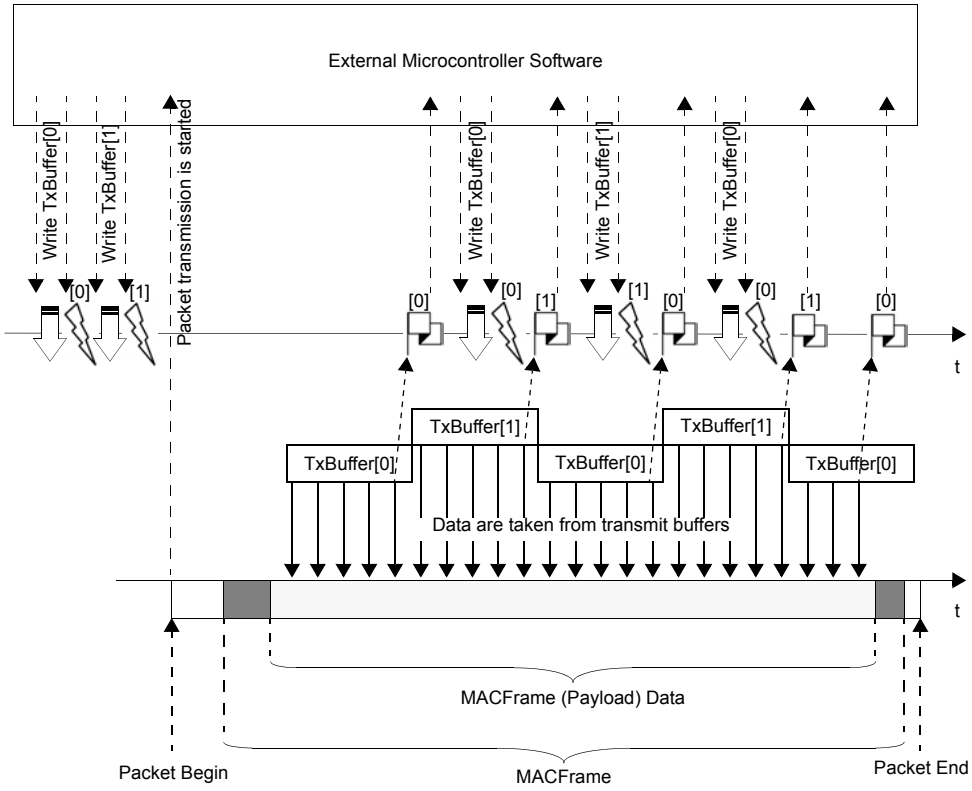


Figure 37: Transmit timing

A transmit underrun exception occurs (`TxUnderrun`) when the transmitter tries to read out a buffer segment that was not indicated as filled up. The transmit operation runs out of data and cannot be completed properly. The flag informs the software, which usually treats the exception in its protocol stack.

8.7 Receive Buffer Control Timing

Before a packet can be received, software starts the reception of a packet. If the receiver detects a packet, the MACFrame (payload) data is stored in the receive buffer segment, but always beginning with the lower buffer segment (`Buffer[0]`). When the receiver has filled up a buffer segment, the corresponding buffer ready flag is triggered. The software can now empty the corresponding receive buffer, which was indicated by the flag. When the last byte has been read from a receive buffer segment, the software issues the receive buffer ready command to indicate to the receiver that the buffer part has been cleared. If the number of MACFrame (payload) data bytes is not an integer number of the buffer part size, the buffer ready flag is also triggered when the last byte of the frame has been stored in a buffer part. In this case, it is not required to read out this buffer segment completely, but it is mandatory to issue the buffer command.

A typical receive buffer control timing is illustrated on the next page.

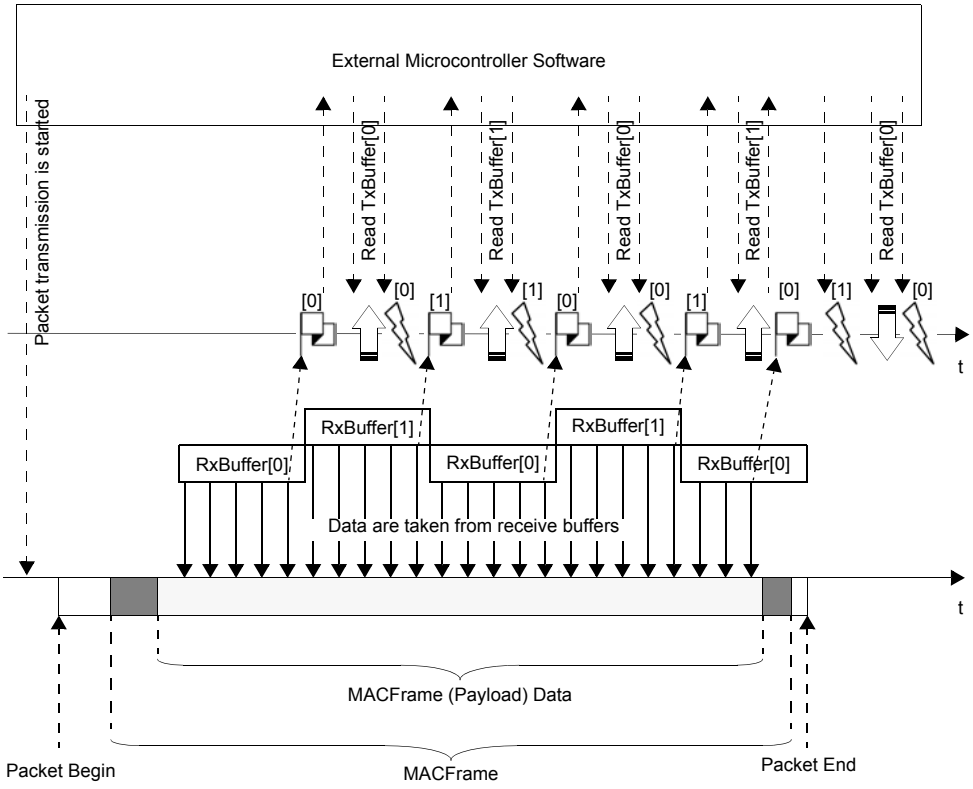


Figure 38: Receive timing

A receive overflow exception occurs (`RxOverflow`) when the receiver tries to store a byte in a buffer part that was not indicated as cleared. The receive operation causes a data overflow and cannot be completed properly. The flag informs the software, which usually treats the exception in its protocol stack.

8.8 Buffer Swapping

The buffer swap feature significantly eliminates overhead of data transactions over the SPI interface and improves the decoupling between transmit or receive processes and data transactions.

Overhead of data transactions over the SPI interface occur when a transceiver forwards the MACFrame (payload) data (sends received data to a next transceiver) and does not consume the data. The data has to be transported twice over the SPI interface and buffered in an external microcontroller, thus consuming time and electrical energy. In this case the swap feature eliminates SPI interface transactions for the data of short MACFrames (in Auto baseband mode when the payload size is less or equal 128 bytes – or in Transparent baseband mode when the number of transparent bytes is less or equal 256 bytes). In addition, this feature can be used if two short MACFrames have to be transmitted or received in a close sequence with a short time gap and the external microcontroller is not able to deliver or consume data in the short time gap between two frames.

The register `TxRxBbBufferSwp` exchanges simply the buffers between the baseband transmitter and receiver. If `TxRxBbBufferSwp = True_BC`, the data for a transmit operation are taken from the receive buffer and the data of a receive operation are stored in the transmit buffer. If `TxRxBbBufferSwp = False_BC`, the data in the buffers belong to their intended direction (default state). This feature works in both Duplex Buffer Configuration Modes: Auto and Transparent.

The figure below illustrates the effect of the register `TxRxBbBufferSwp` in both modes.

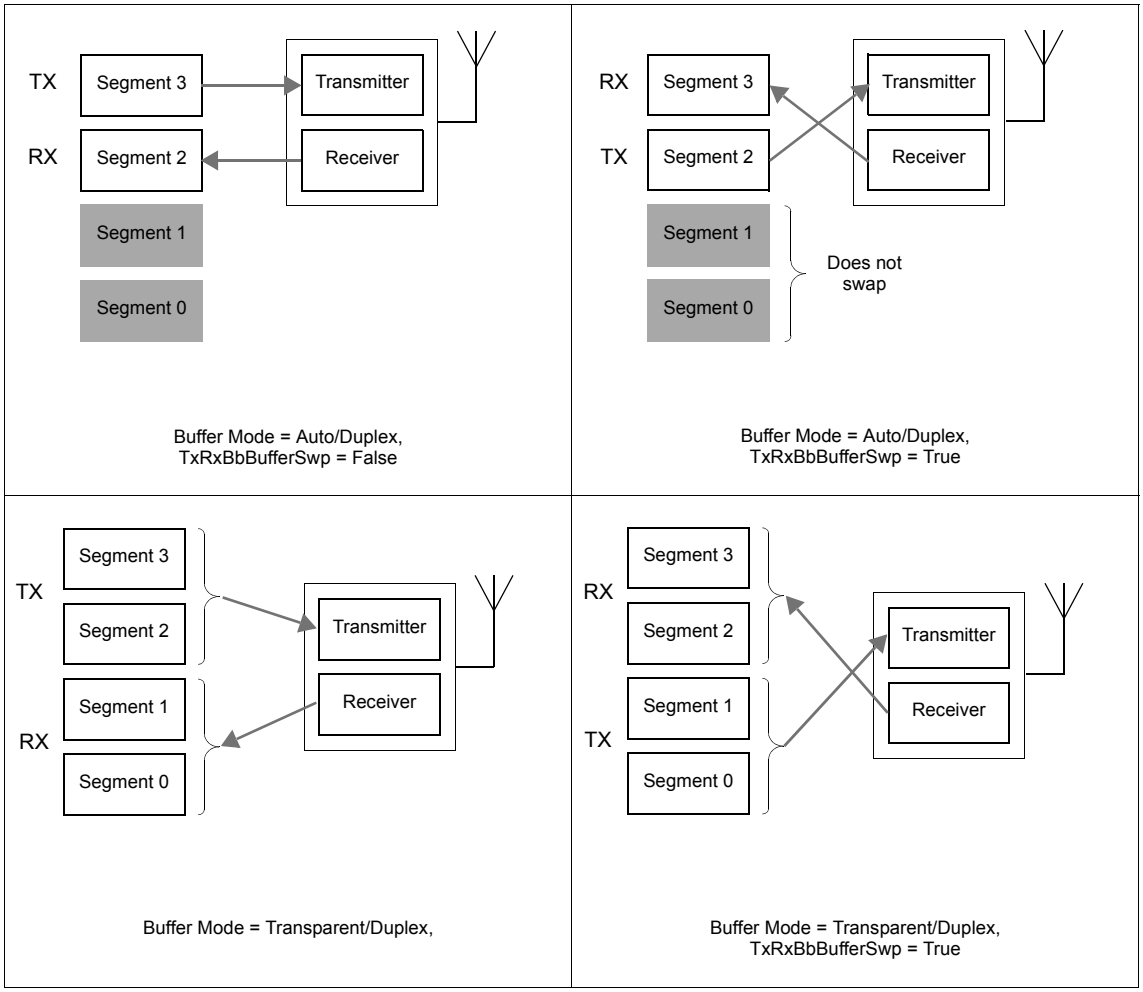


Figure 39: Exchange of buffers in the two different Duplex modes

When frames are to be forwarded, the value of the `TxRxBbBufferSwp` register has to be inverted after a reception but before the next (forwarding) transmission of the MACFrame's (payload) data. It eliminates three operations – reading out the data from the receive buffer, storing it in the external microcontroller, and writing it back in the transmit buffer.

When frames have to be transmitted or received in close sequences, the value of the `TxRxBbBufferSwp` register has to be inverted between the two frames in sequence. Data for both frames can be written to memory before the first one is transmitted or two frames can be received completely before the data of both is read out.

Note: This feature can be used in the Duplex Buffer Configuration modes and only if the payload size is 128 Bytes in Auto baseband mode or if the transparent frame size is 256 Bytes in Transparent baseband mode.

9 Memory Map of Chip Registers 0x00 – 0x7F

Note: Dark Grey Fields: Reserved Fields; Light Grey Fields: Internal Use Only

Table 32: nanoLOC TRX (NA5TR1) Registers 0x00 - 0x7F Memory Map

		MSB				Bit Number			LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x00	R					Irq Driver	Irq Polarity	SpiTx Driver	SpiBit Order
	W					Irq Driver	Irq Polarity	SpiTx Driver	SpiBit Order
0x01	R	Version							
	W	WakeUpTimeByte							
0x02	R	Revision							
	W					WakeUpTimeWe			
0x03	R	Batt Mgmt Enable			Batt Mgmt Threshold				Batt Mgmt Compare
	W	Batt Mgmt Enable			Batt Mgmt Threshold				
0x04	R					DioInValueAlarmStatus			
	W			Dio Use Pulldown	Dio Use Pullup	Dio Alarm Polarity	Dio Alarm Start	DioOut Value Alarm Enable	Dio Direction
0x05	R								
	W					DioPortWe			
0x06	R	Power Down Mode	PowerUpTime					Enable Wake UpDio	Enable Wake UpRtc
	W	Power Down Mode	PowerUpTime					Enable Wake UpDio	Enable Wake UpRtc
0x07	R						Reset BbRadio Ctrl	Reset BbClock Gate	
	W	Internal Use Only	Internal Use Only				Reset BbRadio Ctrl	Reset BbClock Gate	Power Down
0x08	R	Enable Feature Clock	FeatureClockFreq				Bypass BbCrystal	Enable BbClock	Enable BbCrystal
	W	Enable Feature Clock	FeatureClockFreq				Bypass BbCrystal	Enable BbClock	Enable BbCrystal

Table 32: nanoLOC TRX (NA5TR1) Registers 0x00 - 0x7F Memory Map (Continued)

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x09	R								
	W	Use Pulldown 4Spitxd	Use Pullup 4Spitxd	Use Pulldown 4Spirxd	Use Pullup 4Spirxd	Use Pulldown 4Spissn	Use Pullup 4Spissn	Use Pulldown 4Spiclk	Use Pullup 4Spiclk
0x0A	R								
	W	Use Pulldown 4Ucrst	Use Pullup 4Ucrst	Use Pulldown 4Ucirq	Use Pullup 4Ucirq	Use Pulldown 4Pamp	Use Pullup 4Pamp	Use Pulldown 4Por	Use Pullup 4Por
0x0B	R								
	W							Write Pulls 4Pads	Write Pulls 4Spi
0x0C	R					Internal Use Only			
	W					Internal Use Only			
0x0D	R					Internal Use Only			
	W					Internal Use Only			
0x0E	R			DeviceSelect				RamIndex	
	W			DeviceSelect				RamIndex	
0x0F	R	LoIrq Status	BbTimer IrqStatus	RxIrq Status	TxIrq Status	LoIrq Enable	BbTimer IrqEnable	RxIrq Enable	TxIrq Enable
	W					LoIrq Enable	BbTimer IrqEnable	RxIrq Enable	TxIrq Enable
0x10	R			TxIntsRawStat					
	W			TxIntsReset					
0x11	R		RxIntsRawStat						
	W		RxIntsReset						
0x12	R							LoInts RawStat	Internal Use Only
	W	Clear Base band TimerInt						LoInts Reset	Internal Use Only
0x13	R								
	W			TxIntsEn					
0x14	R								
	W		RxIntsEn						
0x15	R								
	W							LoIntsEn	Internal Use Only

Table 32: nanoLOC TRX (NA5TR1) Registers 0x00 - 0x7F Memory Map (Continued)

		MSB				Bit Number			LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x16	R	LoRxCapsValue							
	W	LoRxCapsValue							
0x17	R	LoRxCapsValue							
	W	LoRxCapsValue							
0x18	R			LoRxCapsValue					
	W			LoRxCapsValue					
0x19	R	LoTxCapsValue							
	W	LoTxCapsValue							
0x1A	R	LoTxCapsValue							
	W	LoTxCapsValue							
0x1B	R			LoTxCapsValue					
	W			LoTxCapsValue					
0x1C	R								
	W	Use Lo RxCaps		Internal Use Only	Lo Enable Lsb Neg	LoFastTuningLevel			Lo Enable Fast Tuning
0x1D	R	LoTargetValue							
	W	LoTargetValue							
0x1E	R	LoTargetValue							
	W	LoTargetValue							
0x1F	R								
	W	AgcThresHold1							
0x20	R								
	W	AgcThresHold2							
0x21	R								
	W	Hold Agc InFrame Sync	HoldAgcInBitSync						
0x22	R								
	W	AgcNregLength		Internal Use Only					
0x23	R								
	W	AgcIntTime							
0x24	R								
	W					AgcIntTime			

Table 32: nanoLOC TRX (NA5TR1) Registers 0x00 - 0x7F Memory Map (Continued)

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x25	R								
	W	Internal Use Only	Internal Use Only	Internal Use Only					
0x26	R			AgcGain					
	W	Internal Use Only		AgcRssiThres					
0x27	R			FctPeriod					
	W	EnableTx		StartFct-Measure	Fct-ClockEn	ChirpFilterCaps			
0x28	R								
	W	BasebandTimerStartValue							
0x29	R								
	W	BasebandTimerStartValue							
0x2A	R	Internal Use Only							
	W	SyncWord							
0x2B	R	Internal Use Only			Internal Use Only				
	W	SyncWord							
0x2C	R	Internal Use Only							
	W	SyncWord							
0x2D	R	Internal Use Only							
	W	SyncWord							
0x2E	R		Internal Use Only				Internal Use Only		
	W	SyncWord							
0x2F	R	Internal Use Only							
	W	SyncWord							
0x30	R	Internal Use Only			Internal Use Only				
	W	SyncWord							
0x31	R	RxCrc2 Stat	RxCrc1 Stat	RxAddrMatch		RxPacketType			
	W	SyncWord							
0x32	R					RxCorrBitErr			
	W	RxCorrErrThres							
0x33	R	RxCrypt SeqN	RxCryptId		RxCrypt En			RxAddr Seg IsMatch	RxAddr Seg EsMatch
	W	TxTimeSlotStart							

Table 32: nanoLOC TRX (NA5TR1) Registers 0x00 - 0x7F Memory Map (Continued)

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x34	R	RxFec1BitErr							
	W	TxTimeSlotStart							
0x35	R		RxFec1BitErr						
	W	TxTimeSlotEnd							
0x36	R								
	W	TxTimeSlotEnd							
0x37	R								
	W							RxTime Slot Control	TxTime Slot Control
0x38	R	RxPacketSlot							
	W	RxTimeSlotStart							
0x39	R	RxPacketSlot							
	W	RxTimeSlotStart							
0x3A	R								
	W	RxTimeSlotEnd							
0x3B	R								
	W	RxTimeSlotEnd							
0x3C	R					TxArqCnt			
	W	TxArqMax							
0x3D	R								
	W	Internal Use Only	Csq UseRam	Csq Mem AddrInit	Csq AsyMode	Csq Use 4Phases	CsqUse Phase Shift	CsqDitherValue	
0x3E	R								
	W	Internal Use Only	Internal Use Only	Internal Use Only					
0x3F	R								
	W	D3lUp DownEx				D3lPomLen		D3lPom En	D3lFixn Map
0x40	R								
	W	UseMap Thresh1 InFrame sync	LeaveMapThresh1InBitsync						
0x41	R								
	W	Internal Use Only	Go2MapThresh1InBitsync						

Table 32: nanoLOC TRX (NA5TR1) Registers 0x00 - 0x7F Memory Map (Continued)

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x42	R								
	W	Internal Use Only	Internal Use Only	Internal Use Only	Enable ExtPA	Invert RxClock	Enable CsqClock	Enable LOdiv10	Enable LO
0x43	R								
	W		TxPaBias				LnaFreqAdjust		
0x44	R								
	W			TxOutputPower0					
0x45	R								
	W			TxOutputPower1					
0x46	R								
	W				RfRxCompValueI				
0x47	R								
	W				RfRxCompValueQ				
0x48	R								
	W	Modulation System	SymbolRate				SymbolDur		
0x49	R								
	W	TxRxCryptClkMode				TxRx CryptCrc2 Mode	Use Fec	Crc2Type	
0x4A	R								SwapBb Buffers
	W	TxRx Mode			Fdma Enable		TxRxBb Buffer Mode0	TxRxBb Buffer Mode1	SwapBb Buffers
0x4B	R								
	W		ChirpMatrix1				ChirpMatrix0		
0x4C	R								
	W		ChirpMatrix3				ChirpMatrix2		
0x4D	R								
	W	TxMac CifsDis			TxUnder runIgnore	TxPreTrailMatrix1		TxPreTrailMatrix0	
0x4E	R								
	W	TxFrag Prio	TxBack OffAlg	Tx3Way	TxArq	TxVCarr SensAck	TxPhCarrSenseMode		TxVCarr Sens
0x4F	R								
	W	TxBackOffSeed							

Table 32: nanoLOC TRX (NA5TR1) Registers 0x00 - 0x7F Memory Map (Continued)

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x50	R								
	W	TxCrypt SeqN	TxCryptId		TxCrypt En	TxCryptSeqReset			
0x51	R								
	W	TxScramb En	TxScrambInit						
0x52	R								
	W	TxTransBytes							
0x53	R								
	W				TxTransBytes				
0x54	R								
	W	TxAddr Slct				TxPacketType			
0x55	R								
	W					TxBufferCmd		TxCmd Start	TxCmd Stop
0x56	R								
	W					RxBufferCmd		RxCmd-Start	RxCmd-Stop
0x57	R								
	W					RxCryptSeqReset			
0x58	R								
	W	RxTransBytes							
0x59	R								
	W				RxTransBytes				
0x5A	R								
	W	RxAddrSegDevIdL		RxAddr Seg IsMode	RxAddr Seg EsMode	RxArqMode		RxCrc2 Mode	RxTimeB Crc1 Mode
0x5B	R								
	W	RangingPulses				Rx Addr Mode	Rx TimeBEn	Rx Brdcast En	RxDataEn
0x5C	R								
	W				PulseDetDelay				
0x5D	R								
	W			Up Pulse DetectDis	Down Pulse DetectDis		GateAdjThreshold		

Table 32: nanoLOC TRX (NA5TR1) Registers 0x00 - 0x7F Memory Map (Continued)

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x5E	R								
	W	GateAdj Frame syncEn	GateAdj BitsyncEn	GateSizeFramesync		GateSizeBitsync		GateSizeUnsync	
0x5F	R								
	W		LeaveBitsyncThreshold				Go2BitsyncThreshold		
0x60	R								
	W	RtcTimeBTxAdj							
0x61	R								
	W	RtcTimeBRxAdj							
0x62	R								
	W	Internal Use Only			Rtc TimeB AutoMode			Rtc CmdRd	RtcCmdWr
0x63	R								
	W				AgcAmplitude				
0x64	R								
	W	UseAlter nativeAgc				AgcRangeOffset			
0x65	R								
	W								
0x66	R								
	W								
0x67	R								
	W								
0x68	R								
	W								
0x69	R								
	W								
0x6A	R								
	W								
0x6B	R								
	W								
0x6C	R								
	W								

Table 32: nanoLOC TRX (NA5TR1) Registers 0x00 - 0x7F Memory Map (Continued)

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x6D	R								
	W								
0x6E	R								
	W								
0x6F	R								
	W								
0x70	R								
	W								
0x71	R								
	W								
0x72	R								
	W								
0x73									
	W								
0x74	R								
	W								
0x75	R								
	W								
0x76	R								
	W								
0x77	R								
	W								
0x78	R								
	W								
0x79	R								
	W								
0x7A	R								
	W								
0x7B	R								
	W								
0x7C	R								
	W								

Table 32: nanoLOC TRX (NA5TR1) Registers 0x00 - 0x7F Memory Map (Continued)

		MSB				Bit Number			LSB
Offset	**R/W**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x7D	R					Internal Use Only	Internal Use Only		Internal Use Only
	W	Internal Use Only	Internal Use Only	Internal Use Only	Internal Use Only				Internal Use Only
0x7E	R	Internal Use Only				Internal Use Only			
	W								
0x7F	R	Internal Use Only		Internal Use Only	Internal Use Only	Internal Use Only			
	W								

10 Chip Registers Description: 0x00 to 0x7F

10.1 0x00 – SPI Bit Order and IRQ Pad Configuration

Used for defining the bit order for SPI and for configuring the SPI TX and IRQ pads..

		MSB				Bit Number			LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x00	R/W					Irq Driver	Irq Polarity	SpiTx Driver	SpiBit Order
	init	0	0	0	0	0	0	0	0

Read/Write

Field Properties for Register 0x00

Bits	Mnemonic	Prop	Description
0	SpiBitOrder	R/W brst SPI	Select MSB or LSB Bit Order for SPI *Purpose:* Defines the bit order of the SPI. However, the byte order always remains the same. More information is provided about the SPI Bit Order in the note below. *Register Values/Settings:* • NA_SpiBitOrderLsbFirst_C (0x0) The first bit transmitted over the interface data lines is the LSB, while the last bit is the MSB. Each byte is, therefore, transmitted with LSB first. • NA_SpiBitOrderMsbFirst_C (0x1) The first bit transmitted over the interface data lines is the MSB, while the last bit is the LSB. Each byte is, therefore, transmitted with MSB first. • Default Value = 0x0 *Note:* After PowerUpReset or after wakeup from PowerDownModeFull, the SPI is configured as LSB first.

Field Properties for Register 0x00 (Continued)

Bits	Mnemonic	Prop	Description
1	SpiTxDriver	R/W brst SPI	Select push-pull or open-drain for SPI TxD Output Driver *Purpose:* Switches between push-pull and open-drain for the TxD output driver. *Register Values/Settings:* • NA_SpiTxDriverOpenDrain_C (0x0) The TxD output driver is open-drain. The pad is driven only when a logic 0 is sent from nanoLOC to the SPI master. Otherwise, the output is in high-impedance state. • NA_SpiTxDriverPushPull_C (0x1) The TxD output driver is push-pull. The pad is driven only when data is sent from nanoLOC to the SPI master. Otherwise, the output is in high-impedance state. • Default Value = 0x0 *Note:* A pull-up is always required.
2	IrqPolarity	R/W brst SPI	Select High or Low Active for IRQ Polarity *Purpose:* Defines the polarity of the interrupt request signal. *Register Values/Settings:* • NA_IrqPolarityActiveLow_C (0x0) IRQ is low active. • NA_IrqPolarityActiveHigh_C (0x1) IRQ is high-active. • Default Value = 0x0
3	IrqDriver	R/W brst SPI	Select push-pull or open-drain for IRQ Driver *Purpose:* Switches between the push-pull and the open-drain driver for the IRQ output driver. *Register Values/Settings:* • NA_IrqDriverOpenDrain_C (0x0) The IRQ output driver is open-drain • NA_IrqDriverPushPull_C (0x1) The IRQ output driver is push-pull. • Default Value = 0x0

10.2 Configuring When Bit Order of nanoLOC is Unknown

Because only the lower half of the register is used, the configuration of the SPI transfer is always possible even when the bit order for the nanoLOC transceiver is unknown. This can be easily seen by, for instance, looking at the first two bytes (the Instruction and Address bytes) and at the one-byte write transfer to the address 0x00.

The Instruction and Address bytes are always 0x81 0x0. This means:

• 1st byte (Instruction field): write one byte

• 2nd byte (address field): select address 0

The same value is received when bit order is wrong – mirroring 0x81 leads to 0x81 as well. The same is true for the third byte of the transfer. For bits 0 to 3, mirror these bits to bits 7 to 4 (for example, 0 to 7; 1 to 6; 2 to 5; and 3 to 4). The following table provides four examples where it is possible to set the bit order of the registers and configure bits 1 to 3, even if the bit order already set in the chip is unknown.

Table 33: Configuring nanoLOC when bit order of chip is unknown

Configuring nanoLOC MSB First	Configuring nanoLOC LSB First	Configuration of Bits 1 to 3
0x81 0x0 0x81	0x81 0x0 0x0	SpiTxDriver = Open Drain IrqPolarity = Active Low IrqDriver = Open Drain
0x81 0x0 0xDB	0x81 0x0 0x5A	SpiTxDriver = Push Pull IrqPolarity = Active Low IrqDriver = Push Pull
0x81 0x0 0xE7	0x81 0x0 0x66	SpiTxDriver = Push Pull IrqPolarity = Active High IrqDriver = Open Drain
0x81 0x0 0x99	0x81 0x0 0x18	SpiTxDriver = Open Drain IrqPolarity = Active Low IrqDriver = Push Pull

10.3 0x01 – Digital Controller Version Number and Wake Up Time Byte

Used for reading the version number of the digital controller and for writing a wake-up time value of one byte, which is used with WakeUpTimeWe to program the wake-up time.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x01	R	Version							
	init	0	0	0	0	0	1	0	0
	W	WakeUpTimeByte							
	init	0	0	0	0	0	0	0	0

Read Only Fields

Field Properties for Register 0x01

Bits	Mnemonic	Prop	Description
0-7	Version	RO	Version Number of Digital Controller *Register Values/Settings:* • Default Value = 0x5

Write Only Fields

Field Properties for Register 0x01

Bits	Mnemonic	Prop	Description
0-7	WakeUpTimeByte	WO	RTC Wake-Up Time Byte *Purpose:* This field stores a one byte value for the wake-up time, which is programed to the wake-up time RtcWakeUpTime using WakeUpTimeWe. The complete programmed wake-up time is compared to the bits 31:8 of the Real Time Clock. The LSB of the programmed wake-up time corresponds to a 7812.5 µs cycle (bit 8 of the RTC). *Note:* RtcWakeUpTime can only be accessed through WakeUpTimeByte and WakeUpTimeWe. *Register Values/Settings:* • Default Value = 0x0

10.4 0x02 – Digital Controller Revision Number and Wake-Up Time

Used for reading the revision number of the digital controller and for writing the value of WakeUpTimeByte to the wake-up time circuitry.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x02	R	Revision							
	init	0	0	0	0	0	0	0	1
	W					WakeUpTimeWe			
	init	0	0	0	0	0	0	0	0

Read Only Fields

Field Properties for Register 0x02

Bits	Mnemonic	Prop	Description
0-7	Revision	RO	Revision Number of Digital Controller *Register Values/Settings:* • Default Value = 0x1

Write Only Fields

Field Properties for Register 0x02

Bits	Mnemonic	Prop	Description
1-3	WakeUpTimeWe	WO brst SPI	Wake-Up Time Byte Selector *Purpose:* Loads the value of RtcWakeUpTimeByte to the appropriate byte of the wake-up time in the wake-up time circuitry. *Register Values/Settings:* • Default Value = 0x0 *Note:* A 1-0 sequence must be written to this field before changing RtcWakeUpTimeByte.

10.5 0x03 – Battery Management

Used for enabling the voltage comparator function, for setting the voltage comparator value, and for reporting the voltage status of the battery.

Note: The battery management function is completely realized in the analog part of the chip.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x03	R	Batt Mgmt Enable			BattMgmtThreshold				Batt Mgmt Compare
	init		0	0					0
	W								
	init	0	0	0	0	0	0	0	0

Read/Write Fields

Field Properties for Register 0x03

Bits	Mnemonic	Prop	Description
1-4	BattMgmtThreshold	RW brst SPI	Battery Management Threshold *Purpose:* Sets battery comparator level. These bits set the comparison voltage. The chip checks if the compare value is higher or lower than the real battery voltage. *Register Values/Settings:* • Compare voltage Value • Default Value = 0x0 *Note:* The BattMgmtCompare bit indicates the result of the comparison.
7	BattMgmtEnable	RW brst SPI	Enable Battery Management *Purpose:* Enables the battery voltage comparator function. *Register Values/Settings:* • 0 = Disable • 1 = Enable • Default Value = 0x0 *Note:* Must be enabled before BattMgmtCompare can be read.

Read Only Fields

Field Properties for Register 0x03

Bits	Mnemonic	Prop	Description
0	BattMgmtCompare	RO	Battery Comparator Output *Purpose:* Reports if the battery voltage is above or below the value of BattMgmtThreshold. *Register Values/Settings:* • 0 = Below • 1 = Above • Default Value = 0x0 *Note:* The read value is valid only if the Battery Comparator is enabled, that is, when BattMgmtEnable = 1.

10.6 0x04 – Digital IO Controllers and Digital IO Alarm Status

The digital IO ports have several functions. These include a normal input where the signal level at these ports can be read, or a normal output where a programmable value is driven out of the chip.

Additionally, the digital IO ports can be used as an alarm input which reports the occurrence of an alarm event. This could be used to wake-up the chip. A clock (feature clock) could then be driven out of the chip.

When reading this register, each bit reports the signal level or the occurrence of an alarm at the corresponding digital IO port. When writing to this register, the values are just set inside this register. The values first influence one or more digital IO ports when a write strobe is generated for the desired digital IO port(s) via register 0x05 (see *0x05 – Write Enable Digital IO Port* on page 76). This causes the values in this register to be copied to the corresponding configuration registers of these digital IO ports.

		MSB				Bit Number			LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x04	R					DioInValueAlarmStatus			
	init	0	0	0	0	0	0	0	0
	W			Dio Use Pulldown	Dio Use Pullup	Dio Alarm Polarity	Dio Alarm Start	DioOut Value Alarm Enable	Dio Direction
	init	0	0	0	0	0	0	0	0

Read Only Fields

Field Properties for Register 0x04

Bits	Mnemonic	Prop	Description
0-3	DioInValueAlarmStatus	RO	Signal Level / Alarm Status *Purpose:* Each bit reports the signal level or the occurrence of an alarm at one of the four digital IO ports. *Register Values/Settings:* • Bit 0 belongs to DigIO 0 • Bit 1 belongs to DigIO 1 • Bit 2 belongs to DigIO 2 • Bit 3 belongs to DigIO 3 • Default Value = 0x0 *Note:* Interpreting the bits make sense only when the corresponding digital IO port is configured as an input, that is, when DioDirection = 0. When the digital IO port is used as a normal input, that is, when DioOutValueAlarmEnable = 0, then the read value is the signal level at that port. When the digital IO port is used to report the occurrence of an alarm, that is, when DioOutValueAlarmEnable = 1, then reading a 1 means that an alarm has occurred.

Write Only Fields

Field Properties for Register 0x04

Bits	Mnemonic	Prop	Description
0	DioDirection	WO brst SPI	Control Direction of Digital IO Port *Register Values/Settings:* • 0 = digital IO port is configured as an input • 1 = digital IO port is configured as an output • Default Value = 0x0
1	DioOutValueAlarmEnable	WO brst SPI	Enable Digital IO as Alarm Input / Value *Purpose:* When the digital IO port is configured as an input [DioDirection = 0], this bit selects whether the signal level at that port or the occurrence of an alarm should be reported when reading this field. When the digital IO port is configured as a normal output, that is, when DioDirection = 1 and DioAlarmPolarity = 0, then the value programmed in here is driven out of the port. *Register Values/Settings:* • 0 = Normal input / value to drive out of port • 1 = Enable alarm / value to drive out of port • Default Value = 0x0

Field Properties for Register 0x04 (Continued)

Bits	Mnemonic	Prop	Description
2	DioAlarmStart	WO brst SPI	Start Digital IO Alarm *Purpose:* This bit starts the alarm. It has to be set after the digital IO port is configured to report the occurrence of an alarm, that is, when DioDirection = 0, DioOutValueAlarmEnable = 1, and DioAlarmPolarity=0. *Register Values/Settings:* • 0 = False • 1 = True (start alarm) • Default Value = 0x0 *Note:* Program the same values to the other bits of this register as programmed for the configuration.
3	DioAlarmPolarity	WO brst SPI	Set Digital IO Alarm Polarity /Source to Drive Digital IO Port *Purpose:* When the digital IO port is configured as an input that should report the occurrence of an alarm, that is when DioDirection = 0 and DioOutValueAlarmEnable = 1, then this bit is used to select the edge which should trigger the alarm. When the digital IO port is configured as an output, that is, when DioDirection = 0, then this bit selects whether the value programmed in DioOutValueAlarmEnable or the feature clock should be driven out of the digital IO port. *Register Values/Settings:* • 1 = Triggers alarm on rising edge / drive feature clock • 0 = Triggers alarm on falling edge / drive value programmed in DioOutValueAlarmEnable • Default Value = 0x0

Field Properties for Register 0x04 (Continued)

Bits	Mnemonic	Prop	Description
4	DioUsePullup	WO brst SPI	Connect a Pull-Up Resistor to the Digital IO Pad *Purpose:* When this bit is set to 1, a pull-up resistor is connected to the corresponding digital IO pad. *Register Values/Settings:* • 0 = No pull-up resistor • 1 = Use pull-up resistor • Default Value = 0x0
5	DioUsePulldown	WO brst SPI	Connect a Pull-Down Resistor to the Digital IO Pad *Purpose:* When this bit is set to 1, a pull-down resistor is connected to the corresponding digital IO pad only, but when DioUsePullup = 0. *Register Values/Settings:* • 0 = No pull-down resistor • 1 = Use pull-down resistor • Default Value = 0x0

10.7 0x05 – Write Enable Digital IO Port

Used for generating a write strobe for the configuration registers of the digital IO ports by software. When the write strobe occurs for one digital IO port, the values programmed in the register 0x04 (see *0x04 – Digital IO Controllers and Digital IO Alarm Status* on page 72) are copied into the corresponding registers of that digital IO. When more than one digital IO port should be configured with the same values, the write strobe for these digital IO ports can be programmed in parallel.

Note: A write strobe must always be generated by programming a 1-0-sequence to this register. Do NOT change the content of register 0x04 when one of the bits of this register is active.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x05	R								
	init	0	0	0	0	0	0	0	0
	W					DioPortWe			
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x05

Bits	Mnemonic	Prop	Description
0-3	DioPortWe	WO brst SPI	Write Enable a Digital IO Port *Purpose:* Writes the settings of the following fields to the fields in the digital IO controller: • DioDirection • DioOutValueAlarmEnable • DioAlarmPolarity • DioAlarmStart • DioUsePullup • DioUsePulldown *Note:* A 1-0 sequence must be written to this field before changing register 0x04. Writing a 1-0 sequence to one (or more) bits of DioPortWe takes the value of 0x4 into the registers of the associated digital IO pin(s).

10.8 0x06 – Power Management

Used for selecting the type of power down mode, for configuring the power-up time, and for defining the event that brings the chip into the power-up state.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x06	R/W	Power Down Mode	PowerUpTime					Enable Wake UpDio	Enable Wake UpRtc
	init	0	0	0	0	0	0	0	0

Read/Write Fields

Field Properties for Register 0x06

Bits	Mnemonic	Prop	Description
0	EnableWakeUpRtc	RW brst SPI	Enable Real Time Clock as Wake-Up Source *Purpose:* The Real Time Clock wake-up event brings the chip into the power up state. *Register Values/Settings:* • 0 = Disable • 1 = Enable • Default Value = 0x0
1	EnableWakeUpDio	RW brst SPI	Enable DigIOs as Wake-Up Source *Purpose:* An alarm event (rising/falling edge) at one of the digital IOs configured as a wake-up source (see register 0x4) brings the chip into the power up state. *Register Values/Settings:* • 0 = Disable • 1 = Enable • Default Value = 0x0
4-6	PowerUpTime	RW brst SPI	Configure Power Up Time *Purpose:* Configures the duration of the power-up time (duration of active µCReset). *Register Values/Settings:* • PowerUpTime128Ticks_C (0x0) • PowerUpTime1Ticks_C (0x1) • PowerUpTime2Ticks_C (0x2) • PowerUpTime4Ticks_C (0x3) • PowerUpTime8Ticks_C (0x4) • PowerUpTime16Ticks_C (0x5) • PowerUpTime32Ticks_C (0x6) • PowerUpTime64Ticks_C (0x7) • Default Value = 0x0 *Note:* 1 tick = 1/4096 s.

Field Properties for Register 0x06 (Continued)

Bits	Mnemonic	Prop	Description
7	PowerDownMode	RW brst SPI	Select Power down Mode *Purpose:* Selects the power down mode into which the transceiver chip is brought when the chip enters the powered down state. *Register Values/Settings:* • NA_PowerDownModeFull_C (0x0) Pads and transceiver registers are powered off. Reconfiguration of the transceiver registers is required after wake-up, but the leakage current is the lowest possible in this mode. • NA_PowerDownModePad_C (0x1) All output pads are disabled and all bi-directional pads are switched to input, but all transceiver registers are still powered. Reconfiguration of the transceiver registers is not required, but leakage current is higher.

10.9 0x07 – Reset Digital Baseband/Baseband Clock and Power Down

Used for resetting the digital baseband and radio control circuitries, for resetting the baseband clock distribution circuitry, and for bringing the chip from the power-up state to the configured power-down state.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x07	R						Reset BbRadio Ctrl	Reset BbClock Gate	
	init	0	0	0	0	0			0
	W	Internal Use Only	Internal Use Only						Power Down
	init	0	0	0	0	0	1	1	0

Read/Write Fields

Field Properties for Register 0x07

Bits	Mnemonic	Prop	Description
1	ResetBbClockGate	RW brst SPI	Reset Clock Gates *Purpose:* Resets the baseband clock distribution circuitry. *Register Values/Settings:* • 0 = Inactive reset • 1 = Active reset • Default Value = 0x1
2	ResetBbRadioCtrl	RW brst SPI	Reset Transceiver *Purpose:* Resets the digital baseband and radio control circuitries supplied by the baseband clock. *Register Values/Settings:* • 0 = Inactive reset • 1 = Active reset • Default Value = 0x1 *Note:* The baseband clock must be started before the reset takes effect.

Write Only Fields

Field Properties for Register 0x07

Bits	Mnemonic	Prop.	Description
0	PowerDown	WO brst SPI	Bring Chip to Powered Down State *Purpose:* Setting this bit brings the chip to the configured power-down state. This bit will be automatically cleared when the chip is powered-up. *Register Values/Settings:* • 0 = Ignore • 1 = Go to power-down state • Default Value = 0x0

10.10 0x08 – Power On/Off Baseband Crystal and Clock

Used for enabling or bypassing the internal baseband crystal, for enabling the baseband clock distribution circuitry and the feature clock, as well as for setting the feature clock frequency.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x08	RW	Enable Feature Clock	FeatureClockFreq				Bypass Bb Crystal	Enable BbClock	Enable BbCrystal
	init	0	0	0	0	0	0	0	0

Read/Write Fields

Field Properties for Register 0x08

Bits	Mnemonic	Prop	Description
0	EnableBbCrystal	RW SPI	Enable Baseband Crystal *Purpose:* Powers on the internal baseband quartz oscillator. *Register Values/Settings:* • 0 = Power off • 1 = Power on • Default Value = 0x0 *Note:* Never switch on the internal oscillator when the external oscillator is present.
1	EnableBbClock	RW SPI	Enable Baseband Clock *Purpose:* Enable the baseband clock distribution. *Register Values/Settings:* • 0 = Distribution off • 1 = Distribution on • Default Value = 0x0
2	BypassBbCrystal	RW SPI	Bypass Baseband Crystal *Purpose:* Enables the external oscillator. *Register Values/Settings:* • 0 = Disable • 1 = Enable • Default Value = 0x0 *Note:* Never switch on the power of the internal oscillator when the external oscillator is present. *See also: 0x08 – Power On/Off Baseband Crystal and Clock* on page 81.

Field Properties for Register 0x08 (Continued)

Bits	Mnemonic	Prop	Description
4- 6	FeatureClockFreq	RW brst SPI	Feature Clock Frequency *Purpose:* Defines the feature clock frequency (feature clock is driven out of selected DigIo(s)). *Register Values/Settings:* • NA_FeatureClockDiv1_C (0x7) • NA_FeatureClockDiv2_C (0x6) • NA_FeatureClockDiv4_C (0x5) • NA_FeatureClockDiv8_C (0x4) • NA_FeatureClockDiv16_C (0x3) • NA_FeatureClockDiv32_C (0x2) • NA_FeatureClockDiv64_C (0x1) • NA_FeatureClockDiv128_C (0x0) • Default Value = 0x0 *Note:* Change the frequency only when the feature clock is disabled (EnableFeatureClock = 0) .
7	EnableFeatureClock	RW brst SPI	Enable Feature Clock *Purpose:* Enables the Feature Clock which guarantees clip and glitch free clock waveforms on a digital IO output. *Register Values/Settings:* • 0 = Disable If the Feature Clock is disabled but a digital IO pin is enabled as clock output, the frequency is equal to the Real Time Clock crystal frequency of 32.768 kHz. • 1 = Enable If enabled, the frequency depends on the value set in FeatureClockFreq.

10.11 0x09 – Setting SPI Pads as Pullup or Pulldown

Used for connect the pull-up or the pull-down resistors to the four SPI pads: Spiclk, Spissn, Spirxd, and Spitxd. The values programmed here are applied to the pad when they are written to the corresponding registers through register 0x0B (see *0x0B – Writing Pullup/Pulldown Settings to Pads* on page 87). The resistors are kept during power-down state.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x09	R								
	init	0	0	0	0	0	0	0	0
	W	Use Pulldown 4Spitxd	Use Pullup 4Spitxd	Use Pulldown 4Spirxd	Use Pullup 4Spirxd	Use Pulldown 4Spissn	Use Pullup 4Spissn	Use Pulldown 4Spiclk	Use Pullup 4Spiclk
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x09

Bits	Mnemonic	Prop	Description
0	UsePullup4Spiclk	WO brst SPI	Connect a Pull-Up Resistor to SPI Clock Pad *Purpose:* When this bit is set to 1, a pull-up resistor is connected to the SPI clock pad. *Register Values/Settings:* • 0 = No pull-up resistor • 1 = Use pull-up resistor • Default Value = 0x0
1	UsePulldown4Spiclk	WO brst SPI	Connect a Pull-Down Resistor to SPI Clock Pad *Purpose:* When this bit is set to 1, a pull-down resistor is connected to the SPI clock pad, but only when UsePullup4Spiclk is 0. *Register Values/Settings:* • 0 = No pull-down resistor • 1 = Use pull-down resistor • Default Value = 0x0
2	UsePullup4Spissn	WO brst SPI	Connect a Pull-Up Resistor to SPI Ssn Pad *Purpose:* When this bit is set to 1, a pull-up resistor is connected to the SPI Ssn pad. *Register Values/Settings:* • 0 = No pull-up resistor • 1 = Use pull-up resistor • Default Value = 0x0

Field Properties for Register 0x09 (Continued)

Bits	Mnemonic	Prop	Description
3	UsePulldown4Spissn	WO brst SPI	Connect a Pull-Down Resistor to SPI Ssn Pad *Purpose:* When this bit is set to 1, a pull-down resistor is connected to the SPI Ssn pad, but only when UsePullup4Spissn is 0. *Register Values/Settings:* • 0 = No pull-down resistor • 1 = Use pull-down resistor • Default Value = 0x0
4	UsePullup4Spirxd	WO brst SPI	Connect a Pull-Up Resistor to SPI RxD Pad *Purpose:* When this bit is set to 1, a resistor is connected to the SPI RxD Pad. *Register Values/Settings:* • 0 = No pull-up resistor • 1 = Use pull-up resistor • Default Value = 0x0
5	UsePulldown4Spirxd	WO brst SPI	Connect a Pull-Down Resistor to SPI RxD Pad *Purpose:* When this bit is set to 1, a pull-down resistor is connected to the SPI RxD pad, but only when UsePullup4Spirxd is 0. *Register Values/Settings:* • 0 = No pull-down resistor • 1 = Use pull-down resistor • Default Value = 0x0
6	UsePullup4Spitxd	WO brst SPI	Connect a Pull-Up Resistor to SPI TxD Pad *Purpose:* When this bit is set to 1, a resistor is connected to the SPI TxD Pad. *Register Values/Settings:* • 0 = No pull-up resistor • 1 = Use pull-up resistor • Default Value = 0x0
7	UsePulldown4Spitxd	WO brst SPI	Connect a Pull-Down Resistor to SPI TxD Pad *Purpose:* When this bit is set to 1, a pull-down resistor is connected to the SPI TxD pad, but only when UsePullup4Spitxd is 0. *Register Values/Settings:* • 0 = No pull-down resistor • 1 = Use pull-down resistor • Default Value = 0x0

10.12 0x0A – Setting Additional Pads as Pullup or Pulldown

Used for connecting the pull-up or the pull-down resistors to the four pads: PowerOnReset, Pamp, µCIrq, and µCReset. The values programmed here are applied to the pad when they are written to the corresponding registers through register 0x0B (see *0x0B – Writing Pullup/Pulldown Settings to Pads* on page 87). The resistors are kept during power-down state.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x0A	R								
	init	0	0	0	0	0	0	0	0
	W	Use Pulldown 4Ucrst	Use Pullup 4Ucrst	Use Pulldown 4Ucirq	Use Pullup 4Ucirq	Use Pulldown 4Pamp	Use Pullup 4Pamp	Use Pulldown 4Por	Use Pullup 4Por
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x0A

Bits	Mnemonic	Prop	Description
0	UsePullup4Por	WO brst SPI	Connect a Pull-Up Resistor to POR Pad *Purpose:* When this bit is set to 1, a pull-up resistor is connected to the POR pad. *Register Values/Settings:* • 0 = No pull-up resistor • 1 = Use pull-up resistor • Default Value = 0x0
1	UsePulldown4Por	WO brst SPI	Connect a Pull-Down Resistor to POR Pad *Purpose:* When this bit is set to 1, a pull-down resistor is connected to the POR pad, but only when UsePullup4Por is 0. *Register Values/Settings:* • 0 = No pull-down resistor • 1 = Use pull-down resistor • Default Value = 0x0
2	UsePullup4Pamp	WO brst SPI	Connect a Pull-Up Resistor to PAMP Pad *Purpose:* When this bit is set to 1, a pull-up resistor is connected to the PAMP pad. *Register Values/Settings:* • 0 = No pull-up resistor • 1 = Use pull-up resistor • Default Value = 0x0

Field Properties for Register 0x0A (Continued)

Bits	Mnemonic	Prop	Description
3	UsePulldown4Pamp	WO brst SPI	Connect a Pull-Down Resistor to PAMP Pad *Purpose:* When this bit is set to 1, a pull-down resistor is connected to the PAMP pad, but only when UsePullup4Pamp is 0. *Register Values/Settings:* • 0 = No pull-down resistor • 1 = Use pull-down resistor • Default Value = 0x0
4	UsePullup4Ucirq	WO brst SPI	Connect a Pull-Up Resistor to ucIRQ Pad *Purpose:* When this bit is set to 1, a pull-up resistor is connected to the ucIRQ pad. *Register Values/Settings:* • 0 = No pull-up resistor • 1 = Use pull-up resistor • Default Value = 0x0
5	UsePulldown4Ucirq	WO brst SPI	Connect a Pull-Down Resistor to ucIRQ Pad *Purpose:* When this bit is set to 1, a pull-down resistor is connected to the ucIRQ pad, but only when UsePullup4Ucirq is 0. *Register Values/Settings:* • 0 = No pull-down resistor • 1 = Use pull-down resistor • Default Value = 0x0
6	UsePullup4Ucrst	WO brst SPI	Connect a Pull-Up Resistor to ucRST Pad *Purpose:* When this bit is set to 1, a pull-up resistor is connected to the ucRST pad. *Register Values/Settings:* • 0 = No pull-up resistor • 1 = Use pull-up resistor • Default Value = 0x0
7	UsePulldown4Ucrst	WO brst SPI	Connect a Pull-Down Resistor to ucRST Pad *Purpose:* When this bit is set to 1, a pull-up resistor is connected to the ucRST pad, but only when UsePullup4Ucrst is 0. *Register Values/Settings:* • 0 = No pull-down resistor • 1 = Use pull-down resistor • Default Value = 0x0

10.13 0x0B – Writing Pullup/Pulldown Settings to Pads

Used for writing the settings made in registers 0x09 and/or 0x0A to the appropriate pads on the chip. Because the destination registers are running with the 32.768 kHz clock, the write strobe has to be active for at least 30.6 ms.

Note: A write strobe must always be generated by programming a 1-0-sequence to this register. Do NOT change the content of registers 0x09 (see *0x09 – Setting SPI Pads as Pullup or Pulldown* on page 83) and 0x0A (see *0x0A – Setting Additional Pads as Pullup or Pull-down* on page 85) when one of the bits of this register is active.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x0B	R								
	init	0	0	0	0	0	0	0	0
	W							Write Pulls 4Pads	Write Pulls 4Spi
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x0B

Bits	Mnemonic	Prop	Description
0	WritePulls4Spi	WO brst SPI	Write Pull-up and Pull-Down Settings to Four SPI Pads *Purpose:* Writes the SPI pad settings (see register 0x9) to the appropriate chip pads. *Purpose:* • 0 = True • 1 = False • Default Value = 0x0
1	WritePulls4Pads	WO brst SPI	Write Pull-up and Pull-Down Settings to Four Additional Pads *Purpose:* Writes the additional pad settings (see register 0xA) to the appropriate chip pads. *Purpose:* • 0 = True • 1 = False • Default Value = 0x0

10.14 0x0C – Internal Use Only

Nanotron internal use only. Settings are required for fabrication tests only. During normal operations, this register must be set to “0”.

		MSB				Bit Number			LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x0C	RW					Internal Use Only			
	init	0	0	0	0	0	0	0	0

10.15 0x0D – Internal Use Only

Nanotron internal use only. Settings are required for fabrication tests only. During normal operations, this register must be set to “0”.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x0D	R/W					Internal Use Only			
	init	0	0	0	0	0	0	0	0

10.16 0x0E – Baseband Memory Access

Used for selecting locations inside the baseband RAM, the correlator memory, and the chirp sequencer RAM.

		MSB				Bit Number			LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x0E	R/W			DeviceSelect				RamIndex	
	init	0	0	0	0	0	0	0	0

Read/Write Fields

Field Properties for Register 0x0E

Bits	Mnemonic	Prop.	Description
0-1	RamIndex	RW brst SPI	Select Page in Baseband Memory *Purpose:* Selects one page of selected memory type (see DeviceSelect below) to be mapped into accessible SPI address space. When addresses are greater than 0xFF, the higher bits have to be written to this field. *Register Values/Settings:* • For baseband RAM, select one of: • Baseband RAM block 0 (0x0) • Baseband RAM block 1 (0x1) • Baseband RAM block 2 (0x2) • Baseband RAM block 3 (0x3) • For chirp sequencer (CSQ) RAM, select one of: • Column 0 (0x0) • Column 1 (0x1) • Column 2 (0x2) • Unused (0x3) • For correlator memory, select one of: • I (RamD3IPatI) (0x0) • Q (RamD3IPatQ) (0x1) • Thresholds (RamD3IThresholds) (0x2) • Unused (0x3) • Default Value = 0x0 *Note:* Register access to locations < 0x80 are not influenced by index settings.

Field Properties for Register 0x0E

Bits	Mnemonic	Prop.	Description
4-5	DeviceSelect	RW brst SPI	Select Memory Type *Purpose:* Selects either the baseband RAM, the chirp sequencer RAM or the correlator memory to be mapped into the accessible SPI address space *Register Values/Settings:* • For baseband RAM, select: • NA_DeviceSelectBbRam0_C (0x0) • Unused (0x1) • For chirp sequencer RAM, select: • NA_DeviceSelectCsq_C (0x2) • For correlator memory, select: • NA_DeviceSelectD3l_C (0x3) • Default Value = 0x0 *Note:* Register access to locations < 0x80 are not influenced by index settings.

10.17 0x0F – LO, BBTimer, RX/TX IRQ Event Status and Enabling

Used for selecting the sources (LO, baseband timer, receiver, transmitter) that are allowed to drive the external IRQ when an event occurs. It is also used for reporting the occurance of an interrupt event for one of the enabled receive/transmit interrupts.

Note: The status bits in 4 to 7 are independent of the enable bits 0 to 3.

		MSB				Bit Number			LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x0F	R	LoIrq Status	BbTimer IrqStatus	RxIrq Status	TxIrq Status	LoIrq Enable	BbTimer Irq Enable	RxIrq Enable	TxIrq Enable
	init	0	0	0	0				
	W								
	init	0	0	0	0	0	0	0	0

Read/Write Fields

Field Properties for Register 0x0F

Bits	Mnemonic	Prop	Description
0	TxIrqEnable	RW brst SPI	Enable Transmitter Interrupt *Register Values/Settings:* • 0 = Disable TX interrupt does not drive the interrupt line. • 1 = Enable TX interrupt drives the interrupt line. • Default Value = 0x0
1	RxIrqEnable	RW brst SPI	Enable Receiver Interrupt *Register Values/Settings:* • 0 = Disable RX interrupt does not drive the interrupt line. • 1 = Enable RX interrupt drives the interrupt line. • Default Value = 0x0
2	BbTimerIrqEnable	RW brst SPI	Enable Baseband Timer Interrupt *Register Values/Settings:* • 0 = Disable BbTimer interrupt does not drive the interrupt line. • 1 = Enable BbTimer interrupt drives the interrupt line. • Default Value = 0x0

Field Properties for Register 0x0F (Continued)

Bits	Mnemonic	Prop	Description
3	LoIrqEnable	RW brst SPI	Enable LO Interrupt *Register Values/Settings:* • 0 = Disable LO interrupt does not drive the interrupt line. • 1 = Enable LO interrupt drives the interrupt line. • Default Value = 0x0

Read Only Fields

Field Properties for Register 0x0F

Bits	Mnemonic	Prop	Description
4	TxIrqStatus	RO	Transmitter Interrupt Event Status *Purpose:* Reports the occurance of one or more of the enabled transmitter interrupts. *Register Values/Settings:* • 0 = Event did not trigger This bit is cleared when an enabled (via register 0x13) transmitter interrupt is either cleared via register 0x10 or disabled via register 0x13. • 1 = Event is triggered This bit is 1 when one or more of the enabled (via register 0x13) transmitter interrupts have occurred. Their raw status is reported in register 0x10. • Default Value = 0x0
5	RxIrqStatus	RO	Receiver Interrupt Event Status *Purpose:* Reports the occurance of one or more of the enabled receiver interrupts. *Register Values/Settings:* • 0 = Event did not trigger This bit is cleared when an enabled (via register 0x14) receiver interrupt is either cleared via register 0x11 or disabled via register 0x14. • 1 = Event is triggered This bit is 1 when one or more of the enabled (via register 0x14) receiver interrupts have occurred. Their raw status is reported in register 0x11. • Default Value = 0x0

Field Properties for Register 0x0F (Continued)

Bits	Mnemonic	Prop	Description
6	BbTimerIrqStatus	RO	Baseband Timer Event Status *Purpose:* Reports the occurance of a baseband timer event. *Register Values/Settings:* • 0 = Event did not trigger This bit is cleared when the BBTimer interrupt is reset via the register 0x12. • 1 = Event is triggered This bit is 1 when the baseband timer has reached its end. • Default Value = 0x0
7	LoIrqStatus	RO	LO IRQ Event Status *Purpose:* Reports the occurance of a LO IRQ event. *Register Values/Settings:* • 0 = Event did not trigger This bit is cleared when an enabled (via register 0x15) LO interrupt is either cleared via register 0x12 (WARNING: one of the sources is state triggered) or disabled via register 0x15. • 1 = Event is triggered This bit is 1 when one or more of the enabled (via register 0x15) LO interrupts haVE occurred. Their raw status is reported in register 0x12. • Default Value = 0x0

10.18 0x10 – TX Raw Interrupt Status and Reset [Index]

Used for reporting the raw interrupt status of the transmitter and for clearing the raw interrupt status by resetting it.

		MSB		Bit Number					LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x10	R			TxIntsRawStat					
	init	0	0	0	0	0	0	0	0
	W			TxIntsReset					
	init	0	0	0	0	0	0	0	0

Read Only Fields

Field Properties for Register 0x10

Bits	Mnemonic	Prop	Description
0-5	TxIntsRawStat	RO brst BbClk	Transmitter Interrupt Raw Status *Purpose:* Reports the TX raw interrupt of each source. *Register Values/Settings:* • See Bit Offsets (Indexes) section below.

Write Only Fields

Field Properties for Register 0x10

Bits	Mnemonic	Prop	Description
0-5	TxIntsReset	WO brst strb BbClk	Transmitter Interrupt Reset *Purpose:* Clears the interrupt status of the corresponding source. *Register Values/Settings:* • See Bit Offsets (Indexes) section below.

Bit Offsets (Indexes) for TxIntsRawStat and TxIntsReset

	MSB				Bit Number			LSB
Offset	7	6	5	4	3	2	1	0
Index			TxTime SlotEnd	TxTime SlotTOut	Tx Under run	TxEnd	TxBufferRdy	
	0	0	0	0	0	0	0	0

Index properties for Register 0x10

Bits	Interrupt	Description
0-1	TxBufferRdy	Transmit Buffer Ready *Purpose:* Indicates that the appropriate buffer has been transmitted and can, therefore, be filled with raw data, if necessary. *Register Values/Settings:* • Default Value = 0x0 *Note:* The LSB (bit 0x00) is related to the lower half of the TX buffer (TxRx buffer when using a combined buffer – TxRxBbBufferMode1), while the MSB (bit 0x01) is related to the upper half of the TX Buffer.
2	TxEnd	Transmit End *Purpose:* Indicates that the transmission has ended. *Register Values/Settings:* • Default Value = 0x0 *Note:* Conditions for successful transmissions are as follows: • If ArqScheme is used for transmission (TxArq = 1) and TxArqCnt ≤ TxArqMax, then the transmission was successful. • If ArqScheme is used for transmission (TxArq = 1) and TxArqCnt > TxArqMax, then the transmission was not successful. • If ArqScheme is not used for transmission (TxArq =0), then transmission was always successful.

Index properties for Register 0x10 (Continued)

Bits	Interrupt	Description
3	TxUnderrun	Transmit Buffer Underrun *Purpose:* Indicates that the buffer was not filled when the transmitter tried to send data. *Register Values/Settings:* • Default Value = 0x0 *Note:* This interrupt is intended for debugging purposes only and indicates a severe error condition of the controller. It must not occur during normal operation. The user is responsible for avoiding an underrun condition. How the transmitter has to be handled depends on the setting of the TxUnderrunIgnore field in register 0x4D.
4	TxTimeSlotTOut	Transmit Time Slot Time-out *Purpose:* Indicates that the transmit process exceeded the time slot and that the transmission of packets was aborted automatically. *Register Values/Settings:* • Default Value = 0x0 *Note:* Interrupt is defined only if TxTimeSlotControl = 1.
5	TxTimeSlotEnd	Transmit Time Slot End *Purpose:* Indicates that the transmit time slot has ended. *Register Values/Settings:* • Default Value = 0x0 *Note:* Interrupt is defined only if TxTimeSlotControl = 1.

10.19 0x11 – RX Raw Interrupt Status and Reset [Index]

Used for reporting the raw interrupt status of the receiver and for clearing the raw interrupt status by resetting it.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x11	R		RxIntsRawStat						
	init	0	0	0	0	0	0	0	0
	W		RxIntsReset						
	init	0	0	0	0	0	0	0	0

Read Only Fields

Field Properties for Register 0x11

Bits	Mnemonic	Prop	Description
0-6	RxIntsRawStat	RO brst BbClk	Receiver Interrupt Raw Status *Purpose:* Reports the RX raw interrupt of each source. *Register Values/Settings:* • See Bit Offsets (Indexes) section below.

Write Only Fields

Field Properties for Register 0x11

Bits	Mnemonic	Prop	Description
0-6	RxIntsReset	WO brst strb BbClk	Reset Receiver Interrupt *Purpose:* Clears the interrupt status of the corresponding source. *Register Values/Settings:* • See Bit Offsets (Indexes) section below.

Bit Offsets (Indexes) for RxIntsRawStat and RxIntsReset

MSB				Bit Number				LSB
Offset	7	6	5	4	3	2	1	0
Index		RxTime SlotEnd	RxTime SlotTOut	Rx Under run	Rx Header End	RxEnd	RxBufferRdy	
	0	0	0	0	0	0	0	0

Index properties for register 0x11

Bits	Interrupt	Description
1-0	RxBufferRdy	Receive Buffer Ready *Purpose:* Indicates that the appropriate receive buffer is filled with data and can be read out. *Register Values/Settings:* • Default Value = 0x0 *Note:* The LSB (0x00) is related to the lower half of the RX buffer (TxRx buffer when using a combined buffer – TxRxBbBufferMode1), while the MSB (0x01) is related to the upper half of the RX buffer.
2	RxEnd	End of Packet Reception *Purpose:* Indicates that end of a correct packet was detected. *Register Values/Settings:* • Default Value = 0x0 *Note:* This interrupt depends on the settings of RxCrc2Mode field and RxArqMode field in register 0x5A.
3	RxHeaderEnd	End of Correct Header Reception *Purpose:* Indicates the reception of a correct header. *Register Values/Settings:* • Default Value = 0x0 *Note:* Only usable in auto mode.

Index properties for register 0x11 (Continued)

Bits	Interrupt	Description
4	RxOverflow	Receive Buffer Overflow *Purpose:* Indicates that the receiver was not able to place data in the RX buffer because the RX buffer was full. No RxEnd interrupt is generated and no Ack packet will be transmitted *Register Values/Settings:* • Default Value = 0x0 *Note:* This interrupt is intended for debugging purposes only and indicates an error condition of the controller. It should not occur during normal operation. The user is responsible to avoid the overflow condition. This interrupt must be ignored when RxCrc2Mode field in register 0x5A is set to 1. Before a reception can be restarted through the RxCmdStart command, the pending RxBufferRdy interrupts and the receive buffers (through RxBufferCmd) must be cleared.
5	RxTimeSlotTOut	Receive Time Slot Time-out *Purpose:* Indicates that the receive process exceeded the time slot and that the transmission of Clr2s or Ack packets was aborted automatically. *Register Values/Settings:* • Default Value = 0x0 *Note:* Interrupt is defined only if RxTimeSlotControl = 1.
6	RxTimeSlotEnd	Receive Time Slot End *Purpose:* Indicates that the receive time slot has ended. *Register Values/Settings:* • Default Value = 0x0 *Note:* Interrupt is defined only if RxTimeSlotControl = 1.

10.20 0x12 – LO and BBTimer Raw Interrupt Status and Reset [Index]

Used for reporting the raw interrupt status of the Local Oscillator and for clearing the raw interrupt status by resetting it. It is also used for resetting the baseband timer interrupt or for stopping the baseband timer.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x12	R							LoInts RawStat	Internal Use Only
	init	0	0	0	0	0	0	0	0
	W	Clear Base band Timer Int						LoInts Reset	Internal Use Only
	init	0	0	0	0	0	0	0	0

Read Only Fields

Field Properties for Register 0x12

Bits	Mnemonic	Prop	Description
1	LoIntsRawStat	RO brst BbClk	Local Oscillator Interrupt Raw Status *Purpose:* Stores the LO interrupt of a triggered event. *Register Values/Settings:* • See Bit Offsets (Indexes) section below.

Write Only Fields

Field Properties for Register 0x12

Bits	Mnemonic	Prop	Description
1	LoIntsReset	WO brst strb BbClk	Reset Local Oscillator interrupt *Purpose:* Clears the interrupt status of the corresponding source. *Register Values/Settings:* • See Bit Offsets (Indexes) section below.
7	ClearBasebandTimerInt	WO brst strb BbClk	Baseband timer interrupt reset *Purpose:* Clears the BbTimer interrupt or stops the timer, if it has not reached zero. *Register Values/Settings:* • Default Value = 0x0 *Note:* After ClearBasebandTimerInt, the timer can be restarted again.

Bit Offsets (Indexes) for LO Interrupts

	MSB			Bit Number				LSB
Offset	7	6	5	4	3	2	1	0
Index							Lo Tuning Ready	Lo Tuning Needed
	0	0	0	0	0	0	0	0

Index Properties for Register 0x12

Bits	Interrupt	Description
0	LoTuningNeeded	Local Oscillator Tuning Required *Purpose:* Indicates that the LO requires tuning. *Register Values/Settings:* • Default Value = 0x0 *Note:* While all other interrupts in the chip are event triggered, this interrupt (LoTuningNeeded) is state triggered. To handle this interrupt, disable it first, start the LO tuning, and then (allowed while tuning) reset the interrupt.
1	LoTuningReady	Local Oscillator Tuning Ready *Purpose:* Indicates that the tuning algorithm for the LO has finished. *Register Values/Settings:* • Default Value = 0x0

10.21 0x13 – Enable Transmitter Interrupts [Index]

Used for enabling the different interrupt sources of the transmitter to control TxIrqStatus in register 0x0F (see *0x0F – LO, BBTimer, RX/TX IRQ Event Status and Enabling* on page 92).

Write Only Fields

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x13	R								
	init	0	0	0	0	0	0	0	0
	W			TxIntsEn					
	init	0	0	0	0	0	0	0	0

Field Properties for Register 0x13

Bits	Mnemonic	Prop	Description
0-5	TxIntsEn	WO brst BbClk	Enable Transmitter Interrupt *Purpose:* Enables the different TX interrupt sources to control TxIrqStatus. *Register Values/Settings:* • See Bit Offsets (Indexes) section below.

Bit Offsets (Indexes) for TxIntsEn

MSB			Bit Number					LSB
Offset	7	6	5	4	3	2	1	0
Index			TxTime SlotEnd	TxTime SlotTOut	Tx Under run	TxEnd	TxBufferRdy	
	0	0	0	0	0	0	0	0

Index properties for Register 0x13

Bits	Interrupt	Description
0-1	TxBufferRdy	Transmit Buffer Ready *Purpose:* Indicates that the appropriate buffer has been transmitted and can be filled with raw data, if necessary. *Register Values/Settings:* • Default Value = 0x0 *Note:* The LSB (bit 0x00) is related to the lower half of the TX buffer (TxRx buffer when using a combined buffer – TxRxBbBufferMode1), while the MSB (bit 0x01) is related to the upper half of the TX buffer.
2	TxEnd	Transmit End *Purpose:* Indicates that the transmission has ended. *Register Values/Settings:* • Default Value = 0x0 *Note:* Conditions for a successful transmission are as follows: • If ArqScheme is used for transmission (TxArq = 1) and TxArqCnt ≤ TxArqMax, then the transmission was successful. • If ArqScheme is used for transmission (TxArq = 1) and TxArqCnt > TxArqMax, then the transmission was not successful. • If ArqScheme is not used for transmission (TxArq =0) then transmission was always successful.

Index properties for Register 0x13 (Continued)

Bits	Interrupt	Description
3	TxUnderrun	Transmit Buffer Underrun *Purpose:* Indicates that buffer was not filled when the transmitter tried to send data. *Register Values/Settings:* • Default Value = 0x0 *Note:* This interrupt is intended for debugging purposes only and indicates a severe error condition of the controller. It must not occur during normal operation. The user is responsible for avoiding the underrun condition. How the transmitter has to be handled depends on the setting of the TxUnderrunIgnore field in register 0x4D.
4	TxTimeSlotTOut	Transmit Time Slot Time-out *Purpose:* Indicates that the transmit process exceeded the time slot and that the transmission of packets was aborted automatically. *Register Values/Settings:* • Default Value = 0x0 *Note:* Interrupt is defined only if TxTimeSlotControl = 1.
5	TxTimeSlotEnd	Transmit Time Slot End *Purpose:* Indicates that the transmit time slot has ended. *Register Values/Settings:* • Default Value = 0x0 *Note:* Interrupt is defined only if TxTimeSlotControl = 1.

10.22 0x14 – Receiver Interrupt Enable [Index]

Used for enabling the different interrupt sources of the receiver to control RxIrqStatus in register 0x0F (see *0x0F – LO, BBTimer, RX/TX IRQ Event Status and Enabling* on page 92).

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x14	R								
	init	0	0	0	0	0	0	0	0
	W		RxIntsEn						
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x14

Bits	Mnemonic	Prop	Description
0-6	RxIntsEn	WO brst BbClk	Enable Receiver Interrupt *Purpose:* Enables the different RX interrupt sources to control the combined RxIrqStatus. *Register Values/Settings:* • See Bit Offsets (Indexes) section below.

Bit Offsets (Indexes) for RX Interrupts

	MSB			Bit Number				LSB
Offset	7	6	5	4	3	2	1	0
Index		RxTime SlotEnd	RxTime SlotTOut	Rx Under run	Rx Header End	RxEnd	RxBufferRdy	
	0	0	0	0	0	0	0	0

Index properties for Register 0x14

Bits	Interrupt	Description
1-0	RxBufferRdy	Receive Buffer Ready *Purpose:* Indicates that the appropriate receive buffer is filled with data and can be read out. *Register Values/Settings:* • Default Value = 0x0 *Note:* The LSB (0x00) is related to the lower half of the RX buffer (TxRx buffer when using a combined buffer – TxRxBbBufferMode1), while the MSB (0x01) is related to the upper half of the RX buffer.
2	RxEnd	End of Packet Reception *Purpose:* Indicates that end of a correct packet was detected. *Register Values/Settings:* • Default Value = 0x0 *Note:* This interrupt depends on the settings of RxCrc2Mode field and RxArqMode field in register 0x5A.
3	RxHeaderEnd	End of Correct Header Reception *Purpose:* Indicates the reception of a correct header. *Register Values/Settings:* • Default Value = 0x0 *Note:* Only usable in auto mode.

Index properties for Register 0x14 (Continued)

Bits	Interrupt	Description
4	RxOverflow	Receive Buffer Overflow *Purpose:* Indicates that the receiver was not able to place data in the receive buffer because the receive buffer was full. No RxEnd interrupt is generated and no Ack packet will be transmitted. *Register Values/Settings:* • Default Value = 0x0 *Note:* This interrupt is intended for debugging purposes only and indicates an error condition of the controller. It should not occur during normal operation. The user is responsible to avoid the overflow condition. This interrupt must be ignored when RxCrc2Mode field in register 0x5A is set to 1. Before a reception can be restarted through the RxCmd-Start command, the pending RxBufferRdy interrupts and the receive buffers (through RxBufferCmd) must be cleared.
5	RxTimeSlotTOut	Receive Time Slot Time-out *Purpose:* Indicates that the receive process exceeded the time slot and that the transmission of Clr2s or Ack packets was aborted automatically. *Register Values/Settings:* • Default Value = 0x0 *Note:* Interrupt is defined only if RxTimeSlotControl = 1.
6	RxTimeSlotEnd	Receive Time Slot End *Purpose:* Indicates that the receive time slot has ended. *Register Values/Settings:* • Default Value = 0x0 *Note:* Interrupt is defined only if RxTimeSlotControl = 1.

10.23 0x15 – Local Oscillator Interrupt Enable [Index]

Used for enabling the different interrupt sources of the Local Oscillator to control LoIrqStatus in register 0x0F (see *0x0F – LO, BBTimer, RX/TX IRQ Event Status and Enabling* on page 92).

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x15	R								
	init	0	0	0	0	0	0	0	0
	W							LoIntsEn	Internal Use Only
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x15

Bits	Mnemonic	Prop	Description
1	LoIntsEn	WO	Enable Local Oscillator interrupt *Purpose:* Enables the different LO interrupt sources to control the combined LoIrqStatus. *Register Values/Settings:* See Indexes section below.

Bit Offsets (Indexes) for LO Interrupts

	MSB			Bit Number				LSB
Offset	7	6	5	4	3	2	1	0
Index							Lo Tuning Ready	Lo Tuning Needed
	0	0	0	0	0	0	0	0

Index Properties for Register 0x15

Bits	Interrupt	Description
0	LoTuningNeeded	Local Oscillator Tuning Required *Purpose:* Indicates that the LO requires tuning. *Register Values/Settings:* • Default Value = 0x0 *Note:* While all other interrupts in the chip are event triggered, this interrupt (LoTuningNeeded) is state triggered. To handle this interrupt, disable it first, start the LO tuning, and then (allowed while tuning) reset the interrupt.
1	LoTuningReady	Local Oscillator Tuning Ready *Purpose:* Indicates that the tuning algorithm for the LO has finished. *Register Values/Settings:* • Default Value = 0x0

10.24 0x16 to 0x18 – RF Local Oscillator RX Capacitors

Used for reading the 22 switchable capacitors of the Local Oscillator after tuning or for setting the 22 switchable capacitors of the Local Oscillator for the RX frequencies.

Note: To save time, the capacitor values for receive can be read after the adjustment has been performed. After following a power-down and wake-up, these values can be written to the register instead of adjusting the Local Oscillator again..

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x16	R/W	LoRxCapsValue							
	init	0	1	0	0	0	0	0	0
0x17	R/W	LoRxCapsValue							
	init	0	0	0	0	0	0	0	0
0x18	R/W			LoRxCapsValue					
	init	0	0	1	0	0	0	0	0

Read/Write Fields

Field Properties for Register 0x16 to 0x18

Bits	Mnemonic	Prop	Description
0-22	LoRxCapsValue	R/W brst BbClk	Read or Write the Caps Value for RX *Purpose:* Reads or writes the 22 capacitors of the Local Oscillator for receive frequency. The correct capacitor values can be read after the Local Oscillator has been tuned. *Register Values/Settings:* • Default Value = 0x200040

10.25 0x19 to 0x1B – RF Local Oscillator TX Capacitors

Used for reading the 22 switchable capacitors of the Local Oscillator after tuning or for setting the 22 switchable capacitors of the Local Oscillator for the TX frequencies.

Note: To save time, the capacitor values for transmit can be read after the adjustment has been performed. After following a power-down and wake-up, these values can be written to the register instead of adjusting the Local Oscillator again. .

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x19	R/W	LoTxCapsValue							
	init	0	1	0	0	0	0	0	0
0x1A	R/W	LoTxCapsValue							
	init	0	0	0	0	0	0	0	0
0x1B	R/W			LoTxCapsValue					
	init	0	0	1	0	0	0	0	0

Read/Write Fields

Field Properties for Register 0x19 to 0x1B

Bits	Mnemonic	Prop	Description
0-22	LoTxCapsValue	RW brst BbClk	Read or Write the Caps Value for TX *Purpose:* Reads or writes the 22 capacitors of the Local Oscillator for transmit frequency. The correct capacitor values can be read after the Local Oscillator has been tuned. *Register Values/Settings:* • Default Value = 0x200040

10.26 0x1C – RF Local Oscillator Controls

Used for tuning the LO capacitors to the target frequency, for setting the level of accuracy of the tuning, for accelerating the LO caps tuning, for enabling auto-recalibration of the LO caps, and for switching between TX and RX caps for LO caps tuning.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x1C	R								
	init	0	0	0	0	0	0	0	0
	W	Use Lo RxCaps		Internal Use Only	Lo Enable Lsb Neg	LoFastTuningLevel			Lo Enable Fast Tuning
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x1C

Bits	Mnemonic	Prop	Description
0	LoEnableFastTuning	WO brst BbClk	Enable Accelerated LO Caps Tuning *Purpose:* Enables an algorithm that speeds up the tuning of the LO capacitors to the target frequency. *Register Values/Settings:* • 0 = Normal tuning • 1 = Accelerated tuning • Default Value = 0x0
1-3	LoFastTuningLevel	WO brst BbClk	Set LO Caps Tuning Level *Purpose:* Sets the level of accuracy of the tuning. Generally, the higher the tuning level, the more accurate the tuning to the target frequency. *Register Values/Settings:* • Allowed Values: • If LoEnableLsbNeg = = 0, then 0x0 to 0x2 (maximum 2) • If LoEnableLsbNeg = = 1, then 0x0 to 0x6 (maximum 6) • Default Value = 0x0
4	LoEnableLsbNeg	WO brst BbClk	Enable Higher Precision Accelerated LO Caps Tuning *Purpose:* Accelerates the LO Caps tuning by factor of 2. *Register Values/Settings:* • 0 = Normal tuning • 1 = Accelerated tuning by factor of 2 • Default Value = 0x0

Field Properties for Register 0x1C

Bits	Mnemonic	Prop	Description
7	UseLoRxCaps	WO brst BbClk	Select RX or TX Caps *Purpose:* Switch between TX and RX Caps for LO caps tuning. *Register Values/Settings:* • 0 = Use TX caps • 1 = Use RX caps • Default Value = 0x0 *Note:* This field must be set before starting the LO caps tuning.

10.27 0x1D to 0x1E – RF Local Oscillator Target Value

Used for setting the target value for the LO center frequency, which is used for adjusting either the RX or TX Local Oscillator frequency..

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x1D	R/W	LoTargetValue							
	init	0	0	0	0	0	0	0	0
0x1E	R/W	LoTargetValue							
	init	0	0	0	0	0	0	0	0

Read/Write Fields

Field Properties for Register 0x1D to 1E

Bits	Mnemonic	Prop	Description
0-16	LoTargetValue	WO brst BbClk	Target Value for Center Frequency *Purpose:* 16 bit target value for the Local Oscillator frequency adjustment. This value is used to determines the target LO center frequency. The LOTargetValue is determined as follows: $\lceil (\{LOdiv10/(16MHz)\} - 12) \cdot 8192 \rceil$ *Register Values/Settings:* Before setting this value, the following must be enabled: • Local Oscillator – EnableLO • Clock divider – EnableLOdiv10 Also, the appropriate mode (RX, TX) must be selected using the UseLoRxCaps: • UseLoRxCaps = 1 (RX mode) • UseLoRxCaps = 0 (Tx mode) *Note:* A write operation to the upper byte starts the tuning algorithm automatically.

10.28 0x1F – AGC Threshold 1

Used for setting the lower threshold for the integration value.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x1F	R								
	init	0	0	0	0	0	0	0	0
	W	AgcThresHold1							
	init	0	0	0	0	0	0	1	1

Write Only Fields

Field Properties for Register 0x1F

Bits	Mnemonic	Prop	Description
0-7	AgcThresHold1	WO brst BbClk	Set AGC Threshold1 *Purpose:* Sets the lower level of the integration value. *Register Values/Settings:* • Default Value = 0x3

10.29 0x20 – AGC Threshold 2

Used with AgcThresHold1 for setting the upper threshold for the integration value.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x20	R								
	init	0	0	0	0	0	0	0	0
	W	AgcThresHold2							
	init	0	0	0	0	0	1	1	0

Write Only Fields

Field Properties for Register 0x

Bits	Mnemonic	Prop	Description
0-7	AgcThresHold2	WO brst BbClk	Set AGC Threshold2 *Purpose:* AgcThresHold1 plus the value set in this register is used to determine the upper level of the integration value. *Register Values/Settings:* • Default Value = 0x6

10.30 0x21 – AGC Hold Frame/Bit Synchronization Controls

Used for enabling or disabling the AGC stop and for defining a delay from the bit synchronization state until the AGC stop is enabled in bit synchronized state.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x21	R								
	init	0	0	0	0	0	0	0	0
	W	Hold Agc InFrame Sync	HoldAgcInBitSync						
	init	1	0	0	1	1	0	0	0

Write Only Fields

Field Properties for Register 0x21

Bits	Mnemonic	Prop	Description
0-6	HoldAgcInBitSync	WO brst BbClk	RF AGC Hold Bit Synchronization Control *Purpose:* When in bit synchronization state, gain is not changed (AGC is stopped) after a programmable number of pulses are received. Register Values/Settings: • Default Value = 0x18
7	HoldAgcInFrameSync	WO brst BbClk	RF AGC Hold Frame Synchronization Control *Purpose:* When the receiver reaches frame synchronization state, gain is not changed (AGC is stopped). Register Values/Settings: • 0 = Do not hold AGC • 1 = Hold AGC • Default Value = 0x1

10.31 0x22 – AGC Change Gain Length

Used for setting the gain change mode.

Note: When using this register, bits 0 to 5 MUST be set to 0xC.

		MSB		Bit Number					LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x22	R								
	init	0	0	0	0	0	0	0	0
	W	AgcNregLength		Internal Use Only					
	init	0	0	0	0	1	1	0	0

Write Only Fields

Field Properties for Register 0x

Bits	Mnemonic	Prop	Description
6-7	AgcNregLength	WO brst BbClk	AGC Change Gain Length *Purpose:* Sets the gain change mode. When the AGC has changed (N-1) times during the last N rounds in the same direction, then fast AGC tuning is restarted. *Register Values/Settings:* • 00: N=5 • 01: N=7 • 1X: N=10 • Default Value = 0x0

10.32 0x23 to 0x24 – AGC Integration Time

Used for setting the number of cycles for AGC integration.

Note: One cycle is equal to LO frequency divided by 20.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x23	R								
	init	0	0	0	0	0	0	0	0
	W	AgcIntTime							
	init	0	0	0	0	0	0	0	0
0x24	R								
	init	0	0	0	0	0	0	0	0
	W					AgcIntTime			
	init	0	0	0	0	0	0	1	0

Write Only Fields

Field Properties for Register 0x23 to 24

Bits	Mnemonic	Prop	Description
0-12	AgcIntTime	WO brst BbClk	AGC Integration Time *Purpose:* Sets the number of cycles for AGC integration. *Register Values/Settings:* • Default Value = 0x200 *Note:* One cycle is equal to LO frequency divided by 20.

10.33 0x25 – Internal Use Only

Nanotron internal use only. Settings are required for fabrication tests only. During normal operations, this register must be set to “0”.

		MSB				Bit Number			LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x25	R								
	init	0	0	0	0	0	0	0	0
	W	Internal Use Only	Internal Use Only	Internal Use Only					
	init	0	0	1	1	1	1	1	1

10.34 0x26 – RF RSSI and AGC Controls

Used for setting the RSSI threshold value and for reading the RSSI voltage value.

		MSB				Bit Number			LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x26	R			AgcGain					
	init	0	0	0	0	0	0	0	0
	W	Internal Use Only		AgcRssiThres					
	init	0	0	0	1	1	1	1	0

Read Only Fields

Field Properties for Register 0x26

Bits	Mnemonic	Prop	Description
0-5	AgcGain	RO brst BbClk	Read Gain for Current Packet *Purpose:* The RX gain used for the current packet can be read after the packet header end interrupt. *Register Values/Settings:* • Default Value = 0x0

Write Only Fields

Field Properties for Register 0x26

Bits	Mnemonic	Prop	Description
0-5	AgcRssiThres	WO brst BbClk	RF RSSI Threshold *Purpose:* When gain is below this threshold, media is interpreted as busy when the upper bit TxPhCarrSenseMode field is set to 1. *Register Values/Settings:* • Default Value = 0x1E

10.35 0x27 – RC Oscillator / Leapfrog Filter Tuning

Used for initiating a FCT (Filter Caps Tuning) count cycle, for switching on the FCT generator, for switching the capacitors of the chirp filter, and for enabling the amplitude of the transmitter. It is also used for reading the FCT counter. See also *Adjusting the RCOSC/Leapfrog Filter Frequency*.

		MSB		Bit Number					LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x27	R			FctPeriod					
	init	0	0	0	0	0	0	0	0
	W	Enable Tx		Start Fct Measure	Fct ClockEn	ChirpFilterCaps			
	init	0	0	0	0	0	1	1	0

Read Only Fields

Field Properties for Register 0x27

Bits	Mnemonic	Prop	Description
0-5	FctPeriod	RO brst BbClk	RF TX FCT Counter *Purpose:* Reports the return value from tuning. It counts the amount of 16 MHz clock periods during a FCT clock cycle. *Register Values/Settings:* • Default Value = 0x0

Write Only Fields

Field Properties for Register 0x27

Bits	Mnemonic	Prop	Description
0-3	ChirpFilterCaps	WO brst BbClk	RF TX Chirp Filter Capacitors *Purpose:* Switches the capacitors of the chirp filter to adjust the FCT clock to 400 kHz. *Register Values/Settings:* • Default Value = 0x06
4	FctClockEn	WO brst BbClk	Enable RF TX FCT *Purpose:* Switches on the FCT generator. This is required for the chirp filter calibration. *Register Values/Settings:* • 0 = Disable • 1 = Enable • Default Value = 0x0

Field Properties for Register 0x27 (Continued)

Bits	Mnemonic	Prop	Description
5	StartFctMeasure	WO brst BbClk	Set RF TX FCT Measurement *Purpose:* Starts the tuning algorithm. It initiates an FCT count cycle. *Register Values/Settings:* • 0 = Ignore • 1 = Start algorithm • Default Value = 0x0 *Note:* FctClockEn must be set to 1 before starting the measurement cycle.
7	EnableTx	WO brst BbClk	Enable RF TX *Purpose:* Enables the transmitter for tuning. It manually starts the transmitter. *Register Values/Settings:* • 0 = Disable manual starting of TX • 1 = Manual starting of TX • Default Value = 0x0

10.36 0x28 to 0x29 – Baseband Timer Start Values

Used for setting the start value of the baseband timer. The baseband timer is running with 1 MHz. It is started when the upper byte of BasebandTimerStartValue is written. The baseband timer is stopped when the timer has expired or when writing ClearBasebandTimerInt.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x28	R/W	BasebandTimerStartValue							
	init	0	0	0	0	0	0	0	0
0x29	R/W	BasebandTimerStartValue							
	init	0	0	0	0	0	0	0	0

Read/Write Fields

Field Properties for Register 0x28 to 0x29

Bits	Mnemonic	Prop	Description
0-15	BasebandTimerStartValue	WO brst BbClk	Baseband Timer Start Value *Purpose:* Sets the start value of the timer. The interrupt BbTimerInt is triggered if the timer reaches zero. The timer starts automatically when the upper byte is written to the register. *Register Values/Settings:* • Default Value = 0x0 *Note:* Timer tick period is 1 µs. Timer values range from 1 to 65535.

10.37 0x2A to 0x2B – Internal Use Only (Read Only)

Nanotron internal use only. During normal operations, this register must be set to “0”.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x2F	R	Internal Use Only							
	init	0	0	0	0	0	0	0	0
0x30	R	Internal Use Only			Internal Use Only				
	init	0	0	0	0	0	0	0	0

10.38 0x2C to 0x2D – Internal Use Only (Read Only)

Nanotron internal use only. During normal operations, this register must be set to “0”.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x2F	R	Internal Use Only							
	init	0	0	0	0	0	0	0	0
0x30	R	Internal Use Only							
	init	0	0	0	0	0	0	0	0

10.39 0x2A to 0x31 – Transceiver SyncWord (Write Only)

Used for defining the synchronization word, which is transmitted and is used for frame synchronization during reception (correlation).

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x2A	W	SyncWord							
	init	1	0	1	0	1	0	1	1
0x2B	W	SyncWord							
	init	0	0	1	0	1	1	0	0
0x2C	W	SyncWord							
	init	1	1	0	1	0	1	0	1
0x2D	W	SyncWord							
	init	1	0	0	1	0	0	1	0
0x2E	W	SyncWord							
	init	1	0	0	1	0	1	0	0
0x2F	W	SyncWord							
	init	1	1	0	0	1	0	1	0
0x30	W	SyncWord							
	init	0	1	1	0	1	0	0	1
0x31	W	SyncWord							
	init	1	0	1	0	1	0	1	1

Write Only Fields

Field Properties for Register 0x2A to 0x31

Bits	Mnemonic	Prop	Description
0-63	SyncWord	WO brst BbClk	Set Transceiver SyncWord *Purpose:* Defines the synchronization word which is used for frame synchronization. *Register Values/Settings:* • Default Value = 0x0xAB69CA9492D52CAB *Usage:* Auto and transparent mode. *This register must be defined before:* TxCmdStart = True or RxCmdStart = True

10.40 0x2E – Internal Use Only (Read Only)

Nanotron internal use only. During normal operations, this register must be set to “0”.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x2E	R		Internal Use Only				Internal Use Only		
	init	0	0	0	0	0	0	0	0

10.41 0x2F to 0x30 – Internal Use Only (Read Only)

Nanotron internal use only. During normal operations, this register must be set to “0”.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x2F	R	Internal Use Only							
	init	0	0	0	0	0	0	0	0
0x30	R	Internal Use Only			Internal Use Only				
	init	0	0	0	0	0	0	0	0

10.42 0x31 – Receiver Mode Controls (Read Only)

Used for reporting the status of CRC1 and CRC2 checks, and for reporting the stored status of the address matching circuitry and the received packet type.

		MSB		Bit Number					LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x31	R	RxCrc2 Stat	RxCrc1 Stat	RxAddrMatch		RxPacketType			
	init	0	0	0	0	0	0	0	0

Read Only Fields

Field Properties for Register 0x31

Bits	Mnemonic	Prop	Description
0-3	RxPacketType	RO brst BbClk	Receive Packet Type *Purpose:* Stores the received packet type. *Register Values/Settings:* • Default Value = 0x0 *Note:* Valid only when the RxHeaderEnd event is triggered. *Usage:* Auto mode only.
4-5	RxAddrMatch	RO brst BbClk	Receive Address Match for Data Packets *Purpose:* Reports the address matching status of Data packets. It is reported if either the destination address is equal the station address set in RamStaAddr0 or if the destination address, with ES mode disabled, is equal RamStaAddr1. *Register Values/Settings:* • RxAddrMatch[0]: • 0 = Received destination address does not match the station address set in RamStaAddr0 • 1 = Received destination address matches the station address set in RamStaAddr0 • RxAddrMatch[1]: • 0 = Received destination address does not match the station address set in RamStaAddr1 • 1 = Received destination address matches the station address set in RamStaAddr1 • Default Value = 0x0 *Note:* Address matching must be enabled (RxAddrMode). Also, valid only when the RxHeaderEnd event is triggered *Usage:* Auto mode only.

Field Properties for Register 0x31 (Continued)

Bits	Mnemonic	Prop	Description
6	RxCrc1Stat	RO brst BbClk	Status of CRC1 Check (For MAC Header) *Purpose:* Reports the status of the CRC1 check. *Register Values/Settings:* • 0 = CRC1 check has failed • 1 = CRC1 check was successful • Default Value = 0x0 *Note:* Valid only when the RxHeaderEnd event is triggered. This register just makes sense for TimeB packets when RxTimeBCrc1Mode == NA_RxTimeBCrc1ModeOn_BC_C. *Usage:* Auto mode only.
7	RxCrc2Stat	RO brst BbClk	Status of CRC2 Check (For Payload) *Purpose:* Reports the status of the CRC2 check. *Register Values/Settings:* • 0 = CRC2 check has failed • 1 = CRC2 check was successful • Default Value = 0x0 *Note:* Valid only when the RxEnd event is triggered. *Usage:* Auto mode only.

10.43 0x32 – Receive Correlator Error Controls

Used for defining the maximum allowed bit errors when a received pattern is correlated to the SyncWord and for reading the number of bit errors occurred during SyncWord correlation.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x32	R					RxCorrBitErr			
	init	0	0	0	0	0	0	0	0
	W	RxCorrErrThres							
	init	0	0	1	1	0	0	0	0

Read Only Fields

Field Properties for Register 0x32

Bits	Mnemonic	Prop	Description
0-3	RxCorrBitErr	RO brst BbClk	Number of Syncword Errors *Purpose:* Reports the number of bit errors that have occurred during Syncword correlation. *Register Values/Settings:* • Default Value = 0x0 *Note:* Register is valid when the RxHeaderEnd event is triggered. *Usage:* Auto mode only.

Write Only Fields

Field Properties for Register 0x32

Bits	Mnemonic	Prop	Description
4-7	RxCorrErrThres	WO brst BbClk	Maximum Allowable Syncword Errors *Purpose:* It defines the threshold for bit errors allowed during the correlation of a received pattern against the Syncword stored in register 0x2A (SyncWord). If the occurred bit errors are equal to or less than RxCorrErrThres, then the receiver synchronizes. *Register Values/Settings:* • Allowed values are between 0 and 15. • Default Value = 0x3 *This register must be defined before:* RxCmdStart = True *Usage:* Auto and transparent mode only.

10.44 0x33 to 0x34 – Transmit Time Slot Start (Write Only)

Used for defining the beginning of the time slot for a transmission.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x33	W	TxTimeSlotStart							
	init	0	0	0	0	0	0	0	0
0x34	W	TxTimeSlotStart							
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x33 to 0x34

Bits	Mnemonic	Prop	Description
0-15	TxTimeSlotStart	WO brst BbClk	Set Transmit Time Slot Start *Purpose:* Defines the beginning of the time slot for a transmission. Used with TxTimeSlotControl. *Register Values/Settings:* • Only the 16 LSBs of the RTC value are compared to TxTimeSlotStart. If both values are equal, then the time slot begins. • Default Value = 0x0 *This register must be defined before:* TxCmdStart = True. *Usage:* Auto mode only.

10.45 0x35 to 0x36 – Transmit Time Slot End (Write Only)

Used for defining the end of the time slot for a transmission.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x35	W	TxTimeSlotEnd							
	init	0	0	0	0	0	0	0	0
0x36	W	TxTimeSlotEnd							
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x35 to 0x36

Bits	Mnemonic	Prop	Description
0-15	TxTimeSlotEnd	WO brst BbClk	Set Transmit Time Slot End *Purpose:* Defines the end of the time slot for a transmission. Used with TxTimeSlotControl. *Register Values/Settings:* • Only the 16 LSBs of the RTC value are compared to TxTimeSlotEnd. If both values are equal, then the time slot ends. *This register must be defined before:* TxCmdStart = True *Usage:* Auto mode only.

10.46 0x33 – Receiver Encryption (Read Only)

Used for reporting the status of End Station and Intermediate Station address matching, as well as for reporting the value of the three encryption control fields: CryptEn, CryptID, and CryptSeqN.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x33	R	RxCrypt SeqN	RxCryptId		RxCrypt En			RxAddr Seg IsMatch	RxAddr Seg EsMatch
	init	0	0	0	0	0	0	0	0

Read Only Fields

Field Properties for Register 0x33

Bits	Mnemonic	Prop	Description
0	RxAddrSegEsMatch	RO brst BbClk	RX Address Segment End Station (ES) Match *Purpose:* Shows the status of the segmented address match of end station address part. *Register Values/Settings:* • 0 = End Station address does not match • 1 = End Station address matches • Default Value = 0x0
1	RxAddrSegIsMatch	RO brst BbClk	RX Address Segment Intermediate Station (IS) Match *Purpose:* Shows the status of the segmented address match of Intermediate Station address part. *Register Values/Settings:* • 0 = Intermediate Station address does not match • 1 = Intermediate Station address matches • Default Value = 0x0
4	RxCryptEn	RO brst BbClk	Value of CryptEn Bit *Purpose:* Reads the value of the one bit Encryption Enable field, which is in the four bit EncryptionControl field inside the MAC header. *Register Values/Settings:* • 0 = Disabled • 1 = Enabled • Default Value = 0x0 *Note:* Valid when the RxHeaderEnd event is triggered.

Field Properties for Register 0x33 (Continued)

Bits	Mnemonic	Prop	Description
5-6	RxCryptId	RO brst BbClk	Value of CryptID Bits *Purpose:* Reads the value of the two bit Encryption ID field for encrypted Data, Brdcast, and TimeB packets, which is in the four bit EncryptionControl field inside the MAC header. *Register Values/Settings:* • Default Value = 0x0 *Note:* Valid when the RxHeaderEnd event is triggered.
7	RxCryptSeqN	RO brst BbClk	Value of CryptSeqN Bit *Purpose:* Reads the value of the one bit sequential numbering scheme for encryption. The receiver compares the last received against the present CryptSeqN bit and increments its crypt clock value by one, if they are not identical. *Register Values/Settings:* • Default Value = 0x0 *Note:* Valid when the RxHeaderEnd event is triggered.

10.47 0x34 to 0x35 – Receive FEC Single Bit Error Count (Read Only)

Used for reporting the number of single bit errors that have occurred in a received packet.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x34	R	RxFec1BitErr							
	init	0	0	0	0	0	0	0	0
0x35	R		RxFec1BitErr						
	init	0	0	0	0	0	0	0	0

Read Only Fields

Field Properties for Register 0x34 to 0x35

Bits	Mnemonic	Prop	Description
0-14	RxFec1BitErr	RO brst BbClk	Number of Corrected FEC Errors *Purpose:* Reports the number of correctable single bit errors that have occurred in a receive packet. *Register Values/Settings:* • Default Value = 0x0 *Note:* Register is valid when the event RxEnd is triggered and when UseFec == UseFecOn. *Usage:* Auto mode only.

10.48 0x36 – Reserved (Read Only)

The Read Only fields in register 0x36 are reserved.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x36	R								
	init	0	0	0	0	0	0	0	0

10.49 0x37 – Transmitter and Receiver Time Slot Control (TDMA)

Used for enabling or disabling time slot control (TDMA) for the receiver and transmitter.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x37	R								
	init	0	0	0	0	0	0	0	0
	W							RxTime Slot Control	TxTime Slot Control
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x37

Bits	Mnemonic	Prop	Description
0	TxTimeSlotControl	WO brst BbClk	Enable TX Time Slot Control (TDMA) *Purpose:* Enables the TX time slot control so that packets are transmitted only during the defined TX time slot. *Register Values/Settings:* • 0 = Disabled Packets are transmitted independent of the time slot. • 1 = Enabled Packets are transmitted only during the defined TX time slot. • Default Value = 0x0 *This register must be defined before:* TxCmdStart = True *Usage:* Auto mode only.

Field Properties for Register 0x37 (Continued)

Bits	Mnemonic	Prop	Description
1	RxTimeSlotControl	WO brst BbClk	Receive Time Slot Control *Purpose:* Enables the RX time slot control so that at the beginning of the defined RX time slot, the receiver is automatically activated. *Register Values/Settings:* • 0 = Disabled Activates the receiver independent of the defined time slot through the RxCmd command. • 1 = Enabled Automatically activates the receiver at the beginning of the defined RX time slot. • Default Value = 0x0 *Note:* When enabled, the receive can still be manually activated through the RxCmd command. *Usage:* Auto mode only.

10.50 0x38 to 0x39 – RX Packet Slot (Read Only)

Used for reporting the start time slot for receiving a packet by reading the 16 LSBs of the RTC value on a header end event.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x38	R	RxPacketSlot							
	init	0	0	0	0	0	0	0	0
0x39	R	RxPacketSlot							
	init	0	0	0	0	0	0	0	0

Read Only Fields

Field Properties for Register 0x38 to 0x39

Bits	Mnemonic	Prop	Description
0-15	RxPacketSlot	RO brst BbClk	Time (RTC) at End of Header *Purpose:* Reports time (16 LSBs of RTC) at the packet header end event. *Register Values/Settings:* • Default Value = 0x0 *Note:* Register is valid when the RxHeaderEnd event is triggered. *Usage:* Auto mode only.

10.51 0x38 to 0x39 – RX Time Slot Start and Packet Slot (Write Only)

Used for defining the start time slot for a reception and for reading the 16 LSBs of the RTC value on a header end event.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x38	W	RxTimeSlotStart							
	init	0	0	0	0	0	0	0	0
0x39	W	RxTimeSlotStart							
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x38 to 0x39

Bits	Mnemonic	Prop	Description
0-15	RxTimeSlotStart	WO brst BbClk	Set Receive Time Slot Start *Purpose:* Defines the beginning of the time slot for a reception. Used with RxTimeSlotControl. *Register Values/Settings:* • Default Value = 0x0 *Note:* Only the 16 LSBs of the RTC value are compared to RxTimeSlotStart. If both values are equal, the time slot begins. *This register must be defined before:* RxCmdStart = True *Usage:* Auto mode only.

10.52 0x3A to 0x3B – RX Time Slot End

Used for defining the end of the time slot for reception.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x3A	R								
	init	0	0	0	0	0	0	0	0
	W	RxTimeSlotEnd							
	init	0	0	0	0	0	0	0	0
0x3B	R								
	init	0	0	0	0	0	0	0	0
	W	RxTimeSlotEnd							
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x3A to 0x3B

Bits	Mnemonic	Prop	Description
0-15	RxTimeSlotEnd	WO brst BbClk	Set Receive Time Slot End *Purpose:* Defines the end of the time slot for a reception. Used with RxTimeSlotControl. *Register Values/Settings:* • Default Value = 0x0 *Register Values/Settings:* *Note:* Only the 16 LSBs of the RTC value are compared to RxTimeSlotEnd. If both values are equal, the time slot ends. *This register must be defined before:* RxCmdStart = True *Usage:* Auto mode only.

10.53 0x3C – ARQ

Used for setting the maximum value for packet retransmissions and for reporting the ARQ retransmission counter value.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x3C	R					TxArqCnt			
	init	0	0	0	0	0	0	0	0
	W	TxArqMax							
	init	1	1	1	0	0	0	0	0

Read Only Fields

Field Properties for Register 0x3C

Bits	Mnemonic	Prop	Description
0-3	TxArqCnt	RO brst BbClk	Transmitter ARQ Count (Required Retransmissions) *Purpose:* Reports the required number of retransmissions. *Register Values/Settings:* • Default Value = 0x0 *Note:* The following conditions are used to determine if the transmission was successful or unsuccessful: • If TxArqCnt ≤ TxArqMax, then the transmission was successful. • If TxArqCnt > TxArqMax, then the transmission was not successful.

Write Only Fields

Field Properties for Register 0x3C

Bits	Mnemonic	Prop	Description
4-7	TxArqMax	WO brst BbClk	Transmit ARQ Maximum *Purpose:* Sets the maximal value for packet retransmissions. *Register Values/Settings:* • The maximal allowed value is 14. *This register must be defined before:* TxCmdStart = True *Usage:* Auto mode only.

10.54 0x3D – RF Chirp Generator Controls

Used for providing settings for the chirp generator and for accessing the Chirp Sequencer RAM.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x3D	R								
	init	0	0	0	0	0	0	0	0
	W	Internal Use Only	Csq UseRam	Csq Mem AddrInit	Csq Asy Mode	Csq Use 4Phases	CsqUse Phase Shift	CsqDitherValue	
	init	0	0	0	0	0	1	0	0

Write Only Fields

Field Properties for Register 0x3D

Bits	Mnemonic	Prop	Description
0-1	CsqDitherValue	WO brst BbClk	Chirp Sequencer Dither Value *Purpose:* Provides a dither function, which is used to delay transmission based on settings made to this field. Each cycle is equal to the frequency of LO div 20. *Register Values/Settings:* • 0 = No delay • 1 = delay is 0 or 1 cycle (distribution 1:1) • 2 = delay is 0, 1, or 2 cycles (distribution 1:1:1) • 3 = delay is 0, 1, or 2 cycles (distribution 2:1:1) • Default Value = 0x0
2	CsqUsePhaseShift	WO brst BbClk	Chirp Sequencer Use Phase Shift *Purpose:* Enables the pseudo-random feature of the chirp generator to improve the RF-spectrum of the transmitted chirps. Causes transmission with 0° and 180° phase shift. *Register Values/Settings:* • 0 = Disable (phase shift is always 0°) • 1 = Enable • Default Value = 0x0
3	CsqUse4Phases	WO brst BbClk	Use Four Phases *Purpose:* Provides an additional 90° and 270° phase shift, along with the 0° and 180° phases enabled by CsqUsePhaseShift. *Register Values/Settings:* • 0 = Disable • 1 = Enable • Default Value = 0x0

Field Properties for Register 0x3D (Continued)

Bits	Mnemonic	Prop	Description
4	CsqAsyMode	WO brst BbClk	Set Asymmetric Mode *Purpose:* When enabled, Chirp Sequencer RAM is addressed asymmetrically. *Register Values/Settings:* • 0 = Disable (access symmetrically: address increment AND decrement) • 1 = Enable (access increment only) • Default Value = 0x0
5	CsqMemAddrInit	WO brst strb BbClk	Initialize Chirp Sequencer Memory Address *Purpose:* Sets the address counter of the chirp generator memory back to 0. Required before writing to a Chirp Sequencer RAM column. *Register Values/Settings:* • 0 = Disable • 1 = Enable • Default Value = 0x0
6	CsqUseRam	WO brst BbClk	Use Chirp Sequencer RAM *Purpose:* Enables the Chirp Sequencer RAM. *Register Values/Settings:* • 0 = Disable (default matrix is used) • 1 = Enable • Default Value = 0x0

10.55 0x3E – Internal Use Only (Write Only_)

For Nanotron Internal use only. These bits must be set to 0.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x3E	R								
	init	0	0	0	0	0	0	0	0
	W	Internal Use Only							
	init	0	0	0	0	0	0	0	0

10.56 0x3F – Correlator (Dispersive Delay Line) Controls

Used for setting the digital correlator in either FIX or MAP mode, for enabling POM mode, and for setting mean values.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x3F	R								
	init	0	0	0	0	0	0	0	0
	W	Internal Use Only				D3lPomLen		D3lPomEn	D3lFixnMap
	init	0	0	0	0	0	0	0	1

Write Only Fields

Field Properties for Register 0x3F

Bits	Mnemonic	Prop	Description
0	D3lFixnMap	WO brst BbClk	Use FIX or MAP Mode *Purpose:* Sets either FIX or MAP mode in the Correlator. FIX mode is default. *Register Values/Settings:* • 0 = Use MAP mode • 1 = Use FIX mode • Default Value = 0x1
1	D3lPomEn	WO brst BbClk	Enable POM Mode *Purpose:* Enables the mean value calculation in the Correlator. *Register Values/Settings:* • 0 = Disable • 1 = Enable • Default Value = 0x0 *Note:* Note: Can only be used in FIX mode.
2-3	D3lPomLen	WO brst BbClk	Set POM Length Values *Purpose:* Select if the last 2, 4, 8, or 16 values should be used for calculating the mean value. *Register Values/Settings:* • 00: 2; 01: 4 10: 8; 11: 16 • Default Value = 0x0

10.57 0x40 – Frame Synchronization and Bit Synchronization

Used for setting the number of detected pulses (in bit synchronization state) before switching back from either MAP mode or FIX mode using correlator threshold 1, which depends on setting of D3lFixnMap, to FIX mode using correlator threshold 0. It is also used for switching to MAP mode or FIX mode using correlator threshold 1 (in frame synchronization state).

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x40	R								
	init	0	0	0	0	0	0	0	0
	W	UseMap Thresh1 InFrame sync	LeaveMapThresh1InBitsync						
	init	0	0	0	0	0	0	1	1

Write Only Fields

Field Properties for Register 0x40

Bits	Mnemonic	Prop	Description
0-6	LeaveMapThresh1InBitsync	WO brst BbClk	Switch Back to FIX Mode with Threshold 0 *Purpose:* Switch back to FIX mode using correlator threshold 0 in bit synchronization state after programmed number of detected pulses. *Register Values/Settings:* • Default Value = 0x3
7	UseMapThresh1InFramesync	WO brst BbClk	Use MAP Mode or FIX mode with Threshold 1 in Frame Sync State *Purpose:* Switch to MAP mode or FIX mode using correlator threshold 1 in frame synchronization state. *Register Values/Settings:* • 0 = FIX with Threshold0 • 1 = FIX with Threshold1 or MAP (D3LFixnMap) • Default Value = 0x0

10.58 0x41 – Bit Synchronization

Used for setting the number of detected pulses (in bit synchronization state) before switching to either MAP mode or FIX mode using correlator threshold 1

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x41	R								
	init	0	0	0	0	0	0	0	0
	W	Internal Use Only	Go2MapThresh1InBitsync						
	init	0	0	0	0	0	1	1	1

Write Only Fields

Field Properties for Register 0x41

Bits	Mnemonic	Prop	Description
0	Go2MapThresh1InBitsync	WO brst BbClk	Switch to FIX Mode with Threshold1 or MAP Mode *Purpose:* Switch from FIX mode using correlator threshold 0 to either MAP mode or FIX mode using correlator threshold 1 (D3LFixnMap) after programmed number of detected pulses in bit synchronization state. *Register Values/Settings:* • Default Value = 0x7

10.59 0x42 – Local Oscillator, Chirp Sequencer, and External PA Controls

Used for enabling the Local Oscillator, the LO divider, the clock for the chirp sequencer, the RX clock, and the external power amplifier control pin.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x42	R								
	init	0	0	0	0	0	0	0	0
	W	Internal Use Only	Internal Use Only	Internal Use Only	Enable ExtPA	Invert RxClock	Enable Csq Clock	Enable LOdiv10	Enable LO
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x42

Bits	Mnemonic	Prop	Description
0	EnableLO	WO brst BbClk	Enable RF Local Oscillator *Purpose:* Enables the Local Oscillator. *Register Values/Settings:* • 0 = Disable • 1 = Enable • Default Value = 0x0 *Note:* Required only for tuning the Local Oscillator and for programming the Chirp Sequencer (CSQ) RAM.
1	EnableLOdiv10	WO brst BbClk	Enable LO Frequency Divide By 10 Function *Purpose:* When enabled, the LO frequency is divided by 10 and delivered to digital part. *Register Values/Settings:* • 0 = Disable • 1 = Enable • Default Value = 0x0 *Note:* Required only for tuning the Local Oscillator and for programming the Chirp Sequencer (CSQ) RAM.

Field Properties for Register 0x42 (Continued)

Bits	Mnemonic	Prop	Description
2	EnableCsqClock	WO brst BbClk	Enable Chirp Sequencer Clock *Purpose:* Enables the Chirp Sequencer (CSQ) clock. *Register Values/Settings:* • 0 = Disable • 1 = Enable • Default Value = 0x0 *Note:* Required only for programming the Chirp Sequencer (CSQ) RAM.
3	InvertRxClock	WO brst BbClk	Changing Sampling Edge for Receiver *Note:* It is recommended that this not be change. Use the default value. *Register Values/Settings:* • 0 = Disable • 1 = Enable • Default Value = 0x0
4	EnableExtPA	WO brst BbClk	Enable External Power Amplifier Output *Purpose:* Enables the external power amplifier control pin to allow the use of an external power amplifier. It must be set when using an external power amplifier *Register Values/Settings:* • 0 = Deactivate pin • 1 = Activate pin *Note:* The pin is low-active during transmit cycles and has high-impedance during non-transmit cycles.

10.60 0x43 – RF Rx Low Noise Amplifier and TX Power Amplifier Bias

Used for adjusting the frequency of the LNA response, and for adjusting the power amplifier bias current.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x43	R								
	init	0	0	0	0	0	0	0	0
	W		TxPaBias				LnaFreqAdjust		
	init	0	0	0	0	0	0	1	1

Write Only Fields

Field Properties for Register 0x43

Bits	Mnemonic	Prop	Description
0-2	LnaFreqAdjust	WO brst BbClk	Adjust RF Receiver LNA Frequency *Purpose:* Frequency adjustment of the LNA (Low Noise Amplifier) frequency response (S21). *Register Values/Settings:* • 111b – Shift the middle frequency of the LNA frequency response to lower frequencies • 000b – Shift the middle frequency of the LNA frequency response to higher frequencies • Default Value = 0x3 (recommended)
4-6	TxPaBias	WO brst BbClk	Adjust RF Transmitter Power Amplifier Bias *Purpose:* Adjusts the PA bias current to compensate process deviations. *Register Values/Settings:* • Default Value = 0x0 (Recommended)

10.61 0x44 – Transmitter Output Power (Data, TimeB, and BrdCast)

Used for setting the RF transmitter output power for Data, TimeB, and Brdcast packets.

		MSB				Bit Number			LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x44	R								
	init	0	0	0	0	0	0	0	0
	W			TxOutputPower0					
	init	0	0	1	1	1	1	1	1

Write Only Fields

Field Properties for Register 0x44

Bits	Mnemonic	Prop	Description
0-5	TxOutputPower0	WO brst BbClk	Adjust RF TX Output Power 0 *Purpose:* Sets the transmitter output power for data (Data) packets, time beacon (TimeB) packets, and broadcast (BrdCast) packets. *Register Values/Settings:* • Default Value = 0x3F

10.62 0x45 – Transmitter Output Power (Ack, Req2S, and Clr2S)

Used for setting the RF Transmitter output power for Ack, Req2S, and Clr2S packets.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x45	R								
	init	0	0	0	0	0	0	0	0
	W			TxOutputPower1					
	init	0	0	1	1	1	1	1	1

Write Only Fields

Field Properties for Register 0x45

Bits	Mnemonic	Prop	Description
0-5	TxOutputPower1	WO brst BbClk	Adjust RF TX Output Power 1 *Purpose:* Sets the transmitter output power for acknowledgement packets (Ack), request to send (Req2S) packets, and clear to send (Clr2S) packets. *Register Values/Settings:* • Default Value = 0x3F

10.63 0x46 – Quantization Threshold for I

Used for programming the quantization threshold for the 5bit ADC for I value.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x46	R								
	init	0	0	0	0	0	0	0	0
	W				RfRxCompValueI				
	init	0	0	0	0	1	1	1	1

Write Only Fields

Field Properties for Register 0x46

Bits	Mnemonic	Prop	Description
0-4	RfRxCompValueI	WO brst BbClk	Quantization Threshold for I *Register Values/Settings:* • Default Value = 0xF

10.64 0x47 – Quantization Threshold for Q

Used for programming the quantization threshold for the 5bit ADC for Q value.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x47	R								
	init	0	0	0	0	0	0	0	0
	W				RfRxCompValueQ				
	init	0	0	0	0	1	1	1	1

Write Only Fields

Field Properties for Register 0x47

Bits	Mnemonic	Prop	Description
0	RfRxCompValueQ	WO brst BbClk	Quantization Threshold for Q *Register Values/Settings:* • Default Value = 0xF

10.65 0x48 – Symbol Duration, Symbol Rate, and Modulation System

Used for determining the transmission behavior, including setting the symbol duration, the symbol rate, and selecting the modulation system.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x48	R								
	init	0	0	0	0	0	0	0	0
	W	Modulation System	SymbolRate				SymbolDur		
	init	0	1	1	0	0	0	1	1

Write Only Fields

Field Properties for Register 0x48

Bits	Mnemonic	Prop	Description
0-2	SymbolDur	WO BbClk	Set Symbol Duration *Purpose:* Set symbol duration between 500 ns and 16000 ns. *Register Values/Settings:* • NA_SymbolDur500ns_C (0x0) • NA_SymbolDur1000ns_C (0x1) • NA_SymbolDur2000ns_C (0x2) • NA_SymbolDur4000ns_C (0x3) • NA_SymbolDur8000ns_C (0x4) • NA_SymbolDur16000ns_C (0x5) • Default Value = 0x3 *Note:* 16000 ns and 8000 ns are allowed only for 22 MHz bandwidth.
4-6	SymbolRate	WO BbClk	Set Symbol Rate *Purpose:* Sets the symbol rate between 31.25 k Symbols and 2M Symbols *Register Values/Settings:* • NA_SymbolRate500kSymbols_VC_C (0x0) • NA_SymbolRate1MSymbols_VC_C (0x1) • NA_SymbolRate2MSymbols_VC_C (0x2) • NA_SymbolRate31k25Symbols_VC_C (0x4) • NA_SymbolRate62k5Symbols_VC_C (0x5) • NA_SymbolRate125kSymbols_VC_C (0x6) • NA_SymbolRate250kSymbols_VC_C (0x7) • Default Value = 0x7

Field Properties for Register 0x48

Bits	Mnemonic	Prop	Description
7	ModulationSystem	WO brst BbClk	Select Transceiver Modulation System *Purpose:* Defines the modulation system of the transceiver (2-ary modulation system or 4-ary modulation system). *Register Values/Settings:* • NA_ModulationSystem2ary_BC_C (0x0) Selects the 2-ary modulation system • NA_ModulationSystem4ary_BC_C (0x1) Selects the 4-ary modulation system. • Default Value = 0x0 *This register must be defined before:* TxCmdStart = True or RxCmdStart = True

10.66 0x49 – CRC2, CRC2 Encryption, FEC, and Encryption Clock Mode

Used for selecting the CRC2 type, for enabling the CRC2 encryption, for selecting the encryption/decryption clock mode, and for enabling FEC.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x49	R								
	init	0	0	0	0	0	0	0	0
	W	TxRxCryptClkMode				TxRx CryptCrc 2 Mode	Use Fec	Crc2Type	
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x49

Bits	Mnemonic	Prop	Description
0-1	Crc2Type	WO brst BbClk	Select Transceiver CRC2 Type *Purpose:* Selects the CRC2 used for reception and transmission. Cyclic Redundancy Checking and generation is calculated over the data field. *Register Values/Settings:* • Select CRC Type 1 (ISO/IEC3309): • NA_Crc2Type1_VC_C (0x0) • NA_Crc2Type1Bits_IC_C (0x10) • Select CRC Type 2 (IEC 60870-5-1): • NA_Crc2Type2_VC_C (0x1) • NA_Crc2Type2Bits_IC_C (0x10) • Select CRC Type 3 (CCITT-32): • NA_Crc2Type3_VC_C (0x2) • NA_Crc2Type3Bits_IC_C (0x20) • Default Value = 0x0 *This register must be defined before:* TxCmdStart = True or RxCmdStart = True *Usage:* Auto mode only.

Field Properties for Register 0x49 (Continued)

Bits	Mnemonic	Prop	Description
2	UseFec	WO brst BbClk	Enable Forward Error Correction (FEC) *Purpose:* Purpose: Enables the forward error correction. Error correction is applied to the complete MAC frame using a (7,4) block code. *Register Values/Settings:* • NA_UseFecOff_BC_C(0x0) Disables FEC. • NA_UseFecOn_BC_C(0x1) Enables FEC. • Default Value = 0x0 *This register must be defined before:* TxCmdStart = True or RxCmdStart = True *Usage:* Auto mode only.
3	TxRxCryptCrc2Mode	WO brst BbClk	Enable Encryption/Decryption CRC2 Mode *Purpose:* Enables or disables the Encryption/Decryption of CRC2. *Register Values/Settings:* • NA_TxRxCryptCrc2ModeUncrypted_BC_C(0x0) In this mode, the CRC2 is calculated on the unencrypted data, then appended and both the CRC2 and Data field are encrypted. The advantage of this method is that integrity checking is possible. The disadvantage is that reception of the packet is not possible without the key. No key means no reception (no forwarding). • NA_TxRxCryptCrc2ModeEncrypted_BC_C(0x1) In this mode, the CRC2 is calculated on the encrypted data, then the CRC2 is appended unencrypted to the encrypted Data field. The advantages of this method is that no key for data error checking is needed and Forwarding is possible. The disadvantage is that no integrity checking is possible. • Default Value = 0x0 *This register must be defined before:* TxCmdStart = True or RxCmdStart = True *Usage:* Auto mode only.

Field Properties for Register 0x49 (Continued)

Bits	Mnemonic	Prop	Description
4-7	TxRxCryptClkMode	WO brst BbClk	Set Encryption/Decryption Clock Mode *Purpose:* Selects the mode of the clock input value of the stream cipher for each CryptId. Bit4 belongs to CryptId0, .. Bit 7 belongs to CryptId3. *Register Values/Settings:* • NA_TxRxCryptClkModeCryptClock_BC_C(0x0) Uses the RamTxCryptClock / RamRxCryptClock values for the clock input value calculating the en-/decryption key. • NA_TxRxCryptClkModeScrambInit_BC_C(0x1) The lowest 7 bits of the crypt clock (TxCrypt-Clock /RxCryptClock are replaced by the value of the ScrambInit field. The MSBs are taken from RamTxCryptClock / RamRxCryptClock registers. *Note:* For TX, the CryptID is taken from the TxCryptID field while for RX, the CryptID is taken from the received packet. *This register must be defined before:* TxCmdStart = True or RxCmdStart = True *Usage:* Auto mode only.

10.67 0x4A – Buffer and MACFrame Configuration

Used for setting the Baseband buffer mode (Duplex or Simplex and Auto or Transparent) and for setting the MACFrame mode (Auto or Transparent). It is also used for enabling FDMA, which uses 22 MHz bandwidth, and for swapping RX and TX baseband buffers.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x4A	R								SwapBb Buffers
	init	0	0	0	0	0	0	0	
	W	TxRx Mode			Fdma Enable		TxRxBb Buffer Mode0	TxRxBb Buffer Mode1	
	init	0	0	0	1	0	0	0	0

Read/Write Fields

Field Properties for Register 0x4A

Bits	Mnemonic	Prop	Description
0	SwapBbBuffers	R/W brst BbClk	Exchange RX and TX Baseband Buffers *Purpose:* Exchanges the buffers between the baseband transmitter and receiver. When enabled, if a station is set up as an intermediate station (IS), the station does not have to move data from the RX buffer to the TX buffer. *Register Values/Settings:* • 0 = Default Data in buffers belong to their intended direction. • 1 = Enable data swapping Data for the transmit operation are taken from the receive buffer, while data of the receive operation are stored in transmit buffer. • Default Value = 0x0 *Note:* This is useful only in duplex mode. *See also:* TxRxBbBufferMode1

Write Only Fields

Field Properties for Register 0x4A

Bits	Mnemonic	Prop	Description
1	TxRxBbBufferMode1	WO brst BbClk	Baseband Buffer Mode 1: Duplex or Simplex *Purpose:* Sets the data buffer for TX and RX as either two blocks (Duplex) or a single block (Simplex). *Register Values/Settings:* • NA_TxRxBufferMode1Duplex_BC_C (0x0) Sets Duplex mode In this mode, the data buffer is split into two blocks, one for TX and one for RX. TX and RX buffer operations are independent of each other. • NA_TxRxBufferMode1Simplex_BC_C (0x1) Sets Simplex mode. In this mode, the complete buffer is used for TX and RX. • Default Value = 0x0 *Note:* Buffer size and configuration depend on the combination of TxRxBbBufferMode0 and TxRxBbBufferMode1.
2	TxRxBbBufferMode0	WO brst BbClk	Baseband Buffer Mode 0: Auto or Transparent *Purpose:* Sets for TX and RX data either two segments (Auto) or all four segments (Transparent). *Register Values/Settings:* • NA_TxRxBufferMode0Auto_BC_C (0x0) Sets Auto mode: TX/RX buffer size = 256 bytes. In this mode, the upper half of the Baseband RAM (two segments totalling 256 bytes) is used for data, as either a TX or a RX buffer. The other two segments totalling 256 bytes are reserved for: • MAC frame header data • Station addresses • Encryption keys and related control values • RTC snapshots • NA_TxRxBufferMode0Transparent_BC_C (0x1) In this mode, the complete Baseband RAM (all four segments totalling 512 bytes) is used for data, as either a TX or a RX buffer. • Default Value = 0x0 *Note:* Buffer size and configuration depend on the combination of TxRxBbBufferMode0 and TxRxBbBufferMode1.

Field Properties for Register 0x4A (Continued)

Bits	Mnemonic	Prop	Description
4	FdmaEnable	WO brst BbClk	Enable FDMA *Purpose:* Enables FDMA (Frequency Division Multiple Access), which uses 22 MHz bandwidth. When disabled, 80 MHz bandwidth is used. *Register Values/Settings:* • 0 = Disable • 1 = Enable • Default Value = 0x0
7	TxRxMode	WO brst BbClk	MACFrame Mode: Auto and Transparent *Purpose:* When using auto mode, the MACFrame is built as a nanoNET MACFrame with header information and data. When using transparent mode, the complete MAC-Frame is considered data. *Register Values/Settings:* • NA_TxRxModeAuto_BC_C (0x0) Sets Auto mode. In this mode, each MACFrame is built as described in the *nanoNET TRX System Specifications* with a header part and a data part. For TX, software need only deliver the bytes for the data part, while for RX only the data part is returned to software. • NA_TxRxModeTransparent_BC_C (0x1) Sets Transparent mode. In this mode, the complete MACFrame is interpreted as data. For TX, software delivers all bytes of the MACFrame, while for RX all bytes are returned to software. • Default Value = 0x0

10.68 0x4B to 0x4C – Transceiver Chirp Matrix

In a 2ary system, each bit, whose possible values are 0 or 1, is represented as a chirp pulse. ChirpMatrix0 is used to select the type of chirp pulse which represents the value 0. ChirpMatrix1 is used for selecting the type of chirp pulse which represents the value 1.

In a 4ary system, each bit pair, whose possible values are 0 to 3, is represented as a chirp pulse. ChirpMatrix0 is used to select the type of chirp pulse which represents the value 0. ChirpMatrix1 is used to select the type of chirp pulse which represents the value 0. ChirpMatrix2 is used for selecting the type of chirp pulse which represents the value 2. ChirpMatrix3 is used to select the type of chirp pulse which represents the value 3.

The pulse types include: Upchirp, Downchirp, Minus Folded Pulse, Plus Folded Pulse, and Off Chirp. For more details about pulse types and 2ary and 4ary systems, see *nanoLOC TRX System Specifications*.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x4B	R								
	init	0	0	0	0	0	0	0	0
	W		ChirpMatrix1				ChirpMatrix0		
	init	0	0	0	1	0	0	0	0
0x4C	R								
	init	0	0	0	0	0	0	0	0
	W		ChirpMatrix3				ChirpMatrix2		
	init	0	1	0	0	0	0	1	1

Pulse Types

For each of ChirpMatrix0, ChirpMatrix1, ChirpMatrix2, and ChirpMatrix3, select one of the pulse types as listed in the following table.

To Set Pulse Type	*Use This Constant*	*Hex Value*
Downchirp	NA_ChirpDown_VC_C	0x0
Upchirp	NA_ChirpUp_VC_C	0x1
Minus Folded Chirp	NA_ChirpFoldMinus_VC_C	0x2
Plus Folded Chirp	NA_ChirpFoldPlus_VC_C	0x3
Off Chirp	NA_ChirpOff_VC_C	0x4

Setting Pulse Types for a 2Ary System

Field Properties for Register 0x4B

Bits	Mnemonic	Prop	Description
0-2	ChirpMatrix0	WO brst BbClk	Set Pulse Type for Values 0 *Register Values/Settings:* • Select pulse type (see table above) • Default Value = 0x0 *This register must be defined before:* TxCmdStart = True or RxCmdStart = True
4-6	ChirpMatrix1	WO brst BbClk	Set Pulse Type for Value 1 *Register Values/Settings:* • Select pulse type (see table above) • Default Value = 0x0 *This register must be defined before:* TxCmdStart = True or RxCmdStart = True

Setting Pulse Types for 4Ary Bit Pairs

Field Properties for Register 0x4B to 0x4C

Bits	Mnemonic	Prop	Description
0-2	ChirpMatrix0	See 2ary table above.	
4-8	ChirpMatrix1	See 2ary table above.	
8-10	ChirpMatrix2	WO brst BbClk	Set Pulse Type for Value 2 *Register Values/Settings:* • Select Pulse Type (see table above) • Default Value = 0x0 *This register must be defined before:* TxCmdStart = True or RxCmdStart = True
12-14	ChirpMatrix3	WO brst BbClk	Set Pulse Type for Value 3 *Register Values/Settings:* • Select Pulse Type (see table above) • Default Value = 0x0 *This register must be defined before:* TxCmdStart = True or RxCmdStart = True

10.69 0x4D – TX Underrun, CIFS Waiting, and Preamble/Tail Sequences

Used for setting whether the chip ignores a TX underrun or aborts after a TX underrun and for disabling waiting for CIFS (Common InterFrame Switching time). It is also used for defining the sequence of the Preamble and the Tail of a MACFrame. Chirp pulses are transmitted in the following sequence:

• TxPreTrailMatrix0

• TxPreTrailMatrix1

• TxPreTrailMatrix0

• TxPreTrailMatrix1

• and so on.

Note: An Off symbol cannot be used in the Preamble or the Tail. Therefore, in an Up/Off or Down/Off modulation system, both values must be the same value.

For more details see *nanoLOC TRX System Specifications*.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x4D	R								
	init	0	0	0	0	0	0	0	0
	W	TxMac CifsDis			TxUnder run Ignore	TxPreTrailMatrix1		TxPreTrailMatrix0	
	init	0	0	0	1	0	1	0	0

Write Fields

Field Properties for Register 0x4D

Bits	Mnemonic	Prop	Description
0-1	TxPreTrailMatrix0	WO brst BbClk	Value for Symbol 0 in Preamble and Tail (Trail) *Purpose:* Sets the value of symbol 0 in the MACFrame Preamble and Tail. *Register Values/Settings:* • Symbol used in TxRxChirpMatrix0 (0x0) • Symbol used in TxRxChirpMatrix1 (0x1) • Symbol used in TxRxChirpMatrix3 (0x2) • Symbol used in TxRxChirpMatrix3 (0x3) • Default Value = 0x0 *This register must be defined before:* TxCmdStart = True or RxCmdStart = True Usage: Auto and transparent mode.

Field Properties for Register 0x4D (Continued)

Bits	Mnemonic	Prop	Description
2-3	TxPreTrailMatrix1	WO brst BbClk	Value for Symbol 1 in Preamble and Tail (Trail) *Purpose:* Sets the value of symbol 1 in the MACFrame Preamble and Tail. *Register Values/Settings:* • Symbol used in TxRxChirpMatrix0 (0x0) • Symbol used in TxRxChirpMatrix1 (0x1) • Symbol used in TxRxChirpMatrix3 (0x2) • Symbol used in TxRxChirpMatrix3 (0x3) • Default Value = 0x1 *This register must be defined before:* TxCmdStart = True or RxCmdStart = True *Usage:* Auto and transparent mode.
4	TxUnderrunIgnore	WO brst BbClk	TX Underrun Ignore/Auto-Abort *Purpose:* When a transmission underrun occurs, if this bit is enabled, the underrun error will be ignored and the transmission can continue or software can abort the transmission. If this bit is disabled, transmission is aborted automatically when a transmission underrun occurs. *Register Values/Settings:* • 0 = Disable Transmission aborts automatically. • 1 = Enable Transmission does not abort automatically. It must be aborted by the command TxCmdStop. • Default Value = 0x1
7	TxMacCifsDis	WO brst BbClk	Disable Waiting for CIFS (Common InterFrame Switching time) *Purpose:* When waiting for an idle media for transmission the transmitter first waits for an idle media then for the CIFS time (time needed for the station which was just transmitting to start its receiver) and the n for several back-off slots. With this register waiting for CIFS time can be disabled. *Register Values/Settings:* • 0 = Enable waiting • 1 = Disable waiting • Default Value = 0x0

10.70 0x4E – Media Access Control for Transmitter

Used for enabling virtual carrier sensing (with or without Ack packets), as well for enabling physical carrier sensing using either RSSI or chirp detection. It is also used for enabling ARQ, which uses acknowledgements, a three-way handshake mechanism (to avoid collisions and eliminate “hidden node” problems), and a back-off mechanism for medium access.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x4E	R								
	init	0	0	0	0	0	0	0	0
	W	TxFrag Prio	TxBack OffAlg	Tx3Way	TxArq	TxVCarr SensAck	TxPhCarr SenseMode		TxVCarr Sens
	init	0	0	0	1	0	0	0	0

Write Only Fields

Field Properties for Register 0x4E

Bits	Mnemonic	Prop	Description
0	TxVCarrSens	WO brst BbClk	Virtual Carrier Sensing *Purpose:* Virtual Carrier Sensing calculates the end of the current transmission based on information taken from the received header. When this carrier sense method is enabled, the NAV (Network Allocation Vector) is calculated using the packet type and Length field of received packets. Also, the transmitter suspends medium access until the NAV expires. *Register Values/Settings:* • NA_TxVCarrSensOff_BC_C (0x0) • NA_TxVCarrSensOn_BC_C (0x1) • Default Value = 0x0 *See also: nanoNET System Specifications* *This register must be defined before:* TxCmdStart = True *Usage:* Auto mode only.

Field Properties for Register 0x4E (Continued)

Bits	Mnemonic	Prop	Description
1-2	TxPhCarrSenseMode	WO brst BbClk	Physical Carrier Sensing Mode: RSSI or Chirp Detection *Purpose:* Physical carrier sensing uses either RSSI or chirp symbol detection. Using RSSI, if AgcGain is lower than AgcRssiThreshold, than the carrier is busy. Using the other method, if a chirp is detected, then the carrier is busy. Physical carrier sensing mode can be based either on chirp detection, RSSI threshold, or both chirp detection and RSSI threshold. *Register Values/Settings:* • NA_TxPhCarrSensModeOff_VC_C (0x0) Physical carrier sensing is not applied. • NA_TxPhCarrSensModeSymbols_VC_C (0x1) Physical carrier sensing is based on chirp symbol detection. • NA_TxPhCarrSensModeRssi_VC_C (0x2) Physical carrier sensing is based on an RSSI threshold. • NA_TxPhCarrSensModeSymbolsRssi_VC_C (0x3) Physical carrier sensing is based on both symbol detection and RSSI threshold. *See also: nanoNET System Specifications* *This register must be defined before:* TxCmdStart = True. Usage: Auto and transparent mode.
3	TxVCarrSensAck	WO brst BbClk	Include Ack Packets for Virtual Carrier Sense *Purpose:* Purpose: When virtual carrier Sense is enabled and this bit is set the time of an Ack packet is taken into calculation when calculating the NAV (Network Allocation Vector). *Register Values/Settings:* • NA_TxVCarrSensAckOff_BC_C (0x0) NAV calculation does not regard Ack packets. • NA_TxVCarrSensAckOn_BC_C (0x1) NAV calculation regards Ack packets. *See also: nanoNET System Specifications* *This register must be defined before:* TxCmdStart = True. *Usage:* Auto mode only.

Field Properties for Register 0x4E (Continued)

Bits	Mnemonic	Prop	Description
4	TxArq	WO brst BbClk	TX ARQ (Automatic Repeat Request) Error Correction Scheme for Data Packets *Purpose:* When this bit is set, the station waits for an Ack packet as a response to a transmitted Data packet. *Register Values/Settings:* • NA_TxArqOff_BC_C (0x0) ARQ is disabled. When ARQ is disabled, the transmitter does not wait for an Ack packet as a response to a Data packet. • NA_TxArqOn_BC_C (0x1) ARQ is enabled. With ARQ, the transmitting station waits for an acknowledgement (ACK packet). The packet is retransmitted automatically if TxArqMax > 0. *Note:* ARQ must be disabled for Brdcast and TimeB packets. *See also: nanoNET System Specifications* *This register must be defined before:* TxCmdStart = True. *Usage:* Auto mode only.
5	Tx3Way	WO brst BbClk	Three-Way Handshake *Purpose:* The three-way handshake uses a Req2S and Clr2S mechanism. It is only used with Data packets. It is not used with Brdcast and TimeB packets. *Register Values/Settings:* • NA_Tx3WayOff_BC_C (0x0) Three-way handshake is disabled. • NA_Tx3WayOn_BC_C (0x1) Three-way handshake is enabled. *See also: nanoNET System Specifications* *This register must be defined before:* TxCmdStart = True. *Usage:* Auto mode only.

Field Properties for Register 0x4E (Continued)

Bits	Mnemonic	Prop	Description
6	TxBackOffAlg	WO brst BbClk	Back-Off Algorithm *Purpose:* The exponential back-off algorithm waits a specific period of time before reattempting a transmission. *Register Values/Settings:* • NA_TxBackOffAlgOff_BC_C (0x0) Back-off algorithm is disabled. The complete seed is taken (see TxBackoffSeed) and the seed is not modified. • NA_TxBackOffAlgOn_BC_C (0x1) Back-off algorithm is enabled. The number of bits taken from seeds are always increased when transmission fails, that is no acknowledgement. 3 bits are taken for the first transmission, and the seed is changed pseudo-randomly. *See also: nanoNET System Specifications* *This register must be defined before:* TxCmdStart = True. *Usage:* Auto mode only.
7	TxFragPrio	WO brst BbClk	Fragmentation Prioritization *Purpose:* Enables fragmentation prioritization scheme used in the back-off time algorithm. *Register Values/Settings:* • 0 = Disable The MSB of the back-off counter is set with the MSB from the random value. • 1 = Enable Sets the MSB of the Back-Off counter to value zero (higher priority). • Default Value = 0x0 *This register must be defined before:* TxCmdStart = True. *Usage:* Auto mode only.

10.71 0x4F – Back-Off Seed for Back-Off Time

Used for setting the number of back-off slots, which is the start value of the random number generator for exponential back-off.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x4F	R								
	init	0	0	0	0	0	0	0	0
	W	TxBackOffSeed							
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x4F

Bits	Mnemonic	Prop	Description
0-7	TxBackOffSeed	WO brst BbClk	Back-Off Seed *Purpose:* Sets either the start value of the random number generator for exponential back-off or the number of the back-off slots. *Register Values/Settings:* • If TxBackOffAlg = TxBackOffAlgOn, then this sets the seed value for the pseudo-number generator. It can be set for every packet and improves the random properties of exponential Back-Off. . • If TxBackOffAlg = TxBackOffAlgOff, then this sets the number of Back-Off slots before a transmission or retransmission starts. *Note:* It is not mandatory to set this register. *Usage:* Auto mode only.

10.72 0x50 – Transmission Encryption

Used for resetting the internally stored values of the CryptSeqN bits (one for each key), which are compared to the programmed TxCryptSeqN bit when their key is selected and encryption starts. When the compared bits are unequal, the crypt clock used for encryption is incremented. It is also used to enable transmission encryption security, to select a secret key, and to enable a one bit sequential numbering scheme for encryption.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x50	R								
	init	0	0	0	0	0	0	0	0
	W	TxCrypt SeqN	TxCryptId		TxCrypt En	TxCryptSeqReset			
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x50

Bits	Mnemonic	Prop	Description
0-3	TxCryptSeqReset	WO brst strb BbClk	TX Decryption Sequence Reset *Purpose:* Resets the last transmitted SeqN bit independently for each key. *Register Values/Settings:* • TxCryptSeqReset[TxCryptId] When one of these bits is set to 1, the internally stored CryptSeqN bit for the corresponding key is reset to 0. *Note:* The internally stored CryptSeqN bits (4 for TX and 4 for RX) are always zero after reset (PowerOnReset or Baseband Reset).
4	TxCryptEn	WO brst BbClk	Encryption Switch *Purpose:* Enables the encryption security feature of the chip, which uses a 32 bit clock value, a 48 bit address, and a 128 bit secret key to generate the encryption cipher. This sets the CryptEn bit in the MACFrame. *Register Values/Settings:* • 0 = Disable • 1 = Enable • Default Value = 0x0 *This register must be defined before:* TxCmdStart = True *Usage:* Auto mode only.

Field Properties for Register 0x50 (Continued)

Bits	Mnemonic	Prop	Description
5-6	TxCryptId	WO brst BbClk	Secret Key Selection for Encryption *Purpose:* Selects one of four secret keys as well as one of the four TX crypt clocks, which are found in page 1 of the baseband RAM. It is only used for Data packets, Brd-cast packets and TimeB packets as only data is encrypted and other packet types have no data fields. *Register Values/Settings:* • Select first secret key (0x0) • Select second secret key (0x1) • Select third secret key (0x2) • Select fourth secret key (0x3) *See also:* 0. *This register must be defined before:* TxCmdStart = True *Usage:* Auto mode only.
7	TxCryptSeqN	WO brst BbClk	Encryption Sequence Number *Purpose:* This bit is compared to the internally stored CryptSeqN bit (the TxCryptseqN bit of last transmission) of the corresponding key. If they are unequal the used crypt clock is incremented before generating the cipher. *Register Values/Settings:* • Default Value = 0x0 *This register must be defined before:* TxCmdStart = True *Usage:* Auto mode only.

10.73 0x51 – Transmit Scrambler

Used for enabling scrambling for TX packets and for initializing the bit scrambler.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x51	R								
	init	0	0	0	0	0	0	0	0
	W	Tx Scramb En	TxScrambInit						
	init	0	1	1	1	1	1	1	1

Write Only Fields

Field Properties for Register 0x51

Bits	Mnemonic	Prop	Description
0-6	TxScrambInit	WO brst BbClk	TX Scrambling Initialization *Purpose:* Initializes the value for the scrambling unit. *Register Values/Settings:* • Do NOT program TxScrambInit with 0x00 • Default Value = 0x7F *Note:* There is no need to initialize the scrambler for each packet. *This register must be defined before:* TxCmdStart = True *Usage:* Auto mode only.
7	TxScrambEn	WO brst BbClk	Transmission Scrambling *Purpose:* Enables scrambling in a transmitted MACFrame. *Register Values/Settings:* • 0 = Disable Value 0 is intended for debugging purposes only. • 1 = Enable • Default Value = 0x1 *Note:* To randomize the data from highly redundant patterns, scrambling must be enabled during normal operations. *This register must be defined before:* TxCmdStart = True *Usage:* Auto mode only.

10.74 0x52 to 0x53 – Data Size in Transparent Mode

Used for setting the number of data bytes for transmission in Transparent mode.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x52	R								
	init	0	0	0	0	0	0	0	0
	W	TxTransBytes							
	init	0	0	0	0	0	0	0	0
0x53	R								
	init	0	0	0	0	0	0	0	0
	W				TxTransBytes				
	init	0	0	0	0	0	0	0	0

Write Fields

Field Properties for Register 0x52 to 0x53

Bits	Mnemonic	Prop	Description
0-12	TxTransBytes	WO brst BbClk	Number of Data Bytes in TX MACFrame in Transparent Mode *Purpose:* When the transceiver is set in Transparent mode, this sets the number of bytes of data in the complete MACFrame ready for transmission. These are all bytes between the Syncword and the Tail. *Register Values/Settings:* • Default Value = 0x0 *This register must be defined before:* TxCmdStart = True *Usage:* Transparent mode only.

10.75 0x54 – Packet Type for Auto Mode and TX Source Address

Used for storing the type of packet that will be transmitted, and for selecting as the source address of the packet for transmission either Station Address 0 (StaAddr0) or Station Address 1 (StaAddr1).

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x54	R								
	init	0	0	0	0	0	0	0	0
	W	TxAddr Slct				TxPacketType			
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x54

Bits	Mnemonic	Prop	Description
0-3	TxPacketType	WO brst BbClk	Packet Type For Transmission in Auto Mode *Purpose:* Stores the type of packet to be transmitted. Only Data packets, TimeB packets, and Broadcast packets can be selected. *Register Values/Settings:* • NA_TypeCodeData_VC_C (0x0) • NA_TypeCodeTimeB_VC_C (0x2) • NA_TypeCodeBrdcast_VC_C (0x3) *This register must be defined before:* TxCmdStart = True *Usage:* Auto mode only.
7	TxAddrSlct	WO brst BbClk	Source Address for Transmission *Purpose:* Selects one of the two programmed station addresses as source address for packets to be transmitted. *Register Values/Settings:* • 0 = Station Address 1 (RamStaAddr0) • 1 = Station Address 2 (RamStaAddr1). *This register must be defined before:* TxCmdStart = True *Usage:* Auto mode only.

10.76 0x55 – Start/Stop Transmissions and TX Buffer Fill Command

Used for starting and stopping the transmitter and for setting a command that indicates that the lower subblock and/or upper subblock of the TX buffer is ready for transmission.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x55	R								
	init	0	0	0	0	0	0	0	0
	W					TxBufferCmd		TxCmd Start	TxCmd Stop
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x55

Bits	Mnemonic	Prop	Description
0	TxCmdStop	WO brst strb BbClk	Stop Transmission *Purpose:* This interrupts the current transmission by aborting the transmission of a packet (in Auto mode) or stops/disables the transmission (in Transparent mode). It also resets the transmit buffer state. *Register Values/Settings:* • 0 = Default • 1 = Stop transmission • Default Value = 0x0
1	TxCmdStart	WO brst strb BbClk	Start Transmission *Purpose:* Starts the configured transmission. It initiates the transmission of a packet (in Auto mode) or starts the transmission of data (in Transparent mode). *Register Values/Settings:* • 0 = Default • 1 = Start transmission • Default Value = 0x0
2-3	TxBufferCmd	WO brst strb BbClk	Transmit Buffer Ready for Transmission *Purpose:* Indicates that either the lower subblock and/or the upper subblock of the TX Buffer is ready (filled) for transmission. *Register Values/Settings:* • Lower subblock filled for transmission LSB • Upper subblock filled for transmission MSB • Default Value = 0x0 *Note:* This command must be written after the TX buffer has been written to with the data to be transmitted.

10.77 0x56 – Start/Stop Receptions and RX Buffer Fill Command

Used for starting and stopping the receiver and for setting a command that indicates that the lower subblock and/or upper subblock of the RX buffer is empty and ready for a received packet.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x56	R								
	init	0	0	0	0	0	0	0	0
	W					RxBufferCmd		RxCmd Start	RxCmd Stop
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x56

Bits	Mnemonic	Prop	Description
0	RxCmdStop	WO brst strb BbClk	Stop Current Reception *Purpose:* This interrupts the current reception by aborting the reception of a packet (in Auto mode) or stops/disables the reception (in Transparent mode). It also resets the receive buffer state. *Register Values/Settings:* • 0 = Default • 1 = Stop reception • Default Value = 0x0
1	RxCmdStart	WO brst strb BbClk	Start Receiver in Configured Mode *Purpose:* Starts the reception of a packet (correlation in Auto or Transparent Mode). If a receive or transmit process is already active, the command is stored until the transceiver gets in the idle state. The command is then executed and reset. *Register Values/Settings:* • 0 = Default • 1 = Start reception • Default Value = 0x0
2	RxBufferCmd	WO brst strb BbClk	Read Receive Buffer *Purpose:* Purpose: Indicates either the lower subblock and/or the upper subblock of the RX Buffer are ready (empty) for reception. *Register Values/Settings:* • Lower subblock of RX buffer is read LSB • Upper subblock of RX buffer is read MSB • Default Value = 0x0

10.78 0x57 – Receiver Decryption Sequence Reset

Used for resetting the internally stored values of the CryptSeqN bits (one for each key; received in the last packet using the same key) which are compared to the currently received RxCrypt-SeqN (part of the MAC header) bit. When the compared bits are unequal the crypt clock used for decryption is incremented before generating the cipher.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x57	R								
	init	0	0	0	0	0	0	0	0
	W					RxCryptSeqReset			
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x57

Bits	Mnemonic	Prop	Description
0-3	RxCryptSeqReset	WO brst strb BbClk	RX Decryption Sequence Reset *Purpose:* Resets the last received SeqN bit independently for each key. *Register Values/Settings:* • RxCryptSeqReset[RxCryptId] When one of these bits is set to 1, the internally stored CryptSeqN bit for the corresponding key is reset to 0. *Note:* The internally stored CryptSeqN bits (4 for TX and 4 for RX) are always zero after reset (PowerOnReset or Baseband Reset).

10.79 0x58 to 0x59 – Received Bytes in Transparent Mode

Used for setting the number of bytes to receive in Transparent mode.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x58	R								
	init	0	0	0	0	0	0	0	0
	W	RxTransBytes							
	init	0	0	0	0	0	0	0	0
0x59	R								
	init	0	0	0	0	0	0	0	0
	W				RxTransBytes				
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x58 to 0x59

Bits	Mnemonic	Prop	Description
0-12	RxTransBytes	WO brst BbClk	Number of Data Bytes in Received MACFrame in Transparent Mode *Purpose:* Because in Transparent mode, the complete MACFrame is interpreted as a Data field and no information exists about how many bytes will follow, the number of bytes the chip should receive must be programmed before these packets can be received. These are all bytes between the Syncword and the Tail. *Register Values/Settings:* • Default Value = 0x0 *Note:* A value of all zeros is interpreted as 8192 bytes.

10.80 0x5A – RX ES and IS Address Matching, CRC1, CRC2, and ARQ

Used for enabling address matching for End Stations and Intermediate Stations, for enabling CRC1 checking on TimeB packets, and for enabling CRC2 checking on received Data, TimeB and Broadcast packets. Also, it is used to configure the format of a segmented address by setting the length of the DeviceID.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x5A	R								
	init	0	0	0	0	0	0	0	0
	W	RxAddrSegDevIdL		RxAddr Seg IsMode	RxAddr Seg EsMode	RxArqMode		RxCrc2 Mode	RxTimeB Crc1 Mode
	init	0	0	0	0	1	0	1	1

Write Only Fields

Field Properties for Register 0x5A

Bits	Mnemonic	Prop	Description
0	RxTimeBCrc1Mode	WO brst BbClk	CRC1 Mode for TimeB Packets *Purpose:* TimeB packets that have failed CRC1 checks can either be received by ignoring the failed CRC1 check, or a failed CRC1 check will cause the reception to terminate. The status of the CRC1 check is reported in the register RxCrc1Stat. *Register Values/Settings:* • NA_RxTimeBCrc1ModeOff_BC_C (0x0) Failed CRC1 check terminates reception. • NA_RxTimeBCrc1ModeOn_BC_C (0x1) Receive TimeB packets and ignore failed CRC1 check. • Default Value = 0x1

Field Properties for Register 0x5A (Continued)

Bits	Mnemonic	Prop	Description
1	RxCrc2Mode	WO brst BbClk	CRC2 Mode for Data, TimeB, and Broadcast Packets *Purpose:* Data, timeB, and Broadcast packets that have failed CRC2 checks can be received by ignoring the failed CRC2 check. *Register Values/Settings:* • NA_RxCrc2ModeTrigOff_BC_C (0x0) Ignore failed CRC2 check and trigger RxEnd interrupt. Receiver is stopped. • NA_RxCrc2ModeTrigOn_BC_C (0x1) RxEnd is only triggered when CRC2 check succeeds. When the check fails the receiver remains active to receive the next packet. When overflow occurs this will be ignored. • Default Value = 0x1
2-3	RxArqMode	WO brst BbClk	RX ARQ (Automatic Repeat Request) Mode for Data Packets *Purpose:* Selects the ARQ mode, including: • Ack should be sent as a reply to a received Data packet • Ack should not be sent when a Data packet is received • Ack should be sent when a CRC1 check succeeds • Ack should be sent when both a CRC1 and a CRC2 check succeeds. *Register Values/Settings:* • NA_RxArqModeNone_VC_C (0x0) ARQ is disabled and an Ack packet is not sent in response to a Data packet. • NA_RxArqModeCrc1_VC_C (0x1) The ARQ scheme is based on the CRC1 only. An Ack packet is sent in response to a Data packet only if CRC1 and address matching succeeded. • NA_RxArqModeCrc2_VC_C (0x2) The ARQ scheme is based on the CRC1 and CRC2. An Ack packet is sent in response to a Data packet only if CRC1, CRC2 , and address matching succeeded. • Default Value = 0x2 *This register must be defined before:* RxCmdStart = True *Usage:* Auto mode only.

Field Properties for Register 0x5A (Continued)

<table>
<tr><th>Bits</th><th>Mnemonic</th><th>Prop</th><th>Description</th></tr>
<tr><td>4</td><td>RxAddrSegEsMode</td><td>WO
brst
BbClk</td><td>End Station (ES) Address Matching

Purpose: Enables the address matching scheme for End Stations. Address matching for the destination station address as set in RamStaAddr1 is automatically disabled. ES matching succeeds when ES is enabled and the following is true:

• IG/UL bits = RamStaAddr1

• ISubnetId = 0

• SubnetID = RamStaAddr1

• DeviceID = RamStaAddr1

Register Values/Settings:
• 0 = Disable
• 1 = Enable
• Default Value = 0x0</td></tr>
<tr><td>5</td><td>RxAddrSegIsMode</td><td>WO
brst
BbClk</td><td>Intermediate Station (IS) Address Matching

Purpose: Enables the address matching scheme for Intermediate Stations. IS matching succeeds when IS is enabled and the following is true:

• IG/UL bits = RamStaAddr1

• ISubnetId = RamStaAddr1

Register Values/Settings:
• 0 = Disable
• 1 = Enable
• Default Value = 0x0</td></tr>
<tr><td>6-7</td><td>RxAddrSegDevIdL</td><td>WO
brst
BbClk</td><td>Segmented Address Format

Purpose: Configures the format of a segmented address by defining the length of the Device ID. Possible lengths include 2, 6, 10, and 14 bits. A segmented address is always 48 bits and can be configured as follows:

<table>
<tr><th>Device ID</th><th>Subnet ID</th><th>ISubnet ID</th><th>IG/UL</th></tr>
<tr><td>2</td><td>22</td><td>22</td><td>2</td></tr>
<tr><td>6</td><td>20</td><td>20</td><td>2</td></tr>
<tr><td>10</td><td>18</td><td>18</td><td>2</td></tr>
<tr><td>14</td><td>16</td><td>16</td><td>2</td></tr>
</table>

Register Values/Settings:
• Device ID = 2 bits (0X0)
• Device ID = 6 bits (0X1)
• Device ID = 10 bits (0X2)
• Device ID = 14 bits (0X3)</td></tr>
</table>

10.81 0x5B – RX Data, Brdcast, TimeB, Address Mode, and Ranging Pulses

Used for enabling the reception of Data packets, Broadcast packets, and TimeB packets. It is also used for setting the address mode for Data packets, as either Address Matching Mode or Promiscuous Mode. Finally, this register is used for setting the number of up and down pulses, which are used for determining the ToA average when performing ranging measurements.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x5B	R								
	init	0	0	0	0	0	0	0	0
	W	RangingPulses				Rx Addr Mode	Rx TimeB En	Rx Brdcast En	Rx DataEn
	init	0	1	0	1	1	1	1	1

Write Only Fields

Field Properties for Register 0x5B

Bits	Mnemonic	Prop	Description
0	RxDataEn	WO brst BbClk	Data Packet Reception *Purpose:* Enables the reception of Data packets. *Register Values/Settings:* • NA_RxDataOff_BC_C (0x0) Data packets are discarded. • NA_RxDataOn_BC_C (0x1) Data packets are received. • Default Value = 0x1 *This register must be defined before:* RxCmdStart = True *Usage:* Auto mode only.
1	RxBrdcastEn	WO brst BbClk	Broadcast Packet Reception *Purpose:* Enable the reception of Broadcast packets. *Register Values/Settings:* • NA_RxBrdcastOff_BC_C (0x0) Broadcast packets are discarded. • NA_RxBrdcastOn_BC_C (0x1) Broadcast packets are received. *This register must be defined before:* RxCmdStart = True *Usage:* Auto mode only.

Field Properties for Register 0x5B (Continued)

Bits	Mnemonic	Prop	Description
2	RxTimeBEn	WO brst BbClk	TimeB Packet Reception *Purpose:* Enables reception of TimeB packets. *Register Values/Settings:* • NA_RxTimeBOff_BC_C (0x0) TimeB packets are discarded. • NA_RxTimeBOn_BC_C (0x1) TimeB packets are received. *This register must be defined before:* RxCmdStart = True *Usage:* Auto mode only.
3	RxAddrMode	WO brst BbClk	Address Mode for Data Packets: Address Matching Mode or Promiscuous Mode *Purpose:* Sets the mode of address comparison. Data packets can be received independent of address matching (Promiscuous Mode), or with address matching (Address Matching Mode). *Register Values/Settings:* • NA_RxAddrModeOff_BC_C (0x0) Sets Promiscuous Mode The complete Data packet is received and receive interrupts are triggered independent of the address set in the received Data packet. • NA_RxAddrModeOn_BC_C (0x1) Sets Address Matching Mode A Data packet is received and receive interrupts are triggered only if the destination address set in the received Data packet matches the receiver station address. • Default Value = 0x1 *This register must be defined before:* RxCmdStart = True *Usage:* Auto mode only.

Field Properties for Register 0x5B (Continued)

Bits	Mnemonic	Prop	Description
4-7	RangingPulses	WO brst BbClk	Number of Up and Down Pulses Used for ToA Measurement Average *Purpose:* Sets the number of up and down ranging pulses used for determining the ToA (Time of Arrival) average measurement. *Register Values/Settings:* • NA_RangingPulses1_VC_C (0x0) Use 1 up and 1 down pulse for average. • NA_RangingPulses2_VC_C (0x1) Use 2 up and 2 down pulses for average. • NA_RangingPulses4_VC_C (0x2) Use 4 up and 4 down pulses for average. • NA_RangingPulses8_VC_C (0x3) Use 8 up and 8 down pulses for average. • NA_RangingPulses16_VC_C (0x4) Use 16 up and 16 down pulses for average. • NA_RangingPulses24_VC_C (0x5) Use 24 up and 24 down pulses for average. • NA_RangingPulses32_VC_C (0x6) Use 32 up and 32 down pulses for average. • NA_RangingPulses40_VC_C (0x7) Use 40 up and 40 down pulses for average. • NA_RangingPulses48_VC_C (0x8) Use 48 up and 48 down pulses for average. • NA_RangingPulses56_VC_C (0x9) Use 56 up and 56 down pulses for average. • NA_RangingPulses64_VC_C (0xA) Use 64 up and 64 down pulses for average. • Default Value = 0x5

10.82 0x5C – Delay Detection Tuning

Used for tuning the delay in the correlator.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x5C	R								
	init	0	0	0	0	0	0	0	0
	W				PulseDetDelay				
	init	0	0	0	0	0	1	0	1

Write Only Fields

Field Properties for Register 0x5C

Bits	Mnemonic	Prop	Description
0-4	PulseDetDelay	WO brst BbClk	Delay Tuning For Pulse Detection *Purpose:* Tunes the delay in the correlator. *Register Values/Settings:* • Default Value = 0x5

10.83 0x5D – Receive Bit Detector Controls (Bit Detectors)

Used for disabling the detection of up pulses (Upchirps) and/or down pulses (Downchirps), and for setting the required number of consecutive pulses needed to be outside of the gate center before a readjustment of the gate occurs.

		MSB				Bit Number			LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x5D	R								
	init	0	0	0	0	0	0	0	0
	W			Up Pulse Detect Dis	Down Pulse Detect Dis		GateAdjThreshold		
	init	0	0	0	0	0	1	1	1

Write Only Fields

Field Properties for Register 0x5D

Bits	Mnemonic	Prop	Description
0-2	GateAdjThreshold	WO brst BbClk	Gate Adjust Threshold *Purpose:* Because of clock drifting, the detected pulse can run out of center of the gate. This sets the required number of consecutive pulses outside of the gate center before a readjustment of the gate takes place. *Register Values/Settings:* • Default Value = 0x7 *This register must be defined before:* RxCmdStart = True
4	DownPulseDetectDis	WO brst BbClk	Disable Detection of Down Pulses *Purpose:* Disables the detection of down pulses (Downchirps) in the bit detector. *Register Values/Settings:* • 0 = Enable • 1 = Disable • Default Value = 0x0
5	UpPulseDetectDis	WO brst BbClk	Disable Detection of Up Pulses *Purpose:* Disables the detection of up pulses (Upchirps) in the bit detector. *Register Values/Settings:* • 0 = Enable • 1 = Disable • Default Value = 0x0

10.84 0x5E – Bit Detection Gate Size and Adjustment

Used for setting the size of the bit detection gate for unsynchronized state, for bit synchronization state, and for frame synchronized state. It is also used for enabling the adjustment of the detection gate in bit synchronization state and frame synchronization state.

		MSB				Bit Number			LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x5E	R								
	init	0	0	0	0	0	0	0	0
	W	GateAdj Frame syncEn	GateAdj Bitsync En	GateSizeFramesync		GateSizeBitsync		GateSizeUnsync	
	init	1	1	0	1	0	1	0	1

Write Only Fields

Field Properties for Register 0x5E

Bits	Mnemonic	Prop	Description
0-1	GateSizeUnsync	WO brst BbClk	Gate Size for Unsynchronized State *Purpose:* Sets the size of the detection gate in the baseband clock cycles for the unsynchronized state. *Register Values/Settings:* • NA_GateSize3Slots_VC_C (0x0) Sets gate size = 3 slots. • NA_GateSize5Slots_VC_C (0x1) Sets gate size = 5 slots. • NA_GateSize7Slots_VC_C (0x2) Sets gate size = 7 slots. • NA_GateSize9Slots_VC_C (0x3) Sets gate size = 9 slots. • Default Value = 0x1 *Note:* 1 slot = 31.25 ns (one baseband clock cycle). *This register must be defined before:* RxCmdStart = True

Field Properties for Register 0x5E (Continued)

Bits	Mnemonic	Prop	Description
2-3	GateSizeBitsync	WO brst BbClk	Gate Size for Bit Synchronization State *Purpose:* Sets the size of the detection gate in baseband clock cycles for the bit synchronization state. *Register Values/Settings:* • NA_GateSize3Slots_VC_C (0x0) Sets gate size = 3 slots. • NA_GateSize5Slots_VC_C (0x1) Sets gate size = 5 slots. • NA_GateSize7Slots_VC_C (0x2) Sets gate size = 7 slots. • NA_GateSize9Slots_VC_C (0x3) Sets gate size = 9 slots. • Default Value = 0x1 *Note:* 1 slot = 31.25 ns (one baseband clock cycle). *This register must be defined before:* RxCmdStart = True
4-5	GateSizeFramesync	WO brst BbClk	Gate Size for Frame Synchronization State *Purpose:* Sets the size of the detection gate in baseband clock cycles for the frame synchronization state. *Register Values/Settings:* • NA_GateSize3Slots_VC_C (0x0) Sets gate size = 3 slots. • NA_GateSize5Slots_VC_C (0x1) Sets gate size = 5 slots. • NA_GateSize7Slots_VC_C (0x2) Sets gate size = 7 slots. • NA_GateSize9Slots_VC_C (0x3) Sets gate size = 9 slots. • Default Value = 0x1 *Note:* 1 slot = 31.25 ns (one baseband clock cycle). *This register must be defined before:* RxCmdStart = True
6	GateAdjBitsyncEn	WO brst BbClk	Detection Gate Adjustment for Bit Synchronization State *Purpose:* Enables gate adjustment in bit synchronization state. *Register Values/Settings:* • 0 = Disable • 1 = Enable • Default Value = 0x1

Field Properties for Register 0x5E (Continued)

Bits	Mnemonic	Prop	Description
7	GateAdjFramesyncEn	WO brst BbClk	Detection Gate Adjustment for Frame Synchronization State *Purpose:* Enables gate adjustment in frame synchronization state. *Register Values/Settings:* • 0 = Disable • 1 = Enable • Default Value = 0x1 *Note:* GateAdjFramesyncEn must be disabled for Ranging.

10.85 0x5F – Bit Synchronization/Unsynchronization Thresholds

Used for setting the threshold (number of consecutive detected chirp pulses) to enter bit synchronization state from the unsynchronized state, as well as for setting the threshold (number of consecutive lost chirp pulses) to enter the unsynchronized state from bit synchronization state.

Note: The frame synchronization state is reached after the SyncWord has been received.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x5F	R								
	init	0	0	0	0	0	0	0	0
	W		LeaveBitsyncThreshold				Go2BitsyncThreshold		
	init	0	1	1	0	0	0	1	0

Write Only Fields

Field Properties for Register 0x5F

Bits	Mnemonic	Prop	Description
0-2	Go2BitsyncThreshold	WO brst BbClk	Threshold for Entering Bit Synchronization *Purpose:* Sets the required number of consecutive chirp pulses detected in the unsynchronized state to go to bit synchronization state. *Register Values/Settings:* • Default Value = 0x2 *This register must be defined before:* RxCmdStart = True
4-6	LeaveBitsyncThreshold	WO brst BbClk	Threshold for Leaving Bit Synchronization *Purpose:* Sets the required number of consecutive non-detected chirp pulses (lost pulses) in bit synchronization state to return to the unsynchronized state. *Register Values/Settings:* • Default Value = 0x6 *This register must be defined before:* RxCmdStart = True

10.86 0x60 – Real Time Clock TimeB Transmission Delay Adjustment

Used for adjusting the RTC values before transmission due to hardware delays inside the transmitter.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x60	R								
	init	0	0	0	0	0	0	0	0
	W	RtcTimeBTxAdj							
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x60

Bits	Mnemonic	Prop	Description
0	RtcTimeBTxAdj	WO brst BbClk	Real Time Clock TimeB Transmission Delay Adjustment *Purpose:* Before transmitting, the Real Time Clock control value is adjusted to compensate for transmitter delays. • NA_MacRtcTimeBTxAdj1M2Ary_IC_C (0x05) Adjustment for 1 Msymbols 2Ary. • NA_MacRtcTimeBTxAdj1M4Ary_IC_C (0x03) Adjustment for 1 Msymbols 4Ary. • NA_MacRtcTimeBTxAdj1M2AryFec_IC_C (0x07) Adjustment for 1 Msymbols 2Ary FEC. • NA_MacRtcTimeBTxAdj1M4AryFec_IC_C (0x04) Adjustment for 1 Msymbols 4Ary FEC. • NA_MacRtcTimeBTxAdj500k2Ary_IC_C (0x09) Adjustment for 500 ksymbols 2Ary. • NA_MacRtcTimeBTxAdj500k4Ary_IC_C (0x07) Adjustment for 500 ksymbols 4Ary. • NA_MacRtcTimeBTxAdj500k2AryFec_IC_C (0x0F) Adjustment for 500 ksymbols 2Ary FEC. • NA_MacRtcTimeBTxAdj500k4AryFec_IC_C (0x0D) Adjustment for 500 ksymbols 4Ary FEC. • Default Value = 0x0 *Note:* This value is added to the RTC value after reading due to the delay in the transmitter while shifting out this value.

10.87 0x61 – Real Time Clock TimeB Reception Delay Adjustment

Used for adjusting the RTC values after reception due to hardware delays inside the receiver.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x61	R								
	init	0	0	0	0	0	0	0	0
	W	RtcTimeBRxAdj							
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x61

Bits	Mnemonic	Prop	Description
0-7	RtcTimeBRxAdj	WO brst BbClk	Real Time Clock TimeB Reception Delay Adjustment *Purpose:* Adjusts the Real Time Clock value after reception to compensate for receiver delays. *Register Values/Settings:* • NA_MacRtcTimeBRxAdj1M2Ary_IC_C (0x04) Adjustment for 1 Msymbols 2Ary. • NA_MacRtcTimeBRxAdj1M4Ary_IC_C (0x08) Adjustment for 1 Msymbols 4Ary. • NA_MacRtcTimeBRxAdj1M2AryFec_IC_C (0x09) Adjustment for 1 Msymbols 2Ary FEC. • NA_MacRtcTimeBRxAdj1M4AryFec_IC_C (0x0A) Adjustment for 1 Msymbols 4Ary FEC. • NA_MacRtcTimeBRxAdj500k2Ary_IC_C (0x08) Adjustment for 500 ksymbols 2Ary. • NA_MacRtcTimeBRxAdj500k4Ary_IC_C (0x0B) Adjustment for 500 ksymbols 4Ary. • NA_MacRtcTimeBRxAdj500k2AryFec_IC_C (0x0C) Adjustment for 500 ksymbols 2Ary FEC. • NA_MacRtcTimeBRxAdj500k4AryFec_IC_C (0x0D) Adjustment for 500 ksymbols 4Ary FEC. • Default Value = 0x0 *Note:* This value is added to the RTC value after reading due to delay in the transmitter while shifting out this value.

10.88 0x62 – Real Time Clock

Used for setting or getting the value of the Real Time Clock and for enabling Auto mode for TimeB packets.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x62	R								
	init	0	0	0	0	0	0	0	0
	W	Internal Use Only			Rtc TimeB Auto Mode			Rtc CmdRd	Rtc CmdWr
	init	0	0	0	0	0	0	0	0

Write Only Fields

Field Properties for Register 0x62

Bits	Mnemonic	Prop	Description
0	RtcCmdWr	WO brst strb BbClk	Set RamRtcReg Value in Real Time Clock *Purpose:* After writing the desired RTC value to RamRtcReg, this register transfers the value into the RTC circuit. This requires 62 µs after the command has been executed before the RTC is updated with the value from RamRtcReg. *Register Values/Settings:* • 0 = Ignore • 1 = Set Value • Default Value = 0x0 *Note:* The commands must not be used after a transmission has been initiated and while the transmit cycle has not ended. Furthermore, this command must not be used after a reception has been started and while the receive cycle has not ended.

Field Properties for Register 0x62 (Continued)

Bits	Mnemonic	Prop	Description
1	RtcCmdRd	WO brst strb BbClk	Set Real Time Clock Value in RtcReg *Purpose:* Gets the value of the internal Real Time Clock and writes it into RamRtcReg, which is the RAM Real Time Clock buffer. This requires 31 µs after the command has been executed before RamRtcReg is updated with the RTC value. *Register Values/Settings:* • 0 = Ignore • 1 = Set Value • Default Value = 0x0 *Note:* The commands must not be used after a transmission has been initiated and while the transmit cycle has not ended. Furthermore, this command must not be used after a reception has been started and while the receive cycle has not ended.
4	RtcTimeBAutoMode	WO brst BbClk	Real Time Clock Auto Mode for TimeB Packets *Purpose:* Automatically sets the RTC values in TimeB packets for transmission and automatically stores the RTC values of received TimeB packets in the RTC. Otherwise, the RTC values in TimeB packets for transmission are taken from RAM in RamRtcTx and the RTC values in received TimeB packets is stored in RamRtcRx. *Register Values/Settings:* • NA_RtcTimeBAutoModeOff_BC_C(0x0) The value of RamRtcTx is transmitted in the RTC field of the TimeB packet, while the RTC value in a received TimeB packet is stored in RamRtcRx. • NA_RtcTimeBAutoModeOn_BC_C(0x1) The RTC value for a transmitted TimeB packet is taken from the Real Time Clock, while the RTC value from a received TimeB is automatically stored in the Real Time Clock. • Default Value = 0x0

10.89 0x63 – AGC Amplitude

Used in the alternative AGC to change gain continuously so that the desired amplitude is reached.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x63	R								
	init	0	0	0	0	0	0	0	0
	W				AgcAmplitude				
	init	0	0	0	0	1	1	0	0

Write Only Fields

Field Properties for Register 0x63

Bits	Mnemonic	Prop	Description
0-4	AgcAmplitude	WO	AGC Amplitude *Purpose:* Gain is changed continuously to reach the required amplitude. *Register Values/Settings:* • Default Value = 0x0

10.90 0x64 – Alternative AGC and AGC Range Offset

Used for switching between standard AGC and alternate AGC and for setting the value in AgcRangeOffset.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x64	R								
	init	0	0	0	0	0	0	0	0
	W	Use Alternative Agc				AgcRangeOffset			
	init	0	0	0	0	1	0	1	0

Write Fields

Field Properties for Register 0x64

Bits	Mnemonic	Prop	Description
0-3	AgcRangeOffset	WO	AGC Range Offset *Purpose:* Sets a value in AgcRangeOffset so that the AGC is temporarily halted when: | Mean Value - Middle | > AgcRangeOffset *Register Values/Settings:* • Default Value = 0x0
1	UseAlternativeAgc	WO	Use Alternative AGC *Purpose:* Switches between the standard and alternative AGC. *Register Values/Settings:* • 0 = Disable • 1 = Enable • Default Value = 0x0 *Note:* Do not switch between AGCs when the receiver is running.

10.91 0x65 to 0x7C – Reserved Registers

Registers between 0x65 and 0x7C inclusive are reserved. The default value for all fields in these registers is 0x0.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x65	R								
	init	0	0	0	0	0	0	0	0
	W								
	init	0	0	0	0	0	0	0	0
■ ■ ■									
0x7C	R								
	init	0	0	0	0	0	0	0	0
	W								
	init	0	0	0	0	0	0	0	0

10.92 0x7D – Internal Use Only

Nanotron Internal Use Only. Must be set to 0.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x7D	R	Internal Use Only							
	init	0	0	0	0	0	0	0	0
	W	Internal Use Only							
	init	0	1	0	1	0	0	0	0

10.93 0x7E – Internal Use Only

Nanotron Internal use only. Must be set to 0.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x7E	R	Internal Use Only							
	init	0	0	0	0	0	0	0	0
	W								
	init	0	0	0	0	0	0	0	0

10.94 0x7F – Internal Use Only

Nanotron Internal use only. Must be set to 0.

		MSB			Bit Number				LSB
Offset	R/W	7	6	5	4	3	2	1	0
0x7F	R	Internal Use Only							
	init	0	0	0	0	0	0	0	0
	W								
	init	0	0	0	0	0	0	0	0

11 Memory Map of RAM Locations

The following tables describe the memory locations of the BBRAM based on the Buffer Configuration Mode of the BBRAM.

Note: All registers in Baseband RAM are both readable and writable.

11.1 Auto/Duplex Mode

11.1.1 Auto/Duplex Page 0

Table 34: Auto/Duplex page 0 memory locations

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x80	0x85	R	RamStaAddr0							
		W								
0x86	0x87	R								
		W								
0x88	0x8D	R	RamStaAddr1							
		W								
0x8E	0x8F	R								
		W								
0x90	0x95	R	RamTxDstAddr							
		W								
0x96	0x97	R								
		W								
0x98	0x98	R	RamTxLength							
		W								
0x99	0x99	R	RamTx LCh	RamTx SeqN	RamTx FragC	RamTxLength				
		W								
0x9A	0xA7	R								
		W								
0xA8	0xAD	R	RamRxDstAddr							
		W								
0xAE	0xAF	R								
		W								
0xB0	0xB5	R	RamRxSrcAddr							
		W								
0xB6	0xB7	R								
		W								

Table 34: Auto/Duplex page 0 memory locations (Continued)

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0xB8	0xB8	R	RamRxLength							
		W								
0xB9	0xB9	R	RamRx-LCh	RamRx-SeqN	RamRx-FragC	RamRxLength				
		W								
0xBA	0xDF	R								
		W								
0xE0	0xE5	R	RamRtcTx							
		W								
0xE6	0xE7	R								
		W								
0xE8	0xED	R	RamRtcRx							
		W								
0xEE	0xEF	R								
		W								
0xF0	0xFF	R	RamRtcReg							
		W								

11.1.2 Auto/Duplex Page 1

Table 35: Auto/Duplex page 1 memory locations

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
Register Space		R								
		W								
0x180	0x18F	R	RamTxRxCryptKey							
		W								
0x190	0x1BF	R								
		W								
0x1C0	0x1CF	R	RamTxCryptClock							
		W								
0x1D0	0x1DF	R								
		W								
0x1E0	0x1EF	R	RamRxCryptClock							
		W								

Table 35: Auto/Duplex page 1 memory locations (Continued)

Offset			MSB							LSB
			Bit Number							
From	To	R/W	7	6	5	4	3	2	1	0
0x1F0	0x1FF	R								
		W								

11.1.3 Auto/Duplex Page 2

Table 36: Auto/Duplex page 2 memory locations

Offset			MSB							LSB
			Bit Number							
From	To	R/W	7	6	5	4	3	2	1	0
Register Space		R								
		W								
0x280	0x2FF	R	RamRxBuffer							
		W								

11.1.4 Auto/Duplex Page 3

Table 37: Auto/Duplex page 2 memory locations

		MSB							LSB
		Bit Number							
Offset	R/W	7	6	5	4	3	2	1	0
Register Space		R							
		W							
0x380	0x3FF	R	RamTxBuffer						
		W							

11.2 Auto/Simplex Mode

11.2.1 Auto/Simplex Page 0

Same as *Auto/Duplex Page 0* on page 207.

11.2.2 Auto/Simplex Page 1

Same as *Auto/Duplex Page 1* on page 208.

11.2.3 Auto/Simplex Pages 2 and 3

Table 38: Auto/Simplex pages 2 and 3 memory locations

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x280	0x2FF	R	RamTxRxBuffer							
		W								
0x380	0x3FF	R	RamTxRxBuffer							
		W								

11.3 Transparent/Duplex Mode

11.3.1 Transparent/Duplex Pages 0 and 1

Table 39: Transparent/Duplex pages 0 and 1 memory locations

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x080	0x0FF	R	RamRxTransBuffer							
		W								
0x180	0x1FF	R	RamRxTransBuffer							
		W								

11.3.2 Transparent/Duplex Pages 2 and 3

Table 40: Transparent/Duplex pages 2 and 3 memory locations

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x280	0x2FF	R	RamTxTransBuffer							
		W								
0x380	0x3FF	R	RamTxTransBuffer							
		W								

11.4 Transparent/Simplex Mode

Transparent/Simplex Pages 0, 1, 2, and 3

Table 41: Transparent/Simplex pages 0, 1, 2, and 3 memory locations

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x080	0x0FF	R	RamTxRxTransBuffer							
		W								
0x180	0x1FF	R	RamTxRxTransBuffer							
		W								
0x280	0x2FF	R	RamTxRxTransBuffer							
		W								
0x380	0x3FF	R	RamTxRxTransBuffer							
		W								

Intentionally Left Blank

12 RAM Locations Descriptions: 0x80 to 0x3FF

12.1 Auto/Duplex [Pg 0] 0x80 to 0x85 – Source Station Address 0

Used to buffer the 48 bit address of the source station based on the IEEE standard addressing convention. The first 24 bits correspond to the Organizationally Unique Identifier assigned by IEEE, while the second 24 bits are administered locally. This address is set in the MACFrame of a Data, Brdcast, TimeB, and Reg2S packet. For more details about address formatting, refer to the *nanoNET System Specifications*.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x80	0x85	R	RamStaAddr0							
		W								

Read/Write

Field Properties for Register 0x80 to 0x85

Bits	Mnemonic	Prop	Description

0-47	RamStaAddr0	R/W
		brst
		BbClk
		RAM
			Station Address Based on IEEE Addressing Convention
			Purpose: Stores a 48 bit universally administered IEEE address of the source station.
			Register Values/Settings:
			• If this convention is used, then set the first two bits of this field as follows:
			  • RamStaAddr0[0] = 0
			  • RamStaAddr0[1] = 0
			• Default Value = 0x0
			Note: It is not mandatory to use this convention for addressing.

12.2 Auto/Duplex [Pg 0] 0x86 to 0x87 – Reserved

These RAM locations are reserved. All bits must be set to 0x0.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x86	0x87	R	Reserved							
		W								

12.3 Auto/Duplex [Pg 0] 0x88 to 0x8D – Source Station Address 1

Used to buffer the 48 bit address of the source station based on a configuration locally administered by the assignee. This address is set in the MACFrame of a Data, Brdcast, TimeB, or Reg2S packet. For more details about address formatting, refer to the *nanoNET System Specifications*.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x88	0x8D	R	RamStaAddr1							
		W								

Read/Write

Field Properties for Register 0x88 to 0x8D

Bits	Mnemonic	Prop	Description

0-47	RamStaAddr1	R/W
		brst
		BbClk
		RAM
			Station Address Based on Locally Administered Configuration
			Purpose: Stores the second address for the station, a 48 bit locally administered address of the source station.
			Register Values/Settings:
			• If this convention is used, then set the first two bits of this field as follows:
			  • RamStaAddr1[0] = 0
			  • RamStaAddr1[1] = 1
			Note: It is not mandatory to use this convention for addressing.

12.4 Auto/Duplex [Pg 0] 0x8E to 0x8F – Reserved

These RAM locations are reserved. All bits must be set to 0x0.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x86	0x87	R	Reserved							
		W								

12.5 Auto/Duplex [Pg 0] 0x90 to 0x95 – TX Destination Address

Used to buffer a 48 bit address of the destination station to be set in the MACFrame of a Data or Brdcast packet that is to be transmitted. This destination address is used in all packet types, except the TimeB packet. In TimeB packets, this RAM location contains a Real Time Clock value. For more details about destination addresses, refer to the *nanoNET System Specifications.*

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x90	0x95	R	RamTxDstAddr							
		W								

Read/Write

Field Properties for Register 0x00

Bits	Mnemonic	Prop	Description
0-47	RamTxDstAddr	R/W brst BbClk RAM	Transmit Destination Address *Purpose:* Stores the 48 bit address of the destination station for a Data packet that is to be transmitted, as well as the 48 bit broadcast/ multicast address of a Brdcast packet to be transmitted. *Register Values/Settings:* • Default Value = 0x0 *This register must be defined before:* TxCmdStart = True. *Usage:* Auto mode only.

12.6 Auto/Duplex [Pg 0] 0x96 to 0x97 – Reserved

These RAM locations are reserved. All bits must be set to 0x0.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x96	0x97	R	Reserved							
		W								

12.7 Auto/Duplex [Pg 0] 0x98 to 0x99 – TX Data Length and Bits for SW Usage

Used to set the length of the data field in packets to be transmitted, as well as to set three bits that are available for use by software.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x98	0x98	R	RamTxLength							
		W								
0x99	0x99	R	TX Transparent Bits for SW usage			RamTxLength				
		W								

Read/Write

Field Properties for Register 0x98 to 0x99

Bits	Mnemonic	Prop	Description
0-12	RamTxLength	R/W brst BbClk RAM	Data Field Length of a Packet to be Transmitted *Purpose:* Sets the number of bytes of the Data field of Data, Brdcast, and TimeB packets. This field will also be transmitted in a Req2s packet when using 3-way handshaking. *Register Values/Settings:* • Default Value = 0x0 *This register must be defined before:* TxCmdStart = True. *Usage:* Auto mode only.
13-15	RamTxFragC	R/W brst BbClk RAM	These bits are transparent for the nanoLOC. There are only loaded from RAM together with the TxLength field and sent in the MACFrame. On the receiver side they can be read from the corresponding RX field called “RX Transparent Bits for SW usage.” In several applications these bits were used on software level to implement functionalities such as Link Control Channel, a sequential numbering scheme, or a packet fragmentation scheme. *See also: Auto/Duplex [Pg 0] 0xB8 to 0xB9 – RX Data Length and Bits for SW Usage* on page 225. *Usage:* Auto mode only.

12.8 Auto/Duplex [Pg 0] 0x9A to 0xA7 – Reserved

These RAM locations are reserved. All bits must be set to 0x0.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x9A	0xA7	R	Reserved							
		W								

12.9 Auto/Duplex [Pg 0] 0xA8 to 0xAD – RX Destination Address

Used to buffer the 48 bit address of the destination address field provided in the MACFrame of a received Data or Brdcast packet. For more details about destination addresses, refer to the *nanoNET System Specifications.*

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0xA8	0xAD	R	RamRxDstAddr							
		W								

Read/Write

Field Properties for Register 0xA8 to 0xAD

Bits	Mnemonic	Prop	Description
0-47	RamRxDstAddr	R/W brst BbClk RAM	Receive Destination Address *Purpose:* Stores the destination address from received Data and Brdcast packets. It allows for the retrieval of the destination address when in promiscuous mode in order to compare broad-cast/multicast addresses (Brdcast packets). *Register Values/Settings:* • Default Value = 0x0 *Note:* Valid when: • RxHeaderEnd event is triggered • RxCrc1 == RxCrc1Succ • RxPacketType == RxPacketTypeData | RxPacketTypeBrdcast *Usage:* Auto mode only.

12.10 Auto/Duplex [Pg 0] 0xAE to 0xAF – Reserved

These RAM locations are reserved. All bits must be set to 0x0.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0xAE	0xAF	R	Reserved							
		W								

12.11 Auto/Duplex [Pg 0] 0xB0 to 0xB5 – RX Source Address

Used to buffer the 48 bit address of the source address field provided in the MACFrame of a received Data or Brdcast packet. For more details about destination addresses, refer to the *nanoNET System Specifications.*

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0xB0	0xB5	R	RamRxSrcAddr							
		W								

Read/Write

Field Properties for Register 0xB0 to B5

Bits	Mnemonic	Prop	Description
0-7	RamRxSrcAddr	R/W brst BbClk RAM	Receive Source Address *Purpose:* Stores the source address of the received Data or Brdcast packet. *Register Values/Settings:* • Default Value = 0x0 *Note:* Valid when: • RxHeaderEnd event is triggered • RxCrc1 == RxCrc1Succ *Usage:* Auto mode only.

12.12 Auto/Duplex [Pg 0] 0xB6 to 0xB7 – Reserved

These RAM locations are reserved. All bits must be set to 0x0.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0xB6	0xB7	R	Reserved							
		W								

12.13 Auto/Duplex [Pg 0] 0xB8 to 0xB9 – RX Data Length and Bits for SW Usage

Used to store a value which indicates the length of the data field in received packets, as well as to store three bits that are available for use by software.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0xB8	0xB8	R	RamRxLength							
		W								
0xB9	0xB9	R	RX Transparent Bits for SW usage			RamRxLength				
		W								

Read/Write

Field Properties for Register 0xB8 to 0xB9

Bits	Mnemonic	Prop	Description
0-12	RamRxLength	R/W brst BbClk RAM	Data Field Length of Received Packet *Purpose:* Stores the length (number of bytes) of the data field of Data, Brdcast, TimeB, Req2S, and Clr2S packets. *Note:* Valid when: • RxHeaderEnd event is triggered • RxCrc1 == RxCrc1Succ *Usage:* Auto mode only
13-15	RamRxFragC	R/W brst BbClk RAM	These bits are transparent for the nanoLOC. They are only stored to RAM together with the RxLength field received in the MACFrame. In several applications these bits were used on software level to implement functionalities such as Link Control Channel, a sequential numbering scheme, or a packet fragmentation scheme. *Usage:* Auto mode only.

12.14 Auto/Duplex [Pg 0] 0xBA to 0xDF – Reserved

These RAM locations are reserved. All bits must be set to 0x0.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0xBA	0xDF	R	Reserved							
		W								

12.15 Auto/Duplex [Pg 0] 0xE0 to 0xE5 – TX Real Time Clock Buffer

Used to temporarily buffer the 48 bit value of the Real Time Clock to prepare time beacon (TimeB) packets for transmission.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0xE0	0xE5	R	RamRtcTx							
		W								

Read/Write

Field Properties for Register 0xE0 to 0xE5

Bits	Mnemonic	Prop	Description
0-47	RamRtcTx	R/W brst BbClk	TX Real Time Clock Value Buffer *Purpose:* Stores the value of the Real Time Clock for use by TimeB packets to be transmitted.

12.16 Auto/Duplex [Pg 0] 0xE6 to 0xE7 – Reserved

These RAM locations are reserved. All bits must be set to 0x0.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0xE6	0xE7	R	Reserved							
		W								

12.17 Auto/Duplex [Pg 0] 0xE8 to 0xED – RX Real Time Clock Buffer

Used to temporarily buffer the value of the Real Time Clock from a received time beacon packet (TimeB).

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0xE8	0xED	R	RamRtcRx							
		W								

Read/Write

Field Properties for Register 0xE8 to ED

Bits	Mnemonic	Prop	Description
0-47	RamRtcRx	R/W brst BbClk	RX Real Time Clock Value Buffer *Purpose:* Stores the value of the Real Time Clock that is provided in the MACFrame of a received TimeB packet.

12.18 Auto/Duplex [Pg 0] 0xEE to 0xEF – Reserved

These RAM locations are reserved. All bits must be set to 0x0.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0xEE	0xEF	R	Reserved							
		W								

12.19 Auto/Duplex [Pg 0] 0xF0 to 0xFF – RX Real Time Clock

Used to buffer the 48 bit value of the internal Real Time Clock for use by software to read or write the RTC value.

Offset		MSB	Bit Number							LSB
From	To	R/W	7	6	5	4	3	2	1	0
0xF0	0xFF	R	RamRtcReg							
		W								

Read/Write

Field Properties for Register 0xF0 to 0xFF

Bits	Mnemonic	Prop	Description
0-47	RtcReg	R/W brst BbClk	RAM Real Time Clock Register *Purpose:* Buffer register for reading or writing the 48 bit internal Real Time Clock value. Since the Real Time Clock is updated every 30.517578125 µs, it is not directly accessible by the user. *Note:* RtcCmdRd reads the value of the Real Time Clock to this buffer. RtcCmdWr writes a value in this buffer to the Real Time Clock.

12.20 Auto/Duplex [Pg 1] 0x100 to 0x17F – Register (Mirrored)

The Register (0x00 to 0x7F) is mirrored to RAM locations 0x100 to 0x17F.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x100	0x17F	R	Mirrored Register (0x00 to 0x7F)							
		W								

12.21 Auto/Duplex [Pg 1] 0x180 to 0x1BF – Encryption Key

Used to store the four 128 bit encryption keys used for cipher generation.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x180	0x18F	R	RamTxRxCryptKey[0]							
		W								
0x190	0x19F	R	RamTxRxCryptKey[1]							
		W								
0x1A0	0x1AF	R	RamTxRxCryptKey[2]							
		W								
0x1B0	0x1BF	R	RamTxRxCryptKey[3]							
		W								

Read/Write

Field Properties for Register 0x180 to 18F

Bits	Mnemonic	Prop	Description
Per key:0-127 Total:0-511	RamTxRxCryptKey	R/W brst BbClk	Encryption keys *Purpose:* Stores the four 128 bit encryption keys used as inputs of the cipher stream generator. *Register Values/Settings:* • RamTxRxCryptKey[CryptId], CryptId = 0..3 *This register must be defined before:* TxCmdStart = True or RxCmdStart = True. *Usage:* Auto mode only.

12.22 Auto/Duplex [Pg 1] 0x1C0 to 0x1CF – TX Encryption Clock Value

Used to store the four 32 bit clock values used for cipher generation (encryption).

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x1C0	0x1C3	R	RamTxCryptClock[0]							
		W								
0x1C4	0x1C7	R	RamTxCryptClock[1]							
		W								
0x1C8	0x1CB	R	RamTxCryptClock[2]							
		W								
0x1CC	0x1CF	R	RamTxCryptClock[3]							
		W								

Read/Write

Field Properties for Register 0x1C0 to 1CF

Bits	Mnemonic	Prop	Description
Per value:0-31 Total: 0-127	RamTxCryptClock	R/W brst BbClk RAM	Encryption Clock Value *Purpose:* Stores the four publicly known 32 bit clock values used as inputs of the cipher stream generator for encryption. *Register Values/Settings:* • RamTxCryptClock[CryptId], CryptId = 0…3. *This register must be defined before:* TxCmdStart = True. *Usage:* Auto mode only.

12.23 Auto/Duplex [Pg 1] 0x1D0 to 0x1DF – Reserved

These RAM locations are reserved. All bits must be set to 0x0.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x1D0	0x1DF	R	Reserved							
		W								

12.24 Auto/Duplex [Pg 1] 0x1E0 to 0x1EF – RX Decryption Clock Value

Used to store the four 32 bit clock values used as input for cipher generation (decryption).

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x1E0	0x1E3	R	RamRxCryptClock[1]							
		W								
0x1E4	0x1E7	R	RamRxCryptClock[1]							
		W								
0x1E8	0x1EB	R	RamRxCryptClock[2]							
		W								
0x1EC	0x1EF	R	RamRxCryptClock[3]							
		W								

Read/Write

Field Properties for Register 0x1E0 to 1EF

Bits	Mnemonic	Prop	Description
Per value:0-31 Total:0-127	RamRxCryptClock	R/W brst BbClk RAM	Receive Decryption Clock *Purpose:* Stores the four publicly known 32 bit clock values used as inputs of the cipher stream generator for decryption. *Register Values/Settings:* • RxCryptClock[CryptId], CryptId = 0…3. *This register must be defined before:* RxCmdStart = True.

12.25 Auto/Duplex [Pg 1] 0x1F0 to 0x1FF – Reserved

These RAM locations are reserved. All bits must be set to 0x0.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x1F0	0x1FF	R	Reserved							
		W								

12.26 Auto/Duplex [Pg 1] 0x200 to 0x27F – Register (Mirrored)

The Register (0x00 to 0x7F) is mirrored to RAM locations 0x200 to 0x27F.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x200	0x27F	R	Mirrored Register (0x00 to 0x7F)							
		W								

12.27 Auto/Duplex [Pg 2] 0x280 to 0x2FF – RX Data Buffer

Used to store 128 bytes (1024 bits) of data in two buffers of 64 bytes each from a received Data packet.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x280	0x2FF	R	RamRxBuffer							
		W								

Read/Write

Field Properties for Register 0x280 to 2FF

Bits	Mnemonic	Prop	Description
0-1023	RamRxBuffer	R/W brst BbClk RAM	128 Byte RX Data Buffer *Purpose:* Stores in two buffers of 64 bytes each the received data from Data packets. *Note:* Data in buffer are valid when the RxBufferRdy event is triggered.

12.28 Auto/Duplex [Pg 3] 0x380 to 0x3FF – TX Data Buffer

Used to store 128 bytes (1024 bits) of data in two buffers of 64 bytes each for a Data packet to be transmitted.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0x380	0x3FF	R	RamTxBuffer							
		W								

Read/Write

Field Properties for Register 0x00

Bits	Mnemonic	Prop	Description
0-1023	RamTxBuffer	R/W brst BbClk RAM	128 Byte TX Data Buffer *Purpose:* Stores in two buffers of 64 bytes each the data to be set in of a Data packet that is to be transmitted.

12.29 Auto/Simplex [Pg 0] 0x80/0x0FF – Same as Auto/Duplex [Pg 0]

Auto/Simplex Page 0 is identical to Auto/Duplex Page 0, which is replicated below.

Table 42: Auto/Simplex page 0 memory locations

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
Register Space		R	Mirrored Register (0x00 to 0x7F)							
		W								
0x80	0x85	R	RamStaAddr0							
		W								
0x86	0x87	R	Reserved							
		W								
0x88	0x8D	R	RamStaAddr1							
		W								
0x8E	0x8F	R	Reserved							
		W								
0x90	0x95	R	RamTxDstAddr							
		W								
0x96	0x97	R	Reserved							
		W								
0x98	0x98	R	RamTxLength							
		W								
0x99	0x99	R	TX Transparent Bits for SW usage			RamTxLength				
		W								
0x9A	0xA7	R	Reserved							
		W								
0xA8	0xAD	R	RamRxDstAddr							
		W								
0xAE	0xAF	R	Reserved							
		W								
0xB0	0xB5	R	RamRxSrcAddr							
		W								

Table 42: Auto/Simplex page 0 memory locations (Continued)

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
0xB6	0xB7	R	Reserved							
		W								
0xB8	0xB8	R	RamRxLength							
		W								
0xB9	0xB9	R	RX Transparent Bits for SW usage			RamRxLength				
		W								
0xBA	0xDF	R	Reserved							
		W								
0xE0	0xE5	R	RamRtcTx							
		W								
0xE6	0xE7	R	Reserved							
		W								
0xE8	0xED	R	RamRtcRx							
		W								
0xEE	0xEF	R	Reserved							
		W								
0xF0	0xFF	R	RamRtcReg							
		W								

12.30 Auto/Simplex [Pg 1] 0x180/0xEFF – Same as Auto/Duplex [Pg 1]

Auto/Simplex Page 1 is identical to Auto/Duplex Page 1, which is replicated below.

Table 43: Auto/Duplex page 1 memory locations

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
Register Space		R	Mirrored Register (0x00 to 0x7F)							
		W								
0x180	0x18F	R	RamTxRxCryptKey							
		W								
0x190	0x1BF	R	Reserved							
		W								
0x1C0	0x1CF	R	RamTxCryptClock							
		W								
0x1D0	0x1DF	R	Reserved							
		W								
0x1E0	0x1EF	R	RamRxCryptClock							
		W								
0x1F0	0x1FF	R	Reserved							
		W								

12.31 Auto/Simplex [Pg 2/3] 0x280 to 0x3FF – TX/RX Data Buffer

Used for storing sequentially transmit and receive data, where the entire 256 bytes are divided into two 128 byte (2048 bit) buffers as a combined receive/transmit buffer. As this is Simplex mode, the transmit and receive buffer operations are dependent on each other, in that the receive operation must be completed before the transmit operation can be initiated. Consequently, the buffer for the RX data and for the TX data is double the size, in this case, 256 bytes.

Offset		MSB	Bit Number							LSB
From	To	R/W	7	6	5	4	3	2	1	0
Register Space		R	Mirrored Register (0x00 to 0x7F)							
		W								
0x280	0x2FF	R	RamTxRxBuffer							
		W								
Register Space		R	Mirrored Register (0x00 to 0x7F)							
		W								
0x380	0x3FF	R	RamTxRxBuffer							
		W								

Read/Write

Field Properties for Register 0x280 to 0x3FF

Bits	Mnemonic	Prop	Description
0-2047	RamTxRxBuffer	R/W brst BbClk RAM	256 Byte Shared Transmit/Receive Data Buffer *Purpose:* Stores both received data and data for transmission (sequentially) in a combined RX/TX buffer.

12.32 Transparent/Duplex Page [Pg 0/1] 0x080 to 0x1FF – RX Data Buffer

Used for storing received data where the entire 256 bytes is divided into two 128 byte buffers which are used to save data from a received packet. As this is Transparent mode, software is responsible fro maintaining important MACFrame variables. As this is Duplex mode, received data can saved to this buffer while simultaneously data to be transmitted can be written to RamTxTransBuffer.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
Register Space		R	Mirrored Register (0x00 to 0x7F)							
		W								
0x080	0x0FF	R	RamRxTransBuffer							
		W								
Register Space		R	Mirrored Register (0x00 to 0x7F)							
		W								
0x180	0x1FF	R	RamRxTransBuffer							
		W								

Read/Write

Field Properties for Register 0x080 to 0x1FF

Bits	Mnemonic	Prop	Description
0-2047	RamRxTransBuffer	R/W brst BbClk RAM	256 Byte Receive Buffer *Purpose:* Stores the received data in two 128 byte buffers.

12.33 Transparent/Duplex Page [Pg 2/3] 0x280 to 0x3FF – TX Data Buffer

Used for storing data to be transmitted, where the entire 256 bytes is divided into two 128 byte buffers which are used for writing the data for transmission. As this is Transparent mode, software is responsible fro maintaining important MACFrame variables. As this is Duplex mode, data for transmission can written to this buffer while simultaneously received data can be saved to RamRxTransBuffer.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
Register Space		R	Mirrored Register (0x00 to 0x7F)							
		W								
0x280	0x2FF	R	RamTxTransBuffer							
		W								
Register Space		R	Mirrored Register (0x00 to 0x7F)							
		W								
0x380	0x3FF	R	RamTxTransBuffer							
		W								

Read/Write

Field Properties for Register 0x00

Bits	Mnemonic	Prop	Description
0-2047	RamTxTransBuffer	R/W brst BbClk RAM	256 Byte Transmit Buffer *Purpose:* Stores the data to be transmitted in two 128 byte buffers.

12.34 Transparent/Simplex [Pg 0/1/2/3] 0x080/0x3FF – RX/TX Data Buffer

Used for storing sequentially received data and data to be transmitted, where the entire 512 bytes is divided into four 128 byte buffers for writing the data for transmission and reading the received data. As this is Transparent mode, software is responsible fro maintaining important MACFrame variables. As this is Simplex mode, the transmit and receive buffer operations are dependent on each other, in that the receive operation must be completed before the transmit operation can be initiated. Consequently, the buffer for the RX data and for the TX data is double the size, in this case, 512 bytes.

Offset			MSB			Bit Number				LSB
From	To	R/W	7	6	5	4	3	2	1	0
Register Space		R	Register (0x00 to 0x7F)							
		W								
0x080	0x0FF	R	RamTxRxTransBuffer							
		W								
Register Space		R	Mirrored Register (0x00 to 0x7F)							
		W								
0x180	0x1FF	R	RamTxRxTransBuffer							
		W								
Register Space		R	Mirrored Register (0x00 to 0x7F)							
		W								
0x280	0x2FF	R	RamTxRxTransBuffer							
		W								
Register Space		R	Mirrored Register (0x00 to 0x7F)							
		W								
0x380	0x3FF	R	RamTxRxTransBuffer							
		W								

Read/Write

Field Properties for Register 0x00

Bits	Mnemonic	Prop	Description
0-4095	RamTxRxTransBuffer	R/W brst BbClk RAM	512 byte Shared Transmit/Receive Buffer *Purpose:* Sequentially stores the received data and the data to be transmitted in a combined 512 byte RX/TX buffer.

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Revision History

Date	Version	Description/Changes
Internal Only	1.01	Initial Version - Preliminary This document contains information on a pre-engineering chip. Specifications and information herein are subject to change without notice.
2006-12-21	1.01	First Draft Release - Preliminary This document contains information on a pre-engineering chip. Specifications and information herein are subject to change without notice.

About Nanotron Technologies GmbH

Nanotron Technologies GmbH develops world-class wireless products for demanding applications based on its patented Chirp Spread Spectrum - an innovation that guarantees high robustness, optimal use of the available bandwidth, and low energy consumption. Since the beginning of 2005, Nanotron's Chirp technology has been a part of the IEEE 802.15.4a draft standard for wireless PANs which require extremely robust communication and low power consumption.

ICs and RF modules include the nanoNET TRX, the nanoLOC TRX, and ready-to-use or custom wireless solutions. These include, but are not limited to, industrial monitoring and control applications, medical applications (Active RFID), security applications, and Real Time Location Systems (RTLS). nanoNET is certified in Europe, United States, and Japan and supplied to customers worldwide.

Headquartered in Berlin, Germany, Nanotron Technologies GmbH was founded in 1991 and is an active member of IEEE and the ZigBee alliance, and ISA-SP100.

Further Information:

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