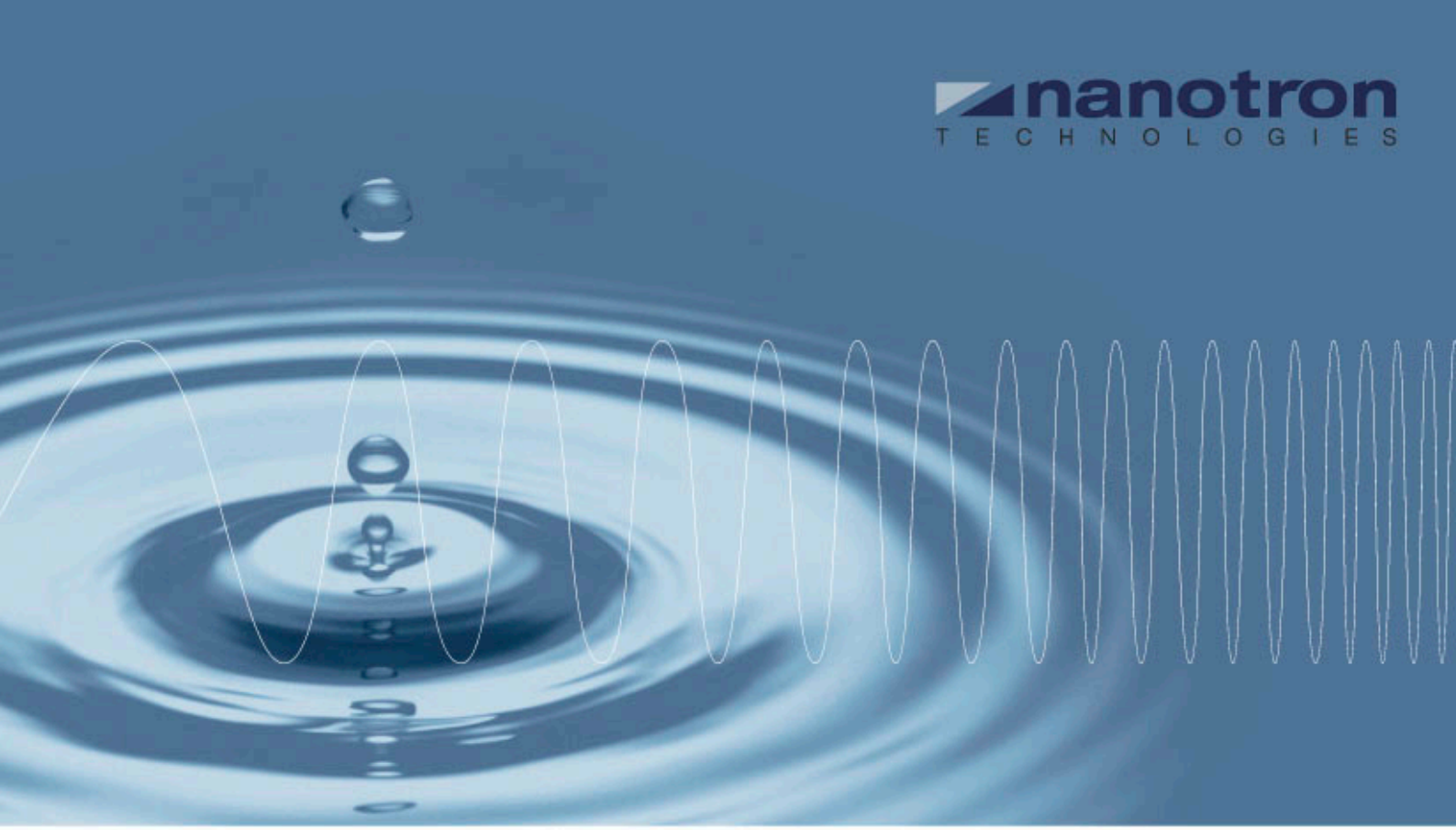


nanoLOC TRX Transceiver (NA5TR1)

Datasheet

Version 2.00

NA-06-0230-0388-2.00

This document contains information on a pre-engineering chip. Specifications and information herein are subject to change without notice.

Document Information

Document Title:	nanoLOC TRX Transceiver (NA5TR1) Datasheet
Document Version:	2.00
Published *(yyyy-mm-dd)*:	2008-04-11
Current Printing:	2008-4-11, 12:09 pm
Document ID:	NA-06-0230-0388-2.00
Document Status:	Released

Disclaimer

Nanotron Technologies GmbH believes the information contained herein is correct and accurate at the time of release. Nanotron Technologies GmbH reserves the right to make changes without further notice to the product to improve reliability, function or design. Nanotron Technologies GmbH does not assume any liability or responsibility arising out of this product, as well as any application or circuits described herein, neither does it convey any license under its patent rights.

As far as possible, significant changes to product specifications and functionality will be provided in product specific Errata sheets, or in new versions of this document. Customers are encouraged to check the Nanotron website for the most recent updates on products.

Trademarks

nanoNET© is a registered trademark of Nanotron Technologies GmbH. All other trademarks, registered trademarks, and product names are the sole property of their respective owners.

Life Support Policy

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nanotron Technologies GmbH customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nanotron Technologies GmbH for any damages resulting from such improper use or sale.

Electromagnetic Interference / Compatibility

Nearly every electronic device is susceptible to electromagnetic interference (EMI) if inadequately shielded, designed, or otherwise configured for electromagnetic compatibility.

To avoid electromagnetic interference and/or compatibility conflicts, do not use this device in any facility where posted notices instruct you to do so. In aircraft, use of any radio frequency devices must be in accordance with applicable regulations. Hospitals or health care facilities may be using equipment that is sensitive to external RF energy.

With medical devices, maintain a minimum separation of 15 cm (6 inches) between pacemakers and wireless devices and some wireless radios may interfere with some hearing aids. If other personal medical devices are being used in the vicinity of wireless devices, ensure that the device has been adequately shielded from RF energy. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

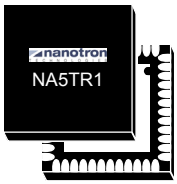
CAUTION! Electrostatic Sensitive Device. Precaution should be used when handling the device in order to prevent permanent damage.

Table of Contents

List of Tables

List of Figures

1 Chip Summary



The *nanoLOC TRX Transceiver* is a low-power, highly integrated mixed signal chip with ranging capabilities utilizing Nanotron's unique wireless Chirp Spread Spectrum (CSS) communication technology.

Supporting a freely adjustable center frequency with three non-overlapping frequency channels, *nanoLOC* enables multiple physically independent networks and improved coexistence with existing 2.45 GHz wireless technologies.

With its unique ranging feature, *nanoLOC* measures the link distance between two nodes, thus supporting location-aware applications. Example applications include location-based services (LBS), enhanced RFID, and asset tracking (2D/3D RTLS). As ranging is performed during regular data communication, additional infrastructure, power, and/or bandwidth is not required.

The nanoLOC chip also includes a sophisticated MAC controller with CSMA/CA, TDMA, and FDMA. Forward Error Correction (FEC) and 128 bit hardware encryption are selectable. To minimize software and microcontroller requirements, scrambling, automatic address matching, and packet retransmission can be enabled. Furthermore, data rates are selectable from 2 Mbps to 125 kbps.

1.1 Target Applications

- Logistics: active RFID / RTLS for asset tracking
- Medical applications
- Industrial monitoring and control
- Security / government applications

Note: For more a more detailed application list, see *8. Target Applications* on page 8.

1.2 Key Features

- Provides built-in precise ranging
- Operates worldwide: 2.45 GHz ISM band
- Programmable data rates: 2 Mbps to 125 kbps
- Modulation technique: CSS (Chirp Spread Spectrum)
- Programmable output power dynamic range[1]: 37.5 dB
- Receiver sensitivity: -95 dBm @ BER=0.001 at nominal conditions[1] (FEC off)
- Receiver sensitivity: -97 dBm @ BER=0.001 at nominal conditions[1] (FEC on)
- Extended operating temperature range (industrial): $T_{ambient}$ = -40°C ... +85°C
- FDMA (Frequency Division Multiplex Access) with 3 non-overlapping frequency channels and 14 overlapping frequency channels
- In-band Carrier to Interference Ratio (C/I): C/I = 0 … 3 dB @ 250 kbps @ C = -65 dBm
- Allows unregulated 2.3 V…2.7 V supply voltage
- Power down mode for increased current saving
- Extremely low shut down current ≤ 2 µA[1]
- Software controlled power supply for external microcontroller allows further energy saving
- 32768 Hz clock available for an external microcontroller and other frequencies are also available (feature clock)
- Integrated fast SPI interface (27 Mbps, slave mode only)
- Integrated frame buffering
- Integrated microcontroller management function
- General purpose 4-bit digital I/Os for easy connection to sensors and actors
- Hardware MAC accelerators for time critical and computation intensive tasks

1. See 10. Nominal Conditions on page 9.

Note: For more a more detailed list, see *5. Main Features* on page 5.

2 Quick Reference Data

Table 1: Quick reference data

Parameter	Value	Unit
Maximum supply voltage	2.7	V
Minimum supply voltage	2.3	V
Maximum output power	0	dBm
Maximum data rate	2	Mbps
Typical sensitivity at nominal conditions[a]	-95	dBm
Typical sensitivity at nominal conditions[a], FEC=ON	-97	dBm
Typical supply current:		
In transmit mode @ -10 dBm output power and nominal conditions[a]	25	mA
In transmit mode @ 0 dBm output power and nominal conditions[a]	30	mA
@ 80 MHz and 1 Mbit/s	35	mA
@ 80 MHz and 250 kbit/s	35	mA
In receive mode and nominal conditions[a]	33	mA
In shut-down mode	2	µA
Operating temperature range	-40 to +85	°C
Frequency channels (FDMA Mode, non-overlapping channels) according to IEEE 802.15.4a standard:[b]		
Number of frequency channels (Europe)	3	Number
Number of frequency channels (USA)	3	Number
Frequency channels (FDMA Mode, overlapping channels) according to IEEE 802.15.4a standard:[c]		
Number of frequency channels	14	Number
Nominal frequency bandwidth of the channel @ -30 dBr	22	MHz
Nominal frequency bandwidth for ranging @ -30 dBr	80	MHz
Typical operational voltages:		
Typical power supply voltage V_{DDA} (analogue block)	2.5	V
Typical power supply voltage V_{DDD} (digital block)	2.5	V

a. *See 10. Nominal Conditions on page 9.*
b. *For a full list of frequency channels used for Europe and USA, see 13.7. Local Oscillator (LO) on page 18*
c. *For a full list of frequency channels, see 13.7. Local Oscillator (LO) on page 18*

3 nanoLOC NA5TR1 Block Diagram - Simplified

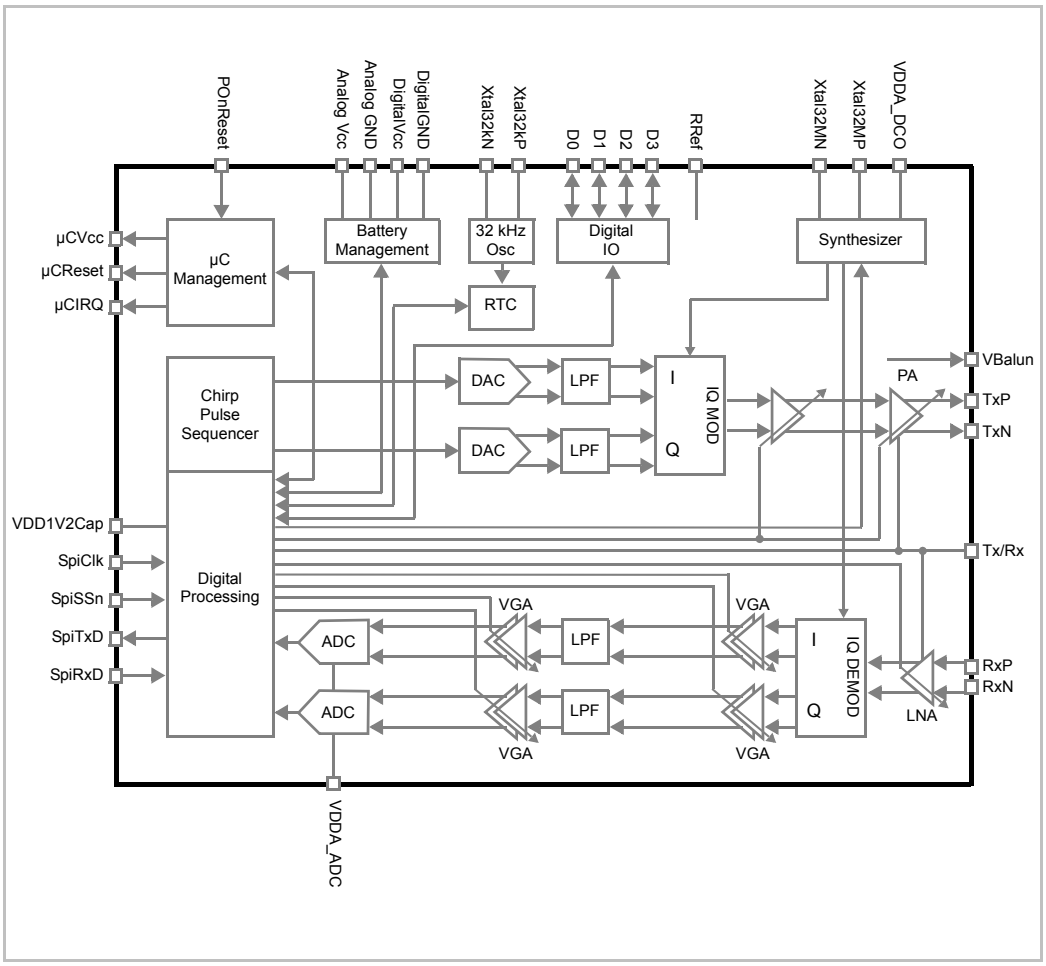


Figure 1: nanoLOC block diagram (simplified)

4 Sample Application With Recommended Circuitry

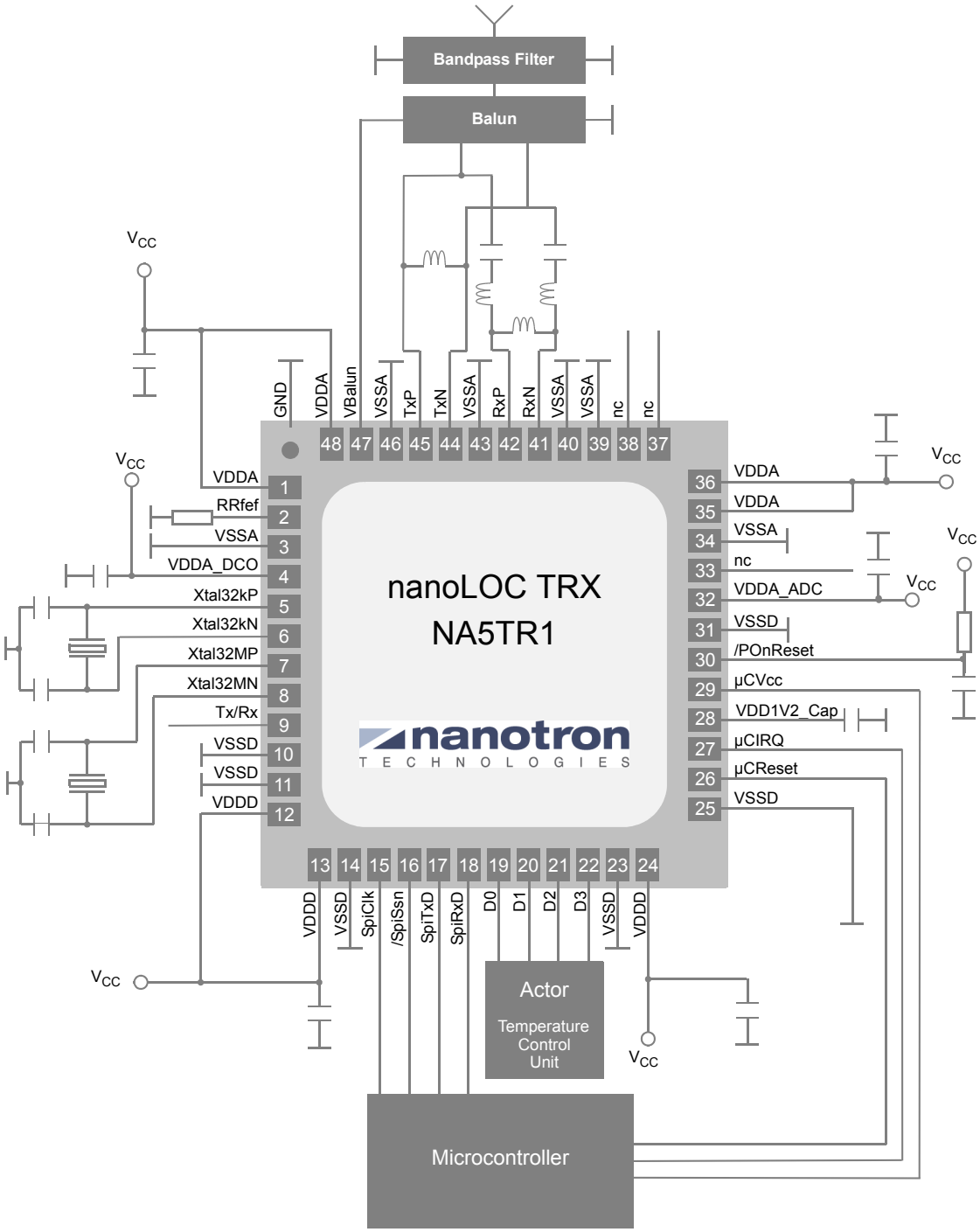


Figure 2: Sample application showing recommended circuitry

Note: For more details, see Appendix 1: *Example Application - RF Module* on page 35.

5 Main Features

Low Radiated Power (Low Human Exposure)

- Reduced radiated power to absolute minimum reduces human exposure.
- Chirp modulation dramatically reduces power spectral density of emitted signal.
- Reduced power spectral density of the signal directly reduces human exposure.

Low Power Consumption

- Extremely low current consumption.
- Operates with batteries.
- Sleep-mode/wake-up operation expands battery lifetime and reduces human exposure.
- Further energy saving possible through software controlled, switchable power supply for external microcontroller.
- Main analog signal processing provides simplicity, low-cost, and low power consumption.

Few Required Additional Components

- DDDL (Digital Dispersive Delay Line) has been integrated into chip so that no external filters are required, thus reducing the BOM.

Small Package

- The *nanoLOC* chip uses a small 7x 7x1 mm leadless Leadframe Package (LLP): VFQFPN-48.

Full-Featured MAC / PHY

- Fully Integrated 2.45 GHz ISM RF transceiver:
  - Full hardware-supported ranging (link distance estimation) capability in either 22 MHz signal bandwidth or 80 MHz signal bandwidth with improved ranging accuracy.
  - FDMA (Frequency Division Multiplex Access) with frequency channels selectable by software.
  - Two independent channel (non-overlapping frequency band) allocations – one for Europe and one for North America.
  - Fourteen FDMA channels (overlapping frequency bands) are available.
- CSMA/CA, TDMA supported.
- Low C/I (Carrier to Interference) ratio.
- Programmable digital support block.
- Programmable RF output power (dynamic range ≥ 37.5 dB).
- Link distances (indoors, outdoors, and free space) for EIRP=1 mW (PEP): 10 m, 100 m, 300 m respectively[1].
- Receiver sensitivity[1] in the range of –95 dBm @ BER = 0.001.
- Low radiated power: -33 dBm for 10 m link distance in free space, with isotropic antennas[1].
- Internal hardware accelerators for all time critical and computing intensive tasks.
- Immunity against Doppler effect.

Configurable Transmit and Receive

- Configurable Rx/Tx buffers.
- 4 kbit Rx/Tx buffers can store several frames.
- Several Rx/Tx frames can be stored simultaneously in the buffers.

Selectable Data Rates

- Data rates selectable between 125 kbit/s and 2 Mbit/s.
- Low data rate over air interface in relationship with theoretical data rate for this particular modulation.
- Big processing gain implicates improved noise immunity.

Simple, Flexible Digital I/O Interface

- Fast (27 Mbps) worldwide-accepted Serial Peripheral Interface (SPI) interface (slave mode only).

nanoLOC Networks

- Network topology not limited by hardware implementation.
- Proposed network topology (if any).

Additional Features

- Simple API access to chip registers using the nTRX Driver.
- *nanoLOC Development Kit* available.

1. At nominal conditions. See *Nominal Conditions* on page 9.

6 General Description

Fully Integrated Chip

nanoLOC is a fully integrated single chip transceiver with ranging capabilities, consisting of:

- Complete analog receiver (from antenna output to the demodulated digital data output) with minimal number of external elements.
- Complete transmitter (from digital data input to output from RF power amplifier, which can be directly connected to the antenna input).
- Programmable support block including power management, battery voltage monitor, and much more. All important functions of this block can be setup and controlled by software.

Programmable Digital Support Block

This programmable digital support block communicates with an external microcontroller via the Serial Peripheral Interface (SPI). This block performs several service functions including RF-front-end control and calibration for the analog part of the chip. Additionally, this block includes support for some fundamental protocol stack functions of the MAC layer. These include MAC Frame coding, frame buffering, bit processing (such as CRC generation/checking and encryption/decryption), as well as MAC protocol handling (such as medium access control and automatic acknowledgement-frame transmission).

Additional functions of this block include ranging support, Real Time Clock maintenance, and power-down/wake-up management. All functions of this block can be setup and controlled by software, which is executed by a microcontroller connected to the chip by means of the SPI interface.

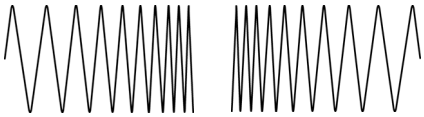
Robust, Short Distance Wireless Networks

nanoLOC is designed for building up robust, short distance wireless networks operating in the 2.45 GHz ISM band, especially networks that require extremely low power consumption over a wide range of the operating temperatures. For battery operating applications requiring a long battery life (for several years, for example), this chip offers an ideal solution.

About Chirp Spread Spectrum (CSS)

For communication over the air, *nanoLOC* uses Nanotron-developed chirp technology – Chirp Spread Spectrum (CSS). A chirp pulse is a frequency modulated pulse that changes monotonic from a lower value to a higher value (Upchirp) or from a higher value to a lower value (Downchirp).

In *nanoLOC*, Upchirps and Downchirps have a symbol duration t_{symbol} = 1 µs, 2 µs, or 4 µs and a frequency bandwidth B_{chirp} = 22 MHz or 80 MHz.



Application software can define and select different data rates between 125 kbit/s and 2 Mbit/s.

Receiver Sensitivity

The sensitivity of the *nanoLOC* chip is defined by the raw data mode (when data is not coded) where BER = 0.001. The typical sensitivity is:

$$P_{sensitivity} = -95 \text{ dBm or better}$$

which is achieved at nominal conditions[1]. The typical link budget is equal to:

$$A_{link\_budget} = 95 \text{ dB}$$

If two transceivers that attempt to establish a wireless communication link are equipped with an identical patch antenna (each with gain G_A = 3 dBi), then for BER = 0.001 and $P_{transmitted\_max}$ = 0 dBm the maximum link attenuation between the two antennas is equal to:

$$A_{path\_att\_max} = P_{transmitted\_max} + 2*G_A + P_{sensitivity} = 101 \text{ dB}$$

To increase the Link Budget value and/or increase the quality of the wireless link (for example, reduce BER value), FEC can be activated. When FEC is on (activated), the typical receiver's sensitivity is[2]:

$$P_{sensitivity\_FEC} = -97 \text{ dBm or better}$$

For this scenario, maximum link attenuation is increased to:

$$A_{path\_att\_max\_fec} = 103 \text{ dB}$$

1. At nominal conditions. See *Nominal Conditions* on page 9.
2. Achieved at nominal conditions, except FEC is on.

Maximum Transmission Output Power

The maximum transmission power of the *nanoLOC* chip is[1]:

$$P_{transmitted\text{-}max} = 0 \text{ dBm}$$

The transmission power can be programmed by the application software and can be stepwise reduced (from maximum 0 dBm) in several steps. It can vary from –33 dBm to 0 dBm (without any additional external power amplifier, attenuator, and so on).

Frame Buffers

Due to *nanoLOC's* use of frame buffers, even a very slow microcontroller can work with this "high speed" chip. *nanoLOC's* 4 kbit receive or transmit buffers can store several frames (depending of the frame length). For instance, several receive and transmit frames can be stored simultaneously in the buffers.

These buffers eliminate potential congestion caused by different peak data rates between the following interfaces:

- Digital interface that is between a slow microncontroller and the high speed *nanoLOC* chip
- Air interface between *nanoLOC* nodes

Minimum Required External Components

The *nanoLOC* chip is designed so that only a minimum number of external elements are required to build up a fully operational bi-directional wireless communication node.

Additional Chip Features

Additional features of *nanoLOC* which are supported and controlled by software include:

- Power management module
- Wake-up circuitry
- Real Time Clock
- Low battery alarm
- Encryption/decryption
- Cyclic Redundancy Checksum (CRC) generation/check block
- Forward Error Correction (FEC) block
- Automatic address matching
- Automatic retransmissions
- Handshake modes

7 nanoLOC System

Ranging Capabilities Based on SDS-TWR

A key feature of the *nanoLOC* chip is its built-in precise ranging capability. This allows the chip to provide both a wireless communication link and the ability to estimate the link distance between two communicating *nanoLOC* nodes.

Ranging in *nanoLOC* is based on precise time measurements of the signals propagating between two nodes[1]. The *nanoLOC* system provides two ranging bandwidths:

- 22 MHz signal bandwidth
- 80 MHz signal bandwidth with improved ranging accuracy

FDMA (Frequency Division Multiple Access)

As the *nanoLOC* chip uses the 2.4 GHz licence-free ISM band[2], other equipment such as microwave ovens also operate in this band. Consequently, services operating in this band, including wireless communication, must accept and tolerate potential interferences and disturbances.

As a means of counteracting in-band and out-of-band disturbances, *nanoLOC* provides FDMA (Frequency Division Multiple Access). This access method divides the 2.4 GHz bandwidth into different frequency bands. The *nanoLOC* chip provides the following channel allocations:

- Two independent channel (non-overlapping frequency bands) allocations: one for Europe and one for USA
- Fourteen FDMA channels (overlapping frequency bands) are available, depending on the frequency allocations for a region

Low C/I (Carrier to Interference) Ratio

The ISM frequency band is very "noisy" as it often has many unwanted signals (noise) that detract from the potential quality of the wanted signals (carrier). Due to *nanoLOC's* high processing gain, the carrier to interference ratio is extremely low and operates effectively in this "noisy" ISM band.

1. For more details, see the *Real Time Location Systems White Paper* available from Nanotron.
2. Allocated worldwide for Industrial, Scientific and Medical applications

8 Target Applications

The *nanoLOC* chip is ideal for applications that require a robust wireless link over short distances, but are license-free, operate with a battery, and permit only low human exposure to RF energy, all at a low cost. For application developers, the chip offers simplicity of development using the full-featured *nanoLOC Development Kit*.

Target applications are primarily in the capital goods market, in particular, OEM customers that install transceivers into their industrial application products.

These applications can be installed either indoors or outdoors.

Logistics applications using low-cost active RFID / RTLS for asset tracking

- Asset identification and tracking
- Inventory management
- Visitor/employee identification and tracking
- Logistics applications (location-aware)

Medical applications requiring low-cost and low-human exposure

- Medical personnel monitoring
- Medical equipment tracking
- Patient monitoring
- Sensitive medical control applications

Industrial monitoring and control applications for sensor and actor networks

- Sensor networks and Actor RF Networks
- Manufacturing and production processing equipment
- Heating, ventilation, and air conditioning
- Condition monitoring

nanoLOC Development Kit

The *nanoLOC Development Kit* is a complete, easy-to-use set of tools for developing RTLS and location-enabled wireless sensor network applications. Everything required is provided to evaluate, prototype and develop applications with robust communication and built-in ranging capabilities. The kit's hardware includes five full-featured *nanoLOC DK Boards* plus a special *nanoLOC USB Stick*. For flashing and debugging, the Atmel® AVR STK 500 Development System and a JTAG adapter are included. A full range of sample application are included that can be used as a basis for your own location-aware and ranging applications. Contact Nanotron Sales for details.

Figure 3: nanoLOC Development Kit

9 Absolute Maximum Ratings

Table 2: Absolute maximum ratings

Parameter	Value[1]	Unit
Temperature:		
Maximum operating temperature	85	°C
Maximum junction temperature	95	°C
Maximum storage temperature	125	°C
Reflow solder temperature (lead-free package)	242	°C
Voltages:		
Power supply voltage VDDA (analogue block)	2.7	V
Power supply voltage VDDD (digital block)	2.7	V
Power:		
Total power dissipation	300	mW
Electrostatic Discharge Protection (ESD Protection):		
Maximum ESD input potential, Human Body Model	1000	V

1. It is critical that the ratings provided in Absolute Maximum Ratings be carefully observed. Stress exceeding one or more of these limiting values may cause permanent damage to the device.

10 Nominal Conditions

Nominal conditions are specified below, except otherwise noted:

- Reference design used[1]
- T_{junct} = 30°C
- V_{SSA} = V_{SSD} = GND
- V_{DDA} = V_{DDD} = +2.5 V
- Transmission / reception @ 250 kbps
- Nominal frequency bandwidth (TX/RX)
  B = 22 MHz @ -30 dBr
- Raw data mode
- No CRC
- No FEC
- No encryption
- Receiver synchronized
- Bit scrambling
- BER = 0.001 during receive mode
- RF output power (PEP) during transmit phase
  = 0 dBm EIRP measured during continuous transmission
- Nominal process
- All RF ports are impedance matched according to the specification.
- All RF power are measured on the IC terminals (pins)
- For link distance measurement, two identical *nanoLOC* systems are used
- Baseband clock = 32 MHz

1. *See Appendix 2. nanoLOC RF Test Module on page 41.*

11 Block Diagram

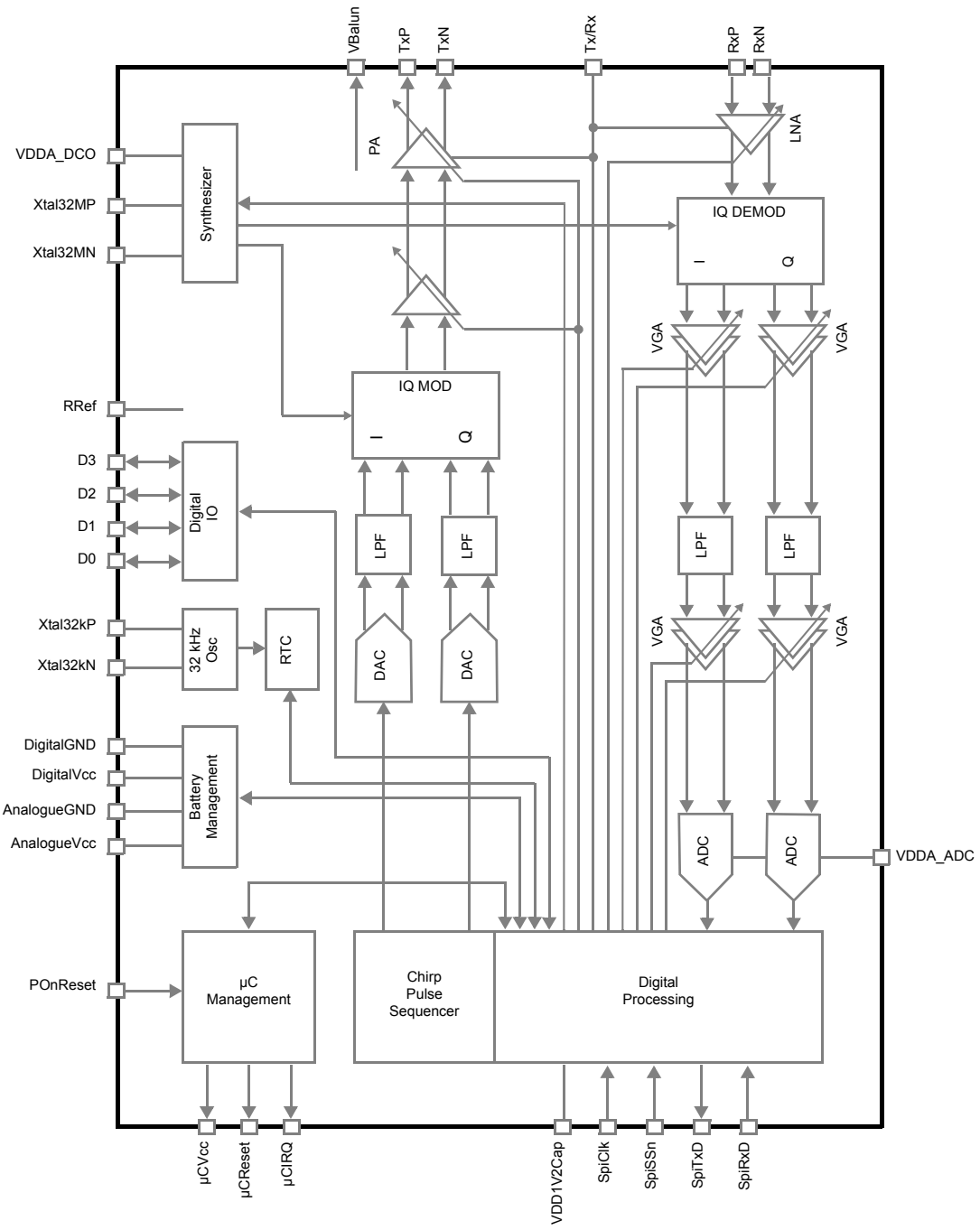


Figure 4: nanoLOC TRX Transceiver (NA5TR1) block diagram (simplified)

12 Pin Connections and Description

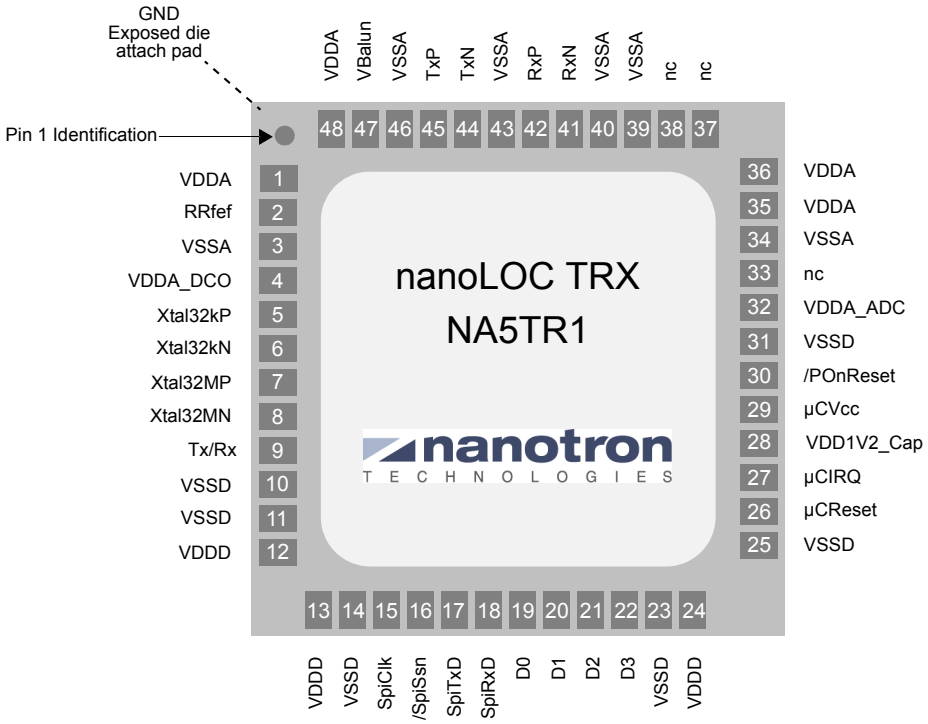


Figure 5: nanoLOC TRX Transceiver (NA5TR1) pin assignment (through top view)

12.1 Pin Descriptions

Table 3: Pin description

Pin	Name	Type	Description
–	GND	Ground (analog)	Exposed die attach pad: must be connected to solid ground plane.
1	VDDA	Supply	Power supply for analog parts.
2	RRef	Analog IO	External precise reference resistor (see *Pin 2: RRef – External Precise Reference Resistor* on page 13 for details).
3	VSSA	Supply	Power supply for analog parts.
4	VDDA_DCO	Supply	Power supply for DCO.
5	Xtal32kP	Analog IO	32768 Hz crystal oscillator pin 1 or input for an external 32768 Hz clock generator. Used to connect crystal or active frequency reference
6	Xtal32kN	Analog IO	32768 Hz crystal oscillator pin 2.
7	Xtal32MP	Analog IO	32 MHz crystal oscillator pin 1 or input for an external 32 MHz clock generator. Usage: Connect crystal or active frequency reference
8	Xtal32MN	Analog IO	32 MHz kHz crystal oscillator pin 2.
9	Tx/Rx	Digital Output	Distinguishes between the TX and RX phase. Can also be used to provide an external power amplifier control. Active Low during TX, otherwise High.
10	VSSD	Supply	Power supply for digital parts.
11	VSSD	Supply	Power supply for digital parts.
12	VDDD	Supply	Power supply for digital parts.

Table 3: Pin description (Continued)

Pin	Name	Type	Description
13	VDDD	Supply	Power supply for digital parts.
14	VSSD	Supply	Power supply for digital parts.
15	SpiClk	Digital Input	SPI Clock.
16	/SpiSSn	Digital Input	SPI Slave Selected; Active Low.
17	SpiTxD	Digital Output	SPI Transmit Data (MISO).
18	SpiRxD	Digital Input	SPI Receive Data (MOSI).
19	D0	Digital IO	General purpose programmable digital I / O line 0.[1]
20	D1	Digital IO	General purpose programmable digital I / O line 1.[1]
21	D2	Digital IO	General purpose programmable digital I / O line 2.[1]
22	D3	Digital IO	General purpose programmable digital I / O line 3.[1] Note: A 32768 Hz clock operates on the pin D3 after reset/ power.
23	VSSD	Supply	Power supply for digital parts.
24	VDDD	Supply	Power supply for digital parts.
25	VSSD	Supply	Power supply for digital parts.
26	µCReset	Digital Output	Used to reset an external microcontroller at power-up and wake-up. Active Low during normal operation.
27	µCIRQ	Digital Output	Microcontroller interrupt request. Can be used to send an interrupt request to an external microcontroller. Logic levels can be programmed.[2]
28	VDD1V2_Cap	Supply	1.2 V digital power supply decoupling.[3]
29	µCVcc	DC Output	Switchable power supply for external microcontroller.
30	/POnReset	Digital Input	Power on reset signal.[4]
31	VSSD	Supply	Power supply for digital parts.
32	VDDA_ADC	Supply	Power supply for analog parts (Rx ADC).
33	nc	–	Not connected.
34	VSSA	Supply	Power supply for analog parts.
35	VDDA	Supply	Power supply for analog parts.
36	VDDA	Supply	Power supply for analog parts.
37	nc	–	Must not be connected.
38	nc	–	Must not be connected.
39	VSSA	Supply	Power supply for analog parts.
40	VSSA	Supply	Power supply for analog parts.
41	RxN	RF Input	Differential receiver input (inverted).
42	RxP	RF Input	Differential receiver input.
43	VSSA	Supply	Power supply for analog parts.
44	TxN	RF Output	Differential transmitter output (Inverted).
45	TxP	RF Output	Differential transmitter output.
46	VSSA	Supply	Power supply for analog parts.
47	VBalun	DC Output	DC voltage for RF output stage.[5]
48	VDDA	Supply	Power supply for analog parts.

1. See 12.3. Pins 19-22: D0 to D3 – Programmable Digital I/Os on page 13
2. See 12.4. Pin 27: µCIRQ – Microcontroller Interrupt Request on page 13.
3. See 12.5. Pin 28: VDD1V2_Cap – 1.2 V Digital Power Supply Decoupling on page 13.
4. See 12.6. Pin 30: /POnReset on page 14.
5. See 12.7. Pin 47: VBalun – DC voltage for RF output stage on page 14.

12.2 Pin 2: RRef – External Precise Reference Resistor

Table 4: RRef (pin 2)

RRef (Pin 2)	Value	Unit
Nominal resistance	10	kΩ
Recommended resistance tolerance	1	%

12.3 Pins 19-22: D0 to D3 – Programmable Digital I/Os

These four digital I/Os are programmed through the use of register 0x04 and 0x05.

The digital IO ports have several functions. These include a normal input where the signal level at these ports can be read, or a normal output where a programmable value is driven out of the chip. Additionally, the digital IO ports can be used as an alarm input which reports the occurrence of an alarm event. This could be used to wake-up the chip. Also a clock (feature clock) can be driven out of the chip on these pins.

When reading this register, each bit reports the signal level or the occurrence of an alarm at the corresponding digital IO port. When writing to this register, the values are just set inside this register. The values first influence one or more digital IO ports when a write strobe is generated for the desired digital IO port(s) via register 0x05. This causes the values in this register to be copied to the corresponding configuration registers of these digital IO ports.

Note: For more details, see the *nanoLOC TRX Transceiver (NA5TR1) User Guide*.

12.4 Pin 27: µCIRQ – Microcontroller Interrupt Request

µCIRQ is a programmable output pin that sends an interrupt request to an external microcontroller. This IRQ pin can be configured as either low or high active, as well as either push-pull or open-drain using register 0x00. The IRQ pin can be driven by either a transmitter interrupt, a receiver interrupt, a baseband timer interrupt, or a local oscillator interrupt using register 0x0F.

Note: For more details, see the *nanoLOC TRX Transceiver (NA5TR1) User Guide*.

12.5 Pin 28: VDD1V2_Cap – 1.2 V Digital Power Supply Decoupling

Table 5: VDD1V2_Cap (Pin 28)

VDD1V2_Cap (Pin 28)	Value	Unit
Decoupling capacitance (typical)	100	nF

12.6 Pin 30: /POnReset

/POnReset signal is active low. Figure 6 shows a timing diagram for pin 30 /POnReset.

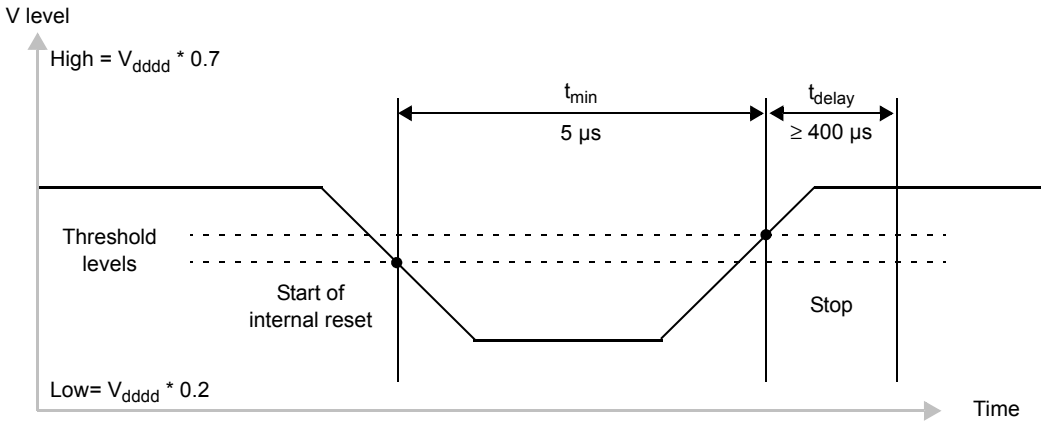


Figure 6: /POnReset timing diagram

12.7 Pin 47: VBalun – DC voltage for RF output stage

This must be fed to TxN and TxP using bias tees or a balun / transformer with center tap. Minimum and maximum values for a decoupling bypass capacitor are shown below. (Note: It is not a block capacitor.) RF ceramic type with low serial inductance is recommended.

Table 6: VBalun (Pin 47)

VBalun (Pin 47)	Value	Unit
Decoupling bypass capacitor minimum capacitance	27	pF
Decoupling bypass capacitor maximum capacitance	47	pF

Note: See also *1. Example Application - RF Module* on page 35.

12.8 Chip Memory Spaces and Registers

The *nanoLOC* chip provides four memory spaces:

- 128 byte programmable chip register (register block) for chip configuration settings
- 512 byte baseband RAM
- Chirp sequencer RAM
- Correlator memory

A complete description of these memory spaces and all end-user registers, as well as information on programming the chip, is provided in *nanoLOC TRX Transceiver (NA5TR1) User Guide*.

13 Electrical Specifications

This section provides the fundamental electrical specifications of the major blocks of the *nanoLOC* chip (NA5TR1). Typical values represent the mean production values (nominal process) at nominal operating conditions (See *10. Nominal Conditions* on page 9). The minimum/maximum values are guaranteed values over the entire operating range (unless otherwise stated). For a balanced signal, all impedances, signal voltages, and so on, refer to the differential signal.

13.1 General / DC Parameters

Table 7: General / DC Parameters

Parameter	Value	Unit
Operating frequency range	2.4	GHz ISM Band
Supply voltage range	2.3 … 2.7	V
Modulation method	Chirp	–
Operating temperature range	-40 … +85	°C
Typical supply current for individual blocks:		
Analog part, Tx block (P_{out} = 0 dBm)	23	mA
Analog part, Tx block, ranging with increased accuracy (P_{out} = 0 dBm)	25	mA
Analog part, Rx block	24	mA
Analog part, Rx block, ranging with increased accuracy	28	mA
Digital part, Tx mode	7	mA
Digital part, Tx mode, ranging with increased accuracy	10	mA
Digital part, Rx mode	9	mA
Digital part, Rx mode, ranging with increased accuracy	20	mA
Typical total supply current:		
Tx Mode (P_{out} = 0 dBm)	30	mA
Tx Mode, ranging with increased accuracy (P_{out} = 0 dBm)	35	mA
Rx Mode	33	mA
Rx Mode, ranging with increased accuracy	48	mA
VDD1V2_Cap (Pin 28): 1.2 V digital power supply decoupling:		
Decoupling capacitance (typical)	100	nF
VBalun (Pin 47): DC voltage for RF output stage		
For Decoupling bypass capacitor Min and Max, see 12.7. Pin 47: VBalun – DC voltage for RF output stage on page 14.		
µCVcc (pin 29): Switchable power supply for external microcontroller:		
Maximum capacitive load	10	µF
Maximum output current	10	mA
RRef (pin 2): External precise reference resistor:		
Nominal resistance	10	kΩ
Recommended resistance tolerance	1	%

13.2 Transmitter (TX)

13.2.1 General Parameters

Note: All values at nominal conditions. See 10. Nominal Conditions on page 9.

Table 8: Transmitter – general parameters

Parameter	Value	Unit
Transmitter nominal output power	0	dBm
Dynamic for output power control (typical)	≥ 37.5	dB
Number of steps for output power control	64	Number
Load impedance	200	Ohm
Type of load	Balanced	–
Transmitter spurious outputs (1 GHz ... 12.5 GHz)	≤ -80	dBm/Hz
Transmitter carrier suppression	≤ -20	dBc
Number of frequency channels (FDMA Mode, non-overlapping channels), according to IEEE 802.15.4a standard[1]	3	Number
Number of frequency channels (FDMA Mode, overlapping channels), according to IEEE 802.15.4a standard[2]	14	Number
Carrier frequency calibration accuracy (relative), CSS mode[3]	± 70	ppm
Carrier frequency calibration accuracy (absolute), CSS mode[1]	± 171	kHz

1. *For a list of frequency allocations for Europe and USA, see 13.7. Local Oscillator (LO) on page 18.*
2. *For a list of frequency allocations, see 13.7. Local Oscillator (LO) on page 18.*
3. *Warming-up, temperature drift and voltage supply changes will cause a drift of the oscillator frequency. Therefore the calibration of the oscillator should be repeated regularly.*

13.2.2 Chirp Specification (CSS - Chirp Spread Spectrum)

Table 9: Transmitter – Chirp specification (CSS)

Parameter	Value	Unit
Chirp duration (programmable)	0.5, 1, 2, and 4	µs
Symbol rate:	–	–
Nominal	1	Mbaud
Reduced	0.5 and 0.25	Mbaud
Chirp Sequencer Clock Frequency f_{Chirp}, FDMA-CSS mode	32	MHz
Chirp Sequencer Clock Frequency f_{Chirp}, CSS Ranging mode	244.175	MHz

13.3 Receiver (RX) General Parameters

Table 10: Receiver – general parameters

Parameter	Value	Unit
Typical receiver sensitivity @ BER=10^{-3}, nominal conditions[1] (FEC=off)	-95	dBm
Typical receiver sensitivity @ BER=10^{-3}, nominal conditions[1] (FEC=on)	-97	dBm
Type of RX input	Balanced	–
Typical noise figure	3.5	dB
Maximum input signal @ BER=10^{-3}	-20	dBm
Number of frequency channels (FDMA Mode, non-overlapping channels), according to IEEE 802.15.4a standard[2]	3	Number
Number of frequency channels (FDMA Mode, overlapping channels), according to IEEE 802.15.4a standard[3]	14	Number
Nominal frequency bandwidth of the channel @ -30 dBr (	22	MHz
Nominal frequency bandwidth of the channel @ -30 dBr (wideband)	80	MHz
LO frequency calibration accuracy (relative), CSS mode[1,4]	± 70	ppm
LO frequency calibration accuracy (absolute), CSS mode[1,2]	± 171	kHz

1. *At nominal conditions. See 10. Nominal Conditions on page 9.*
2. *For a list of frequency allocations for Europe and USA, see 13.7. Local Oscillator (LO) on page 18.*
3. *For a list of frequency allocations, see 13.7. Local Oscillator (LO) on page 18.*
4. *Warming-up, temperature drift and voltage supply changes will cause a drift of the oscillator frequency. Therefore the calibration of the oscillator should be repeated regularly.*

13.4 Dynamic Performance

Note: See figures in *14. Timing Diagrams* on page 21.

Table 11: Dynamic performance

Parameter	Figure	Variable	Value	Unit
Turn-on time Rx[1]	Figure 7	t_{RxTO}	6	µs
Turn-on time Tx	Figure 8	t_{TxTO}	≤ 24	µs
Switch Tx to Rx, ACK to DATA Mode[2]	Figure 9	$t_{TxRxAckData}$	≤ 24	µs
Switch Tx to Rx, DATA to DATA Mode[3]	Figure 10	$t_{TxRxData-Data}$	≤ 8	µs
Switch Tx to Rx, DATA to ACK Mode[3]	Figure 11	$t_{TxRxDataAck}$	≤ 8	µs
Switch Rx to Tx, ACK to DATA Mode	Figure 12	$t_{RxTxAckData}$	≤ 24	µs
Switch Rx to Tx, DATA to DATA Mode	Figure 13	$t_{RxTxData-Data}$	≤ 24	µs
Switch Rx to Tx, DATA to ACK Mode	Figure 14	$t_{RxTxDataAck}$	≤ 8	µs
Start-up time for 32 MHz reference oscillator	Figure 15	t_{XtalSU}	≤ 5	ms
Calibration time	Figure 16	t_{LOFQ}	6	ms

1. *At input power = approx. -80 dBm*
2. *Assuming RX is initialized.*

13.5 Quartz Controlled Oscillator for Reference Frequency

Table 12: Quartz controlled oscillator for reference frequency

Parameter	Value	Unit
Frequency f_{REF}	32	MHz
Oscillation type of the reference quartz resonator	Fundamental	–
Recommended reference quartz resonator	± 40	ppm
Recommended maximum frequency temperature coefficient of the reference quartz resonator	± 20	ppm
Recommended maximum frequency tolerance of the reference quartz resonator	± 10	ppm
Recommended maximum aging of the reference quartz resonator in 10 years	± 10	ppm
Maximum equivalent serial resistance of the reference quartz resonator	40	Ω
Recommended load capacitance	12	pF
Input for external signal with frequency f_{REF}	Yes	–
Pin name for external signal with frequency f_{REF}	Xtal32MP	–

13.6 Quartz Controlled Oscillator for Real Time Clock (RTC)

Table 13: Quartz Controlled Oscillator for Real Time Clock (RTC)

Parameter	Value	Unit
Frequency f_{RTC}	32768	Hz
Oscillation type of the RTC quartz resonator	Fundamental	—
Recommended frequency accuracy of the quartz resonator	± 20	ppm
Maximum equivalent serial resistance of the RTC quartz resonator	80	kΩ
Recommended load capacitance	12.5	pF
Input for external signal with frequency f_{RTC}	Yes	–
Pin name for external signal with frequency f_{RTC}	Xtal32kP	–

13.7 Local Oscillator (LO)

Table 14: Local Oscillator (LO)

Parameter	Value	Unit
Number of frequency channels (FDMA Mode, non-overlapping channels) according to IEEE 802.15.4a standard	3	Number
Nominal LO frequency f_{LO1E} for FDMA channel no. 0 (Europe)	2412	MHz
Nominal LO frequency f_{LO2E} for FDMA channel no. 6 (Europe)	2442	MHz
Nominal LO frequency f_{LO3E} for FDMA channel no. 12 (Europe)	2472	MHz
Nominal LO frequency f_{LO1U} for FDMA channel no. 0 (USA)	2412	MHz
Nominal LO frequency f_{LO2U} for FDMA channel no. 5 (USA)	2437	MHz
Nominal LO frequency f_{LO3U} for FDMA channel no. 10 (USA)	2462	MHz

Table 14: Local Oscillator (LO) (Continued)

Parameter	Value	Unit
Number of frequency channels (FDMA Mode, overlapping channels) according to IEEE 802.15.4a standard	14	Number
Center frequency of channel no. 0 (overlapping)	2412	MHz
Center frequency of channel no. 1 (overlapping)	2417	MHz
Center frequency of channel no. 2 (overlapping)	2422	MHz
Center frequency of channel no. 3 (overlapping)	2427	MHz
Center frequency of channel no. 4 (overlapping)	2432	MHz
Center frequency of channel no. 5 (overlapping)	2437	MHz
Center frequency of channel no. 6 (overlapping)	2442	MHz
Center frequency of channel no. 7 (overlapping)	2447	MHz
Center frequency of channel no. 8 (overlapping)	2452	MHz
Center frequency of channel no. 9 (overlapping)	2457	MHz
Center frequency of channel no. 10 (overlapping)	2462	MHz
Center frequency of channel no. 11 (overlapping)	2467	MHz
Center frequency of channel no. 12 (overlapping)	2472	MHz
Center frequency of channel no. 13 (overlapping)	2484	MHz
Accuracy of the LO frequency calibration, typical CSS mode[1]	± 70	ppm
Accuracy of the LO frequency calibration, worst case, CSS mode[1]	± 100	ppm

1. *Warming-up, temperature drift and voltage supply changes will cause a drift of the oscillator frequency. Therefore the calibration of the oscillator should be repeated regularly.*

13.8 Digital Interface

Note: The following table refers to the Digital IOs D0, D1, D2, D3, µCReset, µCIRQ, SpiTxD, SpiClk, SpiSSn, Tx/Rx.

Table 15: Digital Interface to Sensor / Actor

Symbol	Parameter	Value	Unit
–	Number of general purpose input/outputs	4	Number
–	Width of each interface	1	Bit
–	Direction	In/Out (bi-directional, open-drain with pull-up	–
–	Type	Programmable	–
C_{IN}	Logic Input Capacitance	2.5	pF
	Input Voltage		
V_{IL}	Low level input voltage (minimum)	0.2 x V_{DDD}	V
V_{IH}	High level input voltage (maximum)	0.7 x V_{DDD}	V
	Output Voltage		
V_{OL}	Low level output voltage (maximum)	0.3	V
V_{OH}	High level output voltage (minimum)	V_{DDD} - 0.3	V
–	Maximum output current	2	mA
R_{UP}	Equivalent pull-up resistance (minimum)	50	kΩ

Table 15: Digital Interface to Sensor / Actor (Continued)

Symbol	Parameter	Value	Unit
R_{UP}	Equivalent pull-up resistance (maximum)	193	kΩ
R_{DN}	Equivalent pull-down resistance (minimum)	50	kΩ
R_{DN}	Equivalent pull-down resistance (maximum)	275	kΩ

13.9 Power Supply for the External Microcontroller

Table 16: Power supply for external microcontroller

Parameter	Value	Unit
Typical Output Voltage @ I_{Load} = 10mA	VDD-0.04 [1]	V
Maximum Capacitive Load at µCVcc	10	µF
Maximum Output Current	10	mA
Typical Start-Up Time @ I_{Load} = 10mA, C_{Load} = 10uF	1.5	ms

1. *VDD=2.3 … 2.7 V*

14 Timing Diagrams

Note: The time values in the following diagrams are based on Table 11 on page 17.

14.1 Turn-On Time Rx

The turn-on time[1] for Rx, t_{RxTO}, from the reception via SPI of a user command to the beginning of packet reception is 6 µs (at input power = approximately -80 dBm).

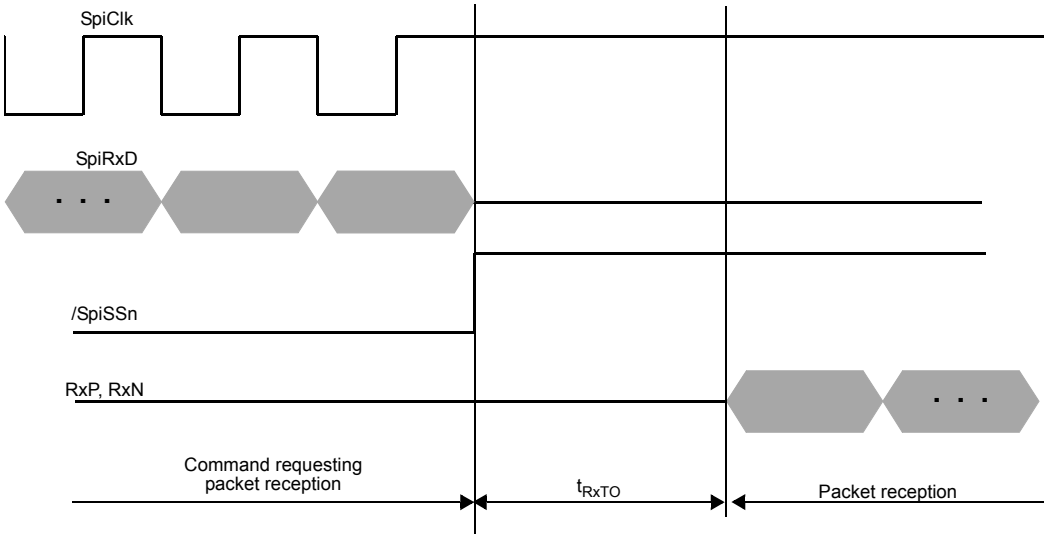


Figure 7: Turn-on time Rx: time = t_{RxTO}

14.2 Turn-On Time Tx

The Turn-on time for Tx, t_{TxTO}, from the reception via SPI of a user command to the beginning of packet transmission is ≤ 24 µs.

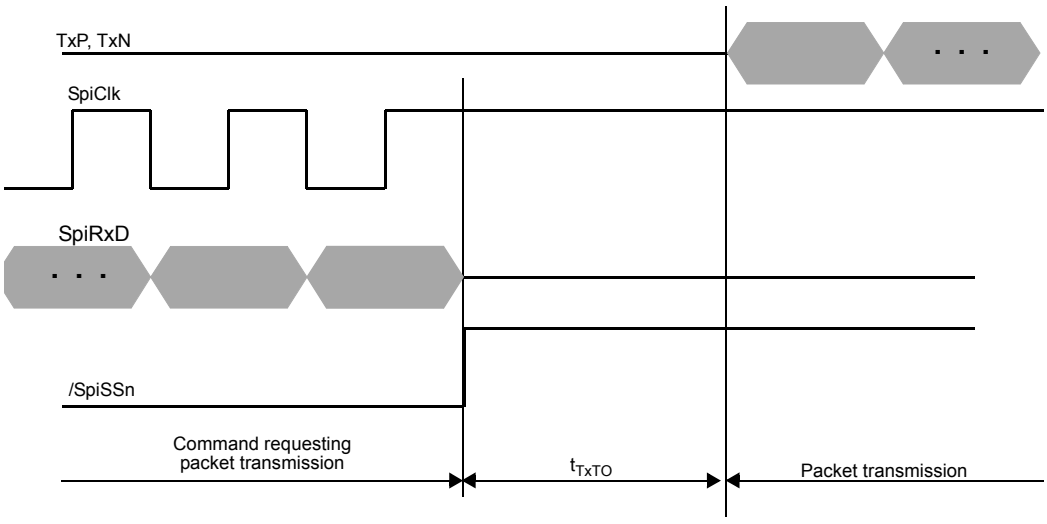


Figure 8: Turn-on time Tx: time = t_{TxTO}

1. At nominal conditions. See 10. Nominal Conditions on page 9.

14.3 Switch Time From Tx to Rx (ACK to DATA Mode)

The switch time[1] from Tx to Rx (ACK to DATA mode), $t_{TxRxAckData}$, is ≤ 24 µs.

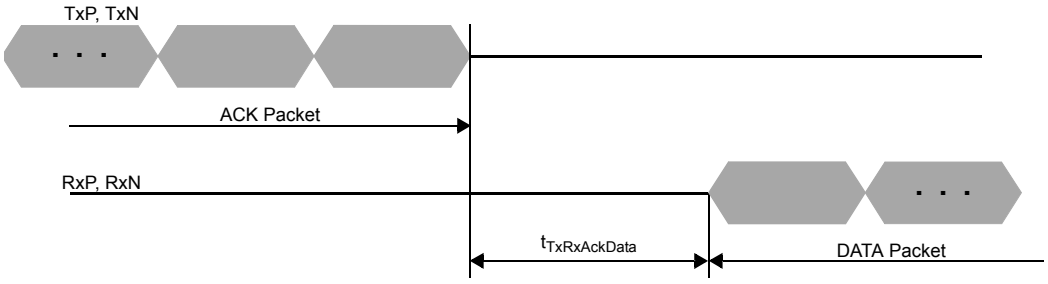


Figure 9: Switch time from Tx to Rx (from ACK to DATA mode)

14.4 Switch Time From Tx to Rx (DATA to DATA Mode)

The switch time[1] from Tx to Rx (DATA to DATA mode), $t_{TxRxDataData}$, is ≤ 24 µs.

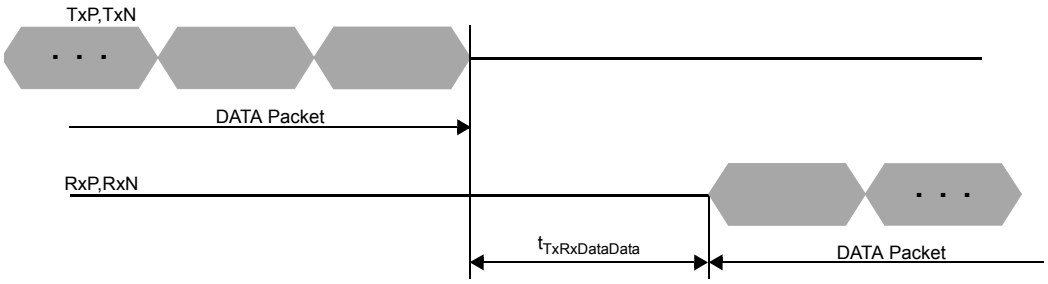


Figure 10: Switch time from Tx to Rx (from DATA to DATA mode)

14.5 Switch Time From Tx to Rx (DATA to ACK Mode)

The switch time[1] from Tx to Rx (DATA to ACK mode), $t_{TxRxDataAck}$, is ≤ 8 µs.

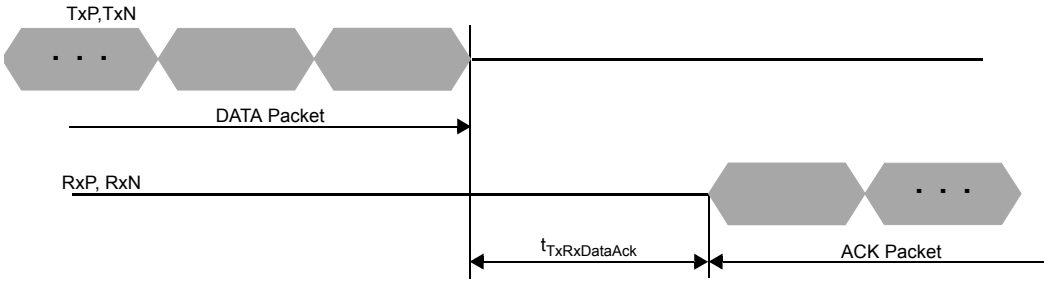


Figure 11: Switch time from Tx to Rx (from DATA to ACK mode)

1. *Assuming RX is initialized.*

14.6 Switch Time From Rx to Tx (ACK to DATA Mode)

The switch time from Rx to Tx (from ACK to DATA mode), $t_{RxTxAckData}$, is ≤ 24 µs.

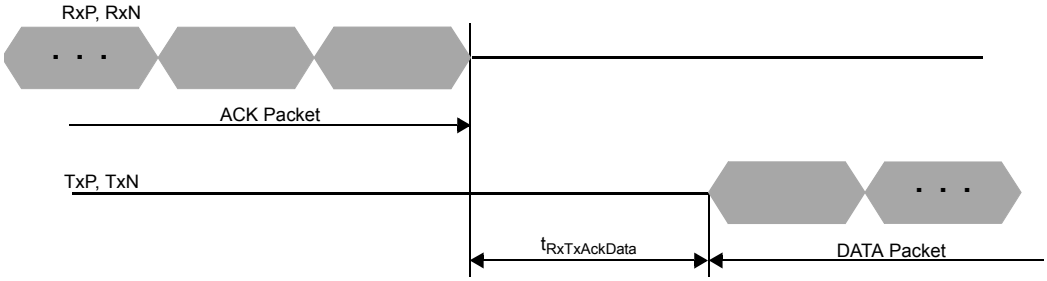


Figure 12: Switch time from Rx to Tx (from ACK to DATA mode)

14.7 Switch Time From Rx to Tx (DATA to DATA Mode)

The switch time from Rx to Tx (from DATA to DATA mode), $t_{RxTxDataData}$, is ≤ 24 µs.

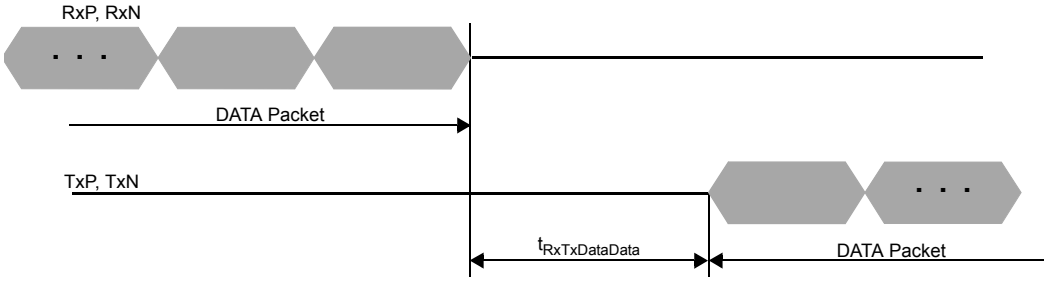


Figure 13: Switch time from Rx to Tx (from ACK to DATA mode)

14.8 Switch Time From Rx to Tx (from DATA to ACK mode)

The switch time from Rx to Tx (from DATA to ACK mode), $t_{RxTxDataAck}$, is ≤ 8 µs.

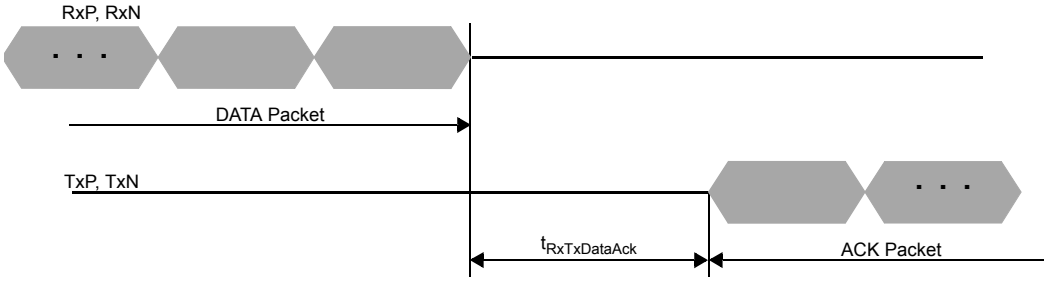


Figure 14: Switch time from Rx to Tx (from DATA to ACK mode)

14.9 Start-up Time for 32 MHz Crystal

The start-up time, t_{XtalSU}, for the 32 MHz quartz oscillator until it reaches a stable frequency generation is ≤ 5 ms.

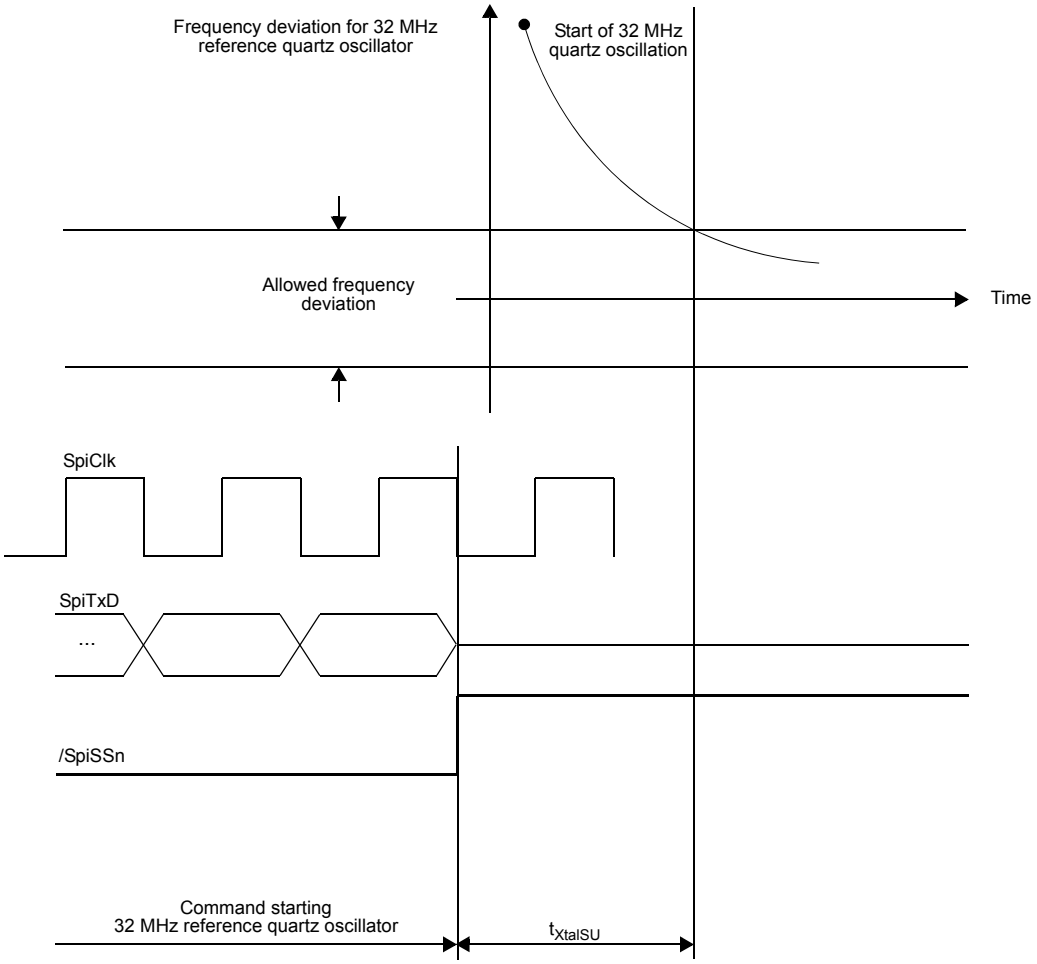


Figure 15: 32 MHz crystal start-up time: time = t_{XtalSU}

14.10 Calibration Time

The calibration time, t_{LOFQ}, is 6 ms.

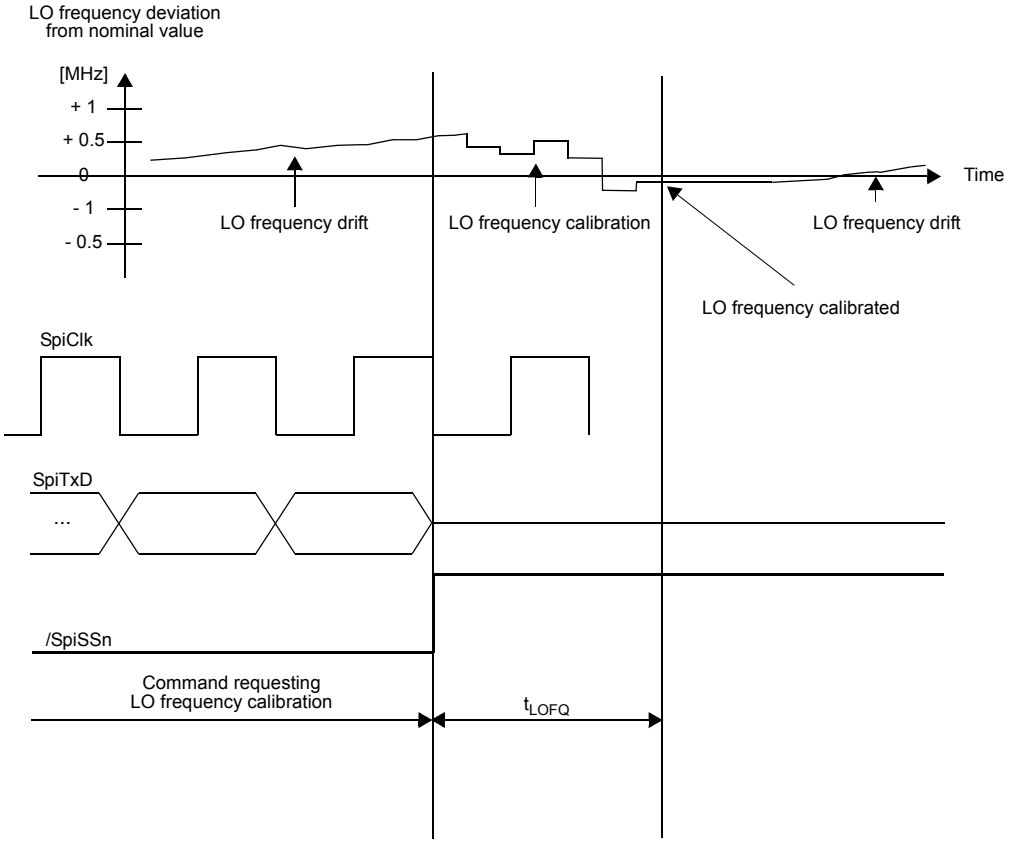


Figure 16: Start-up time for LO frequency calibration

14.11 SPI Bus Write Timing

The following timing diagrams shows the write timing of the SPI bus. For more details, see *the nanoLOC TRX (NA5TR1) Transceiver User Guide*.

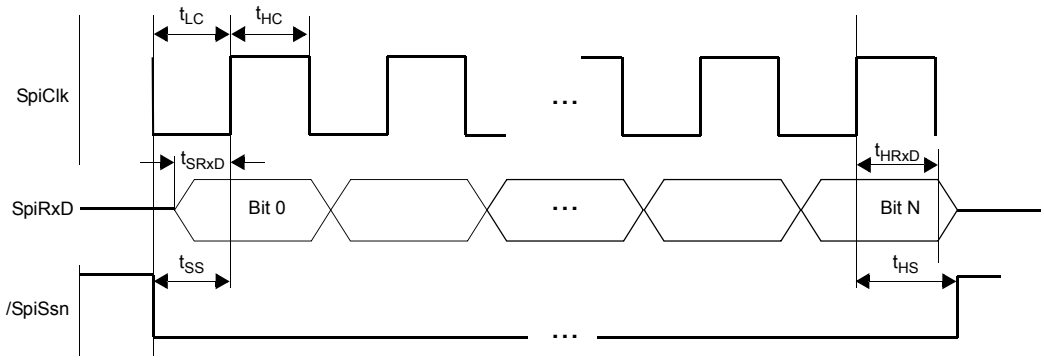


Figure 17: SPI bus write timing

14.12 SPI Bus Read Timing

The following timing diagrams shows the read timing of the SPI bus. For more details, see *nanoLOC TRX (NA5TR1) Transceiver User Guide*.

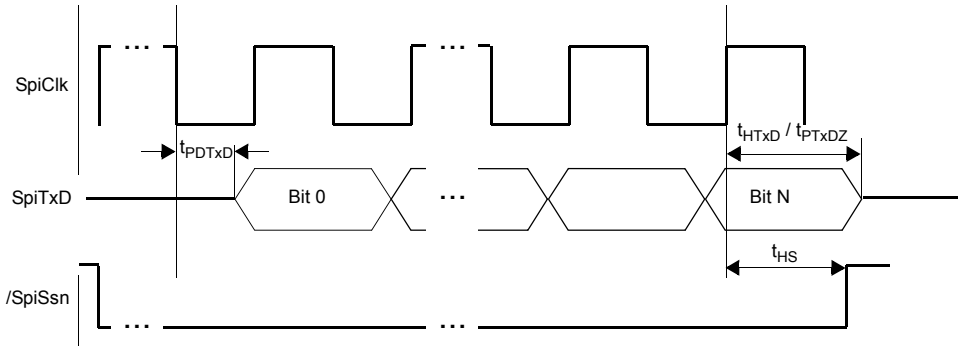


Figure 18: SPI bus read timing

The following table lists the timing values for the SPI bus:

Table 17: SPI bus timing values

Parameter	Minimum	Maximum	Description
f_{max}	–	27 MHz	SpiClk
t_{LC}	18.5 ns	–	Low time SpiClk
t_{HC}	18.5 ns	–	High time SpiClk
t_{SS}	4 ns	–	/SpiSsn Setup
t_{HS}	2 ns	-	SpiSsn Hold
t_{SRxD}	4 ns	–	SpiRxD Setup
t_{HRxD}	2 ns	–	SpiRxD Hold
t_{PDTxD}	–	18.5 ns	SpiTxD Propagation Delay Drive
t_{HTxD}	2.5 ns	–	SpiTxD Hold
t_{PTxDZ}	–	18.5 ns	SpiTxD Propagation Delay High Impedance

15 nanoLOC Ranging

Ranging in the *nanoLOC* chip uses two types of transmissions, which are Data packet and hardware Acknowledgments, to obtain two types of time measurements:

- TX Propagation Delay
- Processing Delay

The chip also offers two ranging modes:

- Normal Ranging Mode
- Fast Ranging Mode

These are briefly discussed below.

15.1 Time Measurements

15.1.1 TX Propagation Delay

This delay is the time for a data or acknowledgement packet to be transmitted from one station to another. As the speed of a signal propagating through the air is known (the speed of light), the time in which a packet is sent from one station to another can be used to calculate the distance between the stations.

15.1.2 Processing Delay

This delay is the time required to process a received data packet and generate and transmit a hardware acknowledgement packet to the sending station. This also is a known value and is used as part of the ranging calculations.

These time measurements are accumulated and with a ranging formula used to obtain a ranging distance between two *nanoLOC* nodes.

15.2 Ranging Modes

15.2.1 Normal Ranging Mode

Normal ranging mode uses a ranging methodology developed by Nanotron called *Symmetrical Double-Sided Two-Way Ranging* (SDS-TWR).[1] This ranging methodology is *symmetrical* in that the measurement from the local *nanoLOC* station to the remote *nanoLOC* station is mirrored by a measurement from the remote *nanoLOC* station to the local *nanoLOC* station (ABA to BAB). It is *Double-Sided* in that only two stations (a remote and a local station) are used for ranging measurements. It is *Two-Way* in that a data packet is sent from one station and a hardware acknowledgement is automatically sent back to the sending station.

1. For more information about SDS-TWR, see the white paper *Real Time Location Systems*.

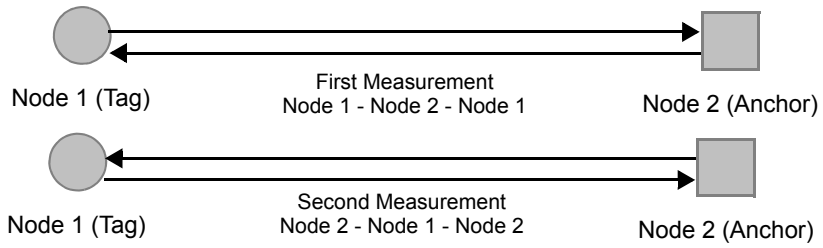


Figure 19: Normal ranging mode

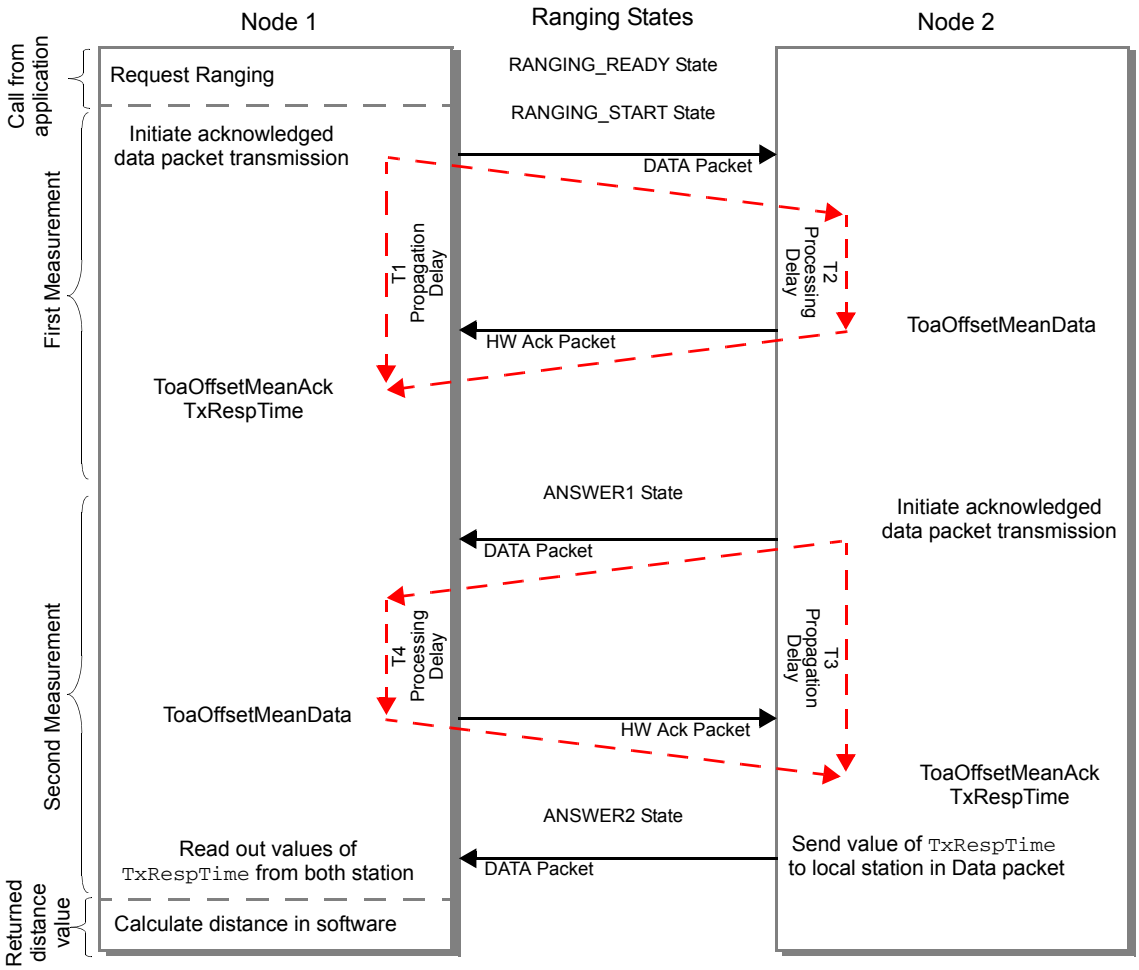


Figure 20: Normal ranging mode using SDS-TWR

Ranging measurements between two nanoLOC stations in normal ranging mode are obtained using the following formula:

$$\text{Distance} = \frac{(T_1 - T_2) + (T_3 - T_4)}{4}$$

Determining ANSWER1

`Answer1` = T_1 - T_2 where

- T_1 = propagation delay time of a round trip between a local and a remote station
- T_2 = processing delay in the remote station

Determining ANSWER2

`Answer2` = T_3 - T_4 where

- T_3 = propagation delay time of a round trip between a remote and a local station
- T_4 = processing delay in the local station

15.2.2 Fast Ranging Mode

Fast ranging mode uses the same ranging methodology as normal ranging mode, except that it is not symmetrical. Only one set of measurements are used (ABA). This increases the speed at which ranging values can be determined, but without the additional validity of the second measurement in normal ranging mode.

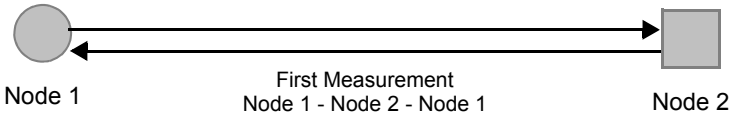


Figure 21: Fast ranging mode

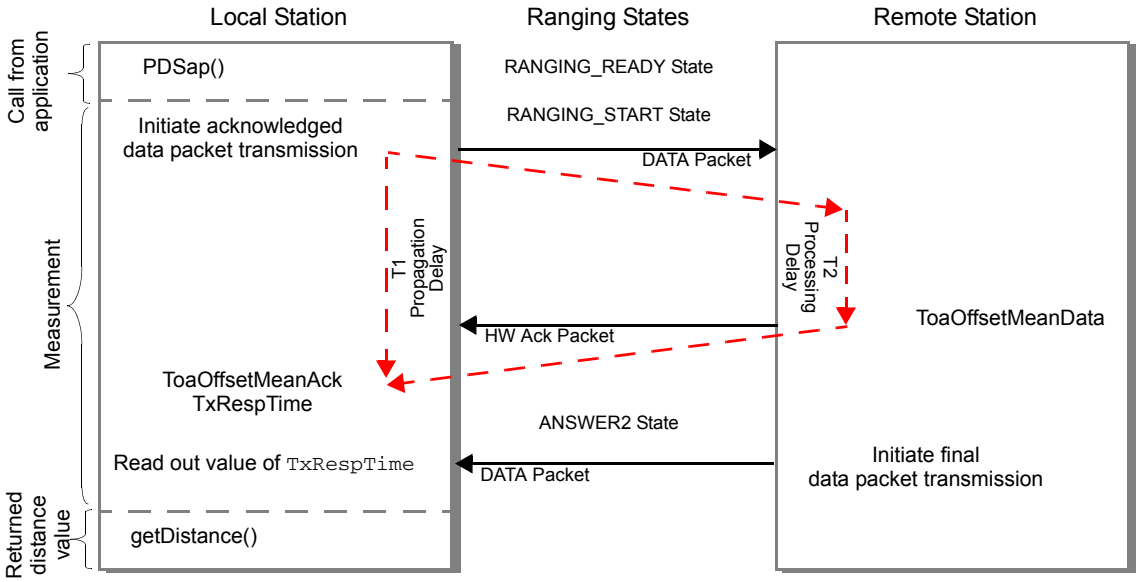


Figure 22: Fast ranging mode using SDS

Ranging measurements between two stations in fast ranging mode are obtained using the following formula:

$$Distance = \frac{(T_1 - T_2)}{2}$$

Determining ANSWER2

$Answer2 = Answer1 = T_1 - T_2$

- T_1 = propagation delay time of a round trip between a local and a remote station
- T_2 = processing delay in the remote station

16 nanoLOC Package (VFQFPN-48)

16.1 MicroLeadFrame® QFN

The *nanoLOC* chip uses the MicroLeadFrame (MLF®), (QFN - Quad Flat No-Lead) package. It is a leadless leadframe based Chip Scale Package (CSP) that enhances chip speed, reduces thermal impedance, and reduces the printed circuit board area required for mounting. The small size and very low profile make it ideal for the *nanoLOC* chip.

MicroLeadFrame® (QFN - Quad Flat No-Lead) package is a near CSP plastic encapsulated package with a copper leadframe substrate. This package uses perimeter lands on the bottom of the package to provide electrical contact to the PCB. The package also offers Exposed Pad technology as a thermal enhancement by having the die attach paddle exposed on the bottom of the package surface to provide an efficient heat path when soldered directly to the PCB. This enhancement also enables stable ground by use of down bonds or by electrical connection through a conductive die attach material.

Figure 23 below shows the basic construction and view of the MLF® QFN package.

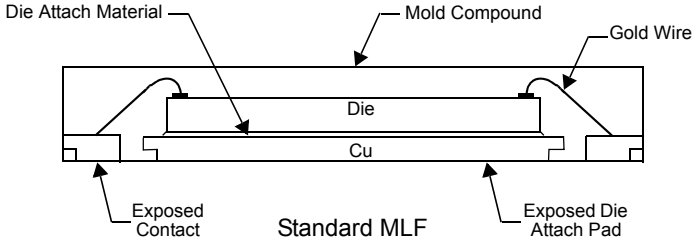


Figure 23: Basic construction of standard MLF package

16.2 VFQFPN-48 Package (7 x 7 x 1.0mm)

The *nanoLOC* chip uses a type of MicroLeadFrame® (QFN - Quad Flat No-Lead) package called VFQFPN-48. It is a thermally enhanced **V**ery thin **F**ine pitch **Q**uad **F**lat **P**ackage **N**o lead chip with 48 pins. Figure 24 below shows the dimensions of the VFQFPN-48 package.

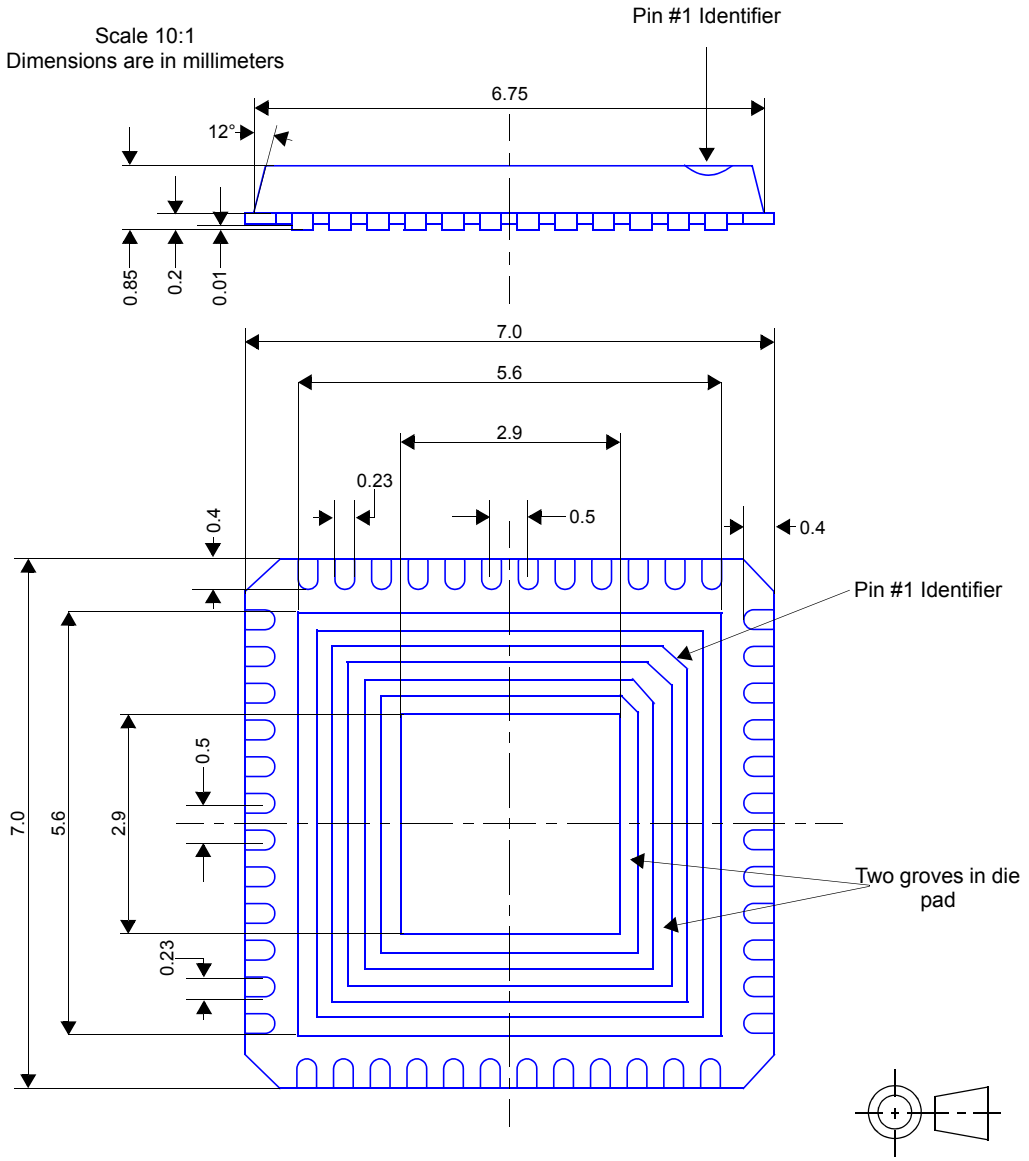


Figure 24: VFQFPN2-48 package dimensions

16.3 Recommended Footprint Dimensions

Figure 25 below shows the recommended footprint data (dimensions) for the *nanoLOC* chip (NA5TR1).

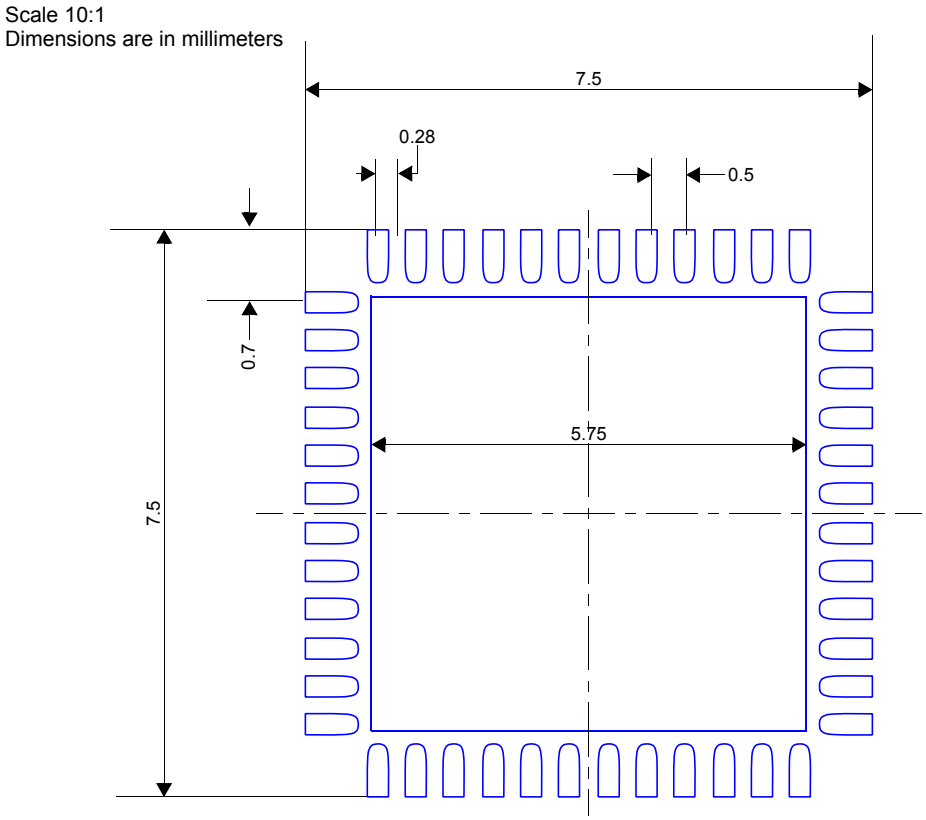


Figure 25: Package VFQFPN2-48 recommended footprint dimensions

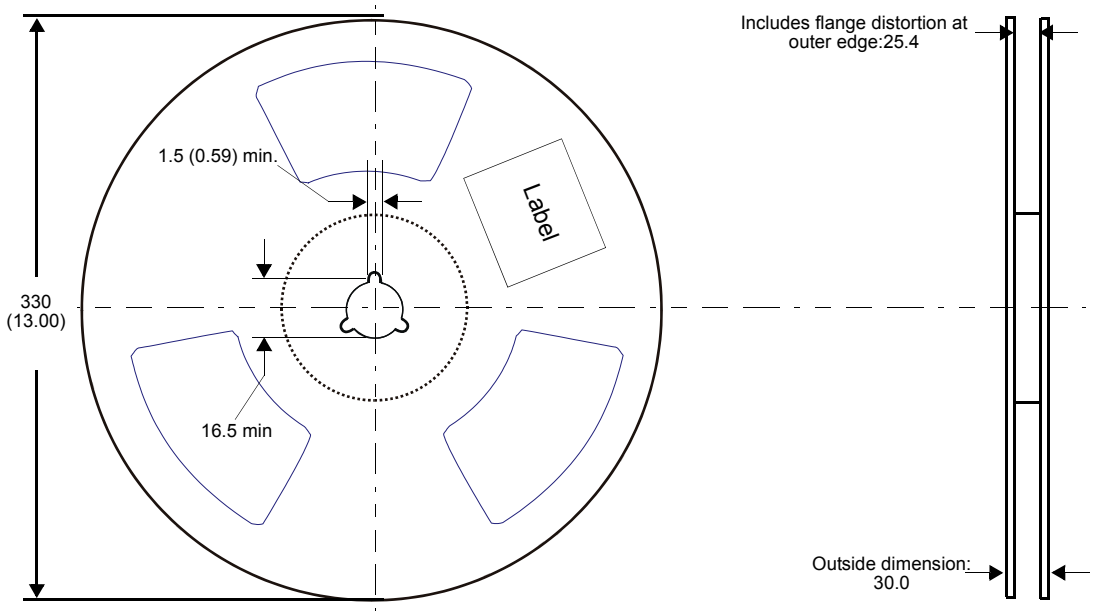
17 Tape and Reel Information

An embossed tape and reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for the *nanoLOC* chip *(NA5TR1)* and requires a minimum of handling. The antistatic/ conductive tape provides a secure cavity for the product when sealed with the peel-back cover tape.

17.1 Reel Dimensions

Reel Diameter	Units Per Reel	Reel and Hub Size[1]
13”	2,500	13/4

1. *Reel and hub size = 13 inch reel with 4 inch hub.*



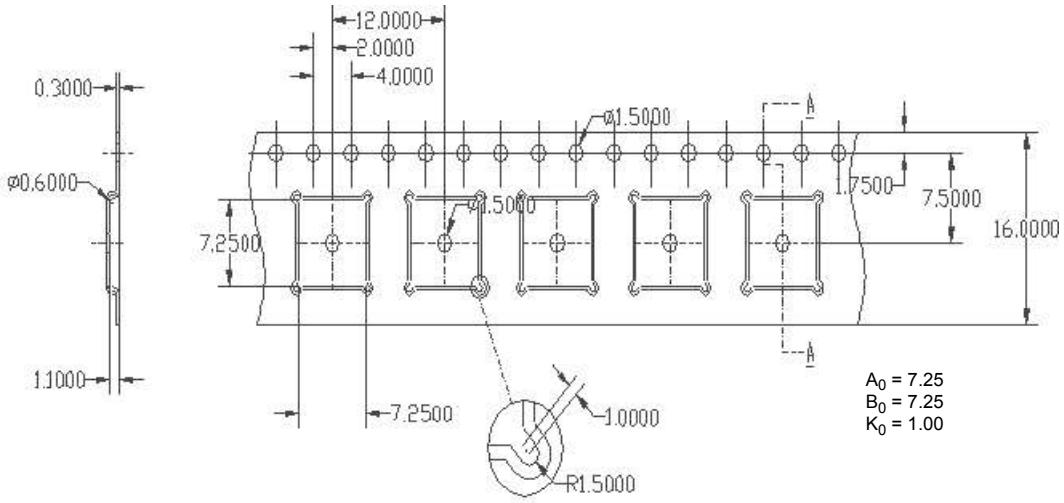
Note: Dimensions are in millimeters

Figure 26: Reel dimensions

17.2 Tape Dimensions

Package Type	Number of Leads	Nominal Package Size	Carrier Tape Width	Carrier Tape Pitch	Leader/Trailer Length[1]
VFQFPN-48	48	7 x 7 x 1 mm	16 mm	12 mm	EIA

1. *The device loading orientation is in compliance with EIA-481.*



Notes:
1. Dimensions are in millimeters
2. 10 sprocket hole pitch cumulative tolerance ± 0.2
3. Carrier in compliance with EIA 481
4. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Figure 27: Tape dimensions

18 Ordering Information

Note: To order the product described in this datasheet, use the following information.

Table 18: nanoLOC TRX Transceiver (NA5TR1) Ordering Information

Part Description	Part Number	Additional Information
nanoLOC TRX Transceiver (NA5TR1)	NLSG0501A	*nanoLOC Development Kit* and *nanoLOC Driver* are also available.

A1 Example Application - RF Module

A1.1 Schematics

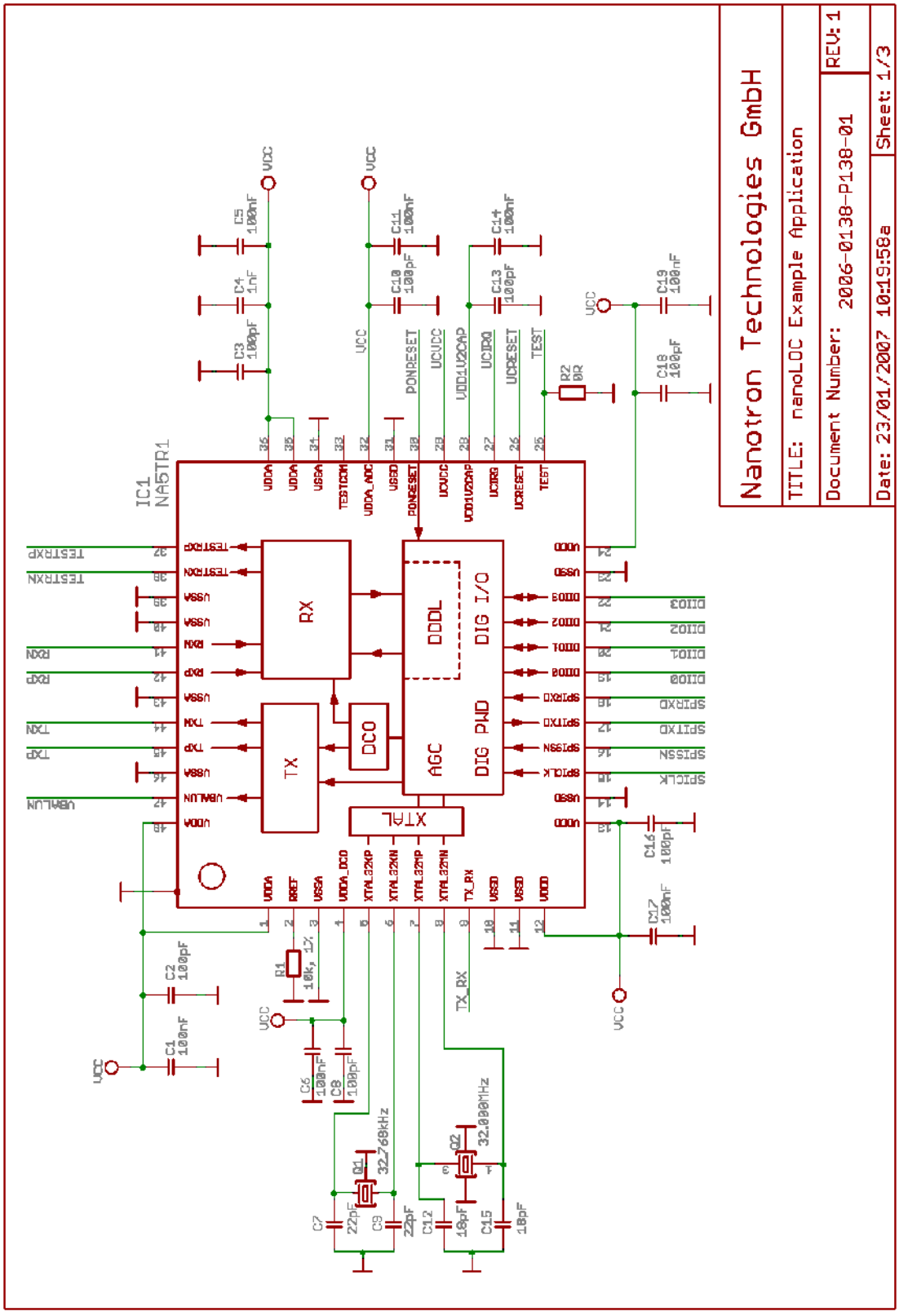


Figure 28: Example Application – schematics 1 of 3

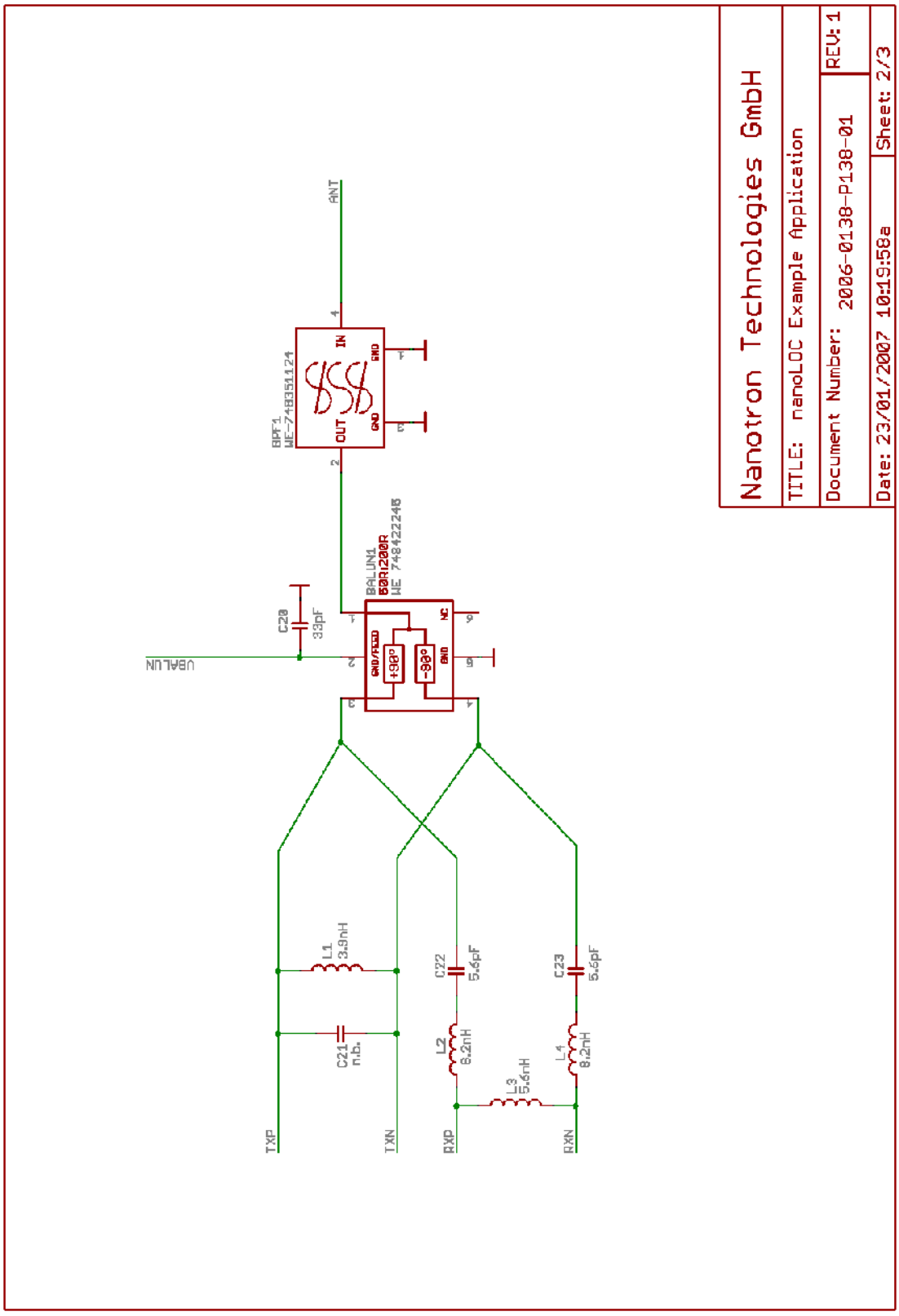


Figure 29: Example Application – schematics 2 of 3

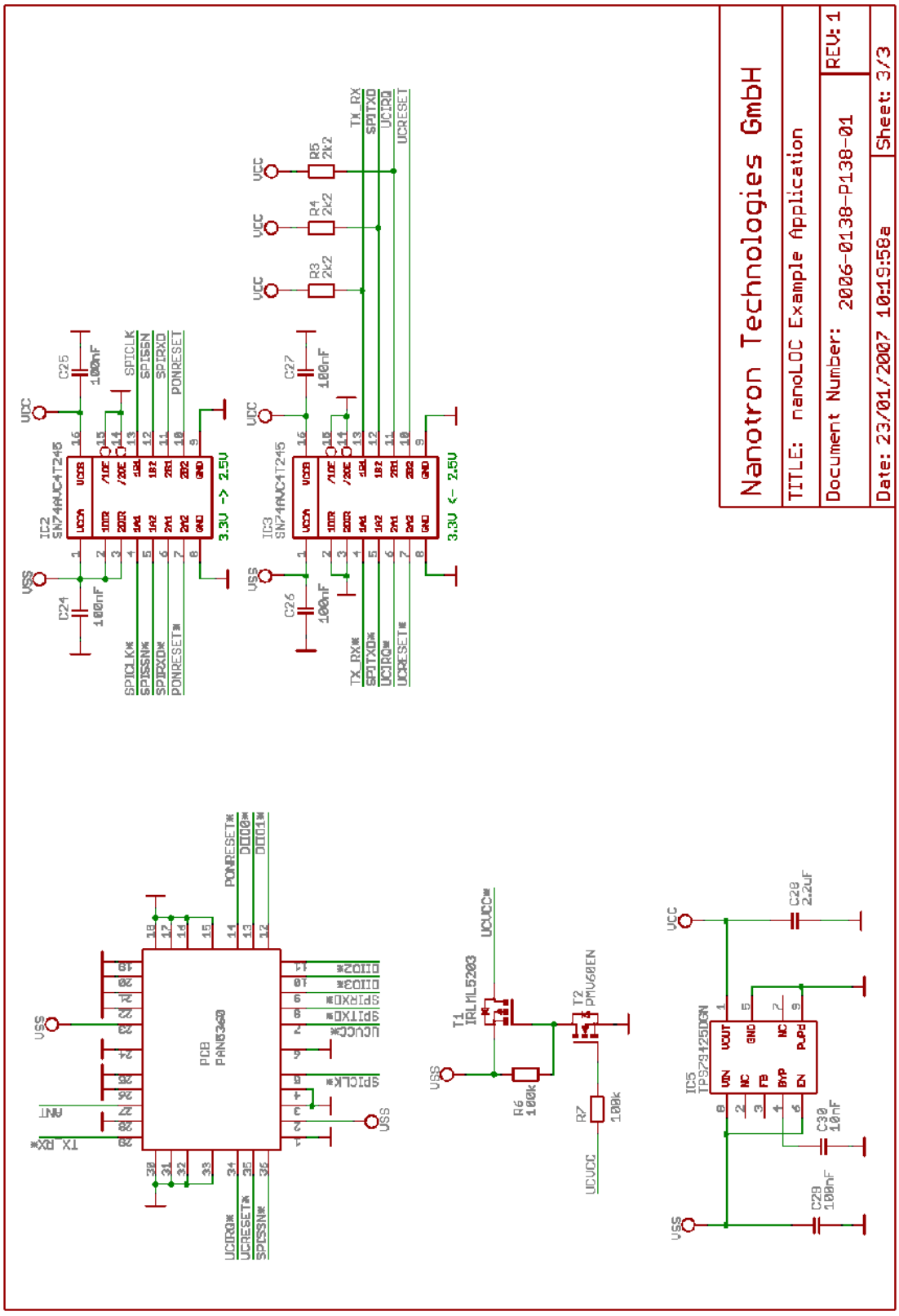


Figure 30: Example Application – schematics 3 of 3

A1.2 PCB Layout

Note: As this example application includes level shifters, it can be used in a variety of 3 volt environments, controllers, and other circuits. To work in a 2.5 volt environment, voltage converters are not required. The board dimensions are 30 mm x 20 mm.

Scale = 3:1

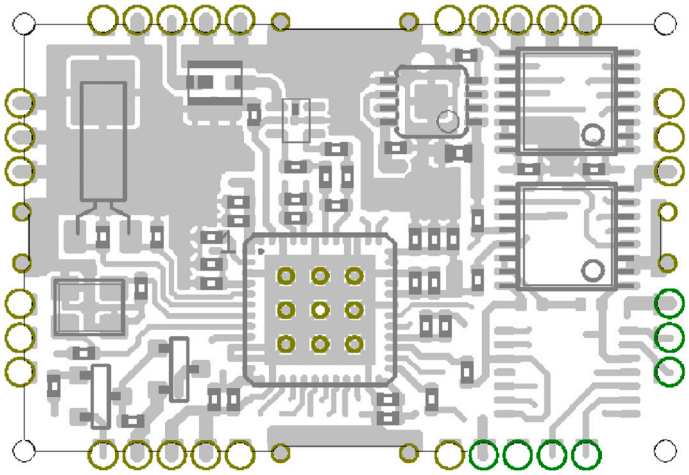


Figure 31: Example Application– top components

Scale = 3:1

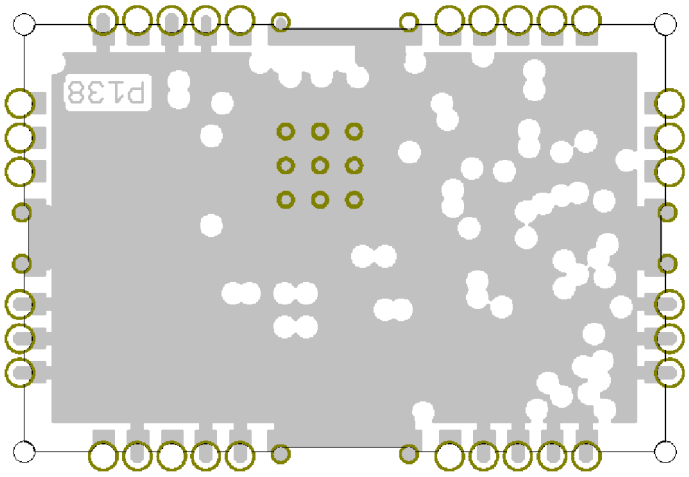


Figure 32: Example Application: bottom layer (inverted)

Scale = 3:1

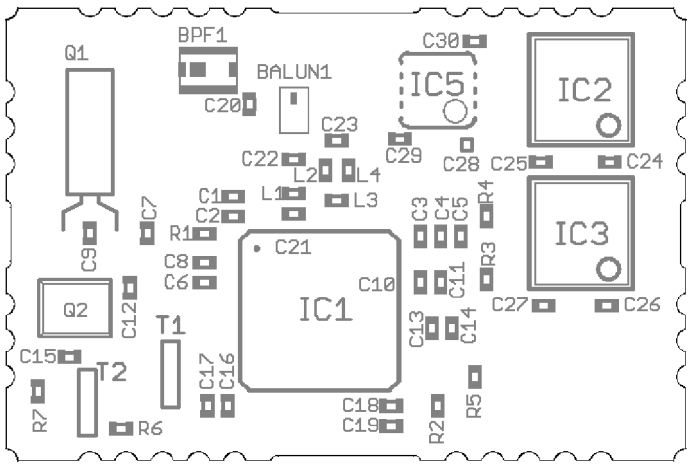


Figure 33: Example Application: top components

A1.3 Example Application Bill of Materials

Table 19: Example Application bill of materials

Description	Label	Value	Qty	Package	Remarks	Supplier/Order No.
Resistor	R2	0R	1	0402	Not specified	Not specified
	R3, R4, R5	2k2	3	0402	63mW, ±5%	Not specified
	R1	10k, 1%	1	0402	63mW, ±1%	Not specified
	R6, R7	100k	2	0402	63mW, ±5%	Not specified
Capacitor	C21	n.a.	–	0402	Not specified	Not specified
	C22, C23	5.6pF	2	0402	NPO, 50V, ±5%	Not specified
	C7, C9	22pF	2	0402	NPO, 50V, ±5%	Not specified
	C12, C15	18pF	2	0402	NPO, 50V, ±5%	Not specified
	C20	33pF	1	0402	NPO, 50V, ±5%	Not specified
	C2, C3, C8, C10, C13, C16, C18	100pF	7	0402	NPO, 50V, ±5%	Not specified
	C4	1nF	1	0402	NPO, 50V, ±5%	Not specified
	C30	10nF	1	0402	X7R, 10V, ±10%	Not specified
	C1, C5, C6, C11, C14, C17, C19, C24, C25, C26, C27, C29	100nF	12	0402	X7R, 10V, ±10%	Not specified
	C28	2.2uF	1	0603	X5R, 6.3V, ±10%	Not specified
Inductor	L1	3.9nH	1	0402	WE-MK	Wuerth Elektronik WE 744784039
	L3	5.6nH	1	0402	WE-MK	Wuerth Elektronik WE 744 784056
	L2, L4	8.2nH	2	0402	WE-MK	Wuerth Elektronik WE 744 784082
Balun 50R:200R	BALUN1	WE 748422245	1	BAL0805	ISM 2.44GHz, 50R:200R	Wuerth Elektronik WE 748422245
Bandpass Filter 2.4GHz	BPF1	WE-748351124	1	WE-BPF1008	ISM 2.44GHz	Wuerth Elektronik WE 748351124
Clock Crystal	Q1	32.768kHz	1	MS1V-TK	±20ppm @ -40°C ... +85°C, CL=12.5pF	GOLLEDGE MS1V-T1K 32.768kHz±20ppm
	Q2	32.000MHz	1	TSX-3225	±20ppm @ -40°C ...+85°C, CL=12pF	Epson Toycoon Q32.0000TSX3225+ET0
P-Channel MOSFET	T1	IRLML5203	1	SOT-23	µTrenchMOS enhancement mode FET	International Rectifier IRLML5203PbF
N-Channel MOSFET	T2	PMV60EN	1	SOT-23	HEXFET Power MOSFET	Philips Semiconductor PMV60EN
nanoLOC TRX Transceiver	IC1	NA5TR1	1	VFQFPN48	nanoLOC chip	Nanotron Technologies NA5TR1
Level Shifters	IC2, IC3	SN74AVC4T245	2	TSSOP16	4 Bit dual supply bus transceiver	Texas Instruments SN74AVC4T245PWT
Voltage Regulator	IC5	TPS79425DGN	1	MSOP-8	LD Voltage Regulator	Texas Instruments TPS79425DGNT
PCB	PCB	P138	1	30 x 20 mm	Not specified	Nanotron Technologies P138

Intentionally Left Blank

A2 nanoLOC RF Test Module

A2.1 Overview

The *nanoLOC RF Test Module* was designed for testing and measurement purposes only. It was used during measurements and simulations to determine parameters published in this document, unless otherwise specified. For conducting tests purposes, the *nanoLOC RF Test Module* includes a 50 Ω coaxial SMA connector.

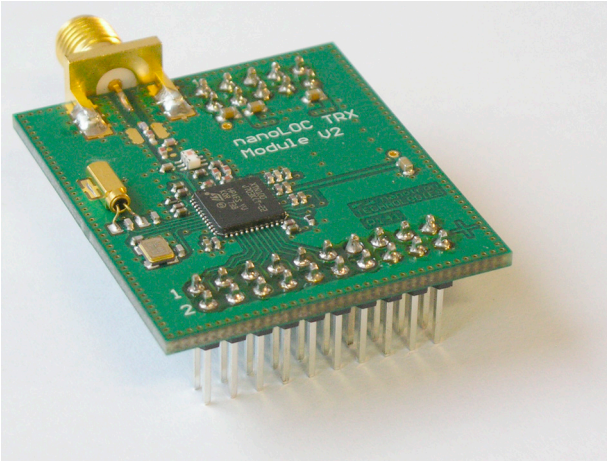


Figure 34: nanoLOC RF Test Module

A2.2 Schematics

The following schematics represents the following major blocks of the design:

- Schematic 1: Power supply for *nanoLOC* chip and connection with crystal resonators.
- Schematic 2: RF interface between *nanoLOC* chip and SMA connector (impedance matching circuitry for Rx and Tx, balun).
- Schematic 3: Interface to the automatic test equipment.

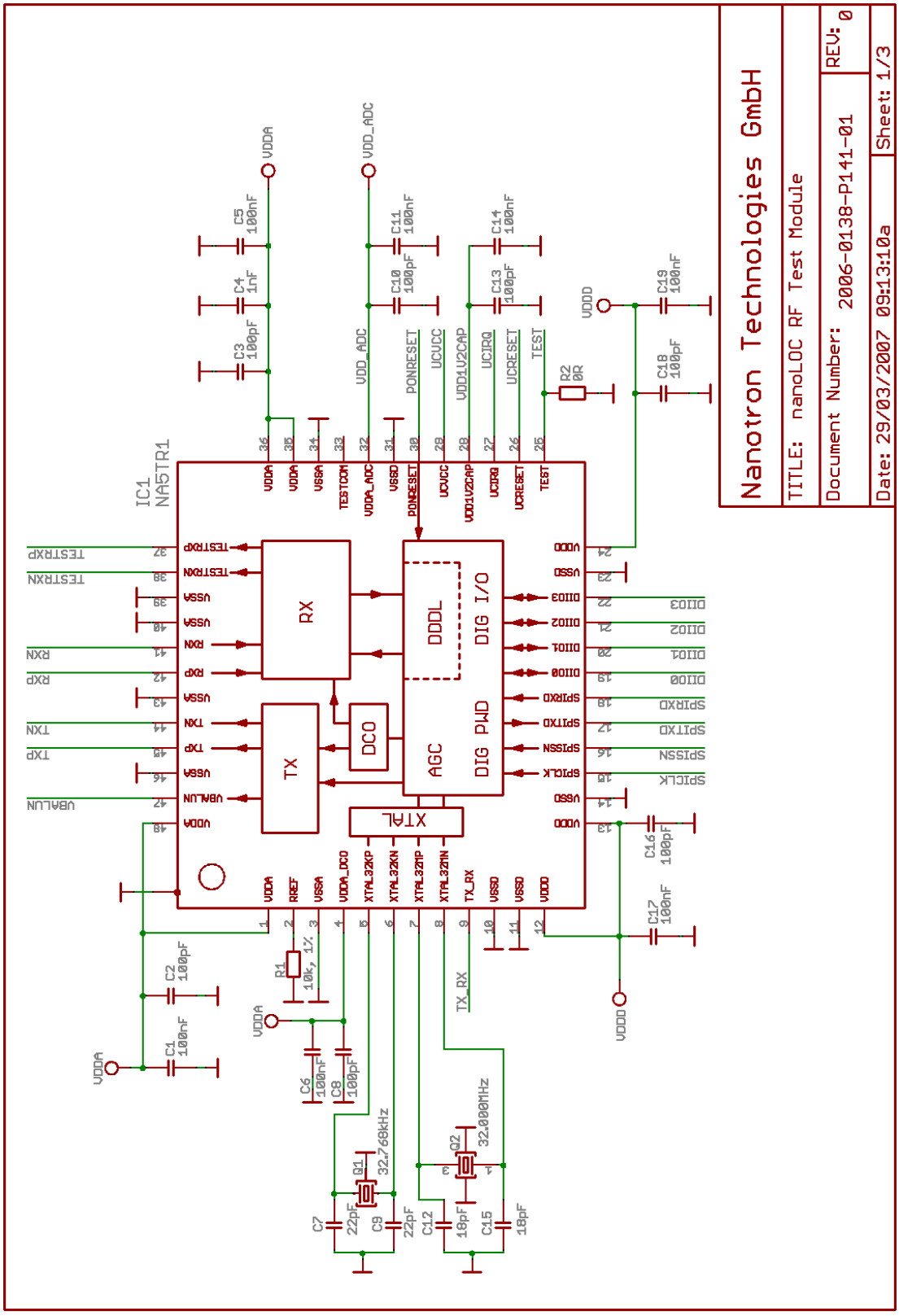


Figure 35: nanoLOC RF Test Module: schematics 1

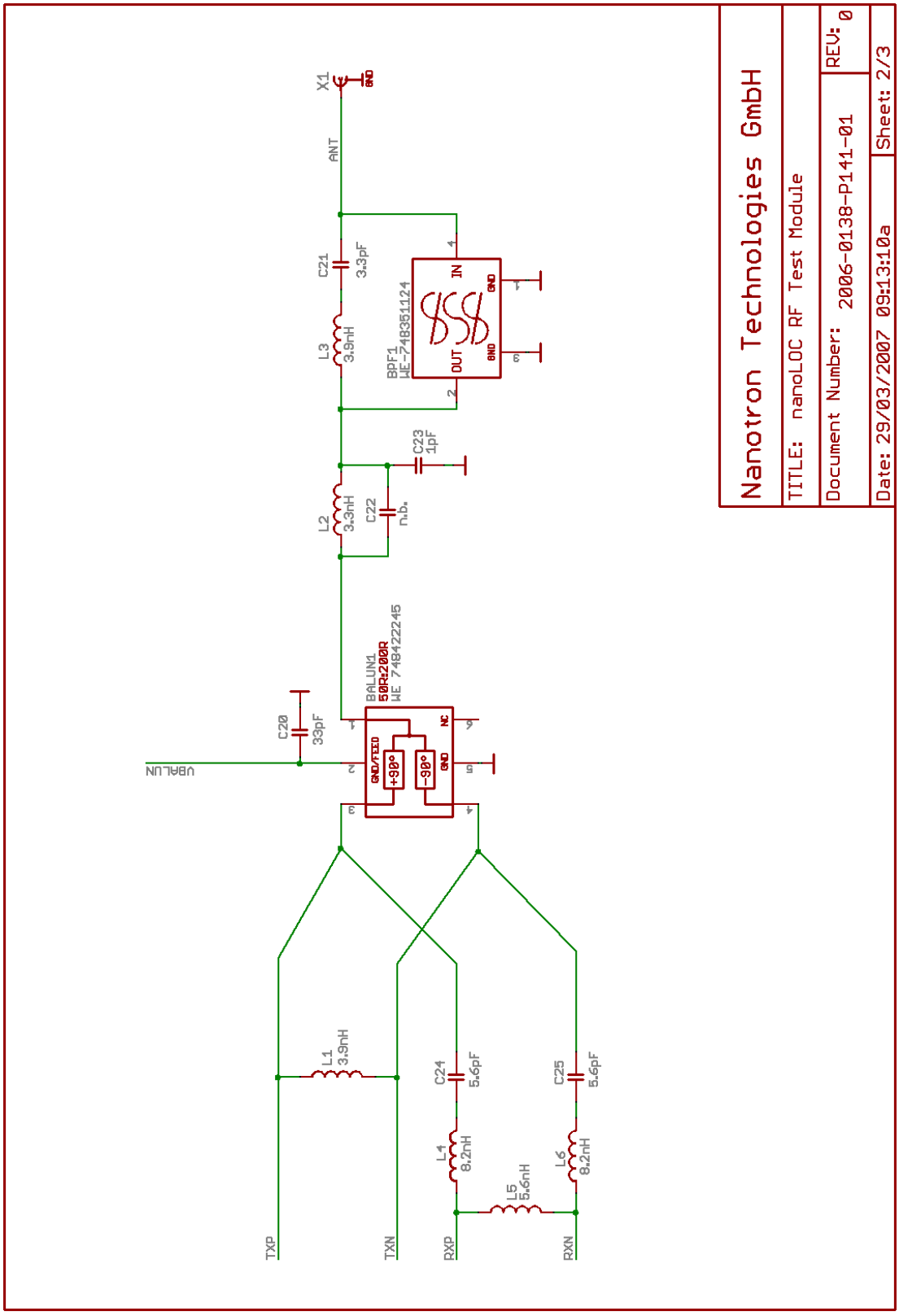


Figure 36: RF Test Module: schematics 2

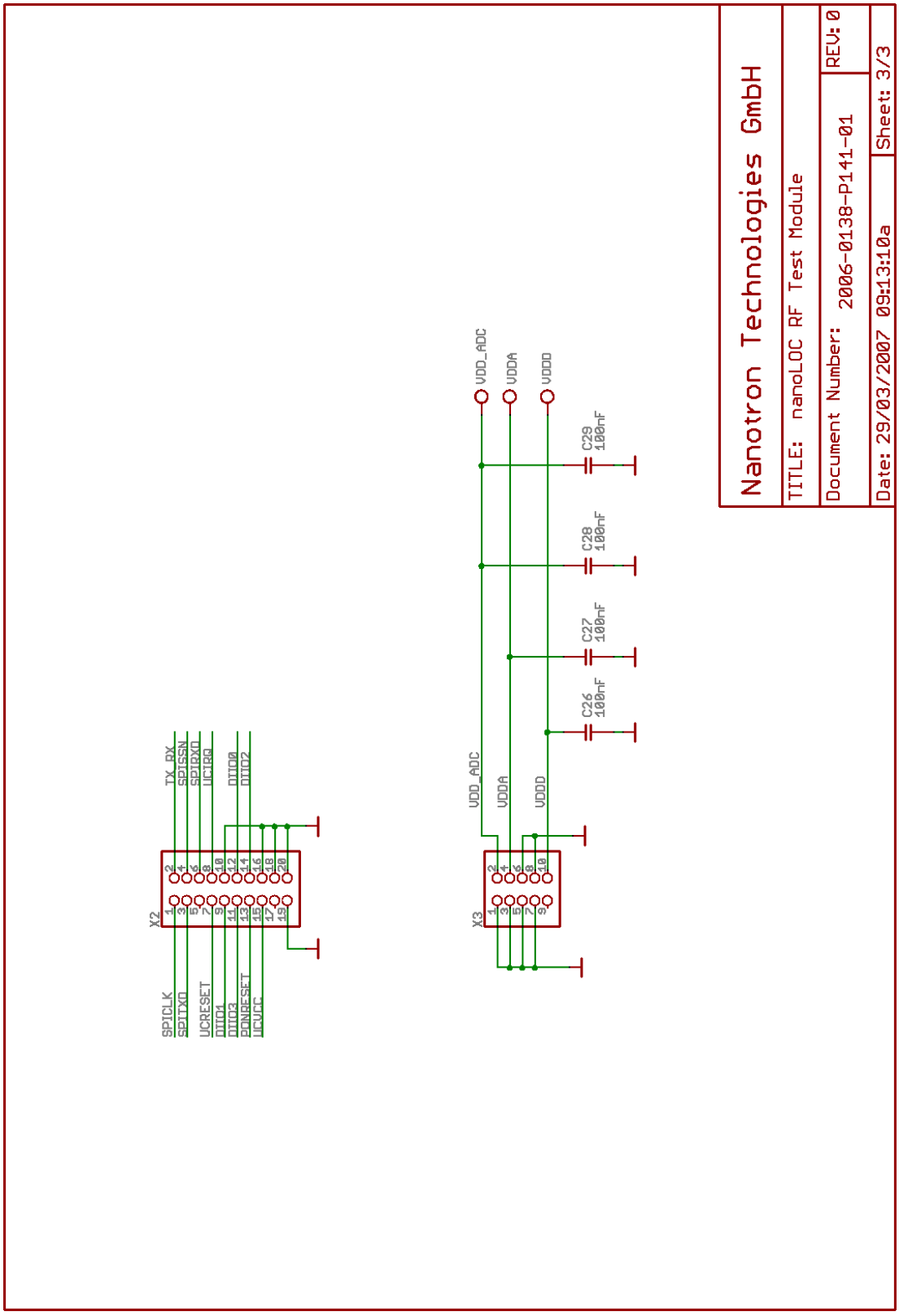


Figure 37: RF Test Module: schematics 3

A2.3 PCB Layout

Scale = 2:1

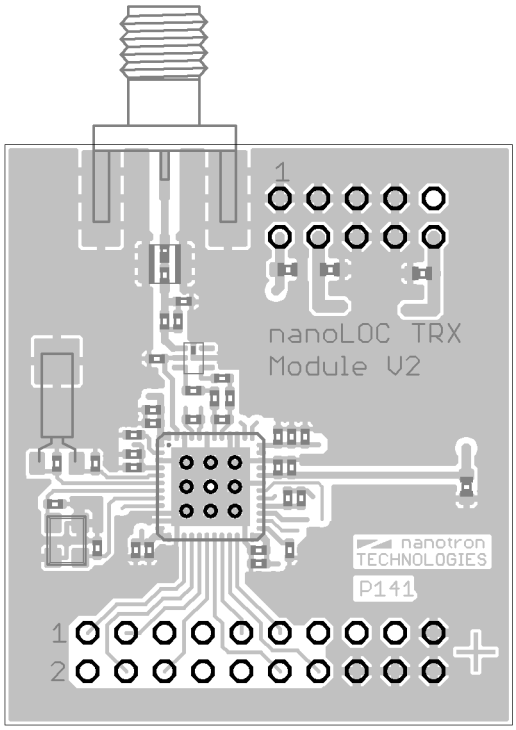


Figure 38: nanoLOC RF Test Module – top layer

Scale = 2:1

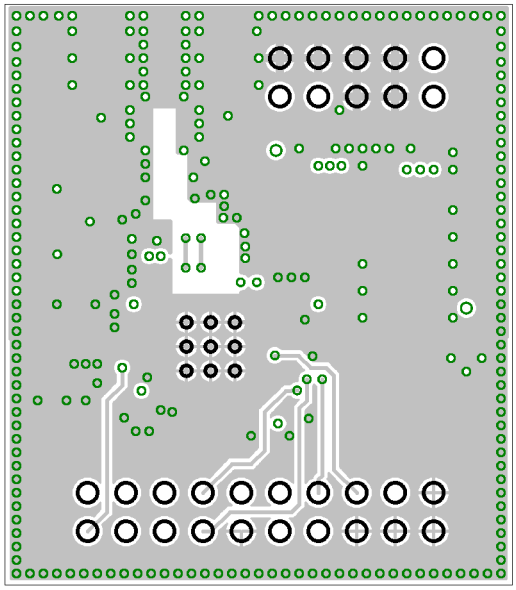


Figure 39: nanoLOC RF Test Module – 2nd layer

Scale = 2:1

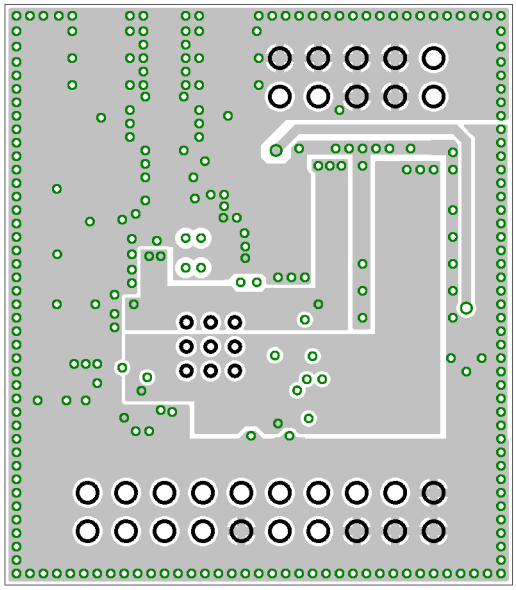


Figure 40: nanoLOC RF Test Module – 3rd layer

Scale = 2:1

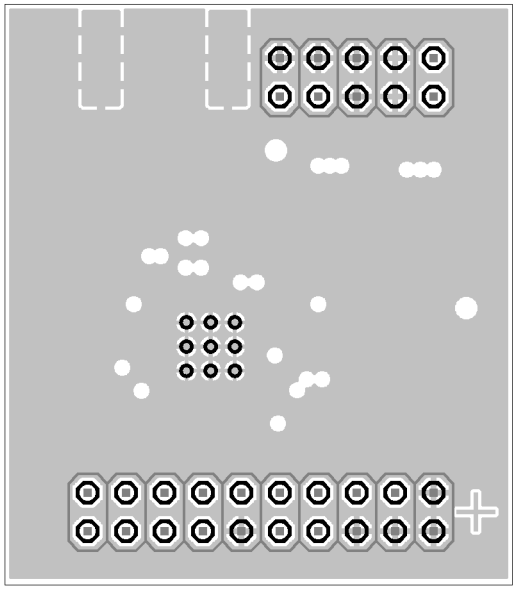


Figure 41: nanoLOC RF Test Module – bottom layer

Scale = 2:1

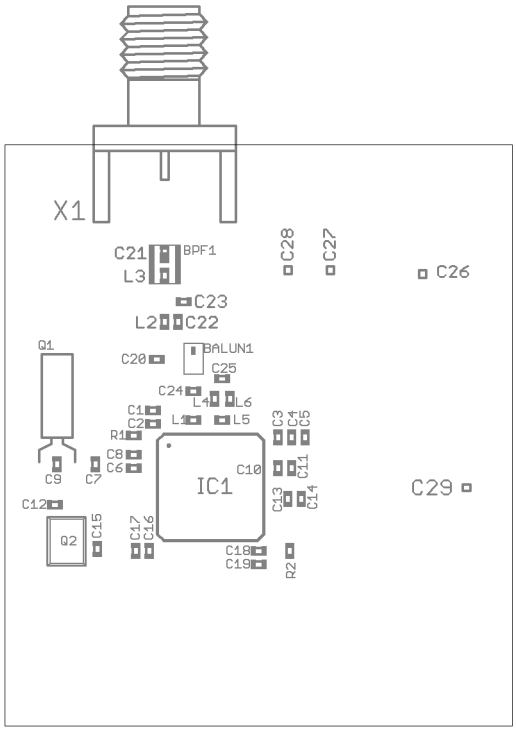


Figure 42: nanoLOC RF Test Module – top components

Scale = 2:1

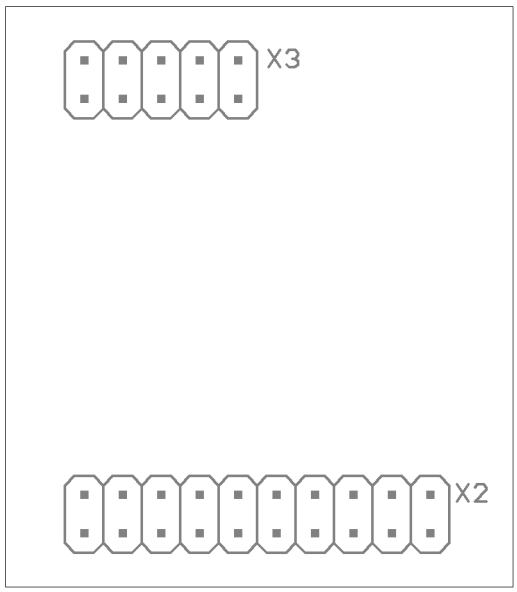


Figure 43: nanoLOC RF Test Module – bottom components (inverted)

A2.4 RF Test Module Bill of Materials (BOM)

Table 20: RF Test Module bill of materials

Description	Label	Value	QTY	Package	Remarks	Company	Product Number
Balun	BALUN1	WE 748422245	1	BAL0805	2x200R:50R	Wuerth Elektronik	WE 748422245
Band pass filter	BPF1	Not assembled	1	–	–	–	–
Capacitors	C23	1pF	0	0402	–	–	–
	C21	3.3pF	1	0402	NPO, 50V, 5%	–	–
	C24, C25	5.6pF	2	0402	NPO, 50V, 5%	–	–
	C12, C15	18pF	2	0402	NPO, 50V, 5%	–	–
	C7, C9	22pF	2	0402	NPO, 50V, 5%	–	–
	C20	33pF	1	0402	NPO, 50V, 5%	–	–
	C2, C3, C8, C10,C13, C16, C18	100pF	7	0402	NPO, 50V, 5%	–	–
	C4	1nF	1	0402	X7R, 10V, ±10%	–	–
	C1, C5, C6, C11, C14, C17, C19	100nF	7	0402	X7R, 10V, ±10%	–	–
	C22	Not assembled	1	–	–	–	–
	C26, C27, C28, C29	100nF	4	0603	X7R, 10V, ±10%	–	–
Connectors	X1	JOHNSON_JACK_GND_2	1	JOHNSON_JACK_GND_2	End Launch Jack Receptacle	Johnson Components	142-0701-851
	X2	2X10	1	Pin Header 2X10	10 Pins, double Row, pitch 2.54mm	Winslow Adaptics	W82120T3825
	X3	2X05	1	Pin Header 2X05	5 Pins, double Row, pitch 2.54mm	Winslow Adaptics	W82110T3825
Clock crystals	Q1	32.768kHz	1	MS1V-TK	CL=12.5pF	Golledge	MS1V-T1K 32.768kHz ±20ppm
	Q2	32.000MHz	1	32SMX	CL=12pF	Petermann Technik	SMD03025/4 32.000 MHz AT-FUND 10/20/-40+85/12pF/40R
Inductors	L2	3.3nH	1	0402	–	Wuerth Elektronik	WE 744784033
	L1, L3	3.9nH	2	0402	–	Wuerth Elektronik	WE 744784039
	L5	5.6nH	1	0402	–	Wuerth Elektronik	WE 744784056
	L4, L6	8.2nH	2	0402	–	Wuerth Elektronik	WE 744784082
ICs	IC1	NA5TR1	1	QFN48	–	Nanotron Technologies	NLSG0501A
PCB	PCB1	P141	1	–	–	–	CONTAG
Resistors	R2	0R	1	0402	–	–	–
	R1	10k, 1%	1	0402	63mW, ±1%	–	–

A3 Abbreviations and Symbols

A3.1 Abbreviations

µA . . . . . Microampere (unit of electrical current)
µC . . . . . Microcontroller
µCIrq . . . . . External microprocessor interrupt request
µCReset . . . External microprocessor reset
µCVcc . . . . . External microprocessor battery supply voltage
µCVccExt. . . External microprocessor power supply voltage
µF . . . . . Microfarad (unit of electrical capacitance)
µH . . . . . Microhenry (unit of electrical inductance)
µs. . . . . Microseconds (unit of time)
Ω . . . . . Ohm (unit of electrical resistance)
AC . . . . . Alternating Current
Ack . . . . . Acknowledgement packet type
ADC. . . . . Analogue to Digital Converter
AFC . . . . . Automatic Frequency Control
AGC. . . . . Automatic Gain Control
ASIC . . . . . Application Specific-IC
B . . . . . Battery
B . . . . . Frequency bandwidth
BA . . . . . Balun (See BALUN)
BALUN . . . . Balun Unbalanced
BCH. . . . . Bose-Chaudhuri-Hochquenghem
BER . . . . . Bit Error Rate
BOM . . . . . Bill of Materials
bps. . . . . Bits per second (unit of data throughput)
C . . . . . Capacitor
C . . . . . Power of signal carrier
°C . . . . . Celsius (unit of temperature)
CCITT . . . . . Comité Consultatif International Téléphonique et Télégraphique
CDDL. . . . . Complementary Dispersive Delay Line
C/I . . . . . Carrier to Interference Ratio
Clk . . . . . Clock
CRC. . . . . Cyclic Redundancy Check
CMMR . . . . . Common Mode Rejection Ratio
CMOS . . . . . Complementary Metal Oxide Semiconductor
CS . . . . . Chip Select
CSMA . . . . . Carrier Sense Multiple Access
CSMA/CA . . Carrier Sense Multiple Access/Collision Avoidance
CSS . . . . . Chirp Spread Spectrum
CSS Mode . . Chirp Spread Spectrum Mode
DAC. . . . . Digital to Analog Converter
Data. . . . . Data packet type
dB . . . . . Decibel (ratio between two values, such as signal power, voltage, or current levels in logarithmic scale)
dBi . . . . . Gain referenced to isotropic antennae
DBO-CSS . . Differentially Bi-Orthogonal Chirp Spread Spectrum
dBm. . . . . dB referenced to one milliwatt (10^{-3}W = 1mW)
dBr. . . . . Decibels relative to reference level
DC . . . . . Direct Current
DiIO . . . . . Digital Input/Output
DPA . . . . . Differential Power Amplifier
DPD. . . . . Differential Peak Detector
DUT. . . . . Device Under Test
E_b . . . . . Energy of bit
EIRP . . . . . Effective Isotropic Radiated Power
ESD. . . . . Electrostatic Discharge
FCD. . . . . Folded Chirp Detector
FCM. . . . . Folded Chirp Mixer
FDMA . . . . . Frequency Division Multiplex Access
FEC. . . . . Forward Error Correction
FET . . . . . Field Effect Transistor
FHSS. . . . . Frequency Hopping Spread Spectrum
FIFO . . . . . First In First Out
FS . . . . . Full Scale
GBWP . . . . . Gain Bandwidth Product
GHz . . . . . Gigahertz (unit of frequency)
GND . . . . . Ground
HBM . . . . . Human Body Model
I . . . . . Inline
IC. . . . . Integrated Circuit
IEC . . . . . International Electrotechnical Commission
IF . . . . . Intermediate Frequency
I/O . . . . . Input/Output
I_{OH} . . . . . Output current high level
I_{OL} . . . . . Output current low level
IRQ . . . . . Interrupt request
IQ. . . . . In-phase, Quadrature
ISM . . . . . Industrial Scientific Medical
ISO . . . . . International Organization for Standardization
kΩ . . . . . Kiloohms (unit of electrical resistance)
kHz . . . . . Kilohertz (unit of frequency)
kpbs. . . . . Kilobits per second (unit of data throughput)
L. . . . . Inductance
LNA . . . . . Low Noise Amplifier
LO . . . . . Local Oscillator
LPF . . . . . Low Pass Filter
LSB . . . . . Least Significant Bit
MΩ. . . . . Megaohms (unit of electrical resistance)
mA. . . . . Milliampere (unit of electrical current)
Mbaud . . . . . Megabauds
Mbps . . . . . Megabits per second (unit of data throughput)
MAC. . . . . Medium Access Control
MHz. . . . . Megahertz (unit of frequency)
MISO . . . . . Master In, Slave Out
MIX . . . . . Mixer
MLF . . . . . Micro Lead Frame Package
MOD . . . . . Modulator
MOSI . . . . . Master Out Slave In
MUX. . . . . Multiplexer
mW . . . . . milliwatt (unit of power)
nc. . . . . Not connected
nF . . . . . Nanofarad (unit of electrical capacitance)
nH . . . . . Nanohenry (unit of electrical inductance)
N_o . . . . . Power spectral density of thermal noises
ns. . . . . Nanosecond (unit of time)
OEM . . . . . Original Equipment Manufacturer
OSC. . . . . Oscillator
OP . . . . . Operational Amplifier
OTA . . . . . Operational Transconductance Amplifier
PA . . . . . Power Amplifier
PAE . . . . . Power Added Efficiency
PAMP. . . . . Power Amplifier
PDK. . . . . Process Development Kit
PEP . . . . . Peak Envelope Power
pF . . . . . Picofarad (unit of electrical capacitance)
PFD . . . . . Phase Frequency Detector
PLL . . . . . Phase Locked Loop
P_{out} . . . . . Power Out
ppm . . . . . parts per million
PCB . . . . . Printed Circuit Board
PGA. . . . . Programmable Gain Amplifier
PGC. . . . . Power Gain Control
POMD . . . . . Peak Over Mean Detector
PSRR. . . . . Power Supply Rejection Ratio
PTAT . . . . . Proportional to Absolute Temperature
Q . . . . . Quadrature
QFN. . . . . Quad Flat No-lead
R . . . . . Resistor
RF . . . . . Radio Frequency
RFID . . . . . Radio Frequency IDentification
ROM . . . . . Read Only Memory
RSSI . . . . . Radio Signal Strength Indicator
RTC . . . . . Real Time Clock
Rx . . . . . Receiver
S . . . . . Switch/button
SAR . . . . . Successive Approximation Register
SAW . . . . . Surface Acoustic Wave
SDS-TWR . . Symmetrical Double Sided Two Way Ranging
SLNA . . . . . Symmetric Low Noise Amplifier
SMIX . . . . . Symmetric Mixer
SNR. . . . . Signal to Noise Ratio
SPI. . . . . Serial Peripheral Interface
SpiClk . . . . . Serial peripheral interface Clock
SpiSsn . . . . . Serial peripheral interface Slave select
SpiRxD. . . . . Serial peripheral interface Receive Data
SpiTxD . . . . . Serial peripheral interface Transmit Data
SRAM . . . . . Static RAM
SSB . . . . . Single Side Band

t . . . . . Time constant
T . . . . . Duration time of the chirp waveform
TBD . . . . . To Be Determined
TDMA . . . . . Time Division Multiple Access
T_{junct} . . . . . Temperature of junction
THD . . . . . Total Harmonic Distortion
TRL . . . . . Transmission Line
TRX . . . . . Transceiver
TTL . . . . . Transistor-Transistor Logic
Tx . . . . . Transmitter
V . . . . . Volts (unit of electrical potential)
V_{IH} . . . . . Input voltage for High level
V_{IL} . . . . . Input voltage for Low level
V_{OH} . . . . . Output voltage for High level
V_{OL} . . . . . Output voltage for Low level
VCA . . . . . Voltage Controlled Amplifier
V_{CC} . . . . . Battery supply voltage
VCO . . . . . Voltage Controlled Oscillator
V_{DDA} . . . . . Power supply for analog part
V_{DDD} . . . . . Power supply for digital part
VFQFPN . . . Very thin Fine pitch Quad Flat Pack Nolead Package
VGA . . . . . Variable Gain Amplifier
V_{SSA} . . . . . Analog ground
V_{SSD} . . . . . Digital ground
VSWR . . . . . Voltage Standing Wave Ratio
XTAL . . . . . Crystal
XCO . . . . . Xtal (crystal) Controlled Oscillator

A3.2 Special Symbols

C_{DS} . . . . . Drain-source capacitance
C_{GD} . . . . . Gate-drain capacitance
C_{GS} . . . . . Gate-source capacitance
C_r . . . . . Feedback capacitance
D . . . . . Drain
E_G . . . . . Energy gap
f_T . . . . . Transit frequency
G . . . . . Gate, Gradient
GaAs . . . . . Gallium-Arsenide
Ge . . . . . Germanium
g_m . . . . . Short-circuit forward transconductance
H . . . . . Hybrid parameter
I_{DSS} . . . . . Drain current with V_{GS}=0
k . . . . . Boltzmann constant, $1.38 \cdot 10^{-23}$J/K or stability factor
q . . . . . Electron charge, $1.602 \cdot 10^{-19}$As
r_{DS} . . . . . Differential drain-source-resistance
RMS . . . . . Root Mean Square
R_{th} . . . . . Thermal resistance in K/W
S . . . . . Source
S_{ij} . . . . . Scattering parameters
Si . . . . . Silicon
T . . . . . Period
T_j . . . . . Junction Temperature
T_C . . . . . Temperature coefficient, e.g. TK(IDSS)
V_{pp} . . . . . Peak-to-Peak Voltage
V_D . . . . . Diffusion voltage
V_{DS} . . . . . Drain-Source voltage
V_{GS} . . . . . Gate-Source voltage
V_T . . . . . Thermal voltage, V_T=kT/q
V_{TO} . . . . . Threshold voltage, Turn-on voltage
a . . . . . Angle
b . . . . . Current gain
d . . . . . Partial derivative
ε_o . . . . . Dielectric constant of a vacuum
ε_r . . . . . Dielectric constant relative to a vacuum
ε_{reff} . . . . . Effective relative dielectric constant
G . . . . . Reflection coefficient
$_o$ . . . . . Permeability of a vacuum
$_r$ . . . . . Permeability relative to a vacuum
m . . . . . Charge carrier mobility
ω . . . . . Angular frequency
Δ . . . . . Difference
Σ . . . . . Sum

Revision History

Date	Version	Description/Changes
1.00	2006-08-29	Pre-engineering preliminary document.
1.01	2006-11-03	Pre-engineering preliminary document. Specifications, pin description, reference design, product descriptions added. Errata: Nominal conditions include Bit scrambling
1.02	2007-02-21	Minor text edits and corrections.
1.03	2007-07-31	Correction to values in rows 3 to 5 in table 11: *Quart controlled oscillator for reference frequency*.
2.00	2008-04-11	/POnReset circuitry added to sample application; small errors in block diagrams corrected; Frequency channel description moved to Local Oscillator table; full listing of frequency allocations updated according to IEEE 802.15.4a standard; data throughout updated to conform to latest chip measurements; extended descriptions of chip pins added; reference to chip registers added; dynamic performance table updated; timing diagrams updated; Local Oscillator table updated; summary of nanoLOC ranging added; recommended footprint dimensions diagram updated; tape and reel information added; new nanoLOC RF Test Module added; minor text edits and corrections throughout.

About Nanotron Technologies GmbH

Nanotron Technologies GmbH develops world-class wireless products for demanding applications based on its patented Chirp transmission system - an innovation that guarantees high robustness, optimal use of the available bandwidth, and low energy consumption. Since the beginning of 2005, Nanotron's Chirp technology has been a part of the IEEE 802.15.4a draft standard for wireless PANs which require extremely robust communication and low power consumption.

ICs and RF modules include the nanoNET TRX, the nanoLOC TRX, and ready-to-use or custom wireless solutions. These include, but are not limited to, industrial monitoring and control applications, medical applications (Active RFID), security applications, and Real Time Location Systems (RTLS). nanoNET is certified in Europe, United States, and Japan and supplied to customers worldwide.

Headquartered in Berlin, Germany, Nanotron Technologies GmbH was founded in 1991 and is an active member of IEEE and the ZigBee alliance.

Further Information

For more information about this product and other products from Nanotron Technologies, contact a sales representative at the following address:

Nanotron Technologies GmbH
Alt-Moabit 60
10555 Berlin, Germany
Phone: +49 30 399 954 - 0
Fax: +49 30 399 954 - 188
Email: sales@nanotron.com
Internet: www.nanotron.com