Date: February 20, 2003

ATMEL-CUPL/WinCUPL Bug List -- PLD Applications

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The following is a list of bugs which have been fixed in the ATMEL-CUPL 5.302 and earlier releases. WINCUPL V5.x bugs to be be fixed are also included. If you notice any bugs not included in this list please contact Atmel PLD Applications.

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Bug # 1
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ATF1500 Bug: (2-21-96)
Atmel-CUPL V4.7a

Symptoms: CSIM generates errors with simulating an ATF1500 design with no pin or node number assigned in the source (.pld) file.

Workaround: Assign pin and node number for the design in the source file

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Bug # 2
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ATV2500B Bug: 11-1-96
Atmel-CUPL V4.7a

Symptom: CUPL configures macrocell S0-S3 bits to illegal (1000) configurations for I/O pins used as an input with Q1 and Q2 buried registered nodes.

Workaround: None

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Bug # 3
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VSIMA Bug: 8-29-96, ATF1500/A
Atmel-CUPL V4.7a,WINCUPL V4.7b

Symptom: Logic with a registered output used a clock to another register (i.e. ripple counter logic) does not simulate correctly. Register clock output is ignored by VSIM.

Workaround: Use a PINNODE to buffer output that clocks second register. Define clock equation for second register to equal buffered output.

For example:

Original Equation	New Equation
reg2.ck = reg1;	PINNODE = temp;
reg1 is a registered output	temp = reg1;
	reg2.ck = temp;

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Bug # 4
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CSIM Bug: 12-6-96
WINCUPL V4.7b

Symptom: Designs using gated sychronous clock option on ATV2500B

fail to simulate.

Workaround: Gated synchronous clock need to be defined using .CK instead of .CE term. Define .CK product term to be Pin1 & <clock equation>. If you do not intend to simulate your design this workaround is not necessary.

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Bug # 5
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CUPL Bug: 12-20-96
WINCUPL V4.7b

Symptom: CUPL is incorrectly compiling equations such as:
D0.AR = RST # ![X0..X1]; . Is reduced to D0.AR = RST # !X0;
extra product term is being dropped.

Workaround: Defined equation as D0.AR = rst # !x0 & !x1; It will compile correctly.

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Bug # 6
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WINCUPL Bug: 2-3-96
ATV2500B Bug
CUPLC.DLL/CUPLC.exe

Symptom: For a I/O pin using an input, > 4PT Q1 nodes and < 4PT Q2 node CUPL is reporting "excessive number of product terms" when implementing the logic into the macrocell. Logic should fit if registered mode is selected.

Workaround: None

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Bug # 7
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WINCUPL Bug: 6-23-97
ATV2500B Bug
CUPLC.DLL/CUPLC.EXE

Symptom: For a I/O pin used as an input, and pinnode equations for both Q1 and Q2 nodes CUPL defaults to configuring the macrocell as combinatorial with two 4PT registered nodes.
Configuring the macrocell as registered with an 8PT Q1 and 4PT Q2 node is a more efficient configuration, since it allows and extra 4 PT's to be allocated to the Q1 node.

Workaround: As an example, define equations as follows:

INSTEAD OF THIS:

```
Pin <number> = INPUT_VARIABLE;
Pinnode <number> = Q1_node;
Pinnode <number> = Q2_node;
INPUT_VARIABLE.oe = 'b'0;
Q1_node = <Logic Expression> ;
Q2_node = <Logic Expression> ;
out1 = Q1_node # Q2_node;
out2 = Q2_node & INPUT_VARIABLE;
```

DO THIS:

```
Pin <number> = INPUT_VARIABLE;
Pinnode <number> = Q2_node;
INPUT_VARIABLE.oe = 'b'0;
INPUT_VARIABLE.d = <Q1_node Logic expression> ;/* Q1 node logic
                                        equation */
Q2_node = <Logic Expression> ;

out1 = INPUT_VARIABLE # Q2_node;
out2 = Q2_node & INPUT_VARIABLE.IO; /* Input Pin feedback */
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This will configure the macrocell correctly.

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Bug # 8

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WinCUPL (4.8a) Bug: 2-18-98
CUPLX Bug:

Symptom: Using the Register_Select(output_name) = 2 Keyword to convert anRS or JK-type FF to T-type flip flop generates the wrong equations.

For example:

```
output_name.s = Set;
output_name.r = Reset
output_name.ck = clock;
```

Compiled equations for T-type FF (DOC file) are:

```
output_name.t = !output_name & Set;
```

Reset term missing from equation. Should be:

```
output_name.t = Set & !output_name # Reset & output_name;
```

Workaround: Define the T-type logic manually.

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Bug # 9

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WinCUPL (4.8a) Bug: 2-20-98
CUPLX Bug:

Symptom: Using the Register_Select(output_name)= 1 Keyword to convert an synchronous RS equations to D-type flip flop results in incorrect equations. Converting JK equations to D works however.

Workaround: Use JK equations instead. This behaviour should be functionally equivalent to the synchronous RS equations.

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Bug # 10

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WinCUPL (4.8a) Bug: 2-23-98
CSIM Bug:

Symptom: For ATF1500AS family of device CUPL simulator does not simulate

active low output correctly. Reports the same results as active high o/p
Works OK on ATV family of devices such as the V750.

For example:
pin !a; pin b; pin !c;
b = a; c = a;

Simulation:

Order !a, b, !c;
Vector:
0 L L
1 H H

Instead of:

Vector:
0 L H
1 H L

Workaround: specify c to be active high: pin = c; c = !a,

Simulation:

Order !a,b,c; Same vectors as before. This should report the correct simulation results.

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Bug #11
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Wincupl5.1x
Install Bug on network drive: 8/31/99

Symptom: Wincupl cannot be installed to a network drive.
It may run through the Install procedure and then freeze. After running (open) WINCUPL program, several device type were missing.

This is a desired feature; Wincupl can only be installed on Local Drives

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Bug #12
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Wincupl5.126

EDITOR Bugs/Features Desired in WINCUPL:

Space is a character and Wincupl can freeze if there are more than 256 characters in a given equation.

Sometimes inserting comments after a file has been saved may not be immediately visible in Green color. Requires user to use the Refresh button.

Workaround: Use the Refresh button in the WinCUPL Window
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Bug #13

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SIMULATOR [WINSIM] 5.128
a) generates messages :-"[0033sa] Please note: jedec vectors cannot be
   created with undefined pin numbers.in0" when auto-run from within
CUPL,
   but does appear to actually append the JED vectors (!)
b) General edit, often causes Runtime rrror 5 error/terminate WinSim.
   Another customer reported:
   Keeps bombing with a 'runtime error' telling me "file already open,"
   when I try to simulate. Also: created the .SI file, but didn't save
my
   signals/vectors. Tried 5 different times.
c) BUS display does not seem to be correct, Help example shows expected
HEX,
   run does not.
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Bug #14
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WinCUPL 5.126
Date: 12/21/99
FIND1500, FIND1502, FIND1508, FIND1504 for WinCUPL 5.x)

WinCUPL is not reading the fitter exit codes. When the 1500 fitter fails
to
fit a design WinCUPL still indicates that compilations was successful.
Should indicate an error:
 "Fatal Fitter Error during Processing. Read Fitter Report File for
Details."
to prompt user to check the fitter's report file for a description of
problem
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Bug #15
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WinCUPL 5.126
Date: (12/23/99)

Symptom:
Design file specified a Node name Chan16_data0
However in the equations sections one inadvertently wrote:
Chan16_data.ck = <expression> instead of: Chan16_data0.ck = <expression>

Cupl Syntax compiler failed to detect this and instead treated it as
another
variable. This resulted in more nodes. The 1508,1504 fitters didn't fit
the design because the .tt2 file generated by CUPL was incorrect.

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Bug #16
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WinCUPL Version 5.134
Date: 02-02-00
Filename: wintec1.si

CSIM Bug Symption:
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When CSIM is run on 1500A simulation file with the append vector option enabled
Simulator generate warning message :
[0033sa]Please note: jedec vectors cannot be created with undefined pin numbers

The .si file has no Field statement but fields are declared in the PLD source
file. Test vectors appear to be appended correctly.

Workaround: Ignore the message, or disable append vector option when running
the simulator.

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Bug #17

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WinCUPL Version 5.141
Date: 04-05-00
Device: Any

Symptom:
If you try to create a new Design and subsequently make changes when the file is
open,the message seen is "Unable to Save". It complains that the file is being
used by some other application.

Workaround:
Copy into another text editor and close WinCUPL Window;

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Bug #18

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WinCUPL Version 5.144
Date: 10-25-00
Device: Any

Symptom:
If you try to use a different name other than the name used for the .PLD file
in the Header section corresponding to the "Name" field, then Wincupl can crash.
This happens when the Compiler Options...General.. have a Checkbox for "JEDEC Name=PLD name".

Workaround:
Use the same name as the filename in the Header section corresponding to the
"Name" field.

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Bug #19

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WinCUPL Version 5.216
Date: 07-18-01
Device: ANY

Symptom:
Cannot save "General Edit" changes to the source file. Complains that the
File is in use with another application.
This happens intermittently.

Workaround:
Save the File with a different "Filename" using the "Save..as" command.

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Bug #20
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WinCUPL Version 5.30.2
Date: 04-01-03
Device: ANY

Symptom:
FIT1500.EXE might not run properly on WinXP.

Workaround:
Use a different PC with Win98, NT, or 2000 to compile ATF1500A designs or target
design into ATF1502 instead.

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Bug #21
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WinCUPL Version 5.30.3
Date: 10-13-03
Device: ANY

Symptom:
WinCUPL does not launch or work properly on WinXP if logged in as User

Workaround:
WinXP users must have Full Control on the permission for the entire WinCUPL
folder (e.g. C:\WinCUPL).

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