This document explains in detail the architecture that corresponds
to each Device Mnemonic that appears in the Compiler.. Device Options
Window.

%G16V8CP
G16V8CP Architecture
Mnemonic: G16V8CP PLCC Mnenomic: NO
DIP Pin Count: 20 Total Product Terms: 64
Extensions: OE D Pin Controlled Power Down: Yes

Manufacturer	Device Name
ATMEL	ATF16V8B/L

Clock Pin(s): 1 Common OE(s): 11
VCC(s): 20 GND(s): 10
Input Only: 2 3 4 5 6 7 8 9
Output Only:
Input/Output: 12 13 14 15 16 17 18 19

Device Notes:
1. This device emulates three different PAL architectures with their
flexible output macro configuration. When this device mnemonic is used, the device
 parameters for the proper sub-mode are automatically selected according to the
following:

A. Registered Mode Mnemonic: G16V8CPMS
    This mode is automatically chosen when the PLD source file has registered
    output. In the registered mode, specifying an output enable term for a
    registered output pin is not flagged as an error by the compiler or
    simulator.

Input only	Output only	Input/Output
2, 3, 4,		12, 13, 14,
5, 6, 7,		15, 16, 17,
8, 9		18, 19

    Pin 1 = common clock Pin 11 = common output enable

    In this mode, the output enable control for registered
    pins is common to pin 11.

B. Complex Mode Mnemonic: G16V8CPMA
    This mode is automatically chosen when the PLD source
    file has an output enable term for a non-registered pin
    and/or combinatorial feedback.

Input only	Output only	Input/Output
1, 2, 3,	12, 19	13, 14, 15,
4, 5, 6,		16, 17, 18
7, 8, 9,		
11		

C. Simple Mode (Default) Mnemonic: G16V8CPAS
    If none of the above are met, the device type defaults
    to the small mode. In this mode, the Input/Output pins
    are configured as either Input Only or Output only
    (that is, no feedback can occur).

Input only	Output only	Input/Output
1, 2, 3,	15, 16	12, 13, 14,
4, 5, 6,		17, 18, 19
7, 8, 9,		
11		

2. Either the automatic selection mechanism or the device
    mnemonic for the specific sub-mode desired can be used.

D. Pin Controlled Power Down
    This device has a new feature which allows pin 4 to be used
    as a power down pin. When this pin is logic high (5.0V) the part
    will be automatically powered down to a 100uA standby mode.
    This feature is automatically enabled if this device type is
    selected. If you do not want to use this feature select the
    either the g16v8 or g16v8a device types instead.
%%
%G16V8
G16V8 Architecture
Mnemonic: G16V8 PLCC Mnemonic: NO
DIP Pin Count: 20 Total Product Terms: 64
Extensions: OE D Pin Controlled Power Down: No

Manufacturer	Device Name

```
ATMEL                          ATF16V8B/L
_____________________________________________________________________
Clock Pin(s): 1                Common OE(s): 11
VCC(s): 20                     GND(s): 10
Input Only: 2  3  4  5  6  7  8  9
Output Only:
Input/Output: 12  13  14  15  16  17  18  19

Device Notes:
1.  This device emulates three different PAL architectures
    with their flexible output macro configuration. When
    this device mnemonic is used, the device parameters for
    the proper sub-mode are automatically selected according
    to the following:

A.  Registered Mode              Mnemonic: G16V8MS
    This mode is automatically chosen when the PLD source
    file has registered output. In the registered mode,
    specifying an output enable term for a registered
    output pin is not flagged as an error by the compiler or
    simulator.

    Input only      Output only    Input/Output

     2, 3, 4,                              12, 13, 14,
     5, 6, 7,                              15, 16, 17,
     8, 9                                  18, 19

    Pin 1 = common clock     Pin 11 = common output enable

    In this mode, the output enable control for registered
    pins is common to pin 11.

B.  Complex Mode                 Mnemonic: G16V8MA
    This mode is automatically chosen when the PLD source
    file has an output enable term for a non-registered pin
    and/or combinatorial feedback.

    Input only     Output only    Input/Output
    ----------     -----------    ------------
     1, 2, 3,         12, 19       13, 14, 15,
     4, 5, 6,                      16, 17, 18
     7, 8, 9,
     11

C.  Simple Mode (Default)        Mnemonic: G16V8S
    If none of the above are met, the device type defaults
    to the small mode. In this mode, the Input/Output pins
    are configured as either Input Only or Output only
    (that is, no feedback can occur).


    Input only     Output only    Input/Output

     1, 2, 3,        15, 16           12, 13, 14,
     4, 5, 6,                           17, 18, 19
     7, 8, 9,
     11

2.  Either the automatic selection mechanism or the device
    mnemonic for the specific sub-mode desired can be used.
%%
%G16V8A
G16V8A Architecture
Mnemonic: G16V8A               PLCC Mnemonic: NO
DIP Pin Count: 20              Total Product Terms:   64
Extensions: OE D               Pin Controlled Power Down: No
-------------------------------------------------------------------------------------------------------------------------
Manufacturer                   Device Name

ATMEL                          ATF16V8B/L
-------------------------------------------------------------------------------------------------------------------------
Clock Pin(s): 1                Common OE(s): 11
VCC(s): 20                     GND(s): 10
Input Only: 2  3  4  5  6  7  8  9
Output Only:
Input/Output: 12  13  14  15  16  17  18  19
_____________________________________________________________________
Device Notes:
1.  This device emulates three different PAL architectures
    with their flexible output macro configuration. When
    this device mnemonic is used, the device parameters for
    the proper sub-mode are automatically selected according
    to the following:

A.  Registered Mode              Mnemonic: G16V8MS
```

This mode is automatically chosen when the PLD source file has registered output. In the registered mode, specifying an output enable term for a registered output pin is not flagged as an error by the compiler or simulator.

Input only	Output only	Input/Output
2, 3, 4,		12, 13, 14,
5, 6, 7,		15, 16, 17,
8, 9		18, 19

Pin 1 = common clock Pin 11 = common output enable

In this mode, the output enable control for registered pins is common to pin 11.

B. Complex Mode Mnemonic: G16V8MA

This mode is automatically chosen when the PLD source file has an output enable term for a non-registered pin.

Input only	Output only	Input/Output
1, 2, 3,	12, 19	13, 14, 15,
4, 5, 6,		16, 17, 18
7, 8, 9,		
11		

C. Simple Mode (Default) Mnemonic: G16V8AS

If none of the above are met, the device type defaults to the simple mode. In this mode, the Input/Output pins are configured as either Input Only, Output only, or Output with combinatorial feedback.

Input only	Output only	Input/Output
1, 2, 3,	15, 16	12, 13, 14,
4, 5, 6,		17, 18, 19
7, 8, 9,		
11		

2. Either the automatic selection mechanism or the device mnemonic for the specific sub-mode desired can be used.

%%
%G20V8
G20V8 Architecture
Mnemonic: G20V8 PLCC Mnemonic: YES (G20V8LCC)
DIP/LCC Pin Count: 24/28 Total Product Terms: 64
Extensions: OE D

Manufacturer	Device Name
ATMEL	ATF20V8B/L

Clock Pin(s): 1 Common OE(s): 13
VCC(s): 24 GND(s): 12
Input Only: 2 3 4 5 6 7 8 9 10 11 14 23
Output Only:
Input/Output: 15 16 17 18 19 20 21 22

Device Notes:
1. This device emulates three different PAL architectures with their flexible output macro configuration. When this device mnemonic is used, the device parameters for the proper sub-mode are automatically selected according to the following:

A. Registered Mode Mnemonic: G20V8MS

This mode is automatically chosen when the PLD source file has registered output. In the registered mode, specifying an output enable term for a registered output pin is not flagged as an error by the compiler or simulator.

Input only	Output only	Input/Output
2, 3, 4,		15, 16, 17,
5, 6, 7,		18, 19, 20,
8, 9, 10,		21, 22
11, 14, 23		

Pin 1 = common clock Pin 13 = common output enable
In this mode, the output enable control for registered pins is common to pin 13.

B. Complex Mode Mnemonic: G20V8MA

This mode is automatically chosen when the PLD source file has an output enable term for a non-registered pin and/or combinatorial feedback.

Input only	Output only	Input/Output
1, 2, 3,	15, 22	16, 17, 18,
4, 5, 6,		19, 20, 21
7, 8, 9,		
10, 11, 13,		
14, 23		

C. Simple Mode (Default) Mnemonic: G20V8S
This mode is automatically chosen when the PLD source file has an output enable term for a non-registered pin and/or combinatorial feedback.

Input only	Output only	Input/Output
1, 2, 3,	18, 19	15, 16, 17,
4, 5, 6,		20, 21, 22
7, 8, 9,		
10, 11, 13,		
14, 23		

2. Either the automatic selection mechanism or the device mnemonic for the specific sub-mode desired can be used.

%%

%G20V8A

G20V8A Architecture

Mnemonic: G20V8A PLCC Mnemonic: YES (G20V8ALCC)

DIP Pin Count: 24 Total Product Terms: 64

Extensions: OE D

Manufacturer Device Name

ATMEL ATF20V8B/L

Clock Pin(s): 1 Common OE(s): 13

VCC(s): 24 GND(s): 12

Input Only: 2 3 4 5 6 7 8 9 10 11 14 23

Output Only:

Input/Output: 15 16 17 18 19 20 21 22

Device Notes:

1. This device emulates three different PAL architectures with their flexible output macro configuration. When this device mnemonic is used, the device parameters for the proper sub-mode are automatically selected according to the following:

A. Registered Mode Mnemonic: G20V8MS
This mode is automatically chosen when the PLD source file has registered output. In the registered mode, specifying an output enable term for a registered output pin is not flagged as an error by the compiler or simulator.

Input only	Output only	Input/Output
2, 3, 4,		15, 16, 17,
5, 6, 7,		18, 19, 20,
8, 9, 10,		21, 22
11, 14, 23		

Pin 1 = common clock Pin 13 = common output enable
In this mode, the output enable control for registered pins is common to pin 13.

B. Complex Mode Mnemonic: G20V8MA
This mode is automatically chosen when the PLD source file has an output enable term for a non-registered pin.

Input only	Output only	Input/Output
1, 2, 3,	15, 22	16, 17, 18,
4, 5, 6,		19, 20, 21
7, 8, 9,		
10, 11, 13,		
14, 23		

C. Simple Mode (Default) Mnemonic: G20V8AS
This mode is automatically chosen when the PLD source file has an output enable term for a non-registered pin and/or combinatorial feedback.

```
    Input only     Output only   Input/Output
    ----------     -----------   ------------
     1, 2, 3,        18, 19       15, 16, 17,
     4, 5, 6,                     20, 21, 22
     7, 8, 9,
     10, 11, 13,
     14, 23

2.  Either the automatic selection mechanism or the device
    mnemonic for the specific sub-mode desired can be used.
%%
%G22V10cp
G22V10 Architecture
Mnemonic: G22V10              PLCC Mnemonic: YES (G22V10CPLCC)
DIP Pin Count: 24             Total Product Terms:  132
Extensions: OE D AR SP        Pin Controlled Power Down: Yes
__________________________________________________________
Manufacturer                  Device Name
------------                            -----------
ATMEL                         ATF22V10C/CZ

Clock Pin(s): 1               Common OE(s):
VCC(s): 24                    GND(s): 12
Input Only: 1  2  3  4  5  6  7  8  9  10  11  13
Output Only:
Input/Output: 14  15  16  17  18  19  20  21  22  23
____________________________________________________________
Device Notes:

A. Pin Controlled Power Down
Select this device type if you want to use the pin-controlled
power down feature enabled. When Pin 4 is set to a logic high
(5V) the device will automatically power down to a standy
current of (100uA) for the ATF22V10C. This feature is
automatically enabled by select this device type. If you
want this feature disabled, select the g22v10 device type.
%%

%%
%G22V10
G22V10 Architecture
Mnemonic: G22V10              PLCC Mnemonic: YES (G22V10LCC)
DIP Pin Count: 24             Total Product Terms:  132
Extensions: OE D AR SP        Pin Controlled Power Down: NO
___________________________________________________________
Manufacturer                  Device Name
------------                  -----------
ATMEL                         ATF22V10B/L
ATMEL                         ATF22V10BQ/BQL

Clock Pin(s): 1               Common OE(s):
VCC(s): 24                    GND(s): 12
Input Only: 1  2  3  4  5  6  7  8  9  10  11  13
Output Only:
Input/Output: 14  15  16  17  18  19  20  21  22  23
%%

%P22V10
P22V10 Architecture
Mnemonic: P22V10
DIP/PLCC Pin Count 24/28      PLCC Mnemonic: YES  (P22V10LCC)
Extensions: OE D AR SP        Total Product Term: 132
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Manufacturer                  Device Name
-----------                   -----------
ATMEL                         AT22V10/L

Clock Pin(s): 1               Common OE(s):
VCC(s): 24                    GND(s): 12
Input Only: 1  2  3  4  5  6  7  8  9  10  11  13
Output Only:
Input/Output: 14  15  16  17  18  19  20  21  22  23
%%

%V750
V750 Architecture
Mnemonic: V750                PLCC Mnemonic: YES (V750LCC)
DIP Pin Count: 24             Total Product Terms:  171
Extensions: D AR CK OE SP DFB IO
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Manufacturer                  Device Name
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ATMEL                         ATV750/L
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Clock Pin(s):                 Common OE(s):
VCC(s): 24                    GND(s): 12
```

```
Input Only: 1  2  3  4  5  6  7  8  9  10  11  13
Output Only:
Input/Output: 14  15  16  17  18  19  20  21  22  23
Q1 REG nodes: 25  26  27  28  29  30  31  32  33  34
Q0 REG nodes: 35  36  37  38  39  40  41  42  43  44
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Device Notes:
1.  Q1 and Q0 registered node numbers for LCC package are
    offset by +4.
    Ex. Q1: 29  30  31 ...
     Q0: 39  40  41 ...
%%
%V750B
V750B Architecture
Mnemonic: V750B              PLCC Mnemonic: YES  (V750BLCC)
DIP Pin Count: 24            Total Product Terms:  171
Extensions: D T AR CK CKMUX OE SP DFB IO
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Manufacturer                 Device Name
------------                 -----------
ATMEL                        ATV750B/L

Clock Pin(s): 1              Common OE(s):
VCC(s): 24                   GND(s): 12
Input Only: 1  2  3  4  5  6  7  8  9  10  11  13
Output Only:
Input/Output: 14  15  16  17  18  19  20  21  22  23
Q1 REG nodes: 25  26  27  28  29  30  31  32  33  34
Q0 REG nodes: 35  36  37  38  39  40  41  42  43  44
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Device Notes:
1. Clock Assignment
    Asynchronous clock - use the .CK extension
     Ex. X.CK = A & B & C;
    Synchronous clock - use the .CKMUX extension
     Ex. X.CKMUX = CLK;
2.  Q1 and Q0 registered node numbers for LCC package are
    offset by +4.
    Ex. Q1: 29  30  31 ...
     Q0: 39  40  41 ...

%%

%F1500
F1500 Architecture
Mnemonic F1500               TQFP Mnenonic: YES
PLCC Pin Count 44            Total Product Terms: 160
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Extensions: D AR CK CE OE AP IO T L LE

Manufacturer                 Device Name
____________                 ___________
ATMEL                        ATF1500/T
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VCC(s): 4                    GND(s): 4
Clock Pin(s): 1              Common OE(s): 2
Common Reset(s): 1           Power Down: YES (Pin 4)

PLCC Pinout:
____________
Input Only:       1   2   43  44
Input/Output:     4   5   6   7   8   9   11  12  13  14  16
                  17  18  19  20  21  24  25  26  27  28  29
                  31  32  33  34  36  37  38  39  40  41
Expander Node(s): 77  78  79  80  81  82  83  84  85  86  87
                  88  89  90  91  92  93  94  95  96  97  98
                  99 100 101 102 103 104 105 106 107 108
Register Node(s): 45  46  47  48  49  50  51  52  53  54  55
                  56  57  58  59  60  61  62  63  64  65  66
                  67  68  69  70  71  72  73  74  75  76

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Device Notes:
1. Expander and Register Node numbers are the same for both
   package types
2. Clock Assignment:
Global Clock:
   X.CK = CLK; Where CLK is assigned to pin 43
Product Term Clock:
   X.CK = A & B & C;
Clock Enable:
   X.CE = A & B;
Latch Clock:
   X.LE = CLK; OR X.LE = !A & B & C;
3. Register Usage:
   D Type Flip-Flop:
       X.D = A & B & C;
```

```
   T Type Flip-Flop:
       X.T = A & B & !C;
Latch:
       X.L = A & !B & C;
4. Reset Usage:
Global Reset:
   X.AR = RESET; Where RESET is assigned to pin 1
Product Term Reset:
   X.AR = A & B & C;
5. Output Enable Usage:
Global Output Enable:
   X.OE = ENABLE; Where ENABLE is assigned to pin(s) 2, 44
Product Term Output Enable:
   X.OE = B & C;
%%

%F1500T
F1500 Architecture
Mnemonic F1500T           PLCC Mnenonic: YES
TQFP Pin Count 44         Total Product Terms: 160
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Extensions: D AR CK CE OE AP IO T L LE

Manufacturer                  Device Name
____________                  ___________
ATMEL                         ATF1500/T

VCC(s): 4                     GND(s): 4
Clock Pin(s): 1               Common OE(s): 2
Common Reset(s): 1            Power Down: YES (Pin 42)

TQFP Pinout:
____________
Input Only:        37  38  39  40
Input/Output:      42  43  44  1   2   3   5   6   7   8   10
                   11  12  13  14  15  18  19  20  21  22  23
                   25  26  27  28  30  31  32  33  34  35

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Device Notes:
1. Expander and Register Node numbers are the same for both
   package types
2. Clock Assignment:
Global Clock:
   X.CK = CLK; Where CLK is assigned to pin 43
Product Term Clock:
   X.CK = A & B & C;
Clock Enable:
   X.CE = A & B;
Latch Clock:
   X.LE = CLK; OR X.LE = !A & B & C;
3. Register Usage:
   D Type Flip-Flop:
       X.D = A & B & C;
   T Type Flip-Flop:
       X.T = A & B & !C;
   Latch:
       X.L = A & !B & C;
4. Reset Usage:
Global Reset:
   X.AR = RESET; Where RESET is assigned to pin 1
Product Term Reset:
   X.AR = A & B & C;
5. Output Enable Usage:
Global Output Enable:
   X.OE = ENABLE; Where ENABLE is assigned to pin(s) 2, 44
Product Term Output Enable:
   X.OE = B & C;
%%

%F1500A
F1500A Architecture
Mnemonic F1500A               TQFP Mnenonic: YES
PLCC Pin Count 44             Total Product Terms: 160
                              Programmable Pin Keeper: YES
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Extensions: D AR CK CE OE AP IO T L LE

Manufacturer                  Device Name
____________                  ___________
ATMEL                         ATF1500A/T
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VCC(s): 4                     GND(s): 4
Clock Pin(s): 1               Common OE(s): 2
Common Reset(s): 1            Power Down: YES (Pin 4)

PLCC Pinout:
```

```
____________
Input Only:       1   2   43  44
Input/Output:     4   5   6   7   8   9   11  12  13  14  16
                  17  18  19  20  21  24  25  26  27  28  29
                  31  32  33  34  36  37  38  39  40  41
Expander Node(s): 77  78  79  80  81  82  83  84  85  86  87
                  88  89  90  91  92  93  94  95  96  97  98
                  99 100 101 102 103 104 105 106 107 108
Register Node(s): 45  46  47  48  49  50  51  52  53  54  55
                  56  57  58  59  60  61  62  63  64  65  66
                  67  68  69  70  71  72  73  74  75  76

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Device Notes:
1. Expander and Register Node numbers are the same for both
   package types
2. Clock Assignment:
Global Clock:
   X.CK = CLK; Where CLK is assigned to pin 43
Product Term Clock:
   X.CK = A & B & C;
Clock Enable:
   X.CE = A & B;
Latch Clock:
   X.LE = CLK; OR X.LE = !A & B & C;
3. Register Usage:
   D Type Flip-Flop:
       X.D = A & B & C;
   T Type Flip-Flop:
       X.T = A & B & !C;
Latch:
       X.L = A & !B & C;
4. Reset Usage:
Global Reset:
   X.AR = RESET; Where RESET is assigned to pin 1
Product Term Reset:
   X.AR = A & B & C;
5. Output Enable Usage:
Global Output Enable:
   X.OE = ENABLE; Where ENABLE is assigned to pin(s) 2, 44
Product Term Output Enable:
   X.OE = B & C;

6. Programmable Pin Keeper
The ATMEL ATF1500A has a feature which allows you to disable the
programmable pin keeper circuits on the device. These circuit are
weak latches that holds the output to its previously defined state
after it is tri-stated. These circuits are easily over-driven when
when the output is not tri-stated. Selecting this device type
allows you to enable or disable this feauture. Disabling this feature
allow all outputs to float when tri-stated. To enable this
feature add the CUPL { pin_keep ON} property to your PLD source file
and re-compile. To disable this feature add the CUPL { pin_keep OFF}
This feature defaults to being always enabled.

7. Security Bit
If you need to secure your ATF1500 designs select this F1500A device
type and use the CUPL property statement { security ON } in you
PLD source file. Re-compile the design. The ATMEL ATF1500 fitter
will automatically generate a JEDEC file with the security bit
enabled.
%%

%F1500AT
F1500A Architecture
Mnemonic F1500AT          PLCC Mnenonic: YES
TQFP Pin Count 44         Total Product Terms: 160
                          Programmable Pin Keeper: YES

Extensions: D AR CK CE OE AP IO T L LE

Manufacturer                  Device Name
____________                ___________
ATMEL                         ATF1500/T

VCC(s): 4                     GND(s): 4
Clock Pin(s): 1               Common OE(s): 2
Common Reset(s): 1            Power Down: YES (Pin 42)


TQFP Pinout:
____________
Input Only:        37  38  39  40
Input/Output:      42  43  44  1   2   3   5   6   7   8   10
                   11  12  13  14  15  18  19  20  21  22  23
                   25  26  27  28  30  31  32  33  34  35
```

```
_____________________________________________________
Device Notes:
1. Expander and Register Node numbers are the same for both
   package types
2. Clock Assignment:
Global Clock:
   X.CK = CLK; Where CLK is assigned to pin 43
Product Term Clock:
   X.CK = A & B & C;
Clock Enable:
   X.CE = A & B;
Latch Clock:
   X.LE = CLK; OR X.LE = !A & B & C;
3. Register Usage:
   D Type Flip-Flop:
       X.D = A & B & C;
   T Type Flip-Flop:
       X.T = A & B & !C;
   Latch:
       X.L = A & !B & C;
4. Reset Usage:
Global Reset:
   X.AR = RESET; Where RESET is assigned to pin 1
Product Term Reset:
   X.AR = A & B & C;
5. Output Enable Usage:
Global Output Enable:
   X.OE = ENABLE; Where ENABLE is assigned to pin(s) 2, 44
Product Term Output Enable:
   X.OE = B & C;

6. Programmable Pin Keeper
The ATMEL ATF1500A has a feature which allows you to disable the
programmable pin keeper circuits on the device. These circuit are
weak latches that holds the output to its previously defined state
after it is tri-stated. These circuits are easily over-driven when
when the output is not tri-stated. Selecting this device type
allows you to enable or disable this feauture. Disabling this feature
allow all outputs to float when tri-stated. To enable this
feature add the CUPL { pin_keep ON } property to your PLD source file
and re-compile. To disable this feature add the CUPL { pin_keep OFF}
This feature defaults to being always enabled.

7. Security Bit
If you need to secure your ATF1500 designs select this F1500A device
type and use the CUPL property statement { security ON } in you
PLD source file. Re-compile the design. The ATMEL ATF1500 fitter
will automatically generate a JEDEC file with the security bit
enabled.

%%

%%
%V2500
V2500 Architecture
Mnemonic: V2500               PLCC Mnemonic: YES (V2500LCC)
DIP Pin Count: 40             Total Product Terms:  416
Extensions: D AR CK OE SP IO

Manufacturer                  Device Name
------------                            -----------
ATMEL                         ATV2500/L
_____________________________________________________
Clock Pin(s):                 Common OE(s):
VCC(s): 1                     GND(s): 3
Input Only: 1  2  3  17  18  19  20  21  22  23  37  38  39
            40
Output Only:
Input/Output:  4   5   6   7   8   9  11  12  13  14  15  16
              24  25  26  27  28  29  31  32  33  34  35  36
Q2 REG Node:  41  42  43  44  45  46  47  48  49  50  51  52
              53  54  55  56  57  58  59  60  61  62  63  64
Q1 REG Node:  65  66  67  68  69  70  71  72  73  74  75  76
              77  78  79  80  81  82  83  84  85  86  87  88
_____________________________________________________
1.  Q2 and Q1 registered node numbers for LCC package are
    offset by +4.
    Ex. Q2: 45  46  47 ...
Q1: 69  70  71 ...
%%
%V2500B
V2500B Architecture
Mnemonic: V2500B              PLCC Mnemonic: YES (V2500BLCC)
DIP Pin Count: 40             Total Product Terms:  416
Extensions: D T AR CK OE SP IO CE
_____________________________________________________
Manufacturer                  Device Name
```

```
ATMEL                          ATV2500B/L
_____________________________________________________
Clock Pin(s): 1                Common OE(s):
VCC(s): 10                     GND(s): 30
Input Only: 1  2  3  17  18  19  20  21  22  23  37  38  39
            40
Output Only:
Input/Output:  4   5   6   7   8   9  11  12  13  14  15  16
              24  25  26  27  28  29  31  32  33  34  35  36
Q2 REG Node:  41  42  43  44  45  46  47  48  49  50  51  52
              53  54  55  56  57  58  59  60  61  62  63  64
Q1 REG Node:  65  66  67  68  69  70  71  72  73  74  75  76
              77  78  79  80  81  82  83  84  85  86  87  88
_____________________________________________________
Device Notes:
1. Clock Assignment
    Asynchronous clock - use the .CK extension
Ex. X.CK = A & B & C;
    Synchronous clock - use the .CE extension
Ex. X.CE = 'b'1;
Set the Clock enable term to 'b'1 to allow the use
of pin 1 to be the clock signal.
    Gated synchronous clock- use the .CE extension
Ex. X.CE = A & B & C;
The Clock pin (pin 1) will be gated by the
(A & B & C) function.
2.  Q2 and Q1 registered node numbers for LCC package are
    offset by +4.
    Ex. Q2: 45  46  47 ...
Q1: 69  70  71 ...
%%
%F1508ispplcc84
F1508ispplcc84 Architecture
Mnemonic: F1508ispplcc84       Mnemonic: PLCC
Pin Count: 84              Total Product Terms:   320
Extensions: D T S R OE OEMUX CK CKMUX AR DQ LQ IO IOD IOL
            IOCK IOAR
_____________________________________________________________________
Manufacturer                   Device Name
------------                   -----------
ATMEL                          ATF1508
_____________________________________________________________________
Clock Pin(s):  2  81  83       Common OE(s): 84
VCC(s): 3  13  26  38  43  53  66  78
GND(s): 7  19  32  42  47  59  72  82
GCLR:  1
Input Only: 1  2  83  84
Output Only:
Input/Output: 4  5  6  8  9  10  11  12  14  15  16  17  18
              20  21  22  23  24  25  27  28  29  30  31  33
              34  35  36  37  39  40  41  44  45  46  48  49
              50  51  52  54  55  56  57  58  60  61  62  63
              64  65  67  68  69  70  71  73  74  75  76  77
              79  80  81
ISP:  12  45  14  23  62  71
%%
%F1508ispqfp100
F1508ispqfp100 Architecture
Mnemonic: F1508ispqfp100        Mnemonic: PQFP
Pin Count: 100             Total Product Terms:   320
Extensions: D T S R OE OEMUX CK CKMUX AR DQ LQ IO IOD IOL
            IOCK IOAR
_____________________________________________________________________
Manufacturer                   Device Name
------------                   -----------
ATMEL                          ATF1508
_____________________________________________________________________
Clock Pin(s):  87  89  92      Common OE(s): 90
VCC(s):  5  20  36  41  53  68  84  93
GND(s):  13  28  40  45  61  76  88  97
Input Only:  89  90  91  92
Output Only:
Input/Output: 1  2  3  4  6  7  8  9  10  11  12  14  15  16
              17  18  19  20  21  22  23  24  25  27  28  29
              30  31  32  33  34  35  37  38  39  42  43  44
              46  48  49  50  51  52  54  55  56  57  58  60
              62  63  64  65  66  67  69  70  71  72  73  74
              75  77  78  79  80  81  82  83  85  86  87  94
              95  96  98  99  100
ISP:  3  43  6  17  64  75
%%
%F1508plcc84
F1508plcc84 Architecture
Mnemonic: F1508plcc84          Mnemonic: PLCC
Pin Count: 84              Total Product Terms:   320
Extensions: D T S R OE OEMUX CK CKMUX AR DQ LQ IO IOD IOL
```

```
            IOCK IOAR
_____________________________________________________________________
Manufacturer                    Device Name
------------                    -----------
ATMEL                           ATF1508
_____________________________________________________________________
Clock Pin(s):  2  81  83        Common OE(s): 84
VCC(s): 3  13  26  38  43  53  66  78
GND(s): 7  19  32  42  47  59  72  82
GCLR:  1
Input Only: 1  2  83  84
Output Only:
Input/Output: 4  5  6  8  9  10  11  12  14  15  16  17  18
              20  21  22  23  24  25  27  28  29  30  31  33
              34  35  36  37  39  40  41  44  45  46  48  49
              50  51  52  54  55  56  57  58  60  61  62  63
              64  65  67  68  69  70  71  73  74  75  76  77
              79  80  81
%%
%F1508qfp100
F1508qfp100 Architecture
Mnemonic: F1508qfp100           Mnemonic: PQFP
Pin Count: 100             Total Product Terms:   320
Extensions: D T S R OE OEMUX CK CKMUX AR DQ LQ IO IOD IOL
            IOCK IOAR
_____________________________________________________________________
Manufacturer                    Device Name
------------                    -----------
ATMEL                           ATF1508
_____________________________________________________________________
Clock Pin(s):  87  89  92       Common OE(s): 90
VCC(s):  5  20  36  41  53  68  84  93
GND(s):  13  28  40  45  61  76  88  97
Input Only:  89  90  91  92
Output Only:
Input/Output: 1  2  3  4  6  7  8  9  10  11  12  14  15  16
              17  18  19  20  21  22  23  24  25  27  28  29
              30  31  32  33  34  35  37  38  39  42  43  44
              46  48  49  50  51  52  54  55  56  57  58  60
              62  63  64  65  66  67  69  70  71  72  73  74
              75  77  78  79  80  81  82  83  85  86  87  94
              95  96  98  99  100
%%
```