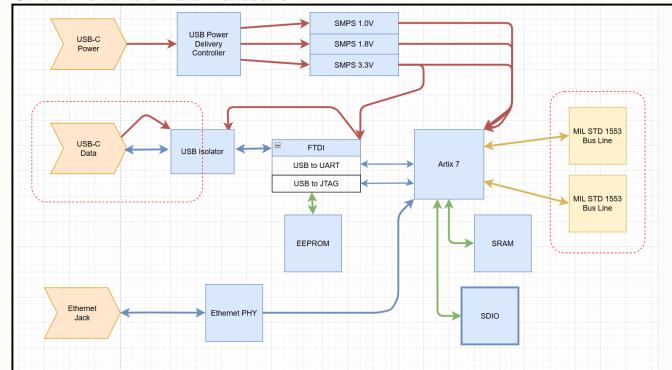


Ethernet to Multi-Military Protocol Adapter

A

General Power and Data Distribution



*Any module receiving data can assume to have the same power rail

B

Power

USB Power Connection

Power Switching Regulators
Power_SwitchRegulators.SchDoc

Artix-7 Power Connections 1
Artix7_Power_1.SchDoc

6

Artix Power Conenctions 2
Artix7_Power_2.SchDoc

Artix-7 Ground Connections
Artix7 Power Grounds.SchDoc

Manufacturing Information

[JLPCB Manufacturing Capabilities \(link\)](#)
[JLPCB BGA Recommendations \(link\)](#)

Reference Documents

Development Board Schematic

Development Board Reference Manual

Class 1,2,3 Via and Pad Guide (link)

Mechanical Components

Title

Size	Number
------	--------

Revision

A

Date: 11/19/2025 Sheet of 1 Page 1

File: C:\Users\..\Eth2Mil1553_Quad_Artix7.SchDoc Down By:

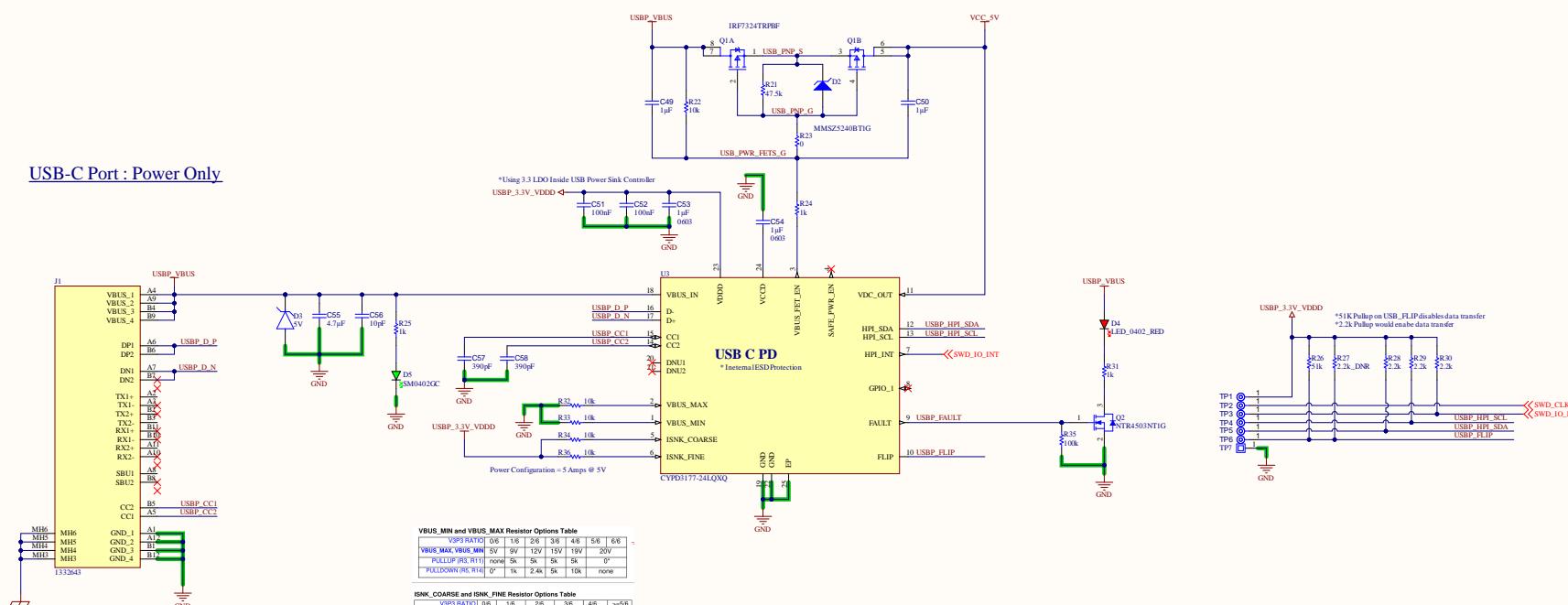
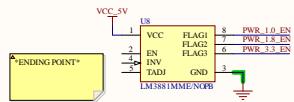
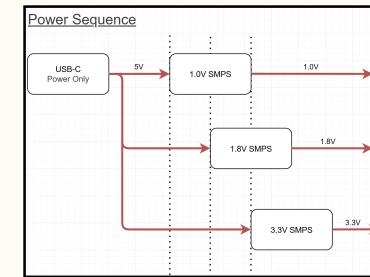
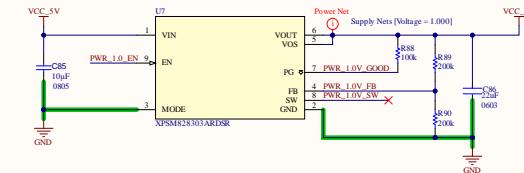
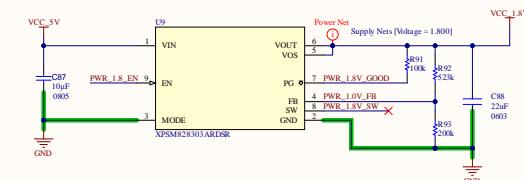
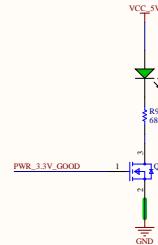
USB-C Port : Power Only

Table 1. Resistor Options for VBUS and VBUS MAX					
VBUS_VDD	16	25	36	46	56
VBUS_MAX_VDD	5V	6V	12V	15V	19V
PULLUP (R3, R11)	none	5k	5k	5k	5k
PULLDOWN (R12, R14)	0"	1k	2.4k	5k	10k

Table 2. Resistor Options for VBUS and VBUS MAX					
VBUS_VDD	16	25	36	46	56
VBUS_MAX_VDD	5V	6V	12V	15V	19V
PULLUP (R3, R11)	none	5k	5k	5k	5k
PULLDOWN (R12, R14)	0"	1k	2.4k	5k	10k

Power Sequencer ICSMPS - Internal Inductor - 1.0VSMPS - Internal Inductor - 1.8VLED : Power Up Success

Title		
Size	Number	Revision
A2		
Date: 11/19/2025	Sheet of:	
File: C:/Users/_Power SwitchRegulationSchematic		

A

A

B

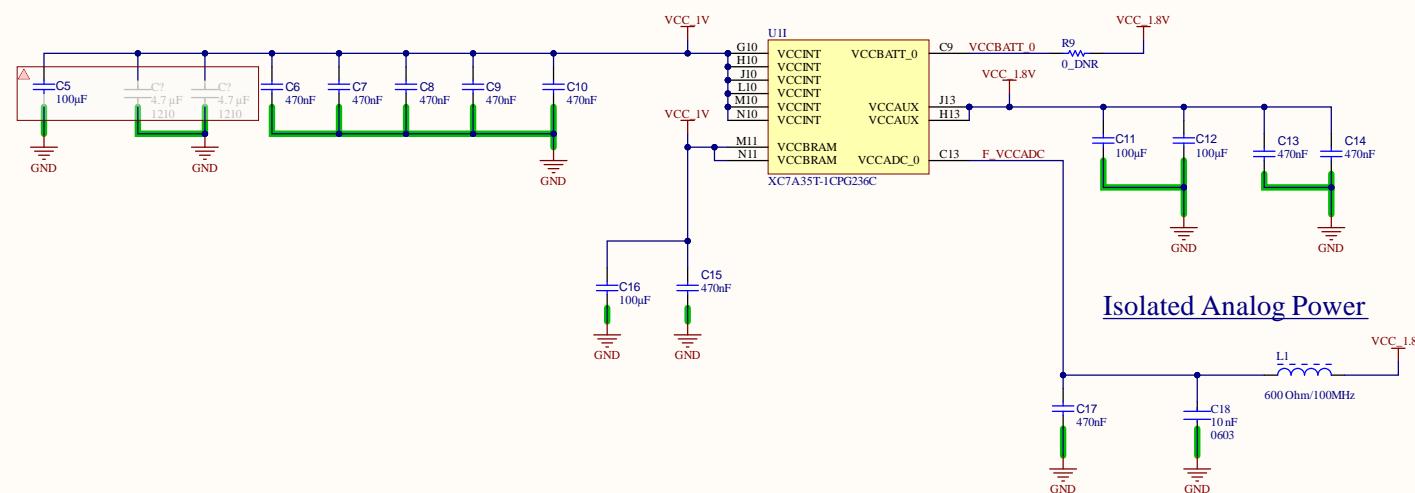
B

C

C

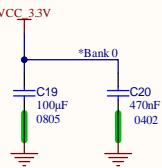
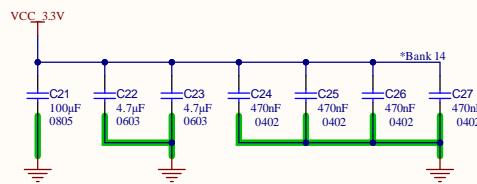
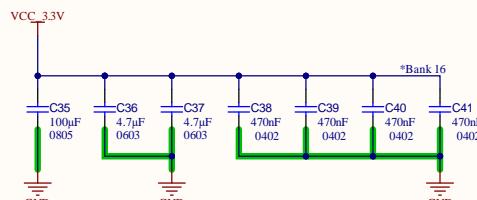
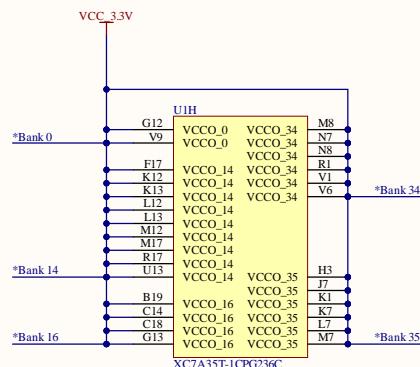
D

D



Title		
Size	Number	Revision
A3		
Date: 11/19/2025	Sheet of	
File: C:\Users\...\Artix7_Power_1.SchDoc	Drawn By:	

A

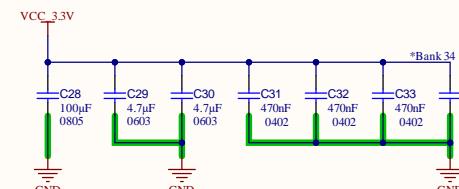
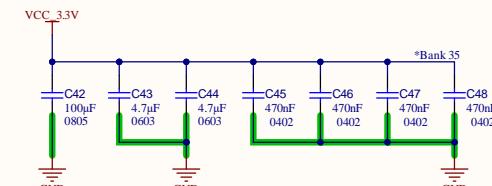
Bank VCCO 0Bank VCCO 14Bank VCCO 16FPGA : 3.3V Power/IO-Bank Connections

Screenshots of minimum recommended capacitor values for EAC IO bank.
 Note: Due to not having area restraints, 4.7 μF capacitors were changed to 1210 for now.

[Screenshot Location, pg 15 \(link\)](#)

V _{CCO} Bank 0	V _{CCO} all other Banks (per Bank)
47 μ F	47 μ F or 100 μ F ⁽³⁾

1 1 2 4

Bank VCCO 34Bank VCCO 35

Title		Revision	
Size	Number	Sheet of	
A3			
Date:	11/19/2025	File:	C:\Users\...\Artix7_Power_2.SchDoc
			Drawn By:

A

A

B

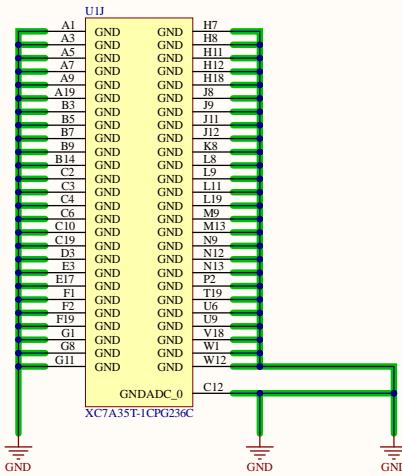
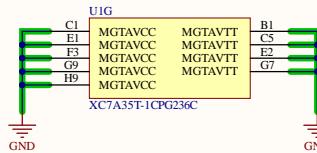
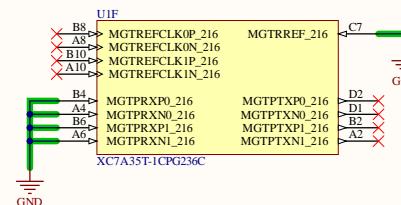
B

C

C

D

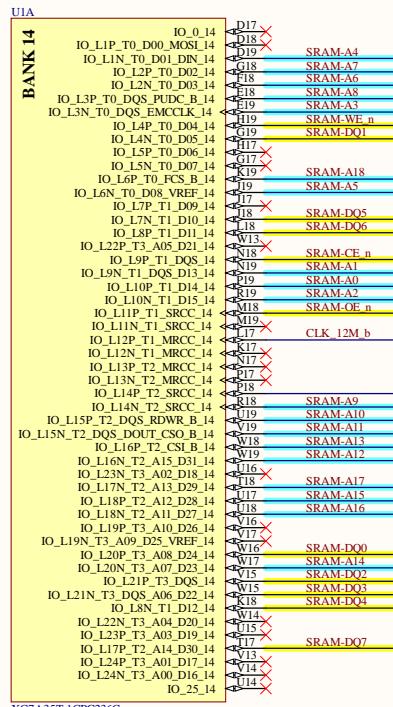
D

FPGA : Ground ConnectsFPGA : Unused High Speed TranscieversFPGA : Ground Connects

Title		
Size	Number	Revision
A3		
Date: 11/19/2025	Sheet of	
File: C:\Users\...\Artix7_Power_Grounds.SchD	Drawn By:	

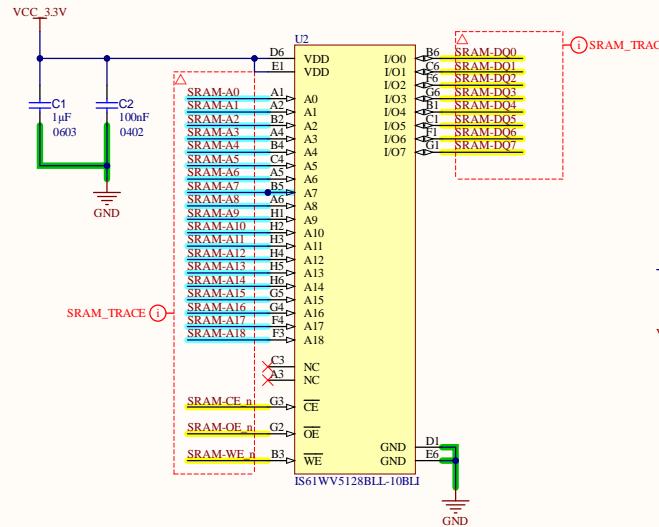
Artix-7 Clock and SRAM Connections

Artix 7 FPGA

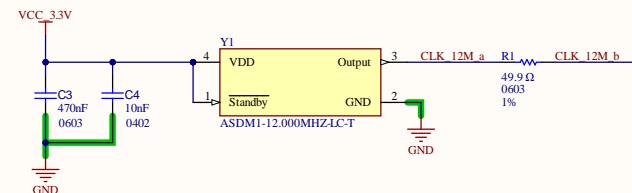


XC7A35T-1CPG236C

SRAM - 512x8



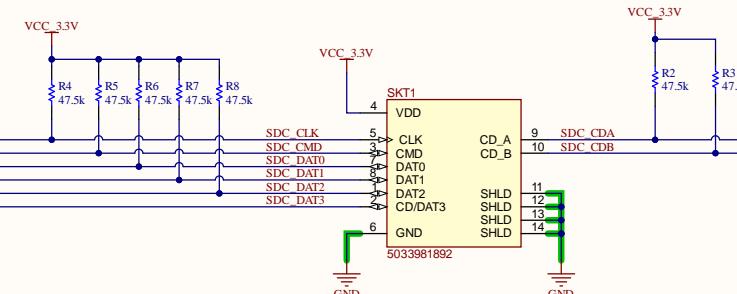
12 Megahertz CMOS Clock



SD Card Holder

BANK 16	IO_L6P_T0_16 IO_L5N_T0_VREF_16 IO_L11P_T1_SRCC_16 IO_L11N_T1_SRCC_16 IO_L12P_T1_MRCC_16 IO_L12N_T1_MRCC_16 IO_L13P_T2_MRCC_16 IO_L13N_T2_MRCC_16 IO_L14P_T2_SRCC_16 IO_L14N_T2_SRCC_16 IO_L19P_T3_16 IO_L19N_T3_VREF_16	A14 A15 A16 A17 A18 A19 A20 A21 A22 A23 A24 A25
---------	--	--

10_EJAV



Title		
Size	Number	Revision
A3		
Date:	11/19/2025	Sheet of
File:	C:\Users\...\Artix7_SRAM.SchDoc	Drawn By:

11

4

E

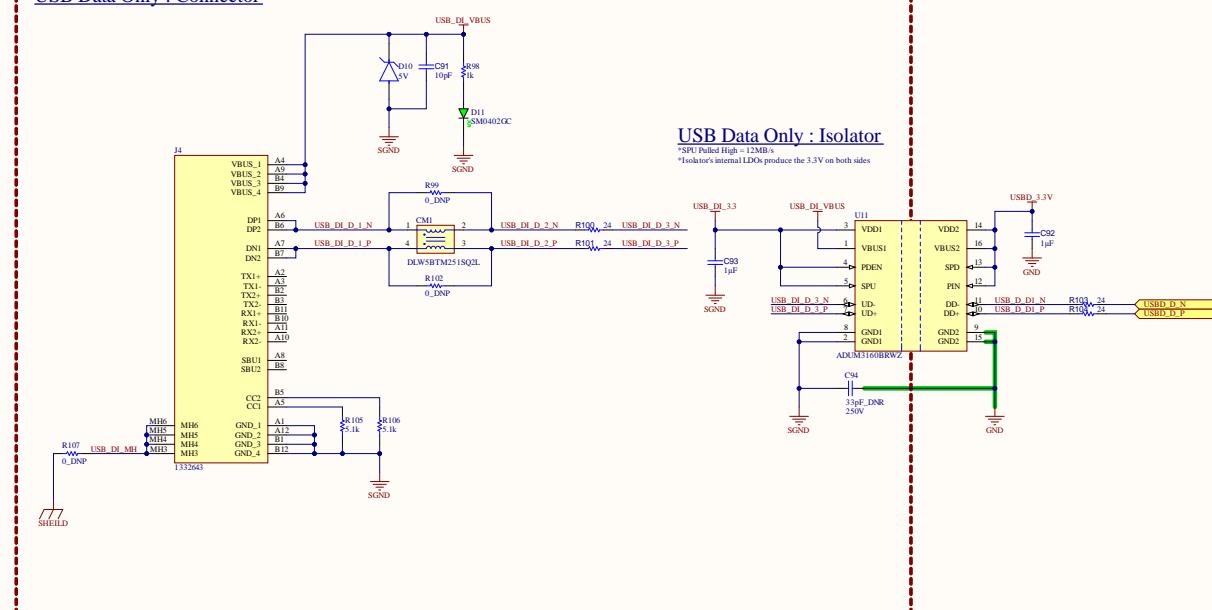
1

6

6

1

USB Data Only : Connector



Title	
Size A2	Number
Date 11/19/2025	Sheet of
File C:\Users\...\USB\DataOnly.SchDoc	Drawn By:

Artix-7 System Connections

A

B

C

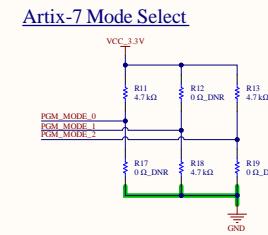
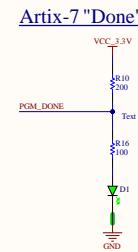
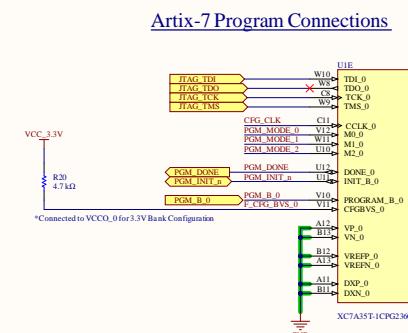
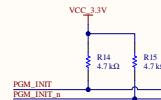
D

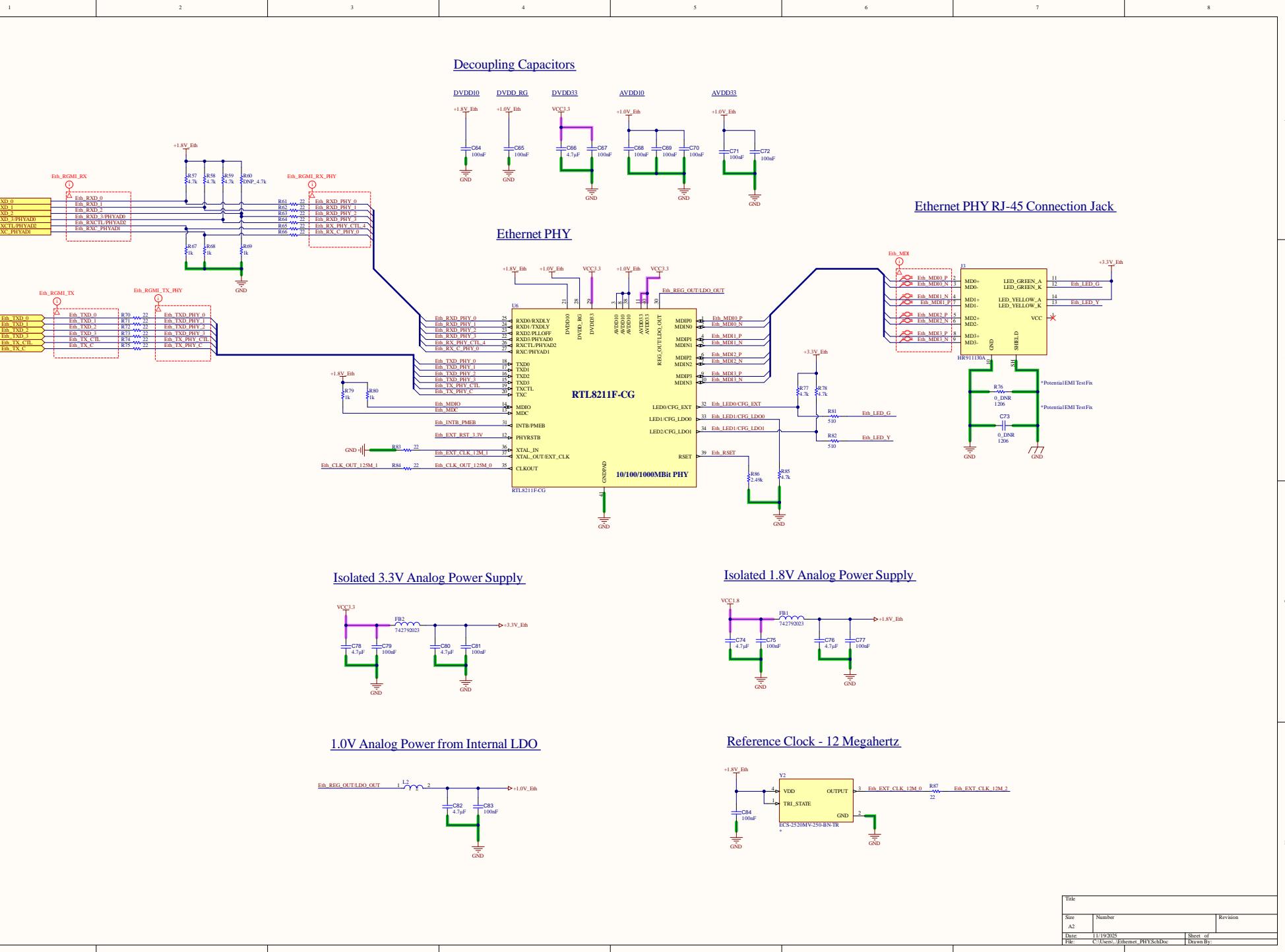
A

B

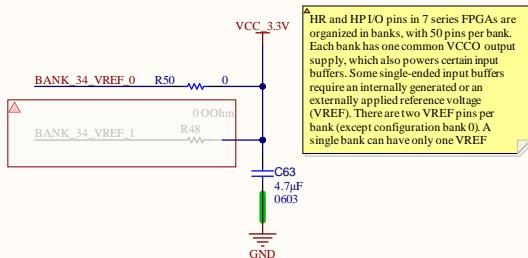
C

D

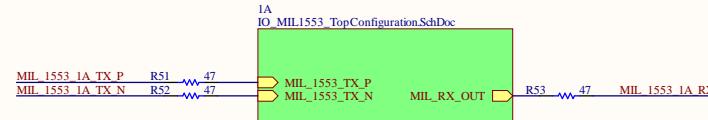




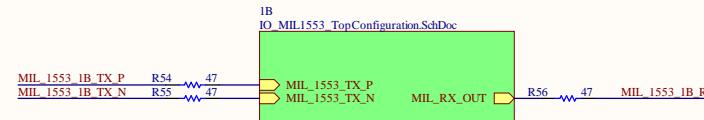
Artix 7 Bank 34 VRef Selection



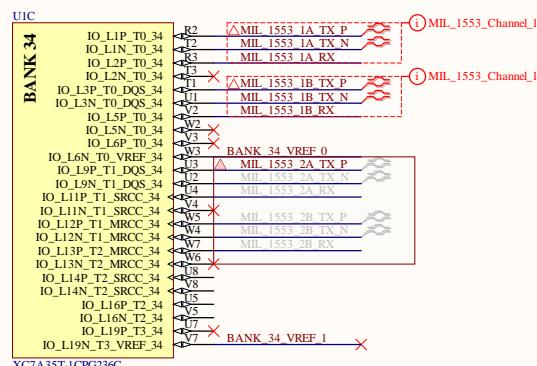
MIL-1553 Channel 1A



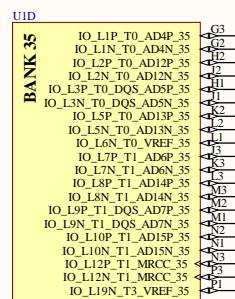
MIL-1553 Channel 1B



Artix 7 IO Channel Connections

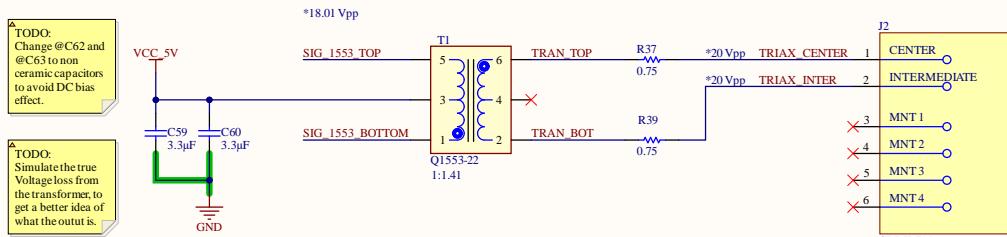


Artix 7 Unused IOs

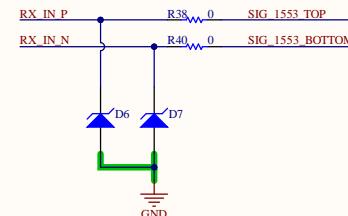


Title		
Size	Number	Revision
A3		
Date:	11/19/2025	Sheet of
File:	C:\Users\...\Artix7_IO_General.SchDoc	Drawn By:

MIL-1553 Triax Connector and Isolation Transformer

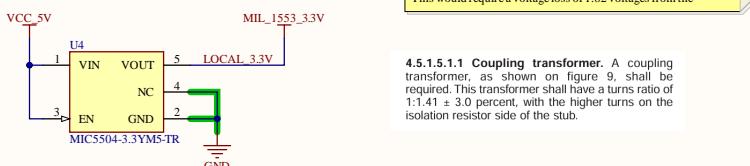


20V Overvoltage Protection for TX MOSFETs



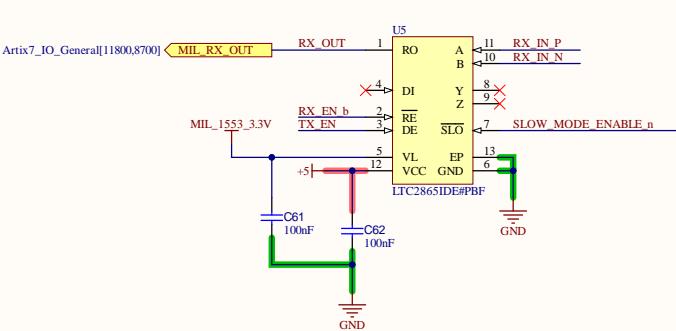
While the LTC2865IDE#PBF does have over voltage protection, the MOSFETs still need extra protection.

Power Supplies



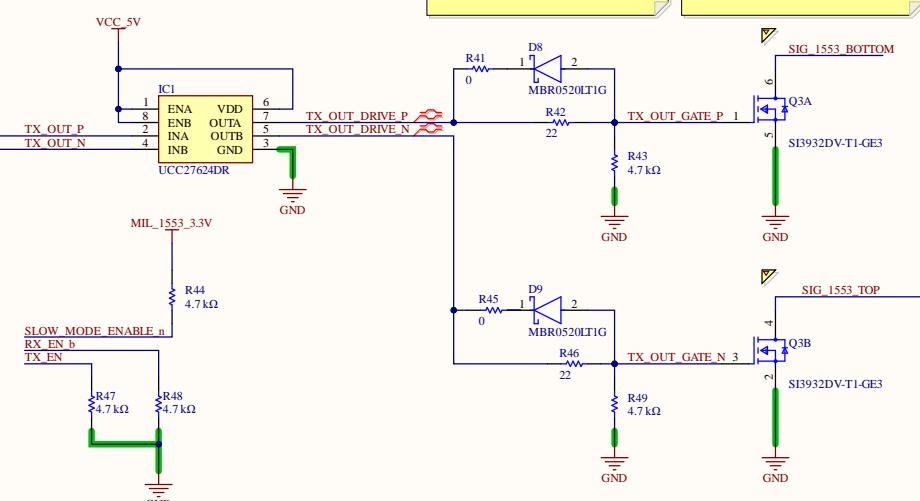
4.5.1.5.1.1 Coupling transformer. A coupling transformer, as shown on figure 9, shall be required. This transformer shall have a turns ratio of $1:1.41 \pm 3.0$ percent, with the higher turns on the isolation resistor side of the stub.

RX Signal Buffer for MIL STD 1553



► TODO: Find full-duplex transciever to replace current half-duplex reciever

TX Signal Generation for MIL-STD 1553



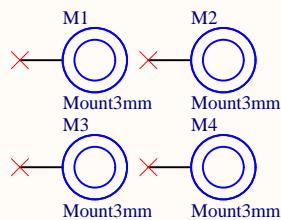
Title		
Size	Number	Revision
A3		
Date:	11/19/2025	Sheet of
File:	C:\Users\...\IO_MIL1553_TopConfig\d\Reliability	

A

A

B

B

Fiducial markers**Mechanical/Manufacturing**

C

C

D

D

Title		
Size A	Number	Revision
Date: 11/19/2025		Sheet of
File: C:\Users\...\Mechancils.SchDoc		Drawn By:

