Project Report: Calc2

A Report
Presented to
The Department of Electrical & Computer Engineering
Concordia University

In Partial Fulfillment
of the Requirements
of COEN 413

by
Noor Al-Musleh ID: 27150865
Christopher Dubuc-Pesetti ID: 40037815
Constantine Kokorogiannis ID: 40032046

Instructor: Dr. Otmane Ait Mohamed, PhD, Eng.

Concordia University
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Objective

The objective of this project was to create a verification plan for the Calc2 design. The environment design is class-based that uses randomization to generate random variables for the inputs. The design of Calc2 is similar to Calc1, with the added change that four commands are able to be sent into the calculator from each of the 4 ports. There are two internal arithmetic pipelines as well, one for the addition and subtraction operations and one for the shift left and shift right operations.

Observations

As what happened last time in the Calc1 design, we observed when we were looking at the waveforms that we could not see any input signals. This was a problem since we were using randomized input values and therefore could not see them directly on the waveform viewer. The workaround for this was to have the testbench output the input values to the terminal output when simulating the design.

When performing our tests, there was extremely odd behaviour occurring with the calculator. Our tests were ordered to do a set of 4 ADDs then 4 SUBs then 4 SHIFTLEFTs then 4 SHIFTRIGHTs. The tag values for each set started at 0 and were incremented by 1 to a final value of 3. On the output we recorded the 4 ADD operations being performed correctly, and then another set of 4 commands afterward that were seemingly not related to any of the commands that were input afterward. After the 4 unknown commands, the output signals became valued at X. This could be an issue with the parallel arithmetic pipelines trying to process the commands at the same time. This behaviour can be observed by simulating and viewing the waveforms of our testbench that was submitted for this project.

Bugs Found

1. When performing too many operations in a row, the calculator design breaks down and does not perform operations correctly.
2. Overflow response not outputting correct values in all ports for ADD operation.

Test Plan

Test Reference Number	Description
1.1	Testing “Add” operation on port 1
1.2	Testing “Add” operation on port 2
1.3	Testing “Add” operation on port 3
1.4	Testing “Add” operation on port 4
2.1	Testing “Subtract” operation on port 1
2.2	Testing “Subtract” operation on port 2
2.3	Testing “Subtract” operation on port 3
2.4	Testing “Subtract” operation on port 4
3.1	Testing “Shift Left” operation on port 1
3.2	Testing “Shift Left” operation on port 2
3.3	Testing “Shift Left” operation on port 3
3.4	Testing “Shift Left” operation on port 4
4.1	Test “Shift Right” operation on port 1
4.2	Test “Shift Right” operation on port 2
4.3	Test “Shift Right” operation on port 3
4.4	Test “Shift Right” operation on port 4
5.1	Testing “Success Response” on port 1
5.2	Testing “Success Response” on port 2
5.3	Testing “Success Response” on port 3
5.4	Testing “Success Response” on port 4
6.1	Testing “Overflow Response” on port 1
6.2	Testing “Overflow Response” on port 2

6.3	Testing “Overflow Response” on port 3
6.4	Testing “Overflow Response” on port 4
7.1	Testing “Underflow Response” on port 1
7.2	Testing “Underflow Response” on port 2
7.3	Testing “Underflow Response” on port 3
7.4	Testing “Underflow Response” on port 4
8.1	Testing “No Response” on port 1
8.2	Testing “No Response” on port 2
8.3	Testing “No Response” on port 3
8.4	Testing “No Response” on port 4
9	Testing Tag outputting in correct order
10	Testing concurrency: performing commands on all ports on the same clock cycle
11	Testing Priority: check that no port has higher priority
12	Testing Reset

Test Cases

Specification	Reference	Test Points	Test Scenarios (Decimal)	Expected Results	Actual Result	Result
Adding	1.1	Adding: Port 1	28 + 11	39	39	Pass
			14 + 20	34	34	Pass
			30 + 6	36	36	Pass

			5 + 30	35	35	Pass
	1.2	Adding: Port 2	21 + 14	35	35	Pass
			23 + 6	29	29	Pass
			20 + 17	37	37	Pass
			31 + 1	32	32	Pass
	1.3	Adding: Port 3	9 + 1	10	10	Pass
			12 + 10	22	22	Pass
			15 + 13	28	28	Pass
			16 + 29	45	45	Pass
	1.4	Adding: Port 4	24 + 10	34	34	Pass
			25 + 24	49	49	Pass
			17 + 2	19	19	Pass
			12 + 1	13	13	Pass
Subtracting	2.1	Subtracting: Port 1	17 - 9	8	-	Fail
			9 - 5	4	-	Fail
			16 - 4	12	-	Fail

			17 - 15	2	-	Fail
	2.2	Subtracting: Port 2	29 - 17	12	-	Fail
			11 - 13	-2	-	Fail
			30 - 26	4	-	Fail
			9 - 3	6	-	Fail
	2.3	Subtracting: Port 3	0 - 18	-18	-	Fail
			11 - 0	11	-	Fail
			20 - 4	16	-	Fail
			18 - 9	9	-	Fail
	2.4	Subtracting: Port 4	9 + 24	-15	-	Fail
			25 - 24	1	-	Fail
			0 - 19	-19	-	Fail
			31 - 19	12	-	Fail
Shift Left	3.1	Shift left: Port 1	1 << 8	256	-	
			4 << 18	1048576	-	
			12 << 6	768	-	
			8 << 13	65536	-	Fail
	3.2	Shift left: Port 2	14 << 8	3584	-	
			25 << 4	400	-	
			21 << 13	172032	-	
			5 << 12	20480	-	Fail
	3.3	Shift left: Port 3	12 << 12	49512	-	Fail

			16 << 18	4194304	-	Fail
			29 << 17	3801088	-	Fail
			23 << 18	6029312	-	Fail
	3.4	Shift left: Port 4	8 << 9	4096	-	Fail
			18 << 19	9437184	-	Fail
			31 << 31	66571993088	-	Fail
			13 << 16	851968	-	Fail
Shift Right	4.1	Shift right: Port 1	28 >> 5	0	-	Fail
			15 >> 19	0	-	Fail
			12 >> 16	0	-	Fail
			20 >> 3	2	-	Fail
	4.2	Shift right: Port 2	15 >> 25	0	-	Fail
			24 >> 2	6	-	Fail
			2 >> 18	0	-	Fail
			16 >> 29	0	-	Fail
	4.3	Shift right: Port 3	6 >> 16	0	-	Fail
			0 >> 11	0	-	Fail
			9 >> 17	0	-	Fail
			7 >> 10	0	-	Fail
	4.4	Shift right: Port 4	24 >> 20	0	-	Fail
			3 >> 26	0	-	Fail
			15 >> 27	0	-	Fail

			13 >> 0	13	-	Fail
Response Values	5.1	Success response: Port 1	30 + 6	b01	b01	Pass
	5.2	Success response: Port 2	23 + 6	b01	b01	Pass
	5.3	Success response: Port 3	0 + 18	b01	b01	Pass
	5.4	Success response: Port 4	17 + 2	b01	b01	Pass
	6.1	Overflow response: Port 1	28 + 11	b10	b01	Fail
	6.2	Overflow response: Port 2	31 + 1	b10	b01	Fail
	6.3	Overflow response: Port 3	12 + 10	b10	b01	Fail
	6.4	Overflow response: Port 4	25 + 24	b10	b01	Fail
	7.1	Underflow response: Port 1	17 - 9	b10	-	Fail
	7.2	Underflow response: Port 2	9 - 3	b10	-	Fail
	7.3	Underflow response: Port 3	18 - 9	b10	-	Fail
	7.4	Underflow response: Port 4	25 - 24	b10	-	Fail
	8.1	No response: Port 1	Data input is 0 (in between cycles)	b00	b00	Pass
	8.2	No response: Port 2		b00	b00	Pass
	8.3	No response: Port 3		b00	b00	Pass
	8.4	No response: Port 4		b00	b00	Pass
Tag	9	Tag inputs for Add command	Tag values: 0 - 1 - 2 - 3	0 - 1 - 2 - 3 on output	0 - 1 - 2 - 3 on output	Pass
Concurrency Tests	10	Test performing commands on all ports on the same	1 add operation on each port during a single clock cycle	Add operations execute properly one after	Add operations execute	Pass

		clock cycle		another	properly one after another	
Priority Tests	11	Test performing commands on all ports on the same clock cycle	Add operations done on same clock cycle	P1 = P2 = P3 = P4	P1 > P2 > P3 > 4	Fail
Reset	12	Hold reset input high for 7 cycles	Reset input held high for 7 cycles	Data Inputs reset to 0	Data Inputs reset to 0	Pass