# Project Report: Calc1

A Report
Presented to
The Department of Electrical & Computer Engineering
Concordia University

In Partial Fulfillment
of the Requirements
of COEN 413

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## Objective

The objective of this project was to create a verification plan for the Calc1 design. We had to also determine the test cases required to verify our plan. Before creating the plan, we had to understand the design. It has four operators (ADD, SUB, SHIFT RIGHT and SHIFT LEFT) and we have 4 input ports to work with for setting values. There are 4 outputs, one for each input port and it takes 2 clock cycles to compute a command, and a third to view the output.

## Observations

First thing we observed when we were looking at the waveform was that we couldn't see any input signals, so it was hard to see if our commands were getting performed on the clock edge. All we had were the outputs, which we can see the results in our test plan below.

Another thing we noticed was that the output gets reset after every command, so it was impossible to test if the reset was working properly, since the registers don’t save their values.

## Bugs Found

1. Adding operation not performing correctly in port 4
2. Subtracting operation not performing correctly in port 4
3. Overflow response not outputting correct values in all ports
4. Underflow response not outputting correct values in all ports
5. Invalid Response not outputting correct values in all ports

# Test Plan

| Test Reference Number | Description |
|---|---|
| 1.1 | Testing “Add” operation on port 1 |
| 1.2 | Testing “Add” operation on port 2 |
| 1.3 | Testing “Add” operation on port 3 |
| 1.4 | Testing “Add” operation on port 4 |
| 2.1 | Testing “Subtract” operation on port 1 |
| 2.2 | Testing “Subtract” operation on port 2 |
| 2.3 | Testing “Subtract” operation on port 3 |
| 2.4 | Testing “Subtract” operation on port 4 |
| 3.1.1 | Testing “Shift Left” operation: shift by 2 places on port 1 |
| 3.1.2 | Testing “Shift Left” operation: shift by 2 places on port 2 |
| 3.1.3 | Testing “Shift Left” operation: shift by 2 places on port 3 |
| 3.1.4 | Testing “Shift Left” operation: shift by 2 places on port 4 |
| 3.2.1 | Testing “Shift Left” operation: shift by 0 places on port 1 |
| 3.2.2 | Testing “Shift Left” operation: shift by 0 places on port 2 |
| 3.2.3 | Testing “Shift Left” operation: shift by 0 places on port 3 |
| 3.2.4 | Testing “Shift Left” operation: shift by 0 places on port 4 |
| 3.3.1 | Testing “Shift Left” operation: shift by 31 places on port 1 |
| 3.3.2 | Testing “Shift Left” operation: shift by 31 places on port 2 |
| 3.3.3 | Testing “Shift Left” operation: shift by 31 places on port 3 |
| 3.3.4 | Testing “Shift Left” operation: shift by 31 places on port 4 |
| 3.4.1 | Testing “Shift Left” operation: checking that the upper 27 bits of operand 2 are ignored on port 1 |
| 3.4.2 | Testing “Shift Left” operation: checking that the upper 27 bits of operand 2 are ignored on port 2 |

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| 3.4.3 | Testing “Shift Left” operation: checking that the upper 27 bits of operand 2 are ignored on port 3 |
| 3.4.4 | Testing “Shift Left” operation: checking that the upper 27 bits of operand 2 are ignored on port 4 |
| 4.1.1 | Test “Shift Right” operation: shift by 2 places on port 1 |
| 4.1.2 | Test “Shift Right” operation: shift by 2 places on port 2 |
| 4.1.3 | Test “Shift Right” operation: shift by 2 places on port 3 |
| 4.1.4 | Test “Shift Right” operation: shift by 2 places on port 4 |
| 4.2.1 | Testing “Shift Right” operation: shift by 0 places on port 1 |
| 4.2.2 | Testing “Shift Right” operation: shift by 0 places on port 2 |
| 4.2.3 | Testing “Shift Right” operation: shift by 0 places on port 3 |
| 4.2.4 | Testing “Shift Right” operation: shift by 0 places on port 4 |
| 4.3.1 | Testing “Shift Right” operation: shift by 31 places on port 1 |
| 4.3.2 | Testing “Shift Right” operation: shift by 31 places on port 2 |
| 4.3.3 | Testing “Shift Right” operation: shift by 31 places on port 3 |
| 4.3.4 | Testing “Shift Right” operation: shift by 31 places on port 4 |
| 4.4.1 | Testing “Shift Right” operation: checking that the upper 27 bits of operand 2 are ignored on port 1 |
| 4.4.2 | Testing “Shift Right” operation: checking that the upper 27 bits of operand 2 are ignored on port 2 |
| 4.4.3 | Testing “Shift Right” operation: checking that the upper 27 bits of operand 2 are ignored on port 3 |
| 4.4.4 | Testing “Shift Right” operation: checking that the upper 27 bits of operand 2 are ignored on port 4 |
| 5.1 | Testing “Success Response” on port 1 |
| 5.2 | Testing “Success Response” on port 2 |
| 5.3 | Testing “Success Response” on port 3 |
| 5.4 | Testing “Success Response” on port 4 |

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| 6.1 | Testing “Invalid Response” on port 1 |
| 6.2 | Testing “Invalid Response” on port 2 |
| 6.3 | Testing “Invalid Response” on port 3 |
| 6.4 | Testing “Invalid Response” on port 4 |
| 7.1 | Testing “No Response” on port 1 |
| 7.2 | Testing “No Response” on port 2 |
| 7.3 | Testing “No Response” on port 3 |
| 7.4 | Testing “No Response” on port 4 |
| 8.1 | Testing “Overflow Response” on port 1 |
| 8.2 | Testing “Overflow Response” on port 2 |
| 8.3 | Testing “Overflow Response” on port 3 |
| 8.4 | Testing “Overflow Response” on port 4 |
| 9.1 | Testing “Underflow Response” on port 1 |
| 9.2 | Testing “Underflow Response” on port 2 |
| 9.3 | Testing “Underflow Response” on port 3 |
| 9.4 | Testing “Underflow Response” on port 4 |
| 10 | Testing concurrency: performing commands on all ports on the same clock cycle |
| 11 | Testing Priority: check that no port has higher priority |

# Test Cases

| Specification | Reference | Test Points | Test Scenarios | Expected Results | Result | Fail Result |
|---|---|---|---|---|---|---|
| Adding | 1.1 | Adding: Port 1 | 0x0000FFFF + 0xFFFF0000 | 0xFFFFFFFF | Success | |
| | 1.2 | Adding: Port 2 | | | Success | |
| | 1.3 | Adding: Port 3 | | | Success | |
| | 1.4 | Adding: Port 4 | 0xFFFFFFFF0 + 0x00000001 | 0xFFFFFFF1 | Fail | Zeroes on output |
| Subtracting | 2.1 | Subtracting: Port 1 | 0xFFFFFFFF - 0xFFFFFFFE | 0x00000001 | Success | |
| | 2.2 | Subtracting: Port 2 | | | Success | |
| | 2.3 | Subtracting: Port 3 | | | Success | |
| | 2.4 | Subtracting: Port 4 | 0xFFFFFFFF - 0xFFFFFFFF | 0x00000000 | Fail | Zeroes on output |
| Shift Left | 3.1.1 | Shift left: Port 1 | 0x00000001 << 2 | 0x00000004 | Success | |
| | 3.1.2 | Shift left: Port 2 | | | Success | |
| | 3.1.3 | Shift left: Port 3 | | | Success | |
| | 3.1.4 | Shift left: Port 4 | | | Success | |
| | 3.2.1 | Shift left: Port 1 | 0x00000009 << 0 | 0x00000009 | Fail | Zeros on output |
| | 3.2.2 | Shift left: Port 2 | | | Fail | |
| | 3.2.3 | Shift left: Port 3 | | | Fail | |
| | 3.2.4 | Shift left: Port 4 | | | Fail | |
| | 3.3.1 | Shift left: Port 1 | 0x00000007 << 31 | 0x80000000 | Success | |
| | 3.3.2 | Shift left: Port 2 | | | Success | |
| | 3.3.3 | Shift left: Port 3 | | | Success | |
| | 3.3.4 | Shift left: Port 4 | | | Success | |
| | 3.4.1 | Shift left: Port 1 | Operand1 : 0x00000001 | | Success | |
| | 3.4.2 | Shift left: Port 2 | | | Success | |

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| | 3.4.3 | Shift left: Port 3 | Operand2: 0xFFFFFFF2 | 0x00040000 | Success | |
| | 3.4.4 | Shift left: Port 4 | | | Success | |
| Shift Right | 4.1.1 | Shift right: Port 1 | 0x80000000 >> 2 | 0x20000000 | Success | |
| | 4.1.2 | Shift right: Port 2 | | | Success | |
| | 4.1.3 | Shift right: Port 3 | | | Success | |
| | 4.1.4 | Shift right: Port 4 | | | Success | |
| | 4.2.1 | Shift right: Port 1 | 0x00000009 << 0 | 0x00000009 | Fail | Zeros on output |
| | 4.2.2 | Shift right: Port 2 | | | Fail | |
| | 4.2.3 | Shift right: Port 3 | | | Fail | |
| | 4.2.4 | Shift right: Port 4 | | | Fail | |
| | 4.3.1 | Shift right: Port 1 | 0xE0000000 << 31 | 0x00000001 | Success | |
| | 4.3.2 | Shift right: Port 2 | | | Success | |
| | 4.3.3 | Shift right: Port 3 | | | Success | |
| | 4.3.4 | Shift right: Port 4 | | | Success | |
| | 4.4.1 | Shift right: Port 1 | Operand1 : 0x80000000<br>Operand2: 0xFFFFFFF2 | 0x00020000 | Success | |
| | 4.4.2 | Shift right: Port 2 | | | Success | |
| | 4.4.3 | Shift right: Port 3 | | | Success | |
| | 4.4.4 | Shift right: Port 4 | | | Success | |
| Response Values | 5.1 | Success response: Port 1 | 0x0000FFFF + 0xFFFF0000 | b01 | Success | |
| | 5.2. | Success response: Port 2 | | | Success | |
| | 5.3 | Success response: Port 3 | | | Success | |
| | 5.4 | Success response: Port 4 | | | Success | |
| | 6.1 | Invalid response: Port 1 | Command input = h7 | b10 | Fail | Response output shows success (b01) |
| | 6.2 | Invalid response: Port 2 | | | Fail | |
| | 6.3 | Invalid response: Port 3 | | | Fail | |
| | 6.4 | Invalid response: Port 4 | | | Fail | |

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| | 7.1 | No response: Port 1 | All command inputs b00, all data in h00000000 | B00 | Success | |
| | 7.2 | No response: Port 2 | | | Success | |
| | 7.3 | No response: Port 3 | | | Success | |
| | 7.4 | No response: Port 4 | | | Success | |
| | 8.1 | Overflow response: Port 1 | 0xFFFFFFFF + 0x00000002 | b10 | Fail | Response output shows X |
| | 8.2 | Overflow response: Port 2 | | | Fail | |
| | 8.3 | Overflow response: Port 3 | | | Fail | |
| | 8.4 | Overflow response: Port 4 | | | Fail | Response output shows no operation (b00) |
| | 9.1 | Underflow response: Port 1 | 0x00000000 - 0x00000001 | b10 | Fail | Response output shows X |
| | 9.2 | Underflow response: Port 2 | | | Fail | |
| | 9.3 | Underflow response: Port 3 | | | Fail | |
| | 9.4 | Underflow response: Port 4 | | | Fail | Response output shows no operation (b00) |
| Concurrency Tests | 10 | Test performing commands on all ports on the same clock cycle | | | Success | |
| Priority Tests | 11 | Test performing commands on all ports on the same clock cycle | | | Fail | Priority of ports is: 1 > 2 > 3 > 4 |
| Reset | | Hold reset input high for 7 cycles | Reset input held high (hFF) for 7 clock cycles | All inputs set to 0 | Untestable | No inputs available when simulating |