Christopher Wilson

Hardware Design Engineer

5645 Cold Water Dr.
Castro Valley, CA 94552
+1 (858) 722 2298
cwilson@cdwilson.us
www.cdwilson.us
cdwilson
cdwilson

Experience

Vocational

2010 – Present **Hardware Engineer**, *Cisco Systems*, San Jose, CA.

Internet of Things (IoT) BU

- Lead design engineer for Connected Grid Endpoint (CGE) SDK hardware reference design.
  - Designed ARM Cortex-M3 based modular reference designs for 802.15.4g 900MHz RF and PLC smart grid endpoints. Schematic capture in Cadence Concept.
  - Managed ECAD and MCAD contractors during PCB layout and enclosure design.
  - Responsible for NPI engineering using Cisco manufacturing tools.
  - Worked closely with Cisco Developer Network (CDN) partners to review partner hardware designs for "Cisco Compatible" certification.
- Developed the worlds largest closed-circuit 900MHz RF and PLC mesh network testbed consisting of over 5000 endpoint devices.
  - Designed sophisticated custom rack-mount chassis and internal backplane PCB with embedded Linux ARM controller, providing networked back-channel and instruction-level JTAG/SWD debug to every endpoint in the testbed.
  - Modified Linux kernel source code and BSP to support custom backplane PCB hardware.
  - Developed user space applications in C for CLI device control.
  - Developed Python CGI web application for device management from a web browser.
- Managed DevOps for the Connected Grid Endpoint firmware team.
  - Set up and maintained Git (SCM), Jenkins (CI and release build), and Gerrit (code review) servers.
  - Developed build scripts in Windows batch and Bash for a hybrid Cygwin/IAR firmware build server.

2007 – 2010 **Hardware Engineer**, *Arch Rock (acquired by Cisco Systems)*, San Francisco, CA.

- Responsible for transition to agile in-house hardware design and manufacturing. Adopted industry standard EDA, DFM, and PLM tools and methodology to scale hardware development for production.
- Designed 802.15.4 2.4GHz “PhyNet” wireless sensor motes and network interface cards.
  - Schematic capture and PCB layout using OrCAD Capture and Cadence Allegro.
  - Board level bring-up and verification using lab test equipment.
  - Hand assembled and reworked prototype PCBs.
- Developed embedded TinyOS firmware applications in nesC (network embedded systems C) for hardware bring-up and manufacturing test. Debugged and optimized production runtime firmware with special emphasis on low power operation.
- Designed and built a fully isolated wireless mesh testbed with reconfigurable RF topologies.
  - Developed integration test scripts in Ruby to allow automated deployment of embedded firmware for devices in the testbed.
  - Tightly integrated the testbed with Buildbot based continuous integration to facilitate automated regression testing for the full mesh network stack.

2006 **Undergraduate Researcher**, *Berkeley Wireless Research Center*, Berkeley, CA.

- Implemented distributed adaptive duty cycling algorithm in nesC for Telos wireless sensor motes running TinyOS 1.x operating system.

2004 **Interim Engineering Intern**, *Qualcomm*, San Diego, CA.

CDMA Technologies form factor accurate (FFA) baseband team

- Developed framework for an intranet website used to track internal development of FFA hardware.

Miscellaneous

2010 – Present **Proprietor**, *Flying Camp Design*, Castro Valley, CA.

Indie hardware and software design

- Designed open source hardware boot-strap loader (BSL) programmer for TI MSP430 MCUs.
- Manufactured and sold over 100 programmers internationally.
- Developed open source cross-platform BSL GUI utility in Python.

2010 – 2015 **Partner**, *Moteware*, Berkeley, CA.

Open source hardware disseminator for the academic research community

- Founded with a group of former graduate students at UC Berkeley.
- Helped manage sales, support, IT, and manufacturing.

Education

2003 – 2007 **B.S. Electrical Engineering and Computer Science**, *University of California, Berkeley*, Berkeley, CA.

Awards: Edward Frank Kraft Scholarship
Activities and Societies: IEEE, Alpha Gamma Omega, FoCUS

Skills & Expertise

Lab	PCA bring-up, electronic test equipment, hand soldering/rework, lab safety
EDA	Cadence Concept and Allegro, OrCAD Capture, Cadsoft EAGLE
PLM	Cisco Agile, Arena Solutions
Advanced	Git, Python
Basic	make, C, nesC, Java, Bash, Ruby, Tcl/Tk, LaTeX, Bazaar, SVN, CVS
Environment	Mac OS X, Linux, Windows, Cygwin

Interests

Travel	Traveled extensively in Europe and parts of Africa.
Social Justice	Projects in Kenya, Haiti, and Mexico.
Sports	Surfing, skateboarding, snowboarding, biking, lacrosse

References

Available upon request.