

Y86 Notes

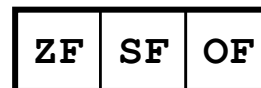
■ Y86 features

- 8 32-bit registers with the same names as the IA32 32-bit registers
 - different names from those in text, such as **%rax**, which are 64-bit
 - F indicates no register
- 3 condition codes: ZF, SF, OF
- a program counter (PC)
- a program status byte: AOK, HLT, ADR, INS
- memory: up to 4 GB to hold program and data

RF: Program registers

0	%eax	6	%esi
1	%ecx	7	%edi
2	%edx	4	%esp
3	%ebx	5	%ebp

CC: Condition codes



PC



Stat: Program Status



DMEM: Memory



Y86 Assembler Directives

Directive	Effect
<code>.pos number</code>	Subsequent lines of code start at address number
<code>.align number</code>	Align the next line to a number -byte boundary
<code>.long number</code>	Put number at the current address in memory

- These can be used to set up memory in various places in the address space
- `.pos` can put sections of code in different places in memory
- `.align` should be used before setting up a static variable
- `.long` can be used to initialize a static variable

Status Conditions

Mnemonic	Code
AOK	1

- Normal operation

Mnemonic	Code
HLT	2

- Halt instruction encountered

Mnemonic	Code
ADR	3

- Bad address (either instruction or data) encountered

Mnemonic	Code
INS	4

- Invalid instruction encountered

Desired Behavior

- If AOK, keep going
- Otherwise, stop program execution

Move Operation

Instruction	Effect	Description
<code>irmovl V,R</code>	$\text{Reg}[R] \leftarrow V$	Immediate-to-register move
<code>rrmovl rA,rB</code>	$\text{Reg}[rB] \leftarrow \text{Reg}[rA]$	Register-to-register move
<code>rmmovl rA,D(rB)</code>	$\text{Mem}[\text{Reg}[rB]+D] \leftarrow \text{Reg}[rA]$	Register-to-memory move
<code>mrmovl D(rA),rB</code>	$\text{Reg}[rB] \leftarrow \text{Mem}[\text{Reg}[rA]+D]$	Memory-to-register move

- `irmovl` is used to place known numeric values (labels or numeric literals) into registers
- `rrmovl` copies a value between registers
- `rmmovl` stores a word in memory
- `mrmovl` loads a word from memory
- `rmmovl` and `mrmovl` are the only instructions that access memory - Y86 is a load/store architecture



Jump Instruction Types

■ Unconditional jumps

- `jmp Dest` $PC \leftarrow Dest$

What about checking OF?

■ Conditional jumps

- `jle Dest` $PC \leftarrow Dest$ if last result ≤ 0
 - $SF=1$ or $ZF=1$
- `jlt Dest` $PC \leftarrow Dest$ if last result < 0
 - $SF=1$ **and** $ZF=0$
- `je Dest` $PC \leftarrow Dest$ if last result $= 0$
 - $ZF=1$
- `jne Dest` $PC \leftarrow Dest$ if last result $\neq 0$
 - $ZF=0$
- `jge Dest` $PC \leftarrow Dest$ if last result ≥ 0
 - $SF=0$ or $ZF=1$
- `jgt Dest` $PC \leftarrow Dest$ if last result > 0
 - $SF=0$ **and** $ZF=0$

If the last result is not what is specified, then the jump is not taken; and the next sequential instruction is executed, i.e., $PC = PC + \text{jump instruction size}$

Stack Operations

stack for Y86 works just the same as with IA32

`pushl rA`



$R[\%esp] \leftarrow R[\%esp] - 4$
 $M[R[\%esp]] \leftarrow R[rA]$

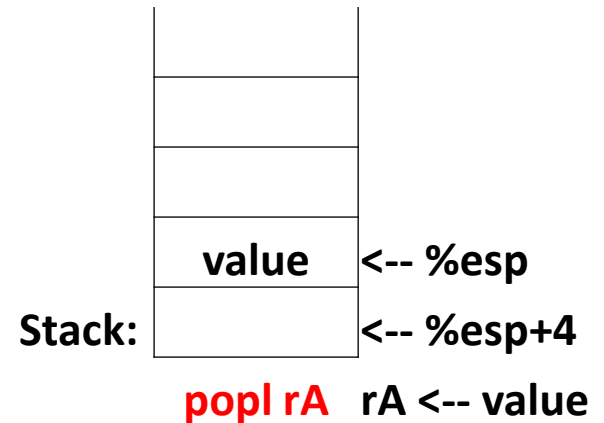
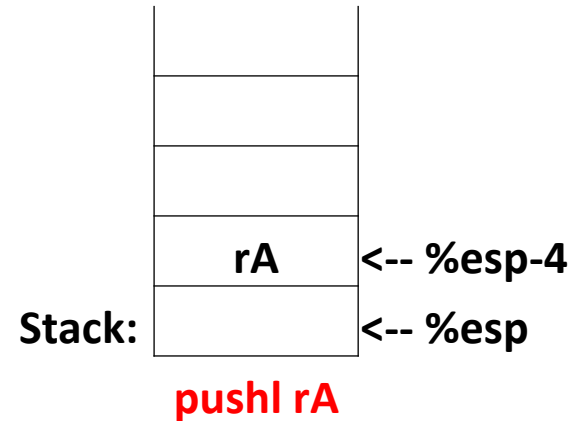
- Decrement `%esp` by 4
- Store word from `rA` to memory at `%esp`
- Like IA32

`popl rA`



- Read word from memory at `%esp`
- Save in `rA`
- Increment `%esp` by 4
- Like IA32

$R[rA] \leftarrow M[R[\%esp]]$
 $R[\%esp] \leftarrow R[\%esp] + 4$



Instruction Encoding (32-bit)

Byte	0	1	2	3	4	5	
nop	0	0					
halt	1	0					
rrmovl rA, rB	2	0	rA	rB			
irmovl V, rB	3	0	F	rB	V		
rmmovl rA, D(rB)	4	0	rA	rB	D		
mrmovl D(rB), rA	5	0	rA	rB	D		
Op1 rA, rB	6	fn	rA	rB			
jXX Dest	7	fn	Dest				
call Dest	8	0	Dest				
ret	9	0					
pushl rA	A	0	rA	F			
popl rA	B	0	rA	F			

addl	6	0
subl	6	1
andl	6	2
xorl	6	3
jmp	7	0
jle	7	1
jl	7	2
je	7	3
jne	7	4
jge	7	5
jg	7	6

Instruction Encoding (64-bit)

Byte	0	1	2	3	4	5	6	7	8	9
halt	0	0								
nop	1	0								
<u>cmovXX</u> <u>rA</u> , <u>rB</u>	2	fn	rA	rB						
<u>irmovq</u> <u>V</u> , <u>rB</u>	3	0	F	rB	V					
<u>rmmovq</u> <u>rA</u> , <u>D(rB)</u>	4	0	rA	rB	D					
<u>mrmovq</u> <u>D(rB)</u> , <u>rA</u>	5	0	rA	rB	D					
<u>OPq</u> <u>rA</u> , <u>rB</u>	6	fn	rA	rB						
<u>jXX</u> <u>Dest</u>	7	fn	Dest							
<u>call</u> <u>Dest</u>	8	0	Dest							
<u>ret</u>	9	0								
<u>pushq</u> <u>rA</u>	A	0	rA	F						
<u>popq</u> <u>rA</u>	B	0	rA	F						

Instruction Encoding

Operations

addq	<table border="1"><tr><td>6</td><td>0</td></tr></table>	6	0
6	0		
subq	<table border="1"><tr><td>6</td><td>1</td></tr></table>	6	1
6	1		
andq	<table border="1"><tr><td>6</td><td>2</td></tr></table>	6	2
6	2		
xorq	<table border="1"><tr><td>6</td><td>3</td></tr></table>	6	3
6	3		

Branches

jmp	<table><tr><td>7</td><td>0</td></tr></table>	7	0	jne	<table><tr><td>7</td><td>4</td></tr></table>	7	4
7	0						
7	4						
jle	<table><tr><td>7</td><td>1</td></tr></table>	7	1	jge	<table><tr><td>7</td><td>5</td></tr></table>	7	5
7	1						
7	5						
jnl	<table><tr><td>7</td><td>2</td></tr></table>	7	2	jg	<table><tr><td>7</td><td>6</td></tr></table>	7	6
7	2						
7	6						
je	<table><tr><td>7</td><td>3</td></tr></table>	7	3				
7	3						

Moves

rrmovq	<table><tr><td>2</td><td>0</td></tr></table>	2	0	cmovne	<table><tr><td>2</td><td>4</td></tr></table>	2	4
2	0						
2	4						
cmovle	<table><tr><td>2</td><td>1</td></tr></table>	2	1	cmovge	<table><tr><td>2</td><td>5</td></tr></table>	2	5
2	1						
2	5						
cmovl	<table><tr><td>2</td><td>2</td></tr></table>	2	2	cmovg	<table><tr><td>2</td><td>6</td></tr></table>	2	6
2	2						
2	6						
cmove	<table><tr><td>2</td><td>3</td></tr></table>	2	3				
2	3						

0	%eax	6	%esi
1	%ecx	7	%edi
2	%edx	4	%esp
3	%ebx	5	%ebp