RTL Specification Design Document

# 1. Document Information

Title: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Author(s): \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Reviewer(s): \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Version: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Date: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Confidentiality Level: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

# 2. Revision History

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Version | Date | Author | Description | Reviewer | Approval |

# 3. Purpose & Scope

Describe the purpose and scope of this RTL design.

# 4. References

List related architecture specifications, standards, and protocols.

# 5. Requirements

* - Functional Requirements: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Performance Requirements: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Power/Area Requirements: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Safety/Security Requirements: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

# 6. High-Level Architecture

Insert block diagram and describe external interfaces, clocking, reset, and power domains.

# 7. Design Description

* - RTL Hierarchy: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Data Path Description: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Interface Details: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - State Machines: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Error Handling & Exceptions: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

# 8. Microarchitecture Details

* - Pipeline stages: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Buffers/FIFOs/Arbiters: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - CDC Handling: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Synchronizers: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Low-power Techniques: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

# 9. Design Constraints

* - Timing Constraints: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Reset Behavior: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Synthesis Constraints: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - DFT Requirements: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

# 10. Verification Plan (Summary)

* - Testbench Architecture: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Coverage Goals: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Assertions: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Formal Checks: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Compliance Tests: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

# 11. Validation Plan (System-Level)

* - Emulation/Prototyping: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Integration Testing: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Performance Validation: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

# 12. Deliverables

* - RTL Code: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Simulation Testbench: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Verification Results: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Synthesis Reports: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
* - Sign-off Checklist: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

# 13. Open Issues & Assumptions

List known limitations, pending design decisions, and assumptions.

# 14. Glossary & Acronyms

Define technical terms and abbreviations used in this document.

# 15. Approval & Sign-off

Prepared by: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Reviewed by: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Approved by: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_