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Homework #9 Solution

Problem 1)

The **noise_ptsi_fast_routed.rpt** report contains the following worst functional noise bump:

```
noise_region: below_high
 pin name (net name)       width    height     slack
 ----------------------------------------------------
u_logic/FE_PHC716_n4980/A (u_logic/n4980)
                           0.2360    0.6138   -0.0269
```

The input pin *u_logic/FE_PHC716_n4980/A* is driven by the *u_logic/Vmj2z4_reg/QN* output pin. We can get a detailed list of the aggressors with the *report_noise_calculation* command as follows:

```
pt_shell> report_noise_calculation -below -high
     -from u_logic/Vmj2z4_reg/QN -to u_logic/FE_PHC716_n4980/A
...
                             Height    Width     Area      Aggressor Attributes
-------------------------------------------------------------------------------
Aggressors:
 u_logic/FE_PHN1031_U329_Z_0  0.2392    0.2329    0.0279    A D
 u_logic/FE_PHN716_n4980      0.2230    0.2512    0.0280    A
 u_logic/FE_PHN1021_U295_Z_0  0.0787    0.2026    0.0080    A
 u_logic/FE_PHN722_n5049      0.0516    0.2381    0.0061    A
 u_logic/FE_PHN772_U594_Z_0   0.0173    0.1926    0.0017    A
 u_logic/FE_PHN1137_n5089     0.0150    0.1909    0.0014    A
 Total:                       0.6138    0.2360    0.0724
```

The most significant aggressor (by area) is *u_logic/FE_PHN716_n4980*. Looking in the *NAME_MAP section of the *CORTEXM0DS_routed.spef* file, we see that the victim net *u_logic/n4980* is mapped to *6703, and the aggressor net *u_logic/FE_PHN716_n4980* is mapped to *1510. Looking for the victim net, we find the following connections to the aggressor net:

```
*D_NET *6703 0.0123425
. . .
24 *6703:11 *1510:8 0.00187151
25 *6703:10 *1510:9 0.00187151
```

Therefore, there is a total of 12.3 fF on the victim, 3.74 fF of which is connected to the aggressor (C_C), and 8.6 fF of which is connected to other nodes (C_W). If we assume that the victim and aggressor are both high initially, and that the aggressor is switching low, then by conservation of charge

$$C_W V_1 = (C_W + C_C)V_2$$

$$\frac{V_2}{V_1} = \frac{C_W}{(C_W + C_C)} = \frac{8.6}{12.3} = 0.697$$

Assuming a supply voltage of 1.1 V, this corresponds to a 334 mV below-high bump, which is a bit larger than the 223 mV below-high bump predicted by PrimeTime SI.

Note that if an "Above Low" bump is analyzed, the equation is slightly different. In this case, the charge on both C_C and C_W is initially zero, and the charge on C_C (referenced from the victim node) after the aggressor switches is $(V_2-V_{DD})C_C$.

$$0 = (V_2 - V_{DD})C_C + V_2 C_W$$

$$\frac{V_2}{V_{DD}} = \frac{C_C}{(C_W + C_C)}$$

Problem 2)

Global wires should be assumed, since this will give the minimum delay.

$$t_{p1} = 0.69(548)(0.61)(1 + 1.4) = 547\ fs$$

$$L_{crit} = \sqrt{\frac{547}{0.38(0.18)(3.0)}} = 51.5\ \mu m$$

$$t_{p,crit} = 2\left(1 + \sqrt{\frac{0.69}{0.38(1 + 1.4)}}\right)(395) = 2.05\ ps$$

$$t_{p(1cm)} = \frac{(10000\ \mu m)}{51.5\ \mu m}(2.05\ ps) = 397\ ps$$

Another way to calculate this value is to use the $t_{p,\min}$ equation

$$t_{p,\min(1cm)} = \left(1.38 + 1.02\sqrt{1 + 1.4}\right)(10000\ um) \times \sqrt{(548\ \Omega - \mu\mathrm{m})(0.61\ fF/\mu m)(0.18\ fF/\mu m)(3.0\ \Omega/\mu m)} = 397\ ps$$

Problem 3)

The simulated power values are given below.

Fibonacci Iterations	Switching Power (μW)	Internal Power (μW)	Leakage Power (μW)	Total Power (μW)
1	74.5	105	614	794
5	74.3	104	614	793
10	72.3	103	614	789