

Open-source standard cell and I/O cell design

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Abstract—Since the release of the open-source SkyWater Sky130 Process Design Kit (PDK) a large number of projects have impacted positively the democratization of semiconductor knowledge. However, within this immense volume of contributions, some design areas like physical digital and analog design have not been exploited due to the lack of information in their design methodologies driven by non-disclosure agreements (NDA). To overcome this difficulty, in this research project, we implement using the open-source Sky130 PDK, a fully open-source methodology that is applied to the design and characterization of 10 standard cells with a fixed 12-track height for high-speed applications. This methodology obtains the widths $W_N = 0.88[\mu\text{m}]$ and $W_P = 2.81[\mu\text{m}]$ as the optimal dimensions for a 12-track inverter cell to meet the specification of $t_r/t_f = 1$ under several process corners. Also, a fully open-source design and characterization methodology is presented for analog signal pad cells, filler cells, and cut-off cells in which dual diodes as ESD protection are considered. This characterization methodology involves the determination of the electromagnetic model of the signal pad cell as an RC circuit and considers the tradeoff between bandwidth, current density between metal layers, and area. The optimal design chosen for the pad cell corresponds to a cell with 12 diodes and "in" nodes with sizes of $6\mu\text{m} \times 7\mu\text{m}$.

Index Terms—Skywater130, Standard cell library, I/O ring

I. INTRODUCTION

Since July 2020, with the launch of the Open Source PDK [1] "Sky130" by Google/SkyWater, the number of projects and initiatives from academia, industry, and enthusiasts has expanded significantly.

This release has generated a positive impact globally on the democratization of semiconductor knowledge and its applications. It has allowed the training, development, and enhancement of academic programs in the field of integrated circuit design that could not have access to the design tools and Process Design Kits (PDK), due to their elevated prices or region restrictions.

Still a large number of contributions to the democratization of integrated circuit design, some design areas have often been left behind due to the reduced or lack of information in their respective design methodologies, mainly due to non-disclosure agreements (NDA). This is the case for the design of digital standard cells and I/O cell design.

Most of the existing works in the design of standard cells are based on closed PDKs, avoiding sharing the knowledge associated with the design methodology. Moreover, there are several open-source projects with designed standard cell libraries but most of them were based on non-manufacturable

PDKs like FreePDK45 [2] [3]. These PDKs have the limitation of not being associated with any real process, avoiding design testing in real-world applications.

In the same way, the field of I/O cells has information on the design, such as ESD-protected pads for K/Ka-band applications [4] and techniques for reducing capacitance in the signal pad [5]. Additionally, there is information related to characterization, such as power dissipation measurement in the signal pad [6]. Still, there is currently no clear and community-accessible methodology that covers the complete process of design and characterization of I/O cells.

To contribute solving the aforementioned challenges, in this research project, a fully open-source methodology with the Sky130 PDK is applied to the design and characterization of 10 standard cells with a fixed height of 12-tracks for high-speed applications. The design is based on the $t_r/t_f = 1$ specification, where (t_r) and (t_f) correspond to the rise and fall times of the output signal.

Continuing with the contributions, a fully open-source design and characterization methodology is presented for analog signal pad cells, filler cells, and cut-off cells. To obtain a more realistic behavior and performance, we included the ESD protection diodes. This characterization methodology involves the electromagnetic model of the signal pad cell considering the tradeoff between bandwidth, current density between the metal layers, and area.

This article is organized as follows. Section II presents an overview of the fundamental concepts about standard cells and I/O cells required to guarantee the correct comprehension of the following sections. Section III introduces the design methodology applied to design each set of cells, with emphasis on the mathematical procedures and simulations performed to meet the specifications. Section IV describes the different methods of characterization employed to measure the performance of the cells designed. Section V summarizes all the design parameters obtained considering the specification established with the design methodologies presented. Finally, section VI presents the main conclusions and contributions of this work.

II. KEY COMPONENTS OF A PROCESS DESIGN KIT

A Process Design Kit (PDK) is essentially a set of guidelines provided by a foundry company. Design teams must adhere to these guidelines to ensure that their design can be manufactured by the foundry company. This kit comprises a user manual, parametric cells, models, design rules, and layouts of active and passive elements. When used alongside compatible Electronic Design Automation (EDA) software, the PDK allows for seamless integration of the design process [7]. In the present work, standard cells and I/O cells are designed using the Sky130 PDK.

A. Standard Cells

Standard cells are the fundamental building blocks used in the design of digital integrated circuits. These blocks, such as inverters, NAND gates, NOR gates, and flip-flops, are grouped in a library accessed by the designer and can be combined and interconnected through a well-defined flow to implement these digital integrated circuits. This flow has made possible the design of most modern, complex processors used in end-user computing devices, servers, and embedded hardware.

In general terms, the design of a digital circuit is a sequential flow involving different steps, such as synthesis, floorplanning, placement, routing, verification, and testing [8]. The inputs of this flow are a digital design described in Register-Transfer-Level (RTL) in a Hardware Description Language (HDL) such as Verilog or VHDL and, a standard cell library. This library will be used by Electronic Design Automation (EDA) tools to implement the design. The output of the flow is the physical layout of the design, stored in Graphic Data System (GDS) format. Once this design is ready, it is sent to a foundry for its manufacturing.

A library of standard cells is provided by the PDK, where a set of files with data from each cell are used in each step of the flow. A Liberty™ (LIB) format file contains the logical function, timing, and power characteristics of the cell. The Library Exchange Format (LEF) describes the physical and geometrical characteristics of a cell, such as height, width, routing layers, and pin locations.

During synthesis, the EDA tool uses the data in the LIB file to select the cells that implement the logic description of the design. Then, the EDA tool estimates the timing and power performance of the resulting netlist. In the floorplanning, placement, and routing (PnR) stages, the tool uses the information provided by the LEF file to connect the cells and then implement the physical layout of the design. [9].

It is a requirement that the cells must have the same height over a fixed grid to facilitate the placement and routing of the design by the tool. This grid is composed of vertical and horizontal tracks made of the two lowest metals in the technology stack. For sky130 these are metal1 and metal2,

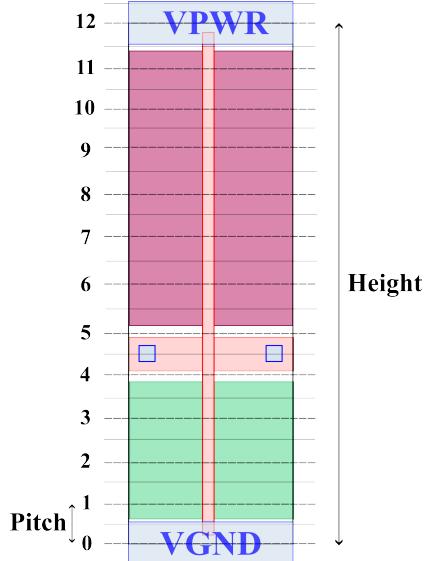


Fig. 1: An standard cell of 12-track height.

which will be used for the horizontal and vertical tracks, respectively. These lowest metal layers are equally separated by a length called pitch. The space between the metal layers depends on a set of rules provided by the foundry associated with the minimum resolution defined by the machines during the manufacturing process. In addition, the horizontal track is used as the reference unit to set the height of the standard cell, e.g. a 12-track height. The 12-track cell height is defined between the middle of the power rail (VPWR) and the middle of the ground rail (VGND) as depicted in Fig. 1 [8]. On the other hand, the cell width is an integer multiple of the pitch, and it is extended up to the multiple where the cell fits adequately. Moreover, the power and ground rails of the cell should be extended to the boundaries of the area set for the standard cell to guarantee continuity with the rails of adjacent cells as shown in Fig. 2.

Cell heights establish a trade-off between speed, power, and area. 11-12 tracks library cells are intended for high-speed applications, and support more complex routing and larger driving strength but exhibit a larger power consumption, especially when the transistors are off (also called leakage power). Libraries containing cells with 7-8 tracks are used for area efficiency and low-power applications. Finally, a height of 9-10 tracks provides a reasonable trade-off between area, efficiency, and performance. [10].

The driving strength of a cell has a directly proportional relationship with the ratio W/L . This ratio can be modified by increasing the height of the cell, however this is not an adequate solution for our design methodology. For cells with a constant height, this ratio can be increased by raising the number of transistors in parallel, such that the effective width W_{eff} is proportional to the number of transistors. For instance,

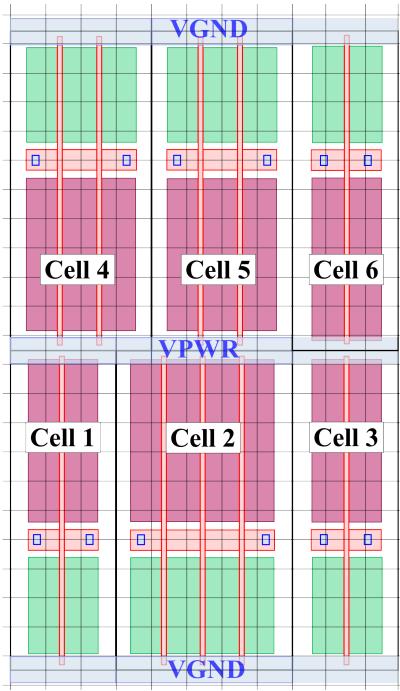


Fig. 2: Placement of 6 standard cells.

the fixed width W can be multiplied by a factor of 2 ($X2$), 3 ($X3$), or 4 ($X4$), when two transistors, three transistors, or four transistors are placed in parallel, respectively.

B. I/O cells

The I/O ring is responsible for providing and sensing analog and digital signals from external sources and the various power domains required by the IC core. It is connected to the external pins of the integrated circuit package through bond wires, as shown in Fig. 3. A bond wire is a fine wire for chip-to-printed circuit board (PCB) connections [11]. It is made of materials such as gold and aluminum. The I/O ring consists mainly of cells such as signal pad cells, power pad cells, filler cells, and cut-off cells. A simplified view of the I/O ring is presented in Fig. 4.

Follows a description of the main cells that compose the I/O ring.

1) Signal pad Cells: Signal pad cells are the fundamental building blocks of an I/O ring. Their purpose is to either receive signals off-chip or transmit signals from inside the die to the outside [8]. The pad cells are mainly composed of bonding pads, integrated power rails, and Electro Static Discharge (ESD) protection structures [12], as shown in Fig. 5.

Depending on the purpose given to the pad cell, several factors should be considered by designers:

- Nature of the signal (whether it is digital, known as GPIO cells, or analog, known as Analog Pad cells)

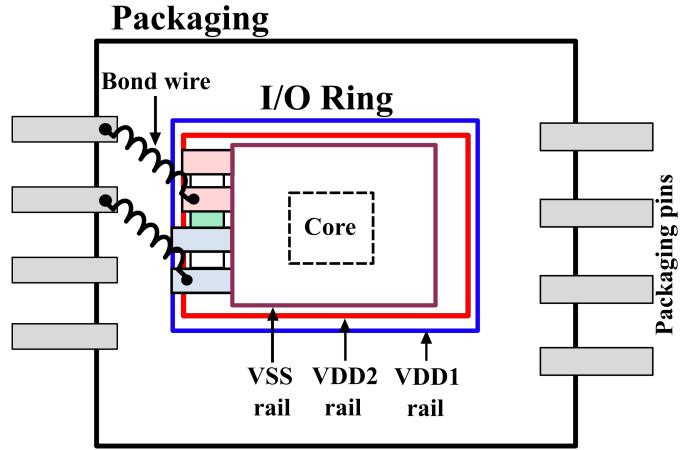


Fig. 3: General structure of an I/O ring.

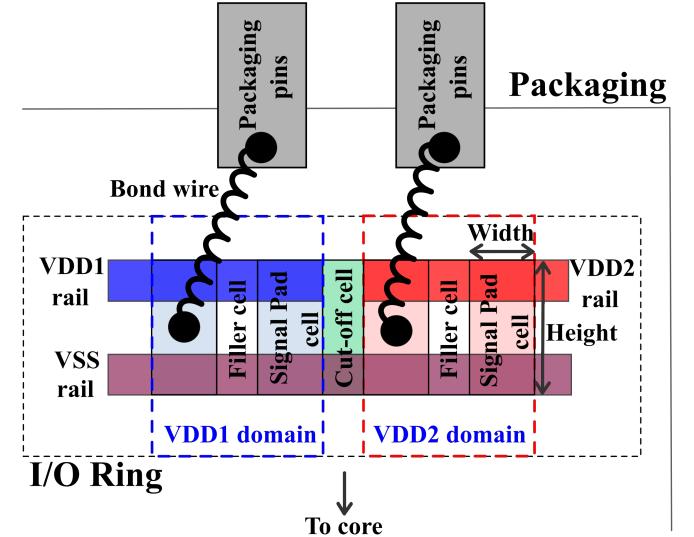


Fig. 4: Portion of an I/O ring and its connections to the packaging pins.

- Limiting factor (whether its core's area or number of pads)
- Number of power domains present in the I/O ring
- Size of the die
- Area of the I/O ring
- Instantiation or not of ESD protection structure

Once the die area is fixed and the core's area is the main limiting factor (Core Limited), the pad cell is designed with a large width and a height as small as possible. Conversely, when the main limiting factor is the number of pads on the die (Pad Limited), the pad cell is designed with a large height and a small width [13]. The sizes of the die and the area of the I/O ring are usually subject to the specifications provided by a foundry company. However, since the PDK used is sky130, this work considers the Caravel structure, which is provided by Efabless. Caravel is a standard System-on-Chip

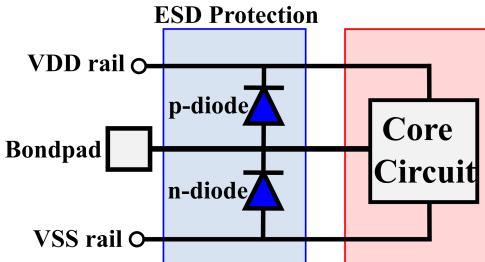


Fig. 5: Signal pad cell schematic.

(SoC) harness with on-chip resources to control and perform read/write operations from a user-dedicated space [14].

2) *Filler and Cut-off Cells*: Filler cells contain the power and ground rails, and they are positioned in the intermediate space between pad cells (Fig. 4) to maintain a continuous voltage domain through the entire I/O ring or a specific part of it [15]. Cut-off cells, on the other hand, are designed to separate adjacent and different power domains within an IC while maintaining continuity for the ground. They ensure multiple electrically isolated power domains within the die [16], as requested by the chip design. A conceptual view of the cut-off cell is depicted in Fig. 4.

III. DESIGN METHODOLOGY

A. Standard Cells

The design methodology is composed of four well-defined stages: The selection of the cell architecture, the selection of the specifications, the calculation of NMOS and PMOS widths W_N, W_P to satisfy the specifications, and the layout implementation.

1) *Cell Architecture*: The cell architecture consists of the height and driving strength selection. Since the Sky130 PDK does not integrate a 12-track standard cell library, we decided to use this height. A 12-track library allows the implementation of larger transistors than the 7- and 9-track libraries present in the PDK, aiming for high-speed applications. Also, a driving strength of x1 was selected.

To determine the height, it is required to set the spacing between tracks, which is named pitch and denoted as P_{m1} and P_{m2} in Fig. 6.

These lengths were obtained by following a design rule checking (DRC) process, which is the verification that the minimum distances set by the technology are respected during the layout implementation. These rules can be summarized as follows: The pitch between horizontal tracks (P_{m1}) is based on three dimensions: the minimum spacing between metal-1 layers (S_{m1}), the minimum metal-1 overlap of metal contacts (O_{m1}) and the minimum size of a metal contact (C_{mcon}) as shown in equation (1). Similarly, the pitch for vertical tracks (P_{m2}) is based on the minimum spacing between

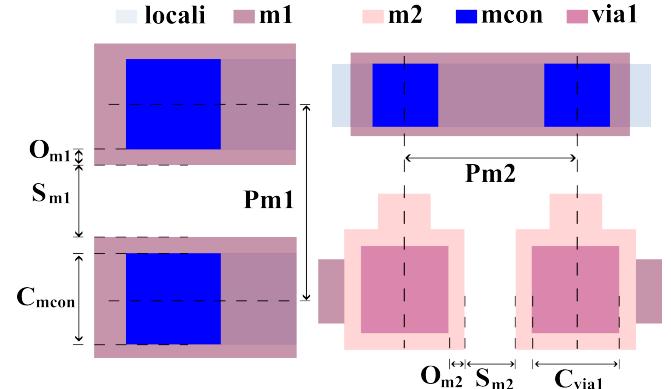


Fig. 6: Pitches P_{m1} and P_{m2} for Sky130.

metal-2 layers (S_{m2}), the minimum metal-2 overlap of via-1 (O_{m2}) and the minimum size of via-1 (C_{via1}), as indicated in equation (2).

$$P_{m1} = S_{m1} + 2 \left(O_{m1} + \frac{C_{mcon}}{2} \right) [\mu\text{m}] \quad (1)$$

$$P_{m2} = S_{m2} + 2 \left(O_{m2} + \frac{C_{via1}}{2} \right) [\mu\text{m}] \quad (2)$$

All these design rules values associated with the Sky130 PDK are summarized in table I.

TABLE I: Design rules for P_{m1} and P_{m2} calculations.

	S	O	C	P
m1	0.14	0.03	0.17	0.37
m2	0.14	0.03	0.26	0.46

In this work, we set $P_{m1} = 0.40[\mu\text{m}]$, as an adequate layout practice, to place at least two contacts in all NMOS diffusions. For P_{m2} , we maintain the same value of $0.46[\mu\text{m}]$ as indicated in Table I.

With P_{m1} determined, the height of the cell is calculated with equation (3). The value obtained is $4.8[\mu\text{m}]$.

$$H_{cell} = P_{m1} \times N_{tracks} \quad (3)$$

The next consideration for the cell architecture is the selection of the position of the poly-contacts in the middle of the cell. Regarding the position of the two contacts, there are two design options, vertically and horizontally as Fig 7a and Fig. 7b illustrate. To achieve a higher speed with larger transistors' width, we placed the contacts horizontally.

2) *Cell Specifications*: This work designs a library for standard cells that will be used for combinational logic circuits, thus we target $t_r/t_f = 1$ to have a symmetrical signal with equal rising and falling edges.

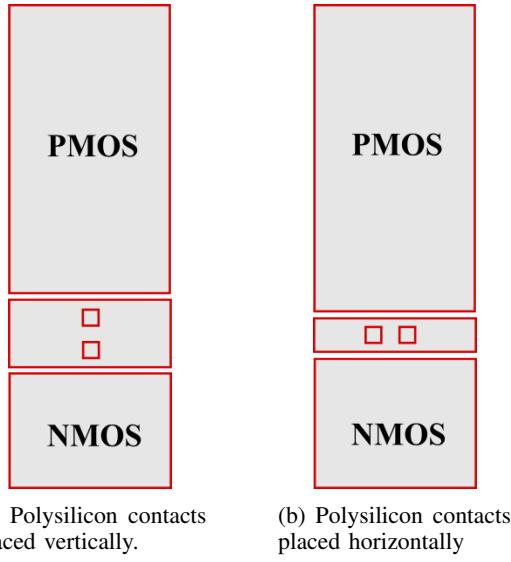


Fig. 7: Options to place polysilicon contacts

3) *Optimal Width Calculation:* The required W_N and W_P to meet the specifications are determined in a three-step procedure: a 12-track layout cell with only the two transistors is first drawn to determine the total space available for the transistor widths (W_T). Then this cell is redrawn to determine the minimum and maximum of both W_N and W_P and finally, a number of simulations are run to compute the width dimensions that meet the specifications.

The value of W_T was determined by drawing a cell consisting of a PMOS and an NMOS with both gates interconnected. This drawing was made by using a layout tool called Magic and its embedded DRC checker. Once we have placed both transistors, an expression for the total width, presented in equation (4), was defined. In this expression, the cell height (H) is subtracted from the DRC rules, as shown in Fig. 8, which are associated with the poly-to-poly spacing (PP), the transistor hanging gate (HG), the poly-to-diffusion spacing (PD), and the height of the polysilicon layer in the middle of the cell (PH). We obtained a W_T of $3.69[\mu\text{m}]$ as shown in (5):

$$W_T = H - 2 \left(\frac{PP}{2} + HG + PD \right) - PH \quad (4)$$

$$W_T = 4.8 - 2 \left(\frac{0.21}{2} + 0.13 + 0.185 \right) - 0.27 \quad (5)$$

To determine the possible minimum and maximum widths W_{Nmin} , W_{Nmax} , W_{Pmin} and W_{Pmax} for both transistors, the cell is redrawn as shown in Fig. 9. We find $W_{Nmin} = W_{Pmin} = W_{min} = 0.42[\mu\text{m}]$ and $W_{Nmax} = W_{Pmax} = W_{max} = 3.27[\mu\text{m}]$.

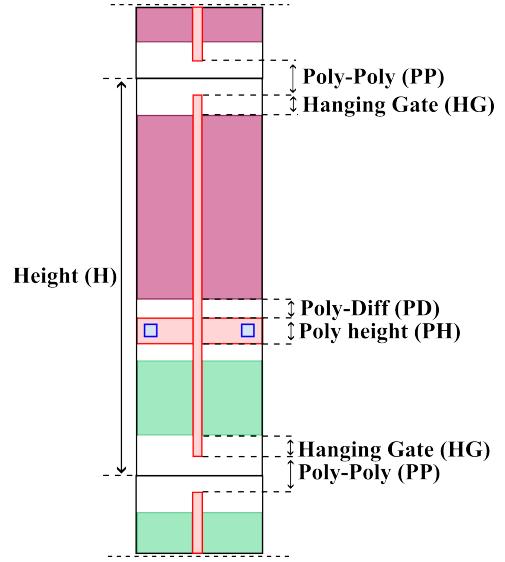


Fig. 8: Design rules for W_T calculation.

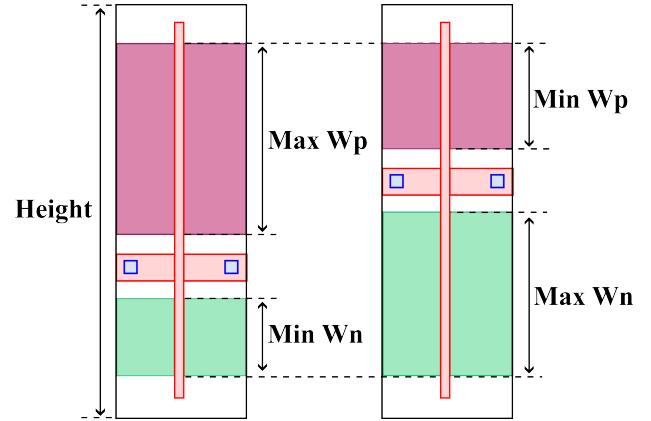


Fig. 9: Maximum and minimum NMOS and PMOS widths calculation.

Once, the range of possible values for W_P and W_N was identified, we determined the W_N and W_P for the specification $t_r/t_f = 1$. To achieve this specification, we implemented two test benches: An inverter chain in Fig. 10 and a fan-out 4 (Fo4) in Fig. 11 each one with a device under test (DUT) enclosed with a red square, which corresponds to the inverter.

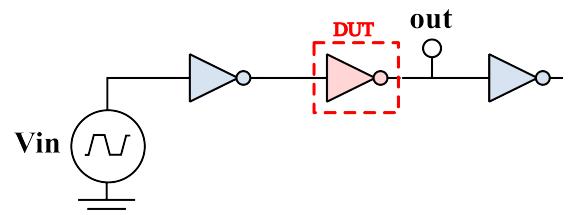


Fig. 10: Inverter chain testbench.

The inverter chain is a circuit that consists of three identical inverters in series, while the Fo4 circuit consists of an inverter

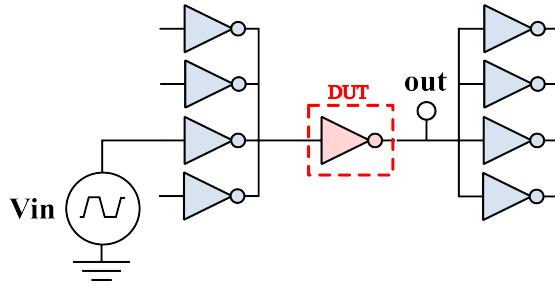


Fig. 11: Fo4 testbench.

with 4 identical inverters connected both at its input and output.

The inverter chain is used to determine the rising and falling times associated with a more realistic behavior. These times are measured at the output of the DUT and their average is calculated. This average is set as the slew rate τ_{in} or voltage ramp duration of the input voltage source (V_{in}) of the Fo4 test. Then, on the Fo4 test bench, we measure the rising and falling times at the output of the DUT. These timing measurements are processed by a Python algorithm to find the W_N and W_P at which $t_r/t_f = 1$.

The simulation data of the inverter chain was generated using a Python script. This script writes a Spice file with an inverter chain test for each corner process. The five process corners (T_C) in Sky130 PDK are summarized in Table II. These process corners describe variations in the MOSFET characteristics, due to fluctuations in the gate etch or doping manufacturing process. [17].

TABLE II: Process corners in Sky130 PDK.

Corner	NMOS	PMOS
TT	Typical	Typical
FF	Fast	Fast
SS	Slow	Slow
FS	Fast	Slow
SF	Slow	Fast

The script executes Ngspice in the backend to run the Spice files created. Each Spice file measures the rise time t_r and fall time t_f while sweeping transistor widths. W_N and W_P sweep from W_{min} to W_{max} with a step size (W_{step}) of 0.005 [μm]. W_{step} corresponds to the minimal drawing grid allowable by the Sky130 PDK.

A total number (T_W) of 570 simulations, as presented in equation (6), per corner were run to obtain the different W_N and W_P values:

$$T_W = \frac{W_{max} - W_{min}}{W_{step}} \quad (6)$$

$$T_W = \frac{3.27 - 0.42}{0.005} = 570 \quad (7)$$

Once Ngspice runs the Spice files, the exported data is processed by a Python algorithm that computes the average values of the rising and falling times using the equation (8).

$$\tau_{in} = \frac{\sum_j^{T_W} \sum_i^{T_C} (t_{ri,j} + t_{fi,j})}{2T_W T_C} \quad (8)$$

The simulation data of the Fo4 is generated with a similar Python script as the inverter chain. This script writes a Spice file with a Fo4 test for each corner. The script executes Ngspice to run the different files to compute t_r and t_f while sweeping W_N and W_P .

The script processes the exported data in two stages: In the first one, it averages the t_r and t_f measured for each couple (W_N, W_P) as equations(9 and 10) indicate:

$$\bar{t}_r = \frac{\sum_i^{T_C} t_{ri}}{T_C} \quad (9)$$

$$\bar{t}_f = \frac{\sum_i^{T_C} t_{fi}}{T_C} \quad (10)$$

In the second stage, the script plots the curves \bar{t}_r vs W_N and \bar{t}_f vs W_N in the same graph and determines the intersection of both curves. This intersection corresponds to the value where the specification $t_r/t_f = 1$ is met.

4) *Layout Implementation:* The layout cells were drawn by using the minimum grid size allowable by the PDK, which is 0.005 [μm]. A template was implemented and used as Fig.12 depicts to guarantee the 12-track height of the cell.

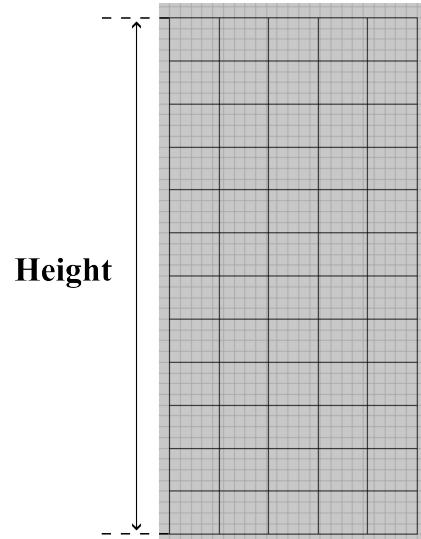


Fig. 12: A 12-track template.

The following considerations were defined during the implementation of the layout cells:

- Placing at least two contacts per layer in case a contact is lost during chip fabrication.
- Reduce metal interconnects as much as possible to avoid capacitances.
- Maintain symmetry with the different layers.

- Expand the (*locali*) layer to cover at least two tracks associated with the grid, to help the PnR tool placing contacts between metal1 and locali (*mcon*).
- Implement one bulk tap for substrate diffusions per cell to reduce area.

B. Signal Pad Cell

To implement the pad cell design suitable for the Caravel SoC, and prioritize the number of pads over the core's active area, a decision was made regarding the size of the pad cell. The dimensions were determined to be $75\mu\text{m} \times 200\mu\text{m}$. Furthermore, the overall architecture of the pad cell is planned to contain only one bias voltage and ground rails. Therefore, the design consists of a single VDD and VSS rail. Finally, a specific pad architecture will be used, including diodes for the purpose of ESD protection, as depicted in Fig. 5.

The design of the pad cell in this project involves constructing layouts from the bottommost layer to the topmost layer. Thus, the layouts are held from the Backend layer to the Metal 5 layer, as defined by the sky130 technology. The design process follows a general flow, which can be summarized as follows:

- 1) Define the layer breakdown for the pad cell
- 2) Set spacing rules based on DRC
- 3) Set specifications for multiple Signal pad cell creation

Follows a Signal pad cell description in the different layers that compose the Sky130 structure.

1) *Backend layers*: In this layer, the ESD protection diodes are located. This structure includes both n-diodes and p-diodes, as illustrated in Fig. 13(a). The n-diodes are connected between the input node (cathode) and VSS (anode), while the p-diodes are connected between the input node (anode) and VDD (cathode). As both the cathode of the n-diodes and the anode of the p-diodes share the same node (bondpad node), any node representing either of these two terminals will be defined as an “in” node in the upper metal layers. Since an “in” node represents a diode terminal, we can set the following expression:

$$\#InNodes = \#Diodes$$

2) *Local Interconnect layer*: In this particular layer, all the cathodes of p-diodes are interconnected to create a single VDD node, as shown in Fig. 13(b). This interconnecting process is not required for n-diodes because their anodes are already interconnected in the substrate. Within this layer, there are three key components: the VDD node, the VSS node, and the “in” nodes.

3) *Metal1 layer*: From this layer emerges a node called the “out” node. This “out” node is where the pad cell input and the pad cell output are interconnected. Therefore all the “in” nodes are connected with the “out” node (see Fig. 13(c)).

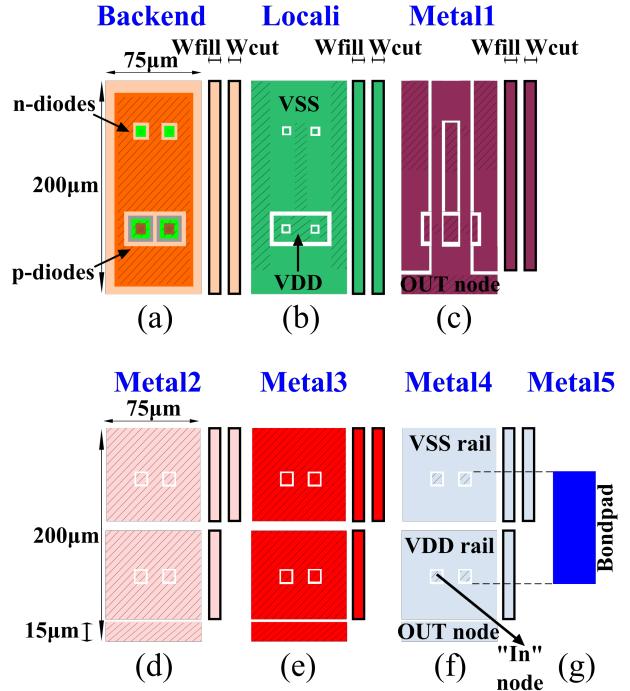


Fig. 13: Signal pad, Filler, and Cut-off cell layer breakdown. The dashed area corresponds to an area with intermediate vias. The figure is not on the scale.

The VDD and VSS nodes occupy the remaining available area and maintain the same topology as they do in the Local Interconnect layer.

4) *Metal 2 to Metal 4 layers*: The “out” node and the VDD and VSS rails are implemented in this stack of layers, and each “in” node is also created separately. This is done to maximize the area for the power rails.

5) *Metal 5 layer*: This layer contains only the bondpad, which is where the “in” nodes are again interconnected into a single node, as shown in Fig. 13(g).

Follows the spacing rules established in order to prioritize the area in the VDD and VSS rails, which are displayed in Fig. 15.

- $1\mu\text{m}$ between metal edges
- $2\mu\text{m}$ between rails
- $2\mu\text{m}$ between p-type diffusion and cell edge
- $1\mu\text{m}$ between p-type diffusion and nwell
- $1\mu\text{m}$ between n-type diffusion and nwell

After defining the structure of each layer and establishing the spacing rules for the pad cell, it is possible to create a layout cell that has a specific number of “in” nodes with a particular size. To establish a clear criterion for proposing a design and studying the bandwidth, the maximum current and area of the pad cell as a function of the size and number of

“in” nodes, this project presents 12 different pad cell designs, varying the amount of “in” nodes and the “in” node sizes.

The starting point for creating these cells is to define the size of the “out” node. In this case, a $75\mu m \times 15\mu m$ “out” node has been chosen, which takes up 7.5% of the pad cell area. This is done to prioritize the VDD and VSS rings. To ensure that the current is limited by the “in” nodes rather than the “out” node, and taking into account that a maximum of 12 diodes will be used, the “out” node area is divided into 12 equal parts. This division determines the maximum allowable size for the “in” node.

$$Area_{Out_Node} \geq \sum_{i=1}^{12} Area_{In_Node_i}$$

$$Area_{Out_Node} \geq 12 \cdot Area_{In_Node}$$

$$\Rightarrow Area_{MaxIn_Node} \leq \frac{Area_{Out}}{12} \leq 93\mu m^2 \quad (11)$$

To ensure that the distance between the “in” nodes is the same as the distance between the “in” nodes and the rail border, the “in” node length is set to $10\mu m$. The width is determined using the following expression:

$$W_{In_Node} = \lfloor \frac{Area_{MaxIn_Node}}{L_{In_Node}} \rfloor = 9\mu m$$

In this project, three sets of designs with different sizes for the “in” node were established. Also, each design in a specific set has a different amount of “in” nodes. The “in” node size of the first set has already been calculated, and the “in” node sizes for the remaining two design sets are obtained by multiplying the maximum size by 1/3 and 2/3.

To ensure that all designs shared the same current through the diodes, the size of the “in” nodes for local interconnect and the size of the contacts were kept the same for all the designs, using the minimum calculated size. The specifications for the 12 designs are presented in Table III, and Fig. 14 depicts the corresponding layout views.

TABLE III: Signal Pad cell designs

“In” size / #“In” nodes	2	4	6	12
$3\mu m \times 4\mu m$	Design1	Design2	Design3	Design4
$6\mu m \times 7\mu m$	Design5	Design6	Design7	Design8
$9\mu m \times 10\mu m$	Design9	Design10	Design11	Design12

C. Filler and Cut-off cells

As mentioned in the previous section, the filler cells and cut-off cells are responsible for maintaining the voltage domain continuity and cutting the voltage domain, respectively. After defining the architecture of the pad cells, the structure of the filler and cut-off cells is also defined to ensure the continuity of both the substrate and power rails, as shown in Figure 13. While moving up the layers from Backend to Metal4, it’s noticed that the VSS node gets smaller. This occurs since

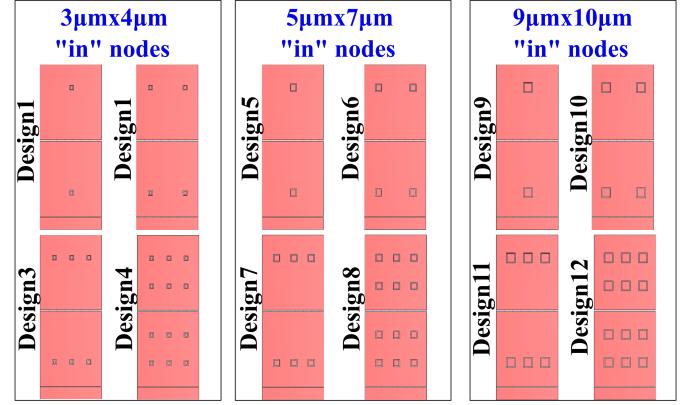


Fig. 14: Metal3 layout view for the 12 Signal pad designs.

it follows the same pattern as the Signal pad in terms of VSS area. To offer designers greater flexibility regarding the distance between pad cells, this work presents filler and cut-off cells with widths of $1\mu m$, $5\mu m$, $10\mu m$, and $20\mu m$.

IV. CHARACTERIZATION

A. Standard Cell Characterization

Cell characterization consists of providing information about the cell logic function, timing, and power performance, in a file format named Liberty™ (LIB) that will be used by the EDA tools during the physical design flow. This section targets the identification of the cell logical function and its timing characterization.

The output time measurements delivered to the designer are the rise time (t_r), fall time (t_f) and the propagation delays (t_{phl}, t_{plh}) for each cell [18]. These characterization times are calculated under specific operating conditions: the input voltage ramp duration or slew rate (τ_{in}) and the output load capacitance (C_L) [19].

The timing measurements at the outputs t_r, t_f, t_{phl} and t_{plh} are performed with respect to each input port of the cell. For each case, the pin to characterize is stimulated with a pulse signal while the remaining ports are driven with a well-defined combination of logic values such that the output Y becomes a function only of the pin to be characterized, as shown in Fig. 16. We observe in Fig. 16 that during the characterization of the performance of the pin A1, the other pins (A2, B1, and B2) of the cell AOI22 are set to a fixed value, set by the designer.

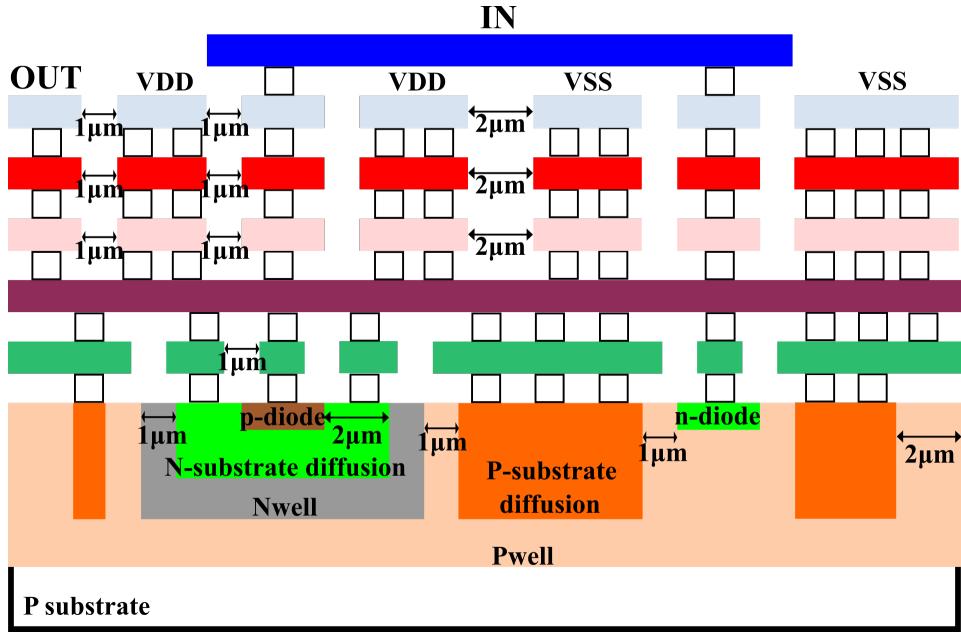


Fig. 15: Signal pad cross-section view with spacing rules. The figure is not on the scale.

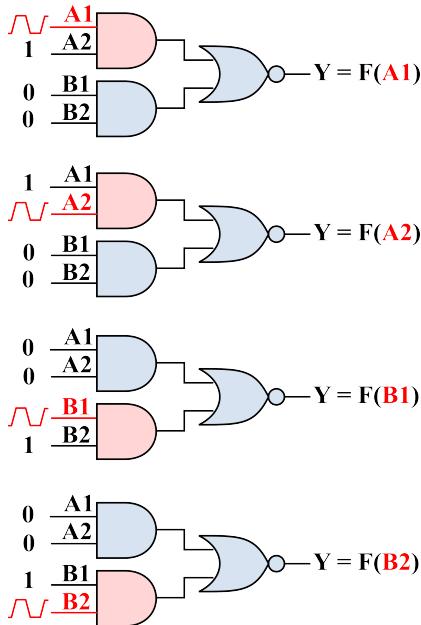


Fig. 16: Characterization process of cell AOI22.

Each timing parameter, $t_r, t_f, t_{phl}, t_{plh}$ is computed for each couple of values (τ_{in}, C_L). We define a list of slew rates [0.1n, 0.2n, 0.4n, 0.8n, 1.6n, 3.2n] and a list of output-loads [0.05p, 0.1p, 0.2p, 0.4p, 0.8p, 1.6p] for characterization. Then, we run the simulations associated with the values mentioned above to build the four tables, for t_r, t_f, t_{phl} , and t_{plh} . These tables are presented in the LIB format as illustrated in Code 1 for t_r , where $index_1$ and $index_2$ represent the load capacitance values and the slew rates, respectively. Table IV presents the LIB Code 1 in a tabular format to illustrate the

relation between indexes and values.

```
index_1("0.05, 0.1, 0.2, 0.4, 0.8, 1.6");
index_2("0.1, 0.2, 0.4, 0.8, 1.6, 3.2");
values("tr11, tr12, tr13, tr14, tr15, tr16",
      "tr21, tr22, tr23, tr24, tr25, tr26",
      "tr31, tr32, tr33, tr34, tr35, tr36",
      "tr41, tr42, tr43, tr44, tr45, tr46",
      "tr51, tr52, tr53, tr54, tr55, tr56",
      "tr41, tr42, tr43, tr44, tr45, tr46");
```

Code 1: Example output timing table for t_r in LIB format.

TABLE IV: Output timing table example for t_r .

	C_L					
τ_{in}	0.05p	0.1p	0.2p	0.4p	0.8p	1.6p
0.1n	tr11	tr12	tr13	tr14	tr15	tr16
0.2n	tr21	tr22	tr23	tr24	tr25	tr26
0.4n	tr31	tr32	tr33	tr34	tr35	tr36
0.8n	tr31	tr32	tr33	tr34	tr45	tr46
1.6n	tr31	tr32	tr33	tr34	tr55	tr56
3.2n	tr31	tr32	tr33	tr34	tr65	tr66

The characterization process was performed by using a Python script. This script named `dscc.py` which stands for *Digital Standard Cell Characterizer*, takes the cell layout file, a list of C_L values in picofarads [pF] and a list of τ_{in} in nanoseconds [ns] as shown in Code 2. Furthermore, it is possible to specify the installation path of sky130 PDK if it differs from the standard library path `/usr/local/`.

```
python3 dscc.py cell.mag \
--output-loads="0.05, 0.1, 0.2, 0.4, 0.8, 1.6" \
--slew-rates="0.1, 0.2, 0.4, 0.8, 1.6, 3.2" \
--pdk-root=/home/user/cad \
```

Code 2: Usage of characterization tool.

This script extracts the Spice model from the layout cell and an algorithm identifies the logic function from the netlist and creates a Spice file per input pin. Then it runs each file using Ngspice, which is the simulation engine, in the backend to generate the output timing data.

Each Spice file has a control section divided into two code blocks: the first code declares a truth table for setting the fixed values of the remaining pins and also defines a pulse voltage source to stimulate the pin to characterize. This section iterates until a combination of the truth table defines the output Y a function of the pin to characterize. The second code executes the simulation with the τ_{in} and C_L values specified for measuring the t_r , t_f , t_{phl} and t_{plh} .

Once the simulation ends, Ngspice exports the timing data in .raw format files, which are read and formatted by another algorithm to generate the LIB file of the characterized cell.

B. Signal pad cell Characterization

This section covers the signal pad characterization considering four design aspects: bandwidth, electromagnetic model, the maximum current density through each metal layer, and the maximum number of pads in the I/O ring.

Due to the nature of the signal pad as an interconnecting cell between an off-chip low or high-frequency signal source, and the input of the core circuit, this project models the signal pad as a transmission line. To assess the signal pad's performance when maximum power transfer is required, the project uses the standard testbench for high-frequencies that sets both the generator circuit resistance and load resistance at 50 Ohms [6]. Furthermore, considering the typical capacitance of an oscilloscope probe tip, a 20pF capacitor is added at the output of the signal pad, as Fig. 17 depicts.

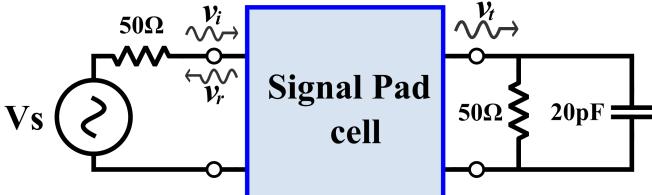


Fig. 17: Signal pad cell testbench with both 50 Ohms resistances at the input and output to guarantee maximum power transfer.

To determine the signal pad bandwidth, it is necessary to obtain its frequency response, which can be obtained from the scattering parameters. These scattering parameters (S -parameters) are widely used in high-frequency circuits to describe the characteristics of a two-port circuit. They represent how the power wave components are transmitted and reflected from the input and output ports of a circuit [20]. The frequency response is represented by the forward gain parameter (S_{21}). Additionally, when considering the reflection coefficient (S_{11}),

it is possible to calculate aspects such as the power dissipation loss at the pad [6]. These parameters are defined as:

$$S_{21} = \frac{v_t}{v_i} \quad S_{11} = \frac{v_r}{v_i} \quad (12)$$

The frequency response (S_{21} parameter) was obtained from two distinct software packages: CST Studio Suite and Ngspice. Both software packages consider the metal layers of Sky130, whose conductivities can be calculated based on the resistance per square and the depth of each layer in the Process Stack Diagram [21], using the following expression:

$$\text{Conductivity} = \frac{1}{\text{Resistance} \cdot \text{Depth}} [\text{S/m}]$$

The conductivity values for each of the layers of the sky130 technology are shown in Table V. Additionally, the following considerations were made particularly for each software:

- In CST, the Signal pad cell only contains the metal layers. This is due to the lack of access to the electrical parameters of the diode materials.
- The circuit simulated in Ngspice and depicted in Fig. 17 has an error since it assumes a short circuit between the input and output nodes. This is because there is no element between them. This error suppresses parasitic elements and makes it impossible to characterize the pad cell. To solve this problem, an additional zero Ohm resistance is added at the input of the pad cell. This resistance is included as a "testbench layout" of the cell and has dimensions of $2\mu\text{m} \times 1\text{cm}$ to ensure that its resistance is as near to zero as possible.

TABLE V: Conductivities for Sky130 metal layers

	Resistance [mΩ/sq]	Depth [μm]	Conductivity [S/m]
Locali	12800	0.1	$7.81 \cdot 10^5$
Metal1	125	0.36	$2.22 \cdot 10^7$
Metal2	125	0.36	$2.22 \cdot 10^7$
Metal3	47	0.845	$2.52 \cdot 10^7$
Metal4	47	0.845	$2.52 \cdot 10^7$
Metal5	29	1.26	$2.74 \cdot 10^7$
MCON	152000	0.44	$1.50 \cdot 10^4$
VIA	4500	0.27	$8.23 \cdot 10^5$
VIA2	3410	0.42	$6.98 \cdot 10^5$
VIA3	3410	0.39	$7.52 \cdot 10^5$
VIA4	380	0.505	$5.21 \cdot 10^6$

In this project, the signal pad is modeled as an RC circuit. The resistance refers to the one between the input and output of the signal pad. The capacitance is approximated using the parallel-plate method [6], where the overall capacitance is located between the output and the ground. The representation of the RC model is illustrated in Fig. 18.

Follows the step-by-step process for obtaining the R, C, and bandwidth of the signal pad.

- 1) The equation (12) is used along with the electromagnetic model shown in Fig. 18 and the testbench illustrated in

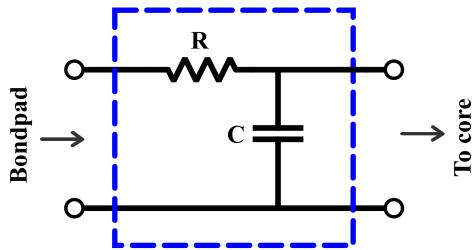


Fig. 18: Signal pad cell electromagnetic model

Fig. 17 to calculate the resistance of the RC electromagnetic model.

$$S_{21}(0 \text{ Hz}) = \frac{50}{R + 50}$$

$$\Rightarrow R = \frac{50}{S_{21}(0 \text{ Hz})} - 50 \quad [\Omega] \quad (13)$$

- 2) Based on the response's cut-off frequency and equation (13), the capacitance can be calculated as follows:

$$f_{c1} = \frac{1}{(R \parallel 50)(C + 20 \cdot 10^{-12})}$$

$$\Rightarrow C = \frac{R + 50}{50R \cdot f_{c1}} - 20 \cdot 10^{-12} \quad [F] \quad (14)$$

- 3) Finally, considering the equivalent capacitance of an oscilloscope probe tip equal to 20pF, the signal pad bandwidth is calculated with the following expression:

$$BW = \frac{1}{R(C + 20 \cdot 10^{-12})} \quad [\text{Hz}] \quad (15)$$

Once we determine the expression for the signal pad bandwidth, we continue with the next design parameter, which is the maximum current that the signal pad can withstand.

The maximum current of a signal pad cell is a crucial parameter in terms of its characterization. This parameter depends on variables such as the current threshold before metal electromigration [18], the number of metal5 to metal4 vias, and their respective sizes.

$$I_{max} = \#Vias_{M5M4} \cdot W_{via} \cdot J_{max} \quad [A]$$

Since there was a lack of access to the information regarding the current threshold for electromigration, it was decided to present the maximum current of a signal pad cell as a function of the number of vias between metal5 and metal4.

Finally, the last design parameter is the quantity that can fit within an I/O ring. For this study, this characterization will be carried out taking into account the Caravel SoC platform. To start the process of getting this parameter, we must define several statements. Let's suppose the area of an IO ring as depicted by Fig. 19:

$$IO_Ring_{Total_Area} = L_{die} \cdot W_{die} \quad (16)$$

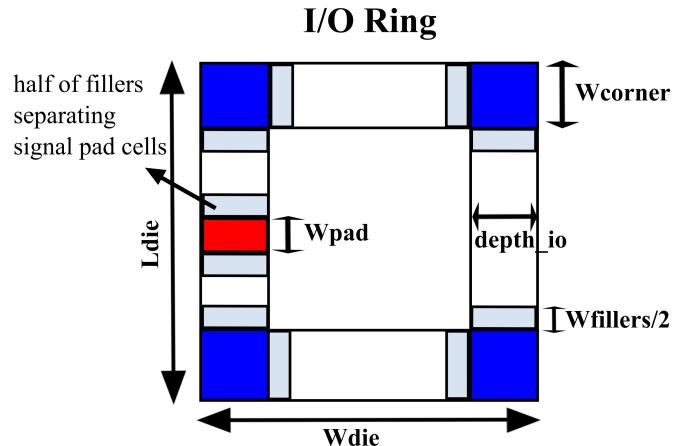


Fig. 19: I/O ring simplified view

Now, let us consider the area of half of the fillers that separate one signal pad cell from another. By positioning this area at the edge of each corner cell or signal pad cell (see Fig. 19), the area occupied by the corner cells and the area occupied by a signal pad cell can be defined as follows:

$$CornerArea = 4depth_{io} \cdot (depth_{io} + W_{fillers}) \quad (17)$$

$$SignalPadArea = depth_{io} \cdot (W_{pad} + W_{fillers}) \quad (18)$$

By using equations 16, 17, and 18, it is possible to determine the number of pads in the I/O ring as follows:

$$\#Pads = \lfloor \frac{IO_Ring_{Total_Area} - CornerArea}{SignalPadArea} \rfloor$$

$$\#Pads = \lfloor \frac{2}{W_{pad} + W_{filler}} (W_{die} + L_{die} - 4depth_{io} - 2W_{filler}) \rfloor \quad (19)$$

V. RESULTS

A. Standard Cells

The W_N and W_P obtained with the Fo4 testbench were $0.88[\mu\text{m}]$ and $2.81[\mu\text{m}]$ respectively. These values were computed as the intersect of the curves $\overline{t_r}$ vs W_N and $\overline{t_f}$ vs W_N as shown in Fig. X. As reported before, the specification was defined as $\overline{t_r}/\overline{t_f} = 1$

To test the cell design with the widths obtained, an inverter shown in Fig. 21 was implemented using these dimensions and tested in a Fo4 testbench for different process corners. During the corner simulations t_r , t_f and their absolute difference $|t_r - t_f|$ were measured and obtained as presented in Table VI

TABLE VI: t_r , t_f and absolute difference $|t_r - t_f|$ for each process corner using the obtained W_N and W_P .

Corner	$t_r[\text{ps}]$	$t_f[\text{ps}]$	$ t_r - t_f [\text{ps}]$
TT	124.1033	119.9666	4.136700
FF	96.91158	97.44748	0.535900
SS	168.8683	154.2748	14.59350
FS	107.6150	124.7381	17.12310
SF	160.9117	123.0885	37.82320

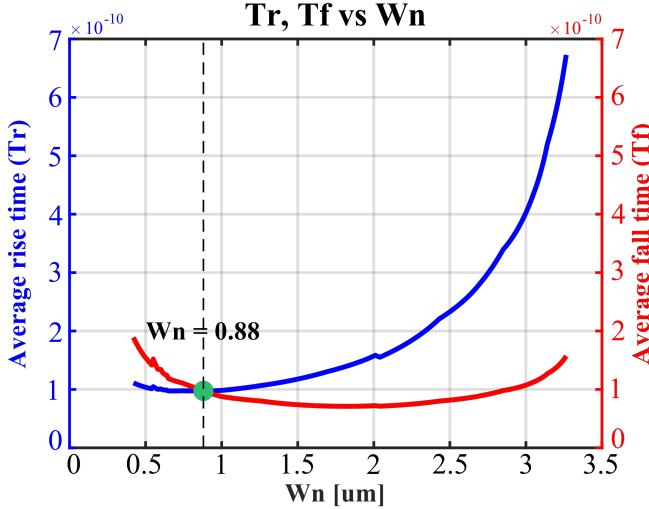


Fig. 20: Intersect at which $\overline{t_r}/\overline{t_f} = 1$

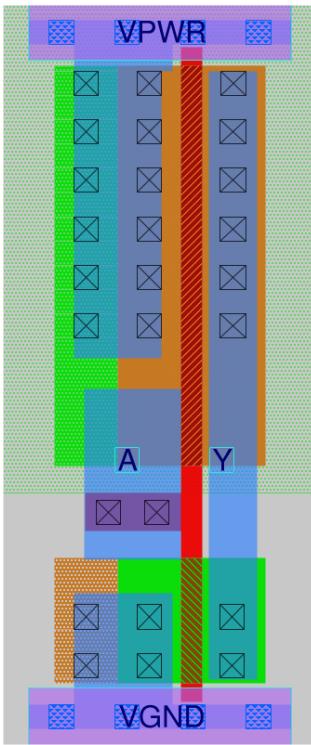


Fig. 21: 12-track inverter cell layout design with Magic.

The largest difference among the obtained results is 37.8232[ps], which is an acceptable value according to the technology used. To implement the standard cell library, ten cells were designed using the reference values for W_N and W_P obtained during the inverter design phase. The standard cells designed and characterized were *INV*, *BUFF*, *NAND2*, *NOR2*, *AOI21*, *OAI21*, *AOI22*, *OAI22*, *AOI211*, and *OAI211*. Table VII presents the layout area and the logic function associated with each cell.

TABLE VII: Area and boolean function of cells.

Cell	Area	Function
INV	8.83	$!A$
BUFF	11.04	A
NAND2	11.04	$!(A_1 \& B_1)$
NOR2	11.04	$!(A_1 B_1)$
AOI21	15.46	$!((A_1 \& A_2) B_1)$
OAI21	15.46	$!((A_1 A_2) \& B_1)$
AOI22	19.87	$!((A_1 \& A_2) (B_1 \& B_2))$
OAI22	19.87	$!((A_1 A_2) \& (B_1 B_2))$
AOI211	19.87	$!((A_1 \& A_2) B_1 C_1)$
OAI211	19.87	$!((A_1 A_2) \& B_1 C_1)$

The main properties used during the design phase of the different cells are described in Table VIII. In this table, we observe the values associated with the pitch, the height of the cell, the driving strength, the operating voltage (VPWR), the width of NMOS and PMOS devices, the models used from the Sky130 PDK and the operating conditions τ_{in} and C_L for characterization.

TABLE VIII: Standard cell library properties.

Property	Value
P_{m1}	0.40[um]
P_{m2}	0.46[um]
Y-Grid	12-Tracks
Height	4.80[um]
Driving Strength	X1
VPWR	1.8[v]
W_N	0.88[um]
W_P	2.81[um]
NMOS device used	sky130_fd_pr_nfet_01v8
PMOS device used	sky130_fd_pr_pfet_01v8
τ_{in}	0.1n, 0.2n, 0.4n, 0.8n, 1.6n, 3.2n
C_L	0.05p, 0.1p, 0.2p, 0.4p, 0.8p, 1.6p

For each one of the standard cells designed, the library contains five files that would be used by future designers:

- The physical implementation or layout (.mag).
- The abstract view with information associated with the geometry, the contact pins, and the metal layers (.lef).
- The model with parasitic resistances and capacitances (.spice).
- The logic function and timing characterization (.lib).
- The timing data is presented in a tabular format for postprocessing (.txt).

B. Signal pad cell results

Follows a description of the results obtained in CST and Ngspice regarding the bandwidth. Table IX and Table X display the results of the extraction process explained by equations 13, 14, and 15 for simulations run in CST and Ngspice.

Two main differences are observed between both tables:

- The resistance values obtained from Ngspice and CST differ significantly. This is because the cell designed in CST has fewer vias compared to the original design used in Ngspice. The reason to use fewer vias is to avoid long

TABLE IX: Results in CST

Design	R [Ω]	C [nF]	BW [MHz]	Vias M5-M4
Design1	1.462	2.491	272.477	8
Design2	1.203	3.146	262.451	16
Design3	1.358	2.817	259.678	24
Design4	1.248	3.029	262.660	48
Design5	1.064	3.423	273.056	32
Design6	1.270	3.031	258.088	64
Design7	1.224	3.181	255.211	96
Design8	1.356	2.839	257.857	192
Design9	0.944	3.884	271.368	60
Design10	1.335	2.931	253.933	120
Design11	1.381	2.879	249.679	180
Design12	1.377	2.831	254.647	360

TABLE X: Results in Ngspice

Design	R [mΩ]	C [nF]	BW [MHz]	Vias M5-M4
Design1	149.952	26.17	254.668	8
Design2	152.538	27.43	238.867	16
Design3	155.171	27.36	235.364	24
Design4	162.981	26.04	235.420	48
Design5	155.576	25.64	250.471	32
Design6	164.750	26.11	232.331	64
Design7	174.593	25.28	226.371	96
Design8	204.477	21.67	225.431	192
Design9	164.757	24.62	246.293	60
Design10	185.567	23.83	225.942	120
Design11	205.518	22.32	217.806	180
Design12	269.435	17.18	215.769	360

simulation times. More vias result in lower resistance, which clarifies the disparity between the two simulations.

- The capacitance obtained by Ngspice is significantly greater than the one obtained by CST. This can be attributed to the fact that the cell modeled in CST does not include the diodes, which contribute significantly to its parasitic capacitances in the bandwidth. The absence of these capacitances decreases the overall capacitance value, which accounts for the discrepancy between the two results.

The information contained in the tables IX and X can be visualized in Fig. 22 and Fig. 23 since we plot the bandwidth against the number of M5-M4 vias for both CST and Ngspice simulations.

The approximations made in CST have shown a significant impact on the resistance and capacitance of the electromagnetic model, which translates into significative errors for the signal pad cell bandwidth. Therefore, the conclusive results obtained by Ngspice were chosen (Table X). However, the results obtained by both CST and Ngspice were considered for selecting the optimal design.

During the selection of the optimal design, the designs with 4 and 6 diodes were the first to be discarded. This was because the designs with 12 diodes outperformed the aforementioned designs in terms of bandwidth and maximum current. Designs with 2 diodes may be attractive due to their high bandwidth, but their negligible maximum current made the set of designs with 12 diodes the optimal choice.

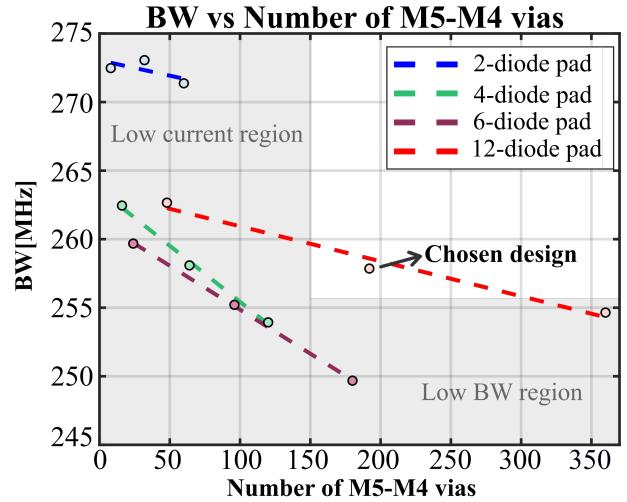


Fig. 22: Bandwidth vs Imax represented as M5-M4 vias. Obtained using CST Studio Suite.

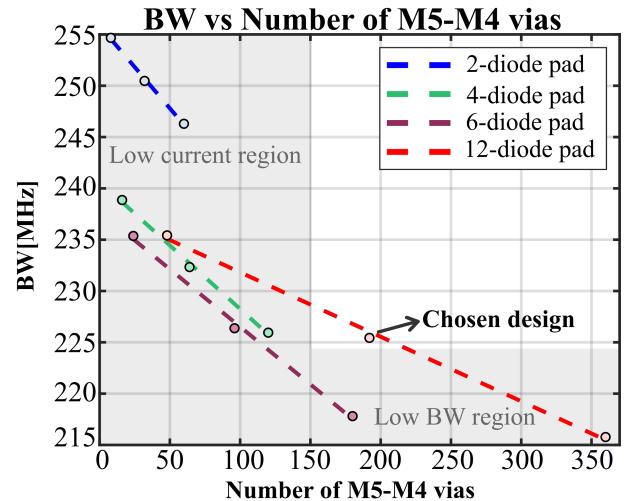


Fig. 23: Bandwidth vs Imax represented as M5-M4 vias. Obtained using Ngspice.

Finally, to provide a design that falls within the middle range of bandwidth, the design with 12 diodes and "in" node sizes of $6\mu\text{m} \times 7\mu\text{m}$ was chosen. Using Equation 19 and considering the chosen design, up to 57 pad cells can fit in the Caravel SoC. The generalized curve for any signal pad cell area is presented in Fig. 24. The specifications for the chosen design are shown in Table XI.

TABLE XI: SigPad_6x7_12di specifications

R [mΩ]	C [nF]	BW [MHz]	#M5-M4 vias	#Pads in Caravel
204.47	21.67	225.43	192	57

When designing a signal pad cell from scratch, it is useful to have a curve that relates the maximum current of the signal pad cell with its area. Therefore, and limited to only cells

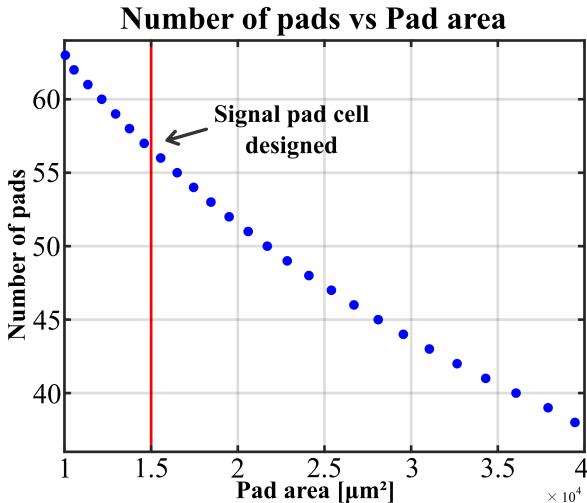


Fig. 24: Number of pads that can fit into Caravel SoC as a function of the pad area.

that are scaled designs from any of the 12 designs already proposed, the maximum current is proposed as:

$$\#Vias = Pad_area \frac{\#Vias_{scaled_design}}{A_{scaled_design}}$$

The relation described above is displayed in Fig. 25 and Fig. 26.

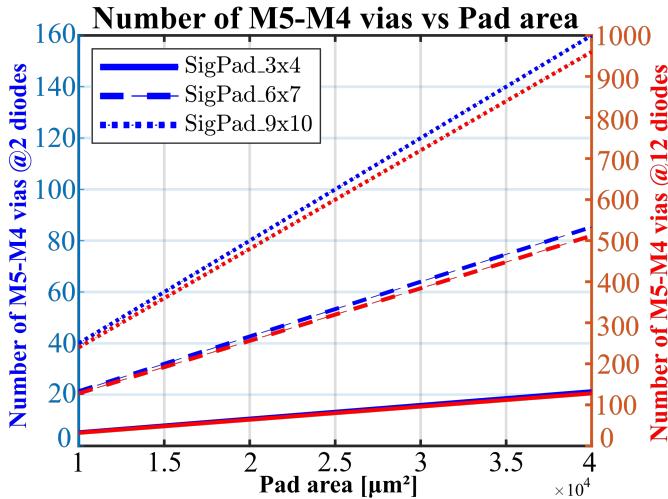


Fig. 25: Number M5-M4 vias vs pad area for a signal pad cell based on one of the 12 designs.

VI. CONCLUSIONS

In this project, a design and characterization methodology for a standard cell library and a set of I/O cells implemented in the sky130 PDK was presented.

The standard cell design methodology determined the widths $W_N = 0.88[\mu\text{m}]$ and $W_P = 2.81[\mu\text{m}]$ as the optimal dimensions for a 12-track inverter cell to meet the specification of $t_r/t_f = 1$ under TT, SS, FF, SF, and

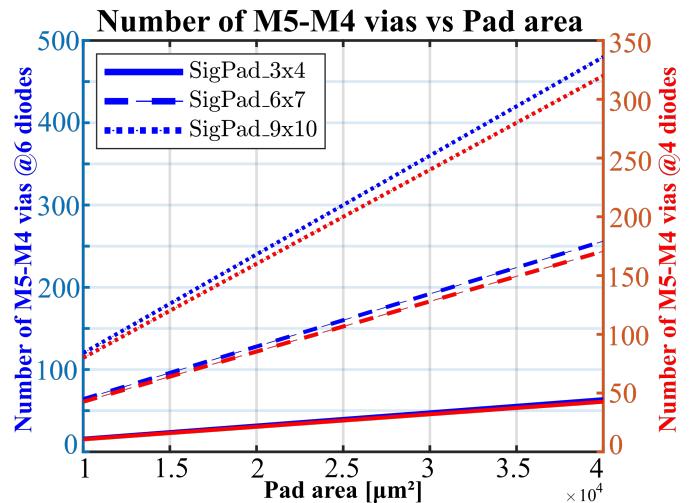


Fig. 26: Number M5-M4 vias vs pad area for a signal pad cell based on one of the 12 designs.

FS process corners. Additionally, ten combinational cells were designed with the W_N and W_P obtained during the design inverter phase to implement a standard cell library. We propose a code that characterizes the library, identifies the logic function associated with each cell, and measures the t_r , t_f , t_{phl} and t_{plh} . The timing measurements were developed in each cell under a typical range of operating conditions for τ_{in} and C_L . Moreover, the library contains five files associated with the layouts (.mag), geometry (.lef), electrical model (.spice), logic and timing characterization (.lib) and timing data for postprocessing (.txt) for each cell.

The designed I/O cells included signal pad cells, filler cells, and cut-off cells, all of which contain only one VDD and one VSS rail. The optimal design chosen for the pad cell corresponds to a cell with 12 diodes and "in" nodes with sizes of $6\mu\text{m} \times 7\mu\text{m}$. The signal pad cell has an electromagnetic model equivalent to an RC circuit. The R, C, and bandwidth parameters of the electromagnetic model were determined using S_{21} scattering parameters. Due to the significant effect of the approximations made in the CST software on resistance and capacitance, the results obtained in Ngspice were considered conclusive.

Among the possible future works that could complement this work, it is possible to apply the design methodology in each standard cell to obtain their respective optimal W_N and W_P . Also, it is desirable to include the power consumption calculation and the timing measurements for sequential cells.

Regarding I/O cells, there are several options such as characterizing the cell by calculating the maximum current in amperes or presenting a design methodology for any signal pad cell area. However, a possible future work with great utility in the work described in this project is to design the cell in CST, including both dual diodes and the entire design layout.

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