

***Processeur***

```
graph TD; P[Processeur] <--> L1I[L1-I]; P <--> L1D[L1-D]; L1I <--> L2[Cache L2]; L1D <--> L2; L2 <--> M[Mémoire principale];
```

**L1-I**

**L1-D**

***Cache***

**Cache L2**

***Mémoire principale***