University of San Carlos | Department of
COMPUTER ENGINEERING

PART #1

CpE 3202 – Computer Organization and Architecture

Basic Concepts and Computer Evolution

UNIT 1: INTRODUCTION

CpE 3202 | Computer Organization and Architecture

ARCHITECTURE: GENERAL CONCEPT

- It is defined as the **art and science** of **designing and building** an **object**.
  - ***building*** is the **most common object** in the **human world**

- It helps in defining the functional, physical, and the performance standards for any object.

Note:

- Every object in the real world is based on some architecture.
  - ***Example:***

    Architect will define the building in terms of building drawings and specifications for various building components.

COMPUTER ARCHITECTURE

- **Computer Architecture:**
  - those attributes of a system visible to a programmer
  - those attributes that have a direct impact on the logical execution of a program

- **Architectural attributes:**
  - Instruction set
  - The number of bits used to represent various data types (e.g., numbers, characters)
  - I/O mechanisms
  - Techniques for addressing memory

  Example: Is there a multiply instruction?

COMPUTER ARCHITECTURE

IMPORTANT NOTES!

- A **term** that is often used interchangeably with **computer architecture** is **Instruction Set Architecture** (**ISA**).

- The **ISA** defines **instruction formats**, **instruction opcodes**, **registers**, **instruction and data memory**; **the effect of executed instructions on the registers and memory**; and **an algorithm for controlling instruction execution**.

ORGANIZATION: GENERAL CONCEPT

- It is the **act or process of organizing** or **of being organized**.
- It is a term that is defined as **arranging and classifying things together logically** to maximize the functional convenience.
- It refers to the **state** wherein things are organized and arranged in a particular manner.

COMPUTER ORGANIZATION

- It is **concerned** with the **way** the ***hardware components*** are **connected together** to **form a computer system**.

- It refers to **the operational units** and their **interconnections** that **realize the architectural specifications**.

- It refers to ***how features are implemented***.

COMPUTER ORGANIZATION

- **Organizational Attributes:**
  - ***Hardware details*** **transparent to the programmer**, such as **control signals**
  - ***Interfaces*** **between the computer and peripherals**
  - The ***memory technology*** **used**
  - ***Example:***
    Is there a ***hardware multiply unit*** or ***is it done by repeated addition***?

COMPUTER ORGANIZATION AND ARCHITECTURE

Architectural Design Issue

A **computer** will have a **multiply instruction**.

Organizational Design Issue

The **instruction** (***multiply instruction***) will be **implemented by a** ***special multiply unit*** or **by a** ***mechanism that makes repeated use of the add unit*** of the system.

COMPUTER ORGANIZATION AND ARCHITECTURE

IMPORTANT NOTES!

- All **Intel x86 family** **share the same basic architecture**
- The **IBM System/370 family** **share the same basic architecture**
- This **gives code compatibility**, at least backwards
- **Organization differs between different versions**
- **Retain the same architecture** to **protect customer's software investment** but **organization is changed** with the **changes in technology**.

STRUCTURE AND FUNCTION

COMPUTER

- ***Computer:*** described as a **complex system**
  - use **top-down approach** to describe the system

- The **hierarchical nature** of the computer should be recognized by the designers.

- In **designing a computer**, the **designer is concerned** with the **structure** and **function** of the system.

COMPUTER: STRUCTURE AND FUNCTION

❖ **Structure**

- It refers to the ***way*** in which the **components of the computer relate to each other**.

❖ **Function**

- It refers to the ***operation*** **of each individual component of the computer** as ***part of the structure***.

COMPUTER: FUNCTION

4 Basic Functions a Computer Can Perform

❖ ***Data Movement:***

- The ***computer's operating environment*** consists of ***devices*** that ***serve*** as either ***sources or destinations of data***.
  - ✓ **When data are received from or delivered to a device** that is **directly connected to the computer**, the **process** is known as ***input–output* (*I/O*),** and the **device** is referred to as a ***peripheral***.
  - ✓ **When *data are moved* over longer distances, to or from a remote device**, the **process** is known as ***data communications***.

❖ ***Control:***

- Within the computer, a **control unit manages the computer's resources** and **orchestrates the performance of its functional parts** in **response to instructions**.

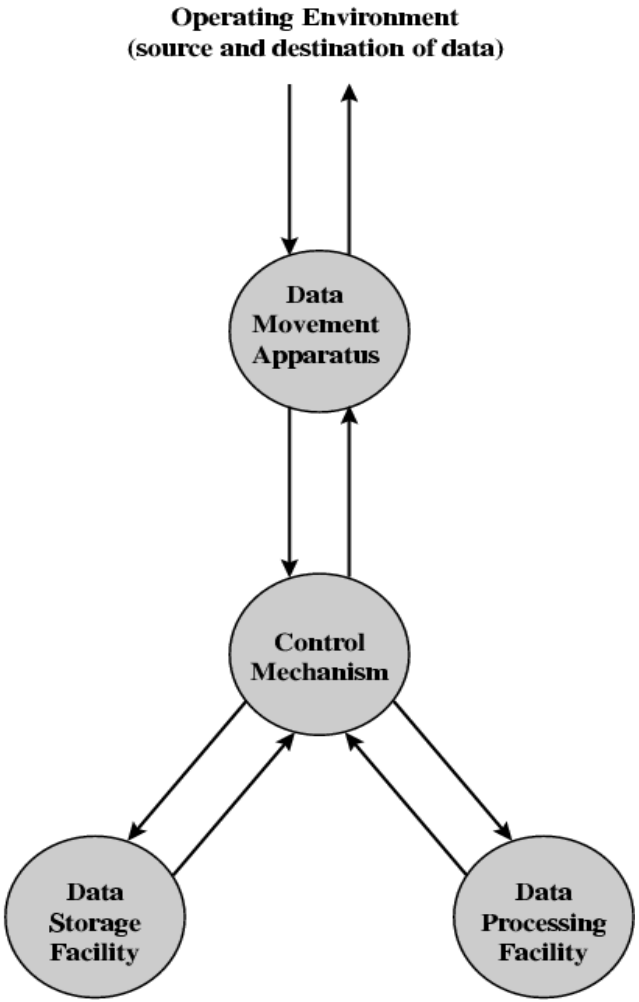
COMPUTER: FUNCTION

4 Basic Functions a Computer Can Perform

- ***Data Processing:***
  - Data may take a wide variety of forms, and the range of processing requirements is broad.

- ***Data Storage:***
  - Files of data are stored on the computer for subsequent retrieval and update.
  - There is at least a short-term data storage function and a long-term data storage function.

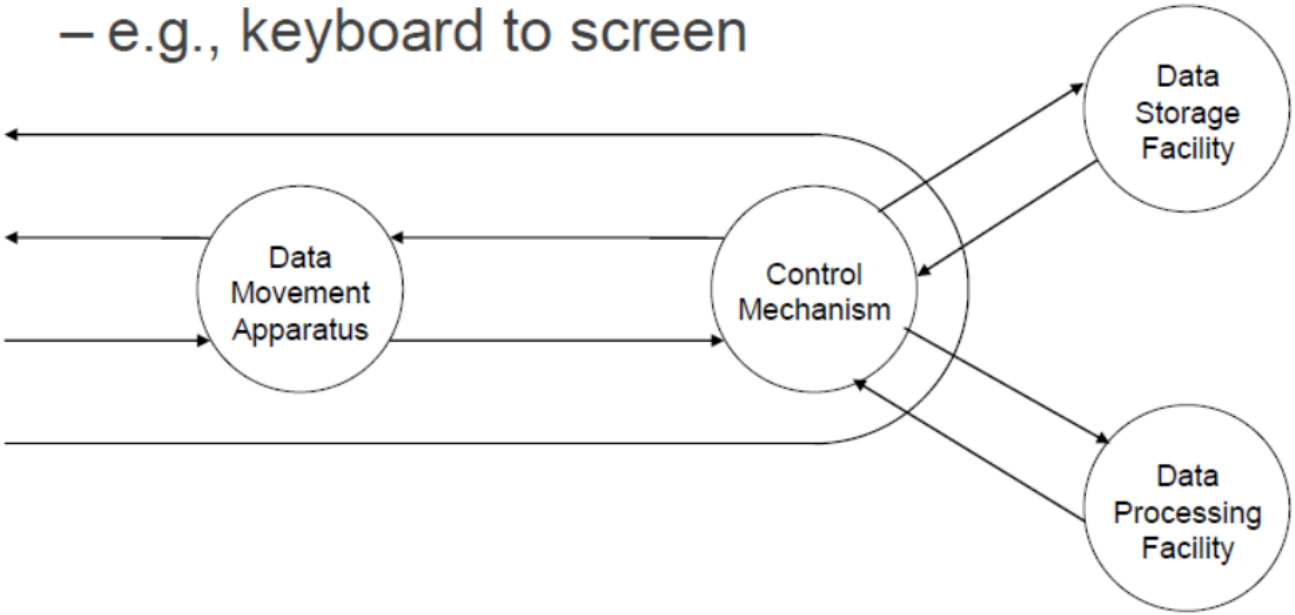
A FUNCTIONAL VIEW OF THE COMPUTER



A FUNCTIONAL VIEW OF THE COMPUTER

OPERATIONS: (1)

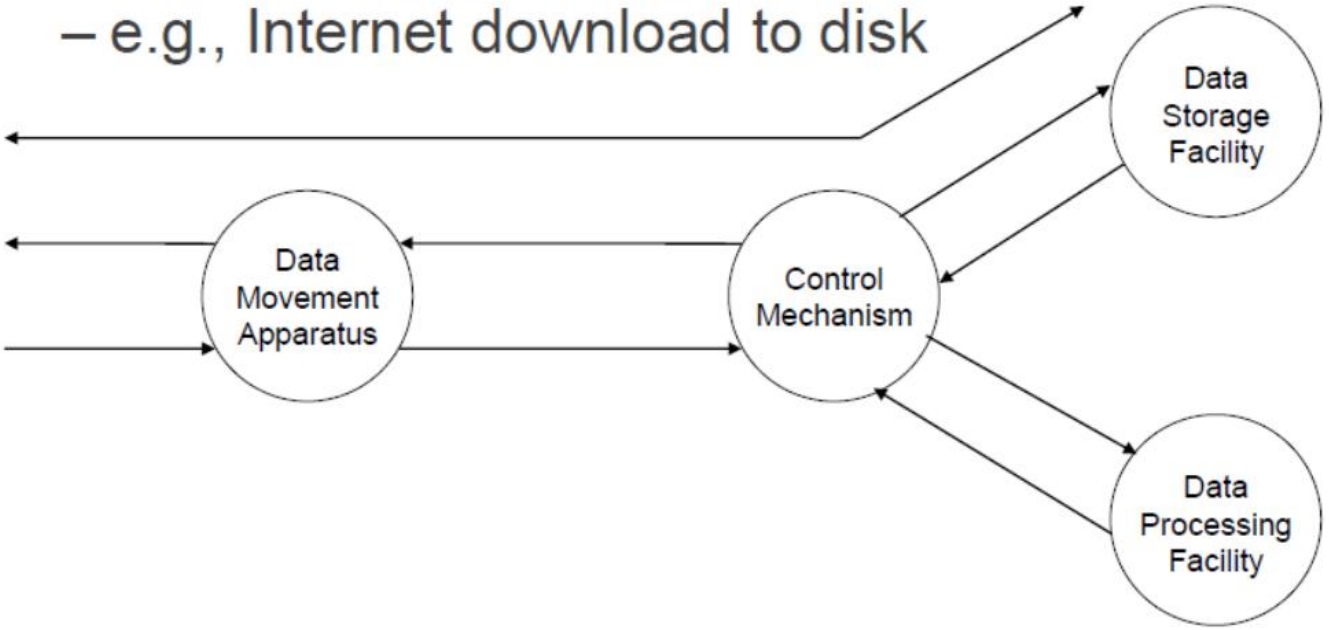
- **Data Movement**
  - e.g., keyboard to screen



A FUNCTIONAL VIEW OF THE COMPUTER

OPERATIONS: (2)

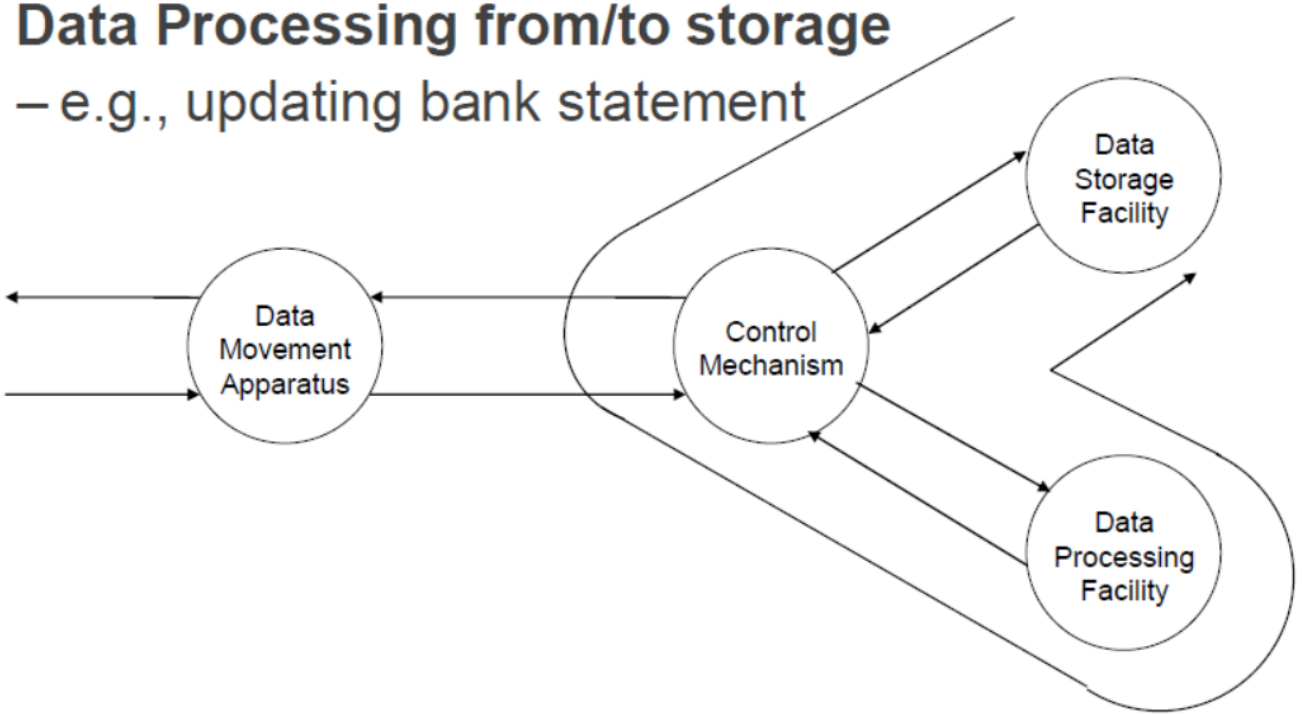
- **Data Storage**
  - e.g., Internet download to disk



A FUNCTIONAL VIEW OF THE COMPUTER

OPERATIONS: (3)

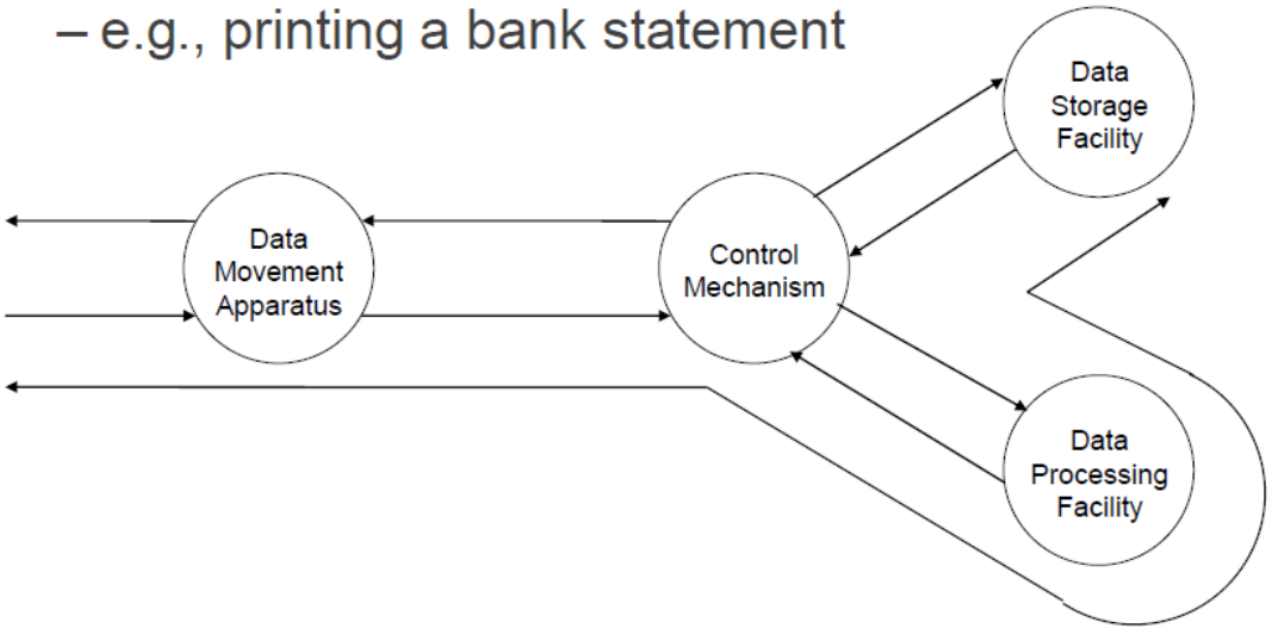
- **Data Processing from/to storage**
  - e.g., updating bank statement



A FUNCTIONAL VIEW OF THE COMPUTER

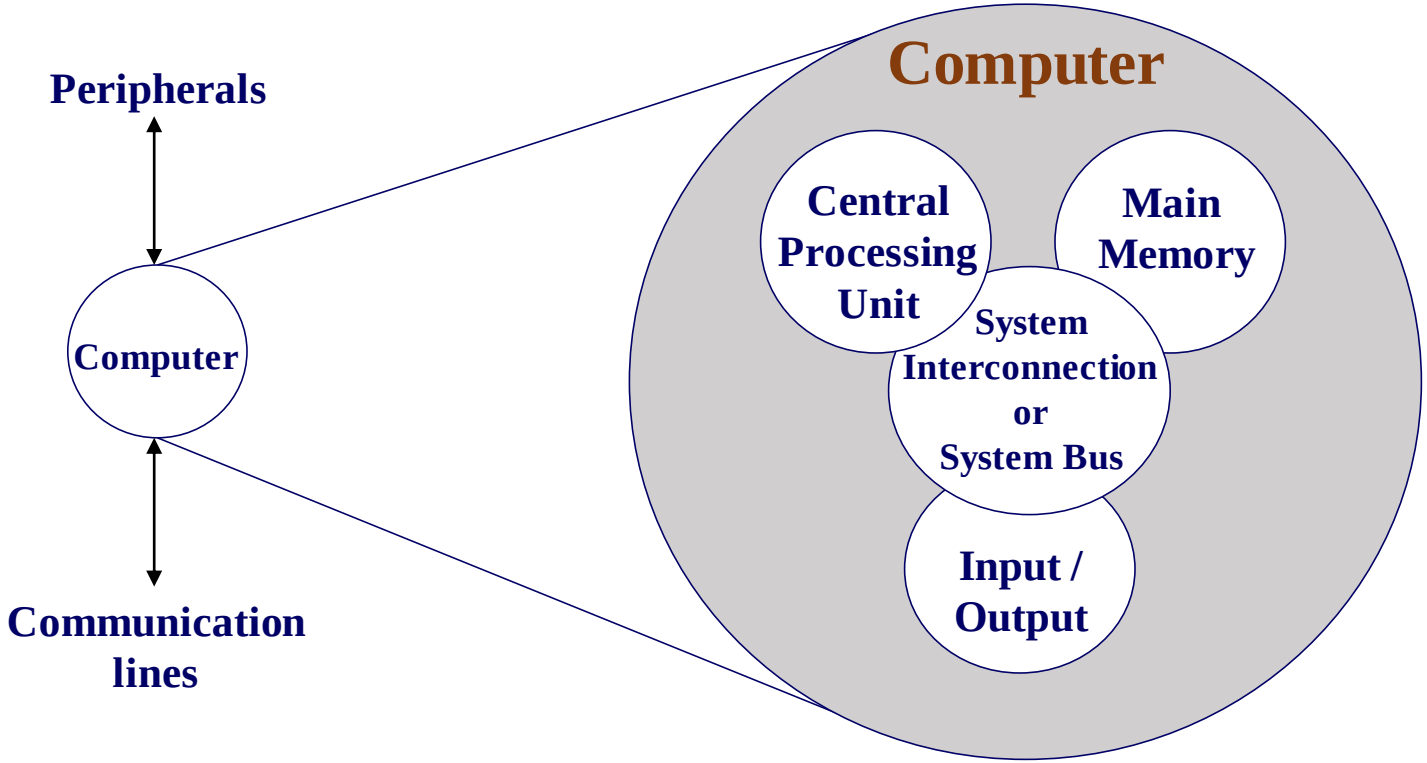
OPERATIONS: (4)

- **Data Processing from storage to I/O**
  - e.g., printing a bank statement



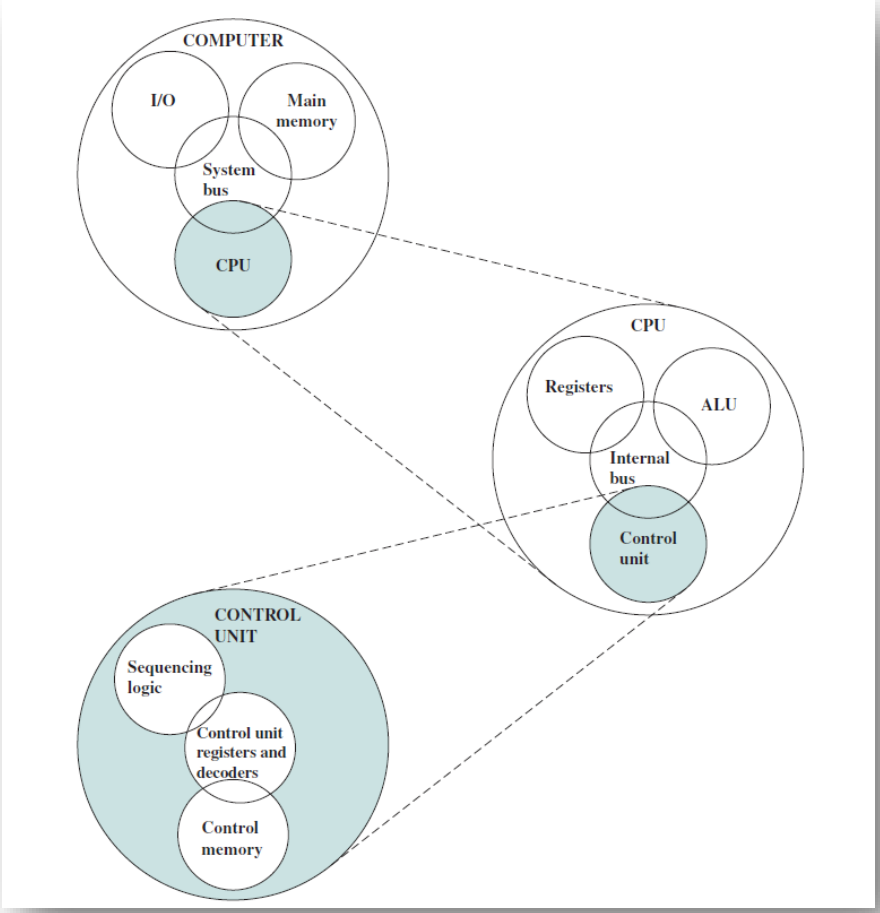
COMPUTER: STRUCTURE

Simple Single-Processor Computer: Top-Level Structure



COMPUTER: STRUCTURE

Simple Single-Processor Computer: Top-Level Structure



SINGLE-PROCESSOR COMPUTER

INTERNAL STRUCTURE
4 Main Structural Components

- ***CPU (Central Processing Unit)***
  - **Controls** the operation of the computer and performs its data processing functions
  - Often simply referred to as **processor**
  - CPU is the **most complex structural component of the computer**

- ***Main Memory***
  - **Stores** data

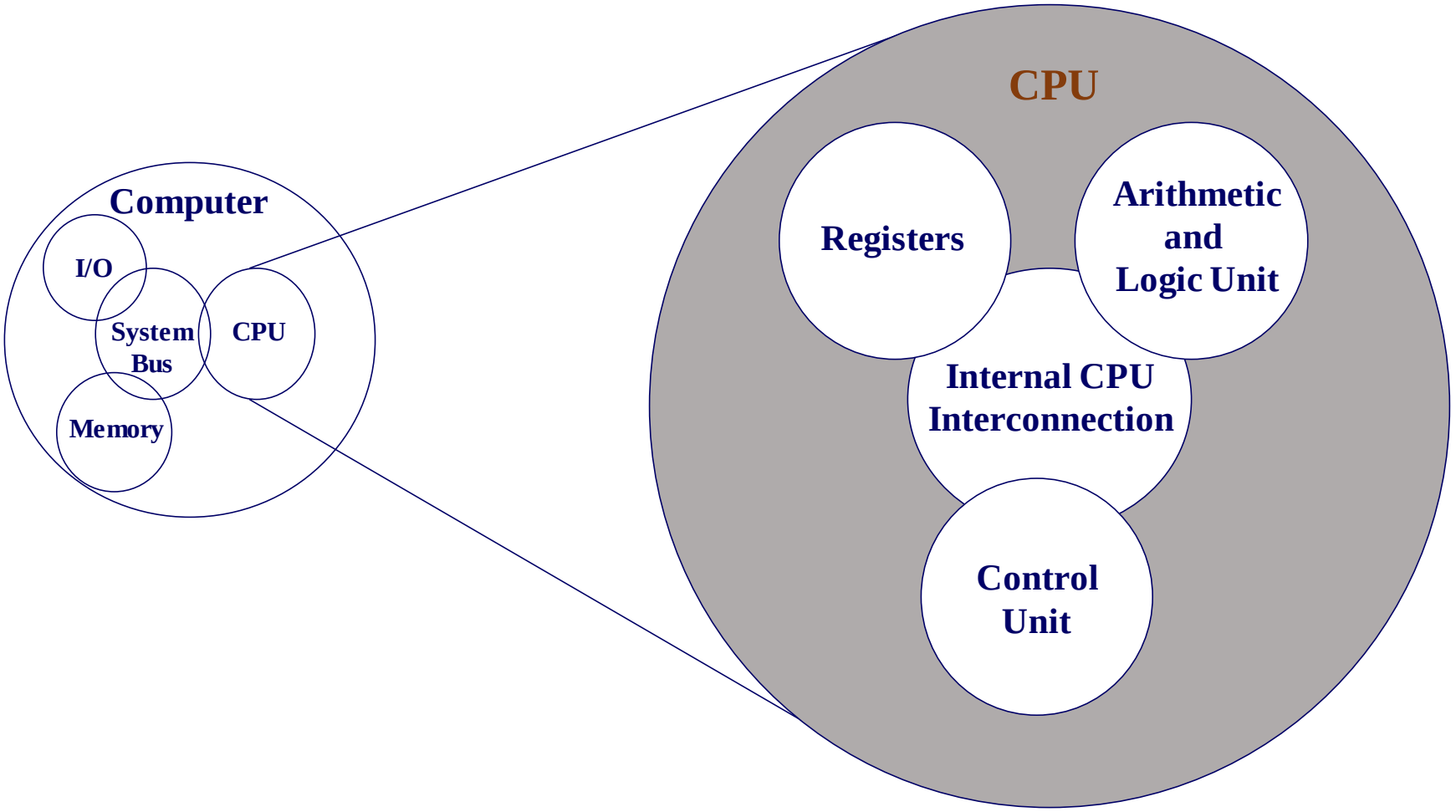
SINGLE-PROCESSOR COMPUTER

INTERNAL STRUCTURE
4 Main Structural Components

- ***I/O***
  - **Moves** data between the computer and its external environment

- ***System Interconnection***
  - Some **mechanism** that provides **for communication** among **CPU, Main Memory, and I/O**
  - **Common example:**
    - ✓ ***System bus:***
      - consisting of **a number of conducting wires** to which **all the other components are attached**

STRUCTURE: THE CPU



4 MAJOR STRUCTURAL COMPONENTS OF THE CPU

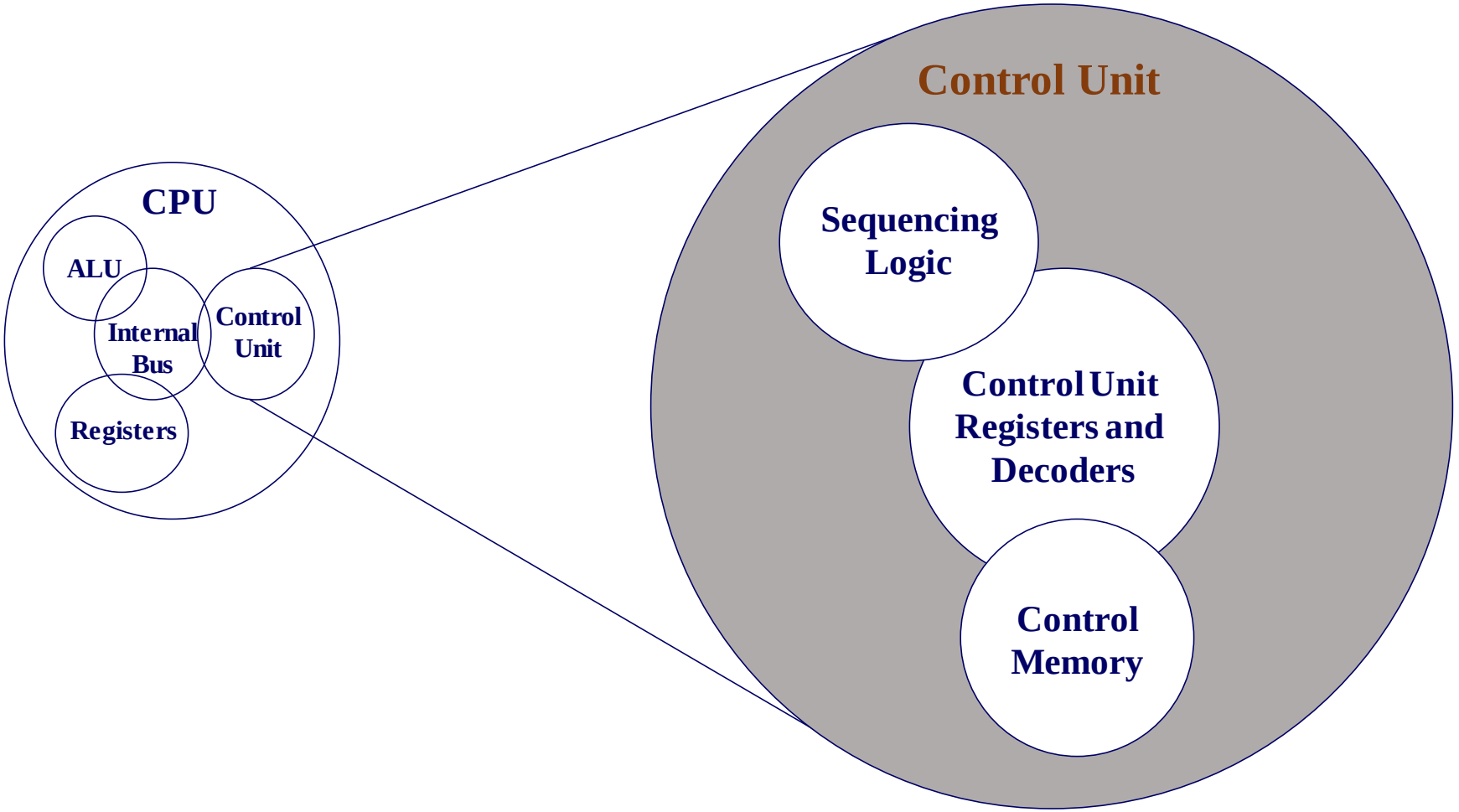
1) **Control Unit**
   - **Controls** the operation of the CPU and hence the computer

2) **ALU**
   - **Performs** the computer's data processing functions (**all the arithmetic and logical operations**)

3) **Registers**
   - **Provides** internal storage to the CPU

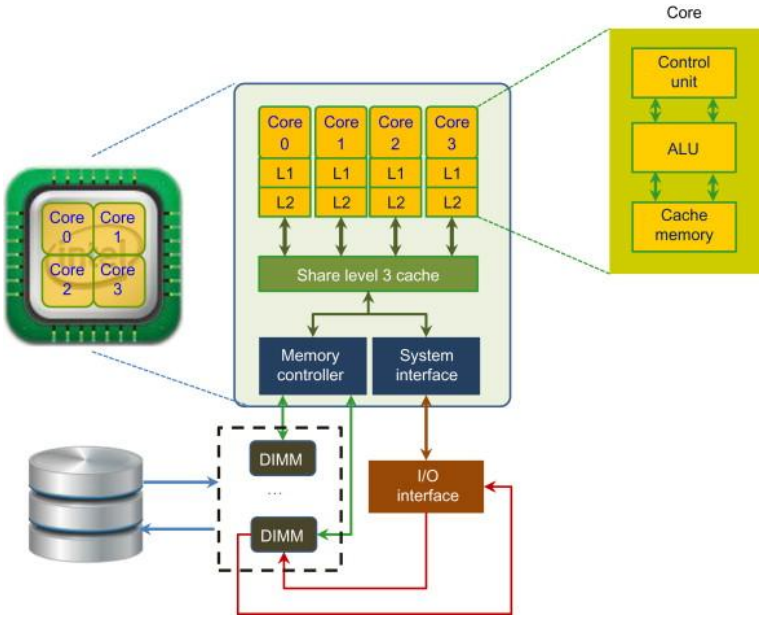
4) **CPU Interconnection**
   - **Some mechanism** that provides for communication among **Control Unit**, **ALU**, and **Registers**

STRUCTURE: THE CONTROL UNIT



COMPUTER: STRUCTURE

Multicore Computer Structure



- ***Contemporary computers*** generally **have multiple processors**
- ***Multicore computer:*** term used to refer to computer with processors all reside on a single chip
- ***Each processing unit*** (consisting of a control unit, ALU, registers, and perhaps cache) is called a ***core***

COMPUTER: STRUCTURE

Multicore Computer Structure

- **Central Processing Unit (CPU):**
  - It is the ***portion of a computer*** that **fetches and executes instructions**.
  - It consists, basically, of an **ALU**, a **control unit**, and **registers**.
  - It is often **simply referred** to as a ***processor*** in a **system** with a ***single processing unit***.

COMPUTER: STRUCTURE

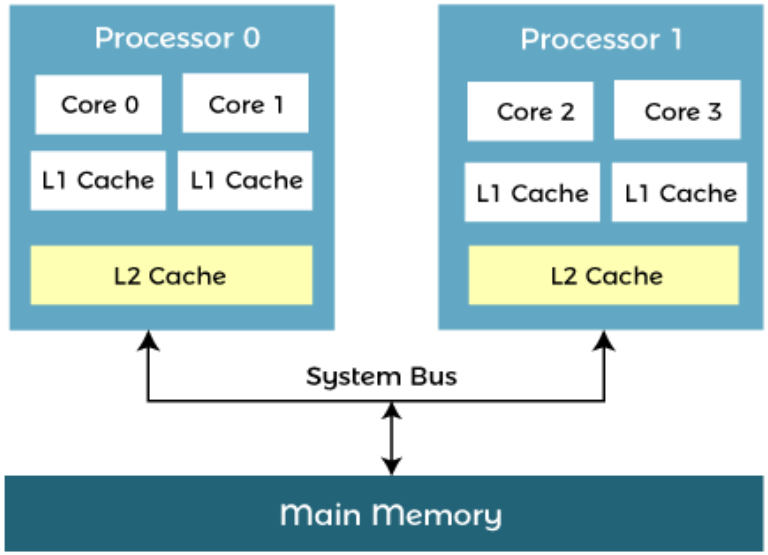
Multicore Computer Structure

- **Processor:**
  - A physical piece of silicon containing one or more cores.
  - The processor is the computer component that interprets and executes instructions.

- **Note:**
  - If a **processor contains multiple cores**, it is referred to as a ***multicore processor***.

COMPUTER: STRUCTURE

Multicore Computer Structure

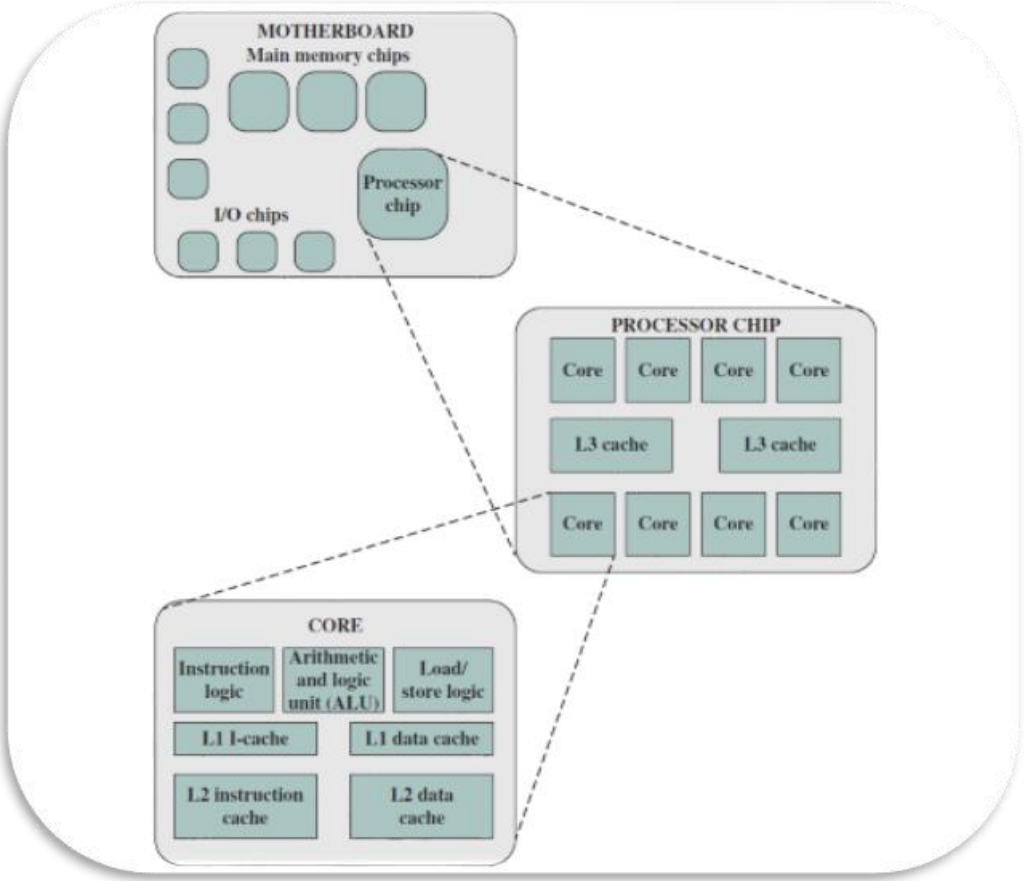


- **Core:**
  - An ***individual processing unit*** on a processor chip.
  - It may be equivalent in functionality to a CPU on a single-CPU system.

- **Note:**
  - **Other specialized processing units**, such as **one optimized for vector and matrix operations**, are also **referred to as *cores***.

COMPUTER: STRUCTURE

Multicore Computer Structure



Simplified View of Major Elements of a Multicore Computer

COMPUTER: STRUCTURE

Multicore Computer Structure

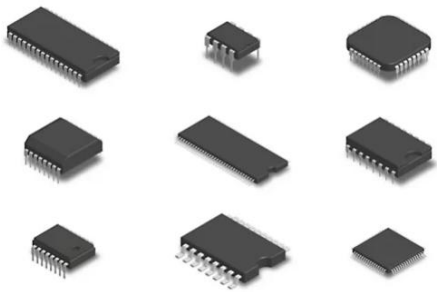
- ***Most of the computers***, including ***embedded computers*** in **smartphones and tablets**, plus **personal computers**, **laptops**, and **workstations**, are housed on a ***motherboard***.
- The ***main printed circuit board*** in a **computer** is called a ***system board*** or ***motherboard***.
- A ***motherboard*** is the ***main printed circuit board*** **(**or ***system board*****)** in **general-purpose computers** and **other expandable systems** that ***holds and allows communication*** between **many of the crucial electronic components of a system**, such as the **central processing unit and memory**, and **provides connectors for other peripherals**.

COMPUTER: STRUCTURE

Multicore Computer Structure

- The ***smaller printed circuit boards*** that **plug into the slots** in the **main board** are called ***expansion boards***.

- The **most prominent elements on the motherboard** are the **chips**.
  - A ***chip*** is **a single piece of semiconducting material**, ***typically silicon***, upon which electronic circuits and logic gates are fabricated.
  - The **resulting product** is referred to as an **Integrated Circuit (IC)**.



COMPUTER: STRUCTURE

Multicore Computer Structure: Important Notes!

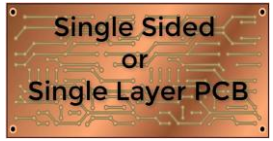
- The **motherboard** contains a **slot or socket** for the ***processor chip***, which typically **contains multiple individual cores**, in what is known as a ***multicore processor***.

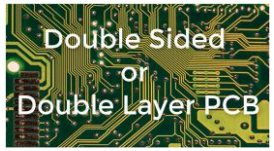
- There are also ***slots*** for **memory chips**, **I/O controller chips**, and o**ther key computer components**.

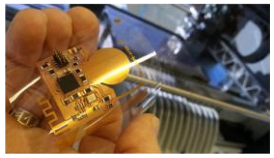
- ***Desktop Computers:***
  - ***Expansion slots*** enable the **inclusion of more components on expansion boards**, thus, a ***modern motherboard connects only a few individual chip components***, with ***each chip containing from a few thousand up to hundreds of millions of transistors***.

COMPUTER: STRUCTURE

Multicore Computer Structure



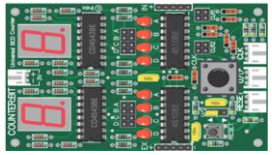


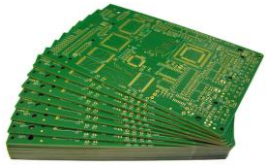


Printed Circuit Board (PCB)

- It is a ***rigid, flat board*** that ***holds and interconnects*** **chips and other electronic components**.

- This **board** is **made of layers**, **typically** ***two to ten***, that ***interconnect components via copper pathways*** that are ***etched into the board***.

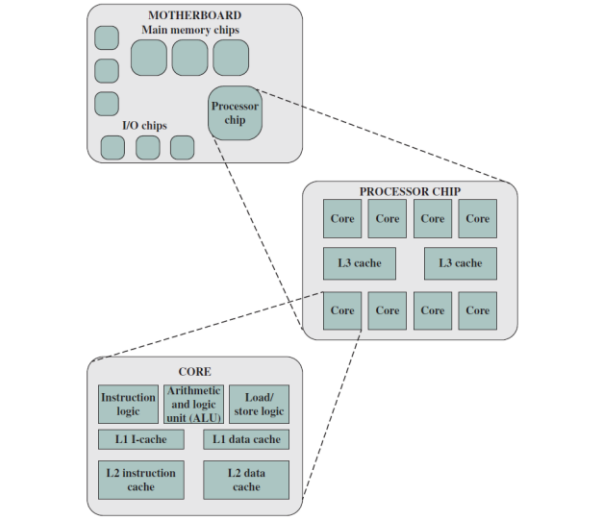




COMPUTER: STRUCTURE

Multicore Computer Structure

The Functional Elements of a CPU Core

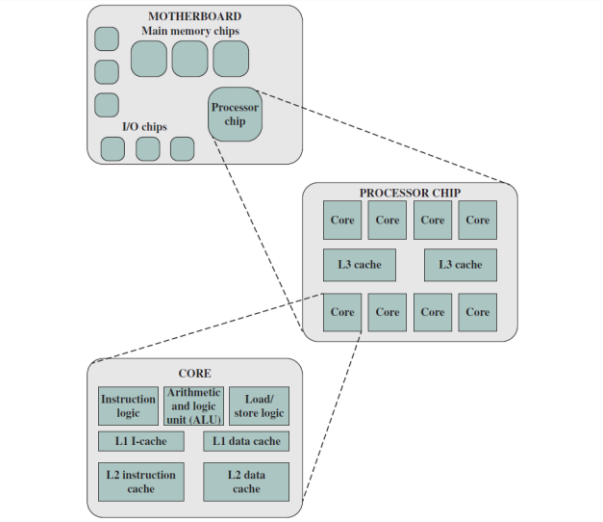


- ***Instruction Logic:***
  - This includes the **tasks** involved in **fetching instructions**, and **decoding each instruction to determine the instruction operation** and the **memory locations of any operands**.
- ***Arithmetic and Logic Unit (ALU):***
  - **Performs** the **operation** specified by an instruction.
- ***Load/Store logic:***
  - **Manages** the ***transfer of data to*** and ***from main memory*** **via cache**.

COMPUTER: STRUCTURE

Multicore Computer Structure

The Functional Elements of a CPU Core

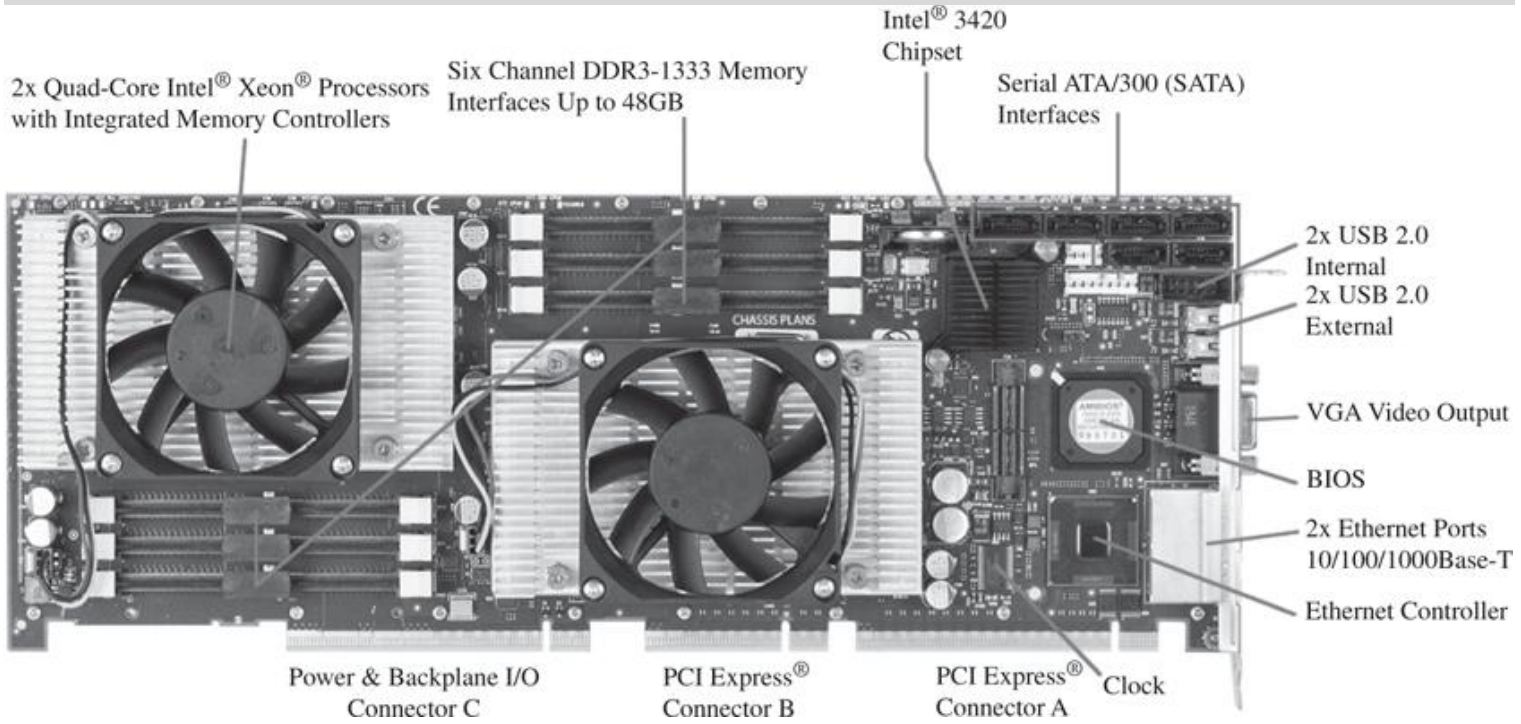


- The **core** also contains an **L1 cache**, **split between an L1 *Instruction cache* (I-cache)** that is **used for the transfer of instructions to and from main memory**, and an **L1 Data cache**, for the **transfer of operands and results**.
- Typically, **today's processor chips also include an L2 cache as part of the core**.
- In many cases, this ***cache is also split*** between **instruction and data caches**, although a ***combined, single L2 cache*** is also used.

HIERARCHICAL STRUCTURE OF COMPUTERS

EXAMPLE 1

Motherboard with Two Intel Quad-Core Xeon Processors



HIERARCHICAL STRUCTURE OF COMPUTERS

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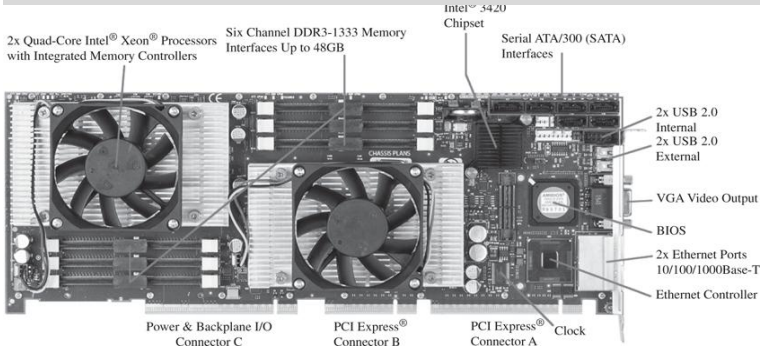
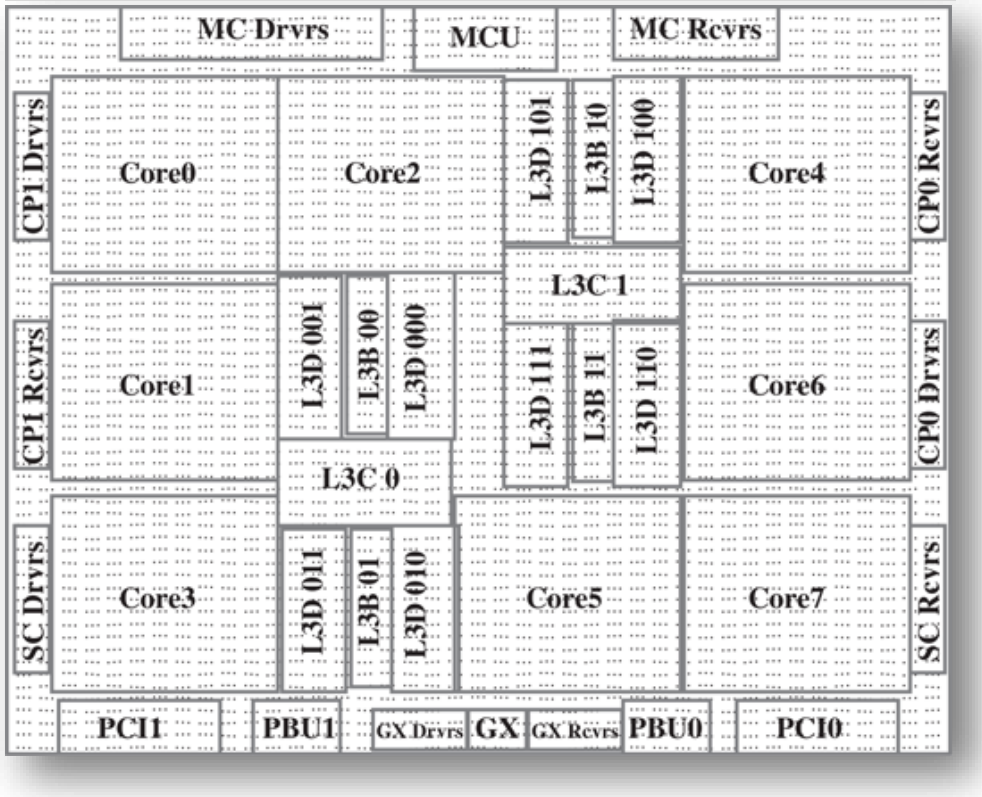


- **PCI-Express (PCIe) slots:** for a high-end display adapter and for additional peripherals
- **Ethernet controller and Ethernet ports:** for network connections
- **USB sockets:** for peripheral devices
- **Serial ATA (SATA) sockets:** for connection to disk
- **Interfaces:** for DDR (double data rate) main memory
- **Intel 3420 chipset:**
  - An **I/O controller** for direct memory access operations between peripheral devices and main memory

PROCESSOR CHIP/UNIT: *INTERNAL STRUCTURE*

EXAMPLE 2

IBM z13 Processor Unit (PU) Chip Diagram



PROCESSOR CHIP/UNIT: *INTERNAL STRUCTURE*

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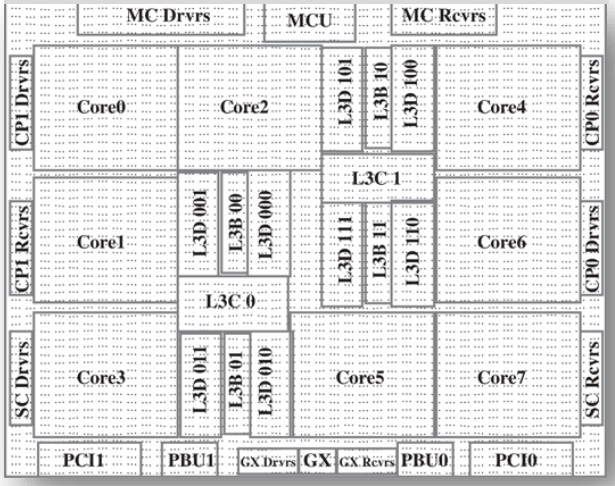
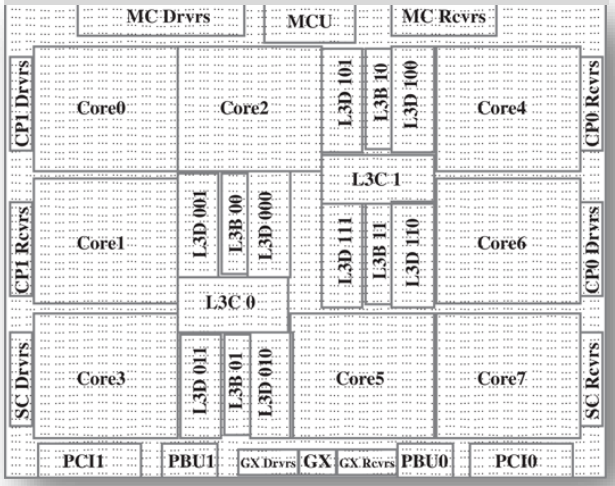


- It is a ***to-scale layout*** of the **processor chip** for the **IBM z13** mainframe computer.
- This **chip has 3.99 billion transistors**.
- The **superimposed labels** indicate **how the silicon surface area of the chip is allocated**.
- This **chip has eight cores, or processors**.
- A **substantial portion of the chip is devoted to the L3 cache**, which is **shared by all eight cores**.

PROCESSOR CHIP/UNIT: *INTERNAL STRUCTURE*

EXAMPLE 2

IBM z13 Processor Unit (PU) Chip Diagram

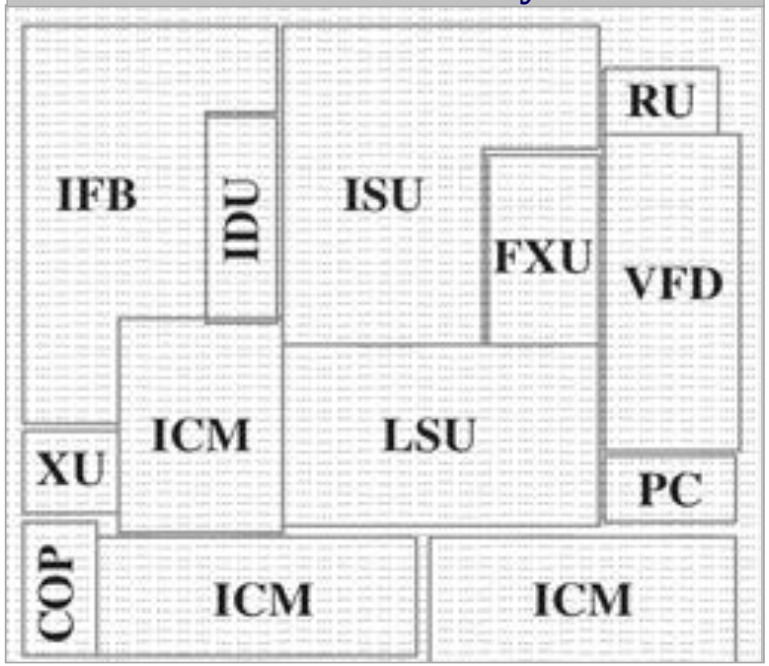


- The **L3 control logic** controls traffic between the **L3 cache and the cores**; and **between the L3 cache and the external environment**.
- There is **storage control (SC) logic** between the **cores and the L3 cache**.
- The **memory controller (MC)** function **controls access to memory external to the chip**.
- The **GX I/O bus controls** the **interface to the channel adapters accessing the I/O**.

INTERNAL STRUCTURE OF A SINGLE CORE

EXAMPLE 3

IBM z13 Core Layout



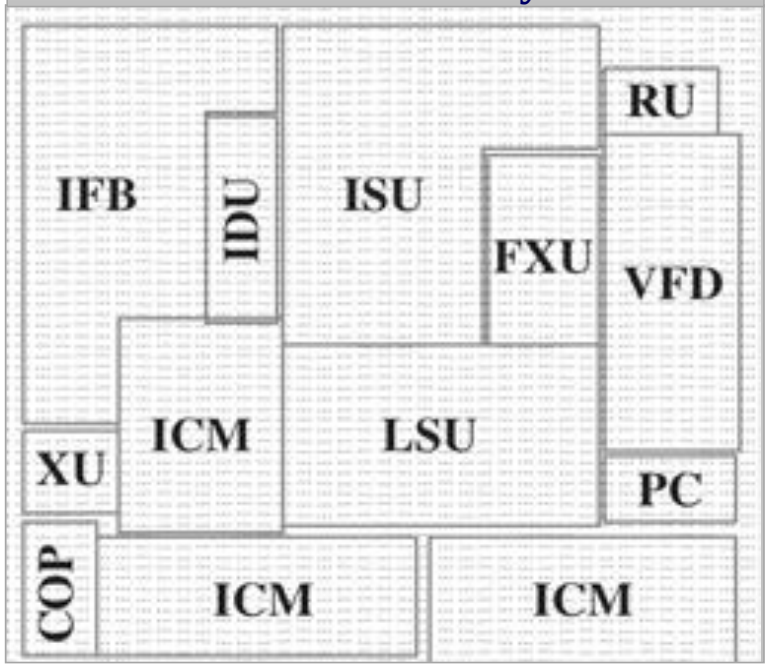
- The **core** implements the **z13 instruction set architecture**, referred to as the **z/Architecture**.

- This is **a portion of the silicon surface area** making up **a single-processor chip**.

INTERNAL STRUCTURE OF A SINGLE CORE

EXAMPLE 3

IBM z13 Core Layout



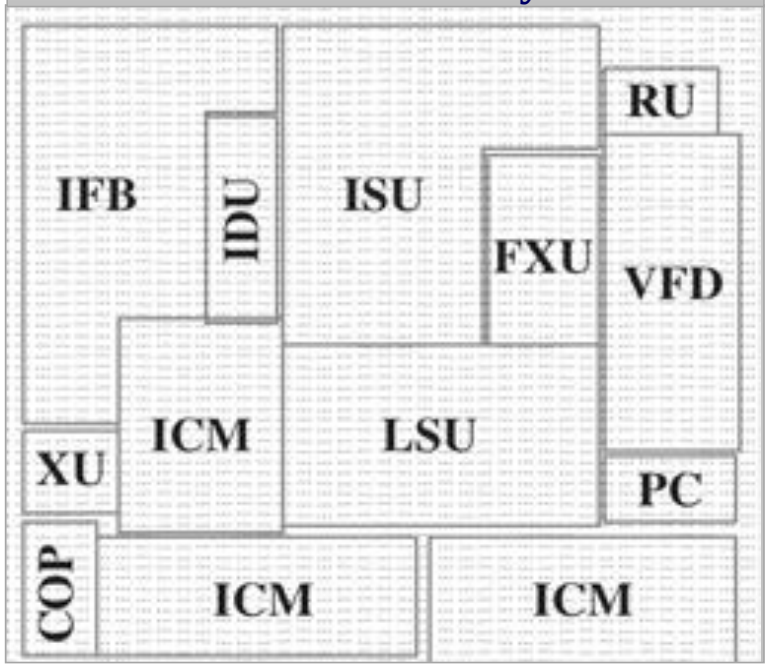
- **Main sub-areas within this core area:**

- **ISU (Instruction Sequence Unit):**
  - Determines the sequence in which instructions are executed in what is referred to as a superscalar architecture
  - Enables the out-of-order (OOO) pipeline
  - Tracks register names, OOO instruction dependency, and handling of instruction resource dispatch

INTERNAL STRUCTURE OF A SINGLE CORE

EXAMPLE 3

IBM z13 Core Layout



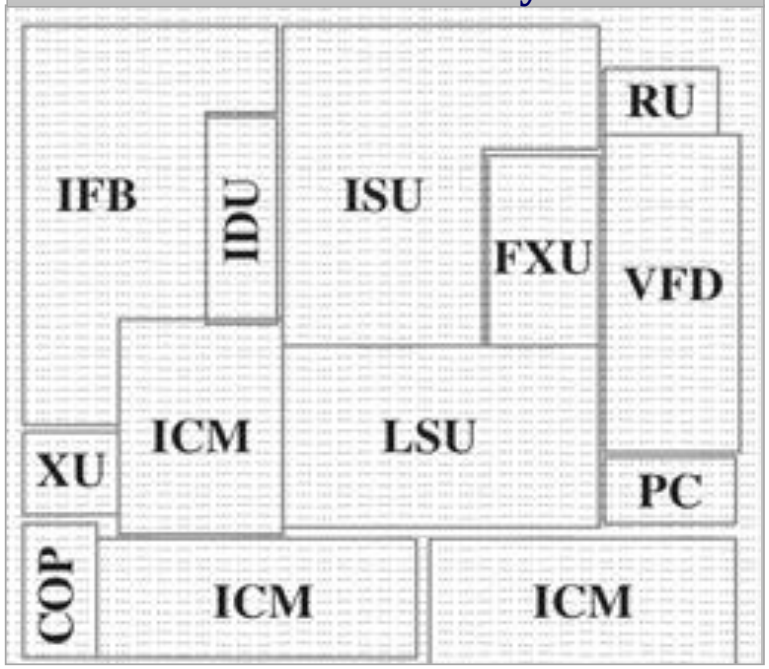
- **Main sub-areas within this core area:**

- **IFB (Instruction Fetch and Branch) and ICM (Instruction Cache and Merge)**
  - These two sub-units contain the 128-kB instruction cache, branch prediction logic, instruction fetching controls, and buffers.
  - The relative size of these sub-units is the result of the elaborate branch prediction design.

INTERNAL STRUCTURE OF A SINGLE CORE

EXAMPLE 3

IBM z13 Core Layout



- **IDU (Instruction Decode Unit):**
  - It is fed from the IFU buffers, and is responsible for the parsing and decoding of all z/Architecture operation codes.

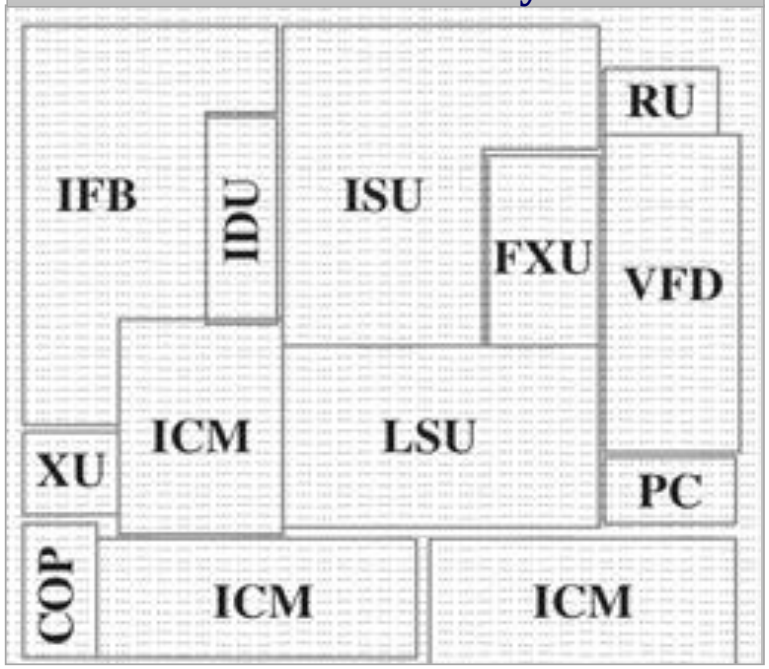
- **LSU (Load-Store Unit):**
  - Contains the 96-kB L1 data cache, and manages data traffic between the L2 data cache and the functional execution units
  - Responsible for handling all types of operand accesses of all lengths, modes, and formats as defined in the z/Architecture

- **XU (Translation Unit):**
  - Translates logical addresses from instructions into physical addresses in main memory
  - Contains a translation lookaside buffer (TLB) used to speed up memory access

INTERNAL STRUCTURE OF A SINGLE CORE

EXAMPLE 3

IBM z13 Core Layout

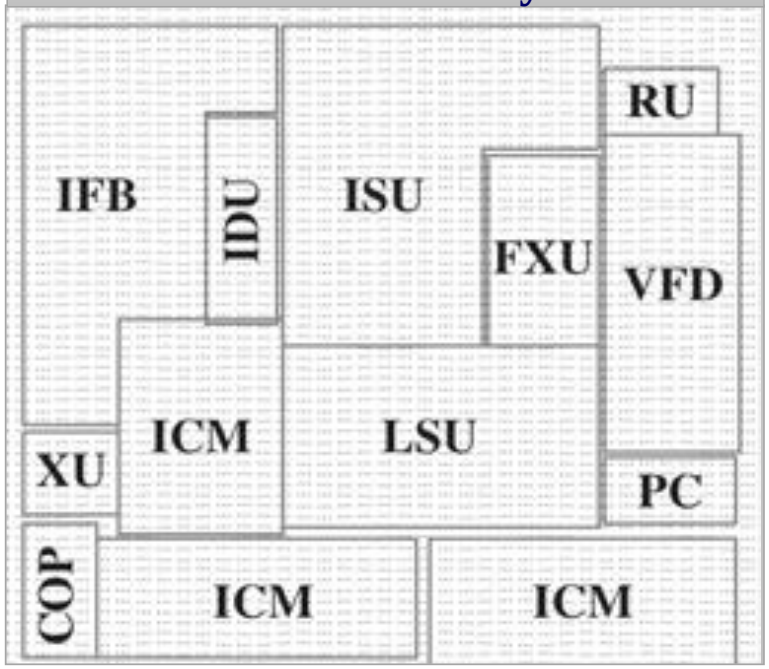


- **PC (Core Pervasive Unit):**
  - Used for instrumentation and error collection
- **FXU (FiXed-point Unit):**
  - Executes fixed-point arithmetic operations
- **VFU (Vector and Floating-point Units):**
  - Binary floating-unit part handles all binary and hexadecimal floating-point operations, as well as fixed-point multiplication operations
  - Decimal floating-unit part handles both fixed-point and floating-point operations on numbers that are stored as decimal digits
  - Vector execution part handles vector operations

INTERNAL STRUCTURE OF A SINGLE CORE

EXAMPLE 3

IBM z13 Core Layout



- **RU (Recovery Unit):**
  - Keeps a copy of the complete state of the system that includes all registers, collects hardware fault signals, and manages the hardware recovery actions
- **COP (dedicated co-processor):**
  - Responsible for data compression and encryption functions for each core
- **L2D:**
  - A 2-MB L2 data cache for all memory traffic other than instructions
- **L2I:**
  - A 2-MB L2 instruction cache

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End of Lecture