Design and Implementation of the Digital Costas Loop Based on Software Defined Radio

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***Abstract*— The frequency offset is the main problem of the conventional SDR receiver for demodulation. In order to overcome this drawback, the new methods are applied to improve the conventional Costas loop which is used to extract carrier. Firstly, the integration and accumulator is designed to realize the function of low-pass filter, which takes up fewer hardware resources. Secondly, the more accurate arctangent phase detector is used to detect the phase. It replaces the multiplier phase detector, which only obtain the approximate phase difference. Based on these two improvements, the realization of each module about the improved loop is presented. In this paper, first of all, the designed algorithm is simulated on the plat of MATLAB and Modelsim. The simulation results show that the design in this paper is feasible and the method is very effective. Moreover the system has been implemented and tested using field programmable gate arrays (FPGA). The test results indicate that the system has many advantages, including the design structure is simple, the convergence speed and the stability are better, and it can eliminate the frequency offset effectively. Therefore, this system can be widely applied in the engineering.**

Keywords—Software Defined Radio (SDR), Costas loop, Carrier synchronization, FPGA

I. INTRODUCTION

Software defined radio (SDR) [1] is an emerging technology which can be applied in the upgrade of hardware and the improvement of function. It takes on many significant advantages. In the SDR receiver, the realization of synchronous carrier and the recovery of the sent information data are always the key and the difficult part in digital signal processing research field.

According to [2], for intermediate frequency BPSK signal, the optimal scheme to extract carrier is the Costas loop. The traditional Costas loop uses the low-pass filter to realize the filtering function which requires the performances of two different low-pass filters are same. However, in practical engineering, it is impossible to have two low-pass filters with the identical filtering performance. Because the low-pass filters need to do convolution, it is difficult to implement on the FPGA [3]. Further more, if the order of low-pass filter is very high, a lot of the multiplier and adder will be needed, so that it will take up a lot of hardware resources. Integration and accumulator not only can achieve the low-pass filtering functions, but also can guarantee that the two channels of I and Q have identical low-pass filter characteristics. Thereby the detect results of next level of the phase detector will be more accurate. Implemented on FPGA, it only requires a cyclic shift accumulator. The structure is very simple. It can save a lot of hardware resources and improve operational efficiency. Hence, the paper has improved the traditional low-pass filter module, using the integration and accumulator instead of the traditional low-pass filter to realize low-pass filtering.

Conventional Costas loop phase detector makes use of multiplier phase detector to achieve the function of phase detection. It is an approximate algorithm, that is, the true value of phase difference is approximated by the sine of the phase difference. Thus the error of the phase detect results will be relatively large. In addition, multiplier phase detector implemented in FPGA, will consume a lot of hardware resources. The result of arctangent phase detector is the value of phase difference, so the accuracy of the phase is higher. In the FPGA implementation, the arctangent algorithm can be implemented using Coordinated Rotation Digital Computer (CORDIC) algorithm, which only needs the operations of simple shift and addition. Therefore, it is relatively easy to achieve. The arctangent phase detector takes less hardware resources compared with the multiplier phase detector. As a result, the paper has improved the traditional phase module detection module as well, where arctangent phase detector is applied to take the place of the traditional multiplier phase detector to implement the function of phase detection.

II. THE PRINCIPLE OF THE IMPROVED DIGITAL COSTAS LOOP

The improved Digital Costas Loop is mainly includes four modules: Numerically Controlled Oscillator (NCO), integration and accumulator, Phase Detector and Loop Filter. The block diagram of Costas loop is shown in Figure 1.

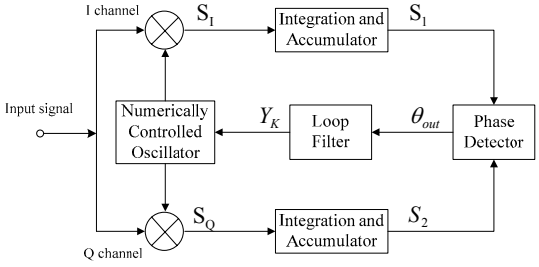

Figure 1.The block diagram of Costas loop

In the loop, the input signal of the Costas loop is from the sampling signal of Analog to Digital Converter which obtains the analog IF [4] (Intermediate Frequency) signal from the receiver. The Numerically Controlled Oscillator

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provides two channels local carrier signals which are orthogonal to each other. Then the two signals mix with the input signal and then complete the down-conversion [5]. Then the mixed signals are sent to the integration and accumulator which can filter the doubling frequency. Then the signals are carried into the phase detector and acquire the phase difference θ_{out}. And then θ_{out} is sent to loop filter. By the adjustment of the θ_{out}, the output signal of the loop filter can be applied to control the frequency control word of the NCO. Then, the closed loop is formed.

Consider the Costas loop input signal is $m(t)\cos\omega_0 t$, where m(t) is the baseband signal and ω_0 is the angular frequency of the transmitter carrier. The local NCO generates the I-channel and Q-channel signals I and Q which are orthogonal, and can be described as:

$$I(t) = \cos(\omega_0 t + \theta), \quad (1)$$

$$Q(t) = \sin(\omega_0 t + \theta), \quad (2)$$

where θ is the phase difference between the local carrier which is generated by NCO and the input modulated signal. From (1) and (2), mixing the two channel signals yields:

$$S_I(t) = m(t)\cos w_0 t \times \cos(w_0 t + \theta)$$

$$= \frac{1}{2} m(t)\left[\cos\theta + \cos(2w_0 t + \theta)\right]. \quad (3)$$

$$S_Q(t) = m(t)\cos w_0 t \times \sin(w_0 t + \theta)$$

$$= \frac{1}{2} m(t)\left[\sin\theta + \sin(2w_0 t + \theta)\right]. \quad (4)$$

Filtering the high frequency by integration and accumulators, the signal S_I(t) and $S_Q(t)$ can be transformed as:

$$S_1(t) = \frac{1}{2} m(t)\cos\theta . \quad (5)$$

$$S_2(t) = \frac{1}{2} m(t)\sin\theta . \quad (6)$$

Applying the PD, taking the arctangent of the phase difference, the output of the PD $\theta_{out}(t)$ is obtained as

$$\theta_{out}(t) = \arctan(S_2(t)/S_1(t)) = \theta . \quad (7)$$

So, when the Costas loop is unlocked, which is the local carrier and the sent carrier are not asynchronous, $\theta_{out}(t)$ is sent to the loop filter. Adjusted by the loop filter, the output of loop filter is taken as the control signal to control NCO in order to change the frequency and phase of local carrier. Thus tracking error is gradually reduced, until the signal tracks on the sent carrier frequency.

When the loop is locked, the steady-state phase difference is very small, to approximate to 0. Then the loop can extract the synchronous carrier signal. Moreover the system can recover the sending information from the In-phase channel.

III. THE DESIGN OF SUB-MODULES DIGITAL COSTAS LOOP

A. The Design of Numerically Controlled Oscillator

The goal of NCO is to produce two local orthogonal carrier signals. The direct frequency synthesizer (DDS) technology is adopted in this paper. Its structure is shown in Figure 2.

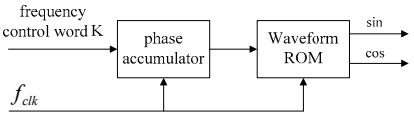

Figure 2. The structure of NCO

It can be seen from Figure 2 that NCO consists of one phase accumulator and one ROM waveform tables. The sine and cosine signals are generated by using the method of lookup table. And the .coe file for lookup table is generated by MATLAB. The output frequency of NCO is defined as:

$$f_{out} = \frac{Kf_{clk}}{2^N} . \quad (8)$$

Where f_{clk} is the system frequency, N is the bits number of phase accumulator, K is the frequency control word. The design uses the programmable NCO. In order to change the output frequency of NCO, the frequency control word is needed to be changed. In the Costas loop, the frequency control word is controlled by the output of loop filter so as to adjust the local carrier frequency.

B. The Design of Integration and Accumulator

The system uses the integration and accumulator instead of traditional low-pass filter to realize the filter function for filtering harmonic components after mixing. For mixed signal, the integration and accumulator accumulates every N point at one time and finish the filtering function. Then the signal output to the next level, phase detector. The size of parameter N relates to the low-pass filter performance of integration and accumulator. The design principle of N is: to ensure that the needed frequency components of input signal falls within the main lobe of integration and accumulator.

In FPGA implementations, integration and accumulator only need one accumulator adder, one subtractor and N registers to complete filtering function. The structure is very simple, relatively easy to implement.

C. The Design of phase detector

Phase detector is used to compare the phase. Its performance directly influent the wobble of Costas loop with white noise. According to the comparison for several common phase detecting methods in [6], it is shown that the arctangent phase detecting method is the only method which could keep linear in the half (+ 90 °) interval of input error range. And its output is the phase difference, not approximation, so the precision of phase detecting is higher. In addition, in this system, the output of the arctangent phase detector is the ratio of In-phase channel and Quadrate

channel signal whose magnitude are same. Therefore, the estimated value of phase difference is independent of the input signal amplitude, so the PD is free from the amplitude modulation and fading.

The FPGA realizing of arctangent phase detecting is important and difficult part of the loop. The quantify model of CORDIC algorithm is adopted in this paper to realize the arctangent. The specific design flow is given in figure 3, where n is the number of iterative calculation of CORDIC algorithm. At the end of the calculation, the value of z_{i+1} is the output of phase detector which is the value of phase difference θ . It only needs simple shift and addition operations for calculating the value of arctangent. Therefore, it is very suitable for the realization of hardware. And it also can take account of speed, precision, simple, efficient and so on.

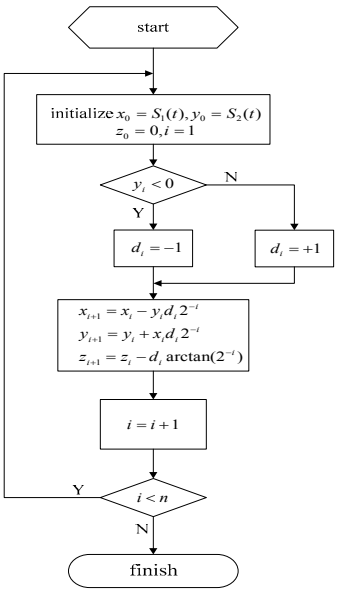

Figure 3. The flow diagram of arctangent implementation using CORDIC

In the realization of hardware circuit, this paper uses the pipeline architecture. Every level of pipeline only needs three adders, two shift registers and one coefficient memory. This architecture can save many resources. It only need simply add pipeline unit to improve its accuracy, so it has good extensibility. In this kind of structure, the output data has (n + l) lags of clock cycle relative to the input data. In normal work, every clock cycle can output a data. Therefore, the design can realize real-time processing of high-speed data. It is quite suitable for application in SDR digital receiver.

D. The Design of Loop Filter

Loop filter is the key role in Costas loop. It not only can filter out the high frequency phase detector leakage component, but also can adjust the parameters of Costas loop. The order and noise bandwidth determine the performance of the loop filter [7]. First-order digital loop filter will produce steady-state difference, and then reduce the system error performance. The actual implementation of third-order digital loop filter is difficult. Second-order digital loop filter in the case of DC gain is infinite and the frequency offset is a constant, it still can be able to achieve steady state, and the difficulty to achieve is appropriate. Considering the difficulty and the stability of the loop, second-order digital loop filter is used in this system. The frequency domain model of second-order digital loop filter is shown in figure 4.

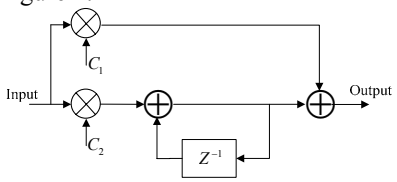

Figure 4. The frequency domain model of second-order digital loop filter

The Z domain transfer function of second-order digital loop filter can be expressed as:

$$F(z) = C_1 + C_2 \frac{1}{1 - z^{-1}}. \tag{9}$$

The corresponding time-domain model is shown in Figure 5.

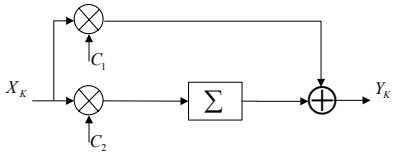

Figure 5. The time domain model of second-order digital loop filter

Then, the time domain difference equation is obtained as:

$$Y_K = C_1 X_K + C_2 \sum_{l=0}^{K} X_l . \tag{10}$$

Where X_K is the input value of loop filter which is the phase difference of phase detector. C_1 and C_2 are the coefficients of loop filter. The two coefficients of the Costas loop are important, which determine the performance of the loop. C_1 and C_2 can be expressed as follows [8]:

$$C_1 = \frac{1}{K_0 K_d} \frac{8\xi\omega_n T}{4 + 4\xi\omega_n T + (\omega_n T)^2}. \tag{11}$$

$$C_2 = \frac{1}{K_0 K_d} \frac{4(\omega_n T)^2}{4 + 4\xi\omega_n T + (\omega_n T)^2}. \tag{12}$$

Where ξ is damping coefficient. Generally, in the engineering, the value of the ξ is set 0.707. ω_n is the natural angular frequency of the loop. And it can be expressed as:

$$\omega_n = \frac{8\xi B_n}{4\xi^2 + 1}. \tag{13}$$

Where B_n is the equivalent noise bandwidth, and the general value meets with the relation $B_n \le 0.1 R_b$, where R_b is the rate of information data. $K_0 K_d$ is the loop gain.

The coefficients C_1 and C_2 are needed to make appropriate optimization or adjustment in the actual process

of debug the circuit. And values of the loop filter coefficients C_1 and C_2 are selected based on the features of the loop.

C_1 is the major decision of the loop with the size of the catch, and C_2 determines the long-term tracking and capture speed of the loop. If C_2 is too large, the loop will need a long time into the state of lock. Therefore, in the actual project, it is still need to select the appropriate values to meet with the needs of the project.

IV. SIMULATION AND ANALYSIS

A. MATLAB Simulation

In order to verify the feasibility of this system, the paper uses MATLAB to realize the functional simulation for the improved Costas loop. Firstly, the paper simulates a transmitter system, and generates a 140MHz analog IF signal. Then at the receiver, the Costas loop receives a 28MHz sampled signal which is from the Analog to Digital Converter. NCO generates two 28.2MHz orthogonal signals. After mixer, integration and accumulator and the arctangent phase detector, the result of phase detector is shown in Figure 6 (a). In the Costas loop, the frequency of the input signal to track the process is shown in Figure 6 (b).

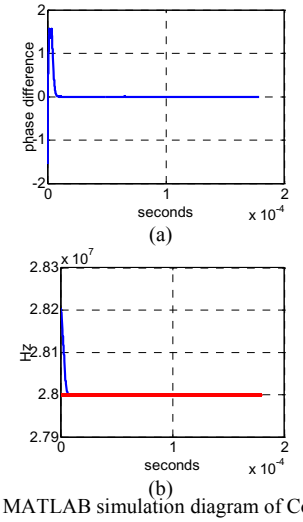

Figure 6. The MATLAB simulation diagram of Costas loop

From figure 6(a), it can be seen that after about 0.01ms, the phase difference which is the output of the phase detector is almost 0, at about 0.057°. The result indicates that the loop is successfully locked. In figure 6(b), the red line denotes the actual carrier frequency; the blue line denotes the Costas loop tracking frequency. The simulation results show that at the beginning, there is a 200KHz frequency difference between two signals. When the loop successfully goes into the state of lock, the loop eliminates the frequency difference. It turned out that the loop can extract out of the synchronous carrier signal successfully.

B. Modelsim Simulation

Combining with the project application, Verilog HDL language is used in the system design and the simulation tool is Modelsim SE 6.5. Then the FPGA Virtex5 series chip of Xilinx Company is used to implement the design. Figure 7 shows the Costas loop simulation in Modelsim.

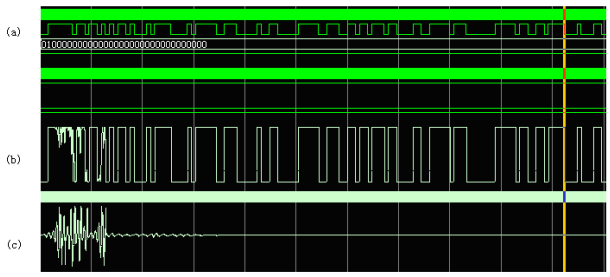

Figure 7. The Modelsim simulation diagram of Costas loop

Where figure (a) is the sent baseband signal. Figure (b) is the In-phase channel output signal of Costas loop, that is, the recovery of baseband signal in the receiver. Figure (c) is the output of loop filter. The simulation results show that, the Costas loop can be succeed to the state of lock. When the loop is locked, the receiver can correctly recover the baseband signal.

V. CONCLUSION

This paper has described an improved Costas loop, and has completed the design of every module, including NCO, integration and accumulators, arctangent phase detector and loop filter. Integration and accumulators is used to realize low-pass filter. The design is very simple and the operational efficiency is higher. The phase detector module uses the arctangent phase detector, which the accuracy of the phase is higher and the real-time is better. Loop filter is the most important part in the Costas loop. The paper took advantage of the second-order loop filter structure which is relatively simple and stable. The simulation results of MATLAB and Modelsim show that the tracking performance of the Costas loop is good and the design is rational. The loop can achieve the carrier tracking well and it can be directly applied to software radio digital receiver.

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