Design and Implementation of the BPSK Modem Based on Software Defined Radio

Zhongjun Zhao
Electronics Engineering Colleges
Heilong Jiang University
Harbin, China
zhaozhongjun715@163.com

Yongliang Shen
Electronics Engineering Colleges
Heilong Jiang University
Harbin, China
shen-yl@163.com

Yuan Bai
Electronics Engineering Colleges
Heilong Jiang University
Harbin, China
heidabaiyuan@163.com

***Abstract*— The BPSK modulation and demodulation algorithm is designed and implemented of software defined radio (SDR) transceiver system in this paper. The paper uses a Costas loop to achieve carrier synchronization when the BPSK demodulator is designed. And the loop realize the purpose of phase detection using the more accurate and fewer hardware resources occupy arc tangent phase detector. Firstly, the BPSK modulation and demodulation algorithm is simulated on the plat of MATLAB, in order to prove the feasibility and superiority of the proposed design. Then the design is implemented and tested using field programmable gate arrays (FPGA). The test result indicates the system has strong versatility, interchangeability and portability. It overcomes the system shortcomings of traditional analog circuit, such as circuit complex, bulky, high cost and poor stability and so on. Therefore, the system has a high value.**

Keywords— Software Defined Radio (SDR), Costas loop, Carrier synchronization, FPGA

I. INTRODUCTION

Software defined radio [1] is a new communication system architecture in the field of wireless communications. It has played a huge role in guiding the development of communication systems. Its core idea is take open, standardized, the modular hardware as the general platform, by loading different software on the hardware platform to realize the flexible configuration of the wireless capabilities, such as the working frequency band, modulation and demodulation, channel access methods and so on. Digital signal processing is a key technology for the software defined radio hardware platform. However, digital signal processing (DSP) can only process the digital signal. Therefore, the modulation and demodulation technology has become the core of SDR technology research. That is, the software of the modulation and demodulation is the key of the SDR implementation of open and versatile.

Binary phase shift keying (BPSK) has high spectrum efficiency, good spectral characteristics, strong anti-interference performance, faster transfer rates, and other prominent features. So BPSK is one of the main modulation modes of SDR system. The conventional digital modulation and demodulation are done using a dedicated chip. So its flexibility has been greatly restricted. With the rapid development of the integrated circuit manufacturing technology and the software defined radio technology, it will become the development trend of mobile communications to use the digital programmable devices to achieve the digital modem and baseband signal processing.

FPGA has both high speed processing capability as Application Specific Integrated Circuit (ASIC) and good reconfigurable performance [2]. Moreover the development cost is low, and the development cycle is short, so the superiority is extremely obvious. This article is based on software defined radio technology, using high-performance FPGA to build a common hardware platform. Through a dynamic configuration of FPGA, the BPSK modulation demodulation is realized on FPGA. Among them, the principle of demodulator is a Costas loop [3] and using arc tangent phase detector to achieve phase. Conventional Costas loop phase detector makes use of multiplier phase detector to achieve the function of phase detection. It is an approximate algorithm, that is, the true value of phase difference is approximated by the sine of the phase difference. Thus the error of the phase detect results will be relatively large. In addition, multiplier phase detector implemented in FPGA, it will consume a lot of hardware resources. The result of arc tangent phase detector is the value of phase difference, so the accuracy of the phase is higher. In the FPGA implementation, the arc tangent algorithm can be implemented using Coordinated Rotation Digital Computer (CORDIC) algorithm, which only needs simple shift and addition operations. Therefore, it is relatively easy to achieve. And relative to multiplier phase detector, the arc tangent phase detector takes less hardware resources. As a result, the paper uses arc tangent phase detector take the place of the traditional multiplier phase detector to implement the function of phase detection.

II. THE DESIGN OF THE BPSK MODULATION

A. The Basic Principle of BPSK Modulation

BPSK is a simple one-dimensional (1D) modulation scheme that the phase of carrier sinusoidal signal changes abruptly by 180° or π radian for every transition of modulating binary sequence (input bit) [4]. That is, binary digital baseband signals 0 and 1 respectively use the coherent modulation 0 and π-phase of the carrier wave to represent. The relation can be expressed as follows:

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$$s(t) = \left[\sum_{n=-\infty}^{\infty} a_n g_T(t - nT_b) \right] \cos(\omega_i t + \theta_i) \qquad (1)$$

Where $\{a_n\}$ is the bipolar sequence of binary digits. That is, the input bit with value of '0' or '1' is mapped to symbol with gain of −1 or +1 respectively through level converter. T_b is binary symbol interval. $g_T(t)$ is baseband transmit shaping filter impulse response which typically have a raised cosine characteristic. ω_i is the carrier frequency of modulation and θ_i is the starting phase of the modulated carrier.

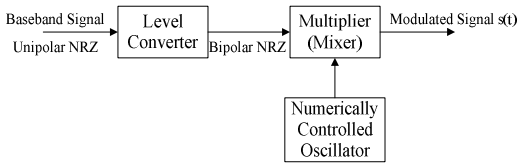


Figure 1. Diagram of BPSK Modulation

B. The FPGA Implementation of BPSK Modulator

According to the principle of BPSK modulator, the general block diagram for BPSK modulator designed in this paper as shown in Figure 2. It is mainly made up of digital controlled oscillator (NCO), phase inverter and alternative selector with control-side.

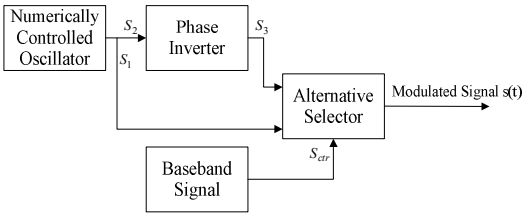


Figure 2. The Design of BPSK Modulation Implemented on FPGA

The goal of NCO [5] is to produce local carrier signal. The paper adopts the direct frequency synthesizer (DDS) technology. Its structure is shown in Figure 3.

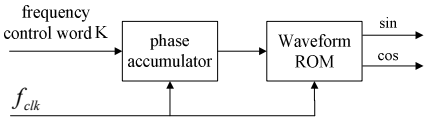


Figure 3. The structure of NCO

It can be seen from Figure 3 that NCO consists of one phase accumulator and one ROM waveform tables. The sine and cosine signals are generated by using the method of lookup table. And the .coe file for lookup table is generated by Matlab. The output frequency of NCO is defined as:

$$f_{out} = \frac{Kf_{clk}}{2^N}. \qquad (2)$$

Where f_{clk} is the system frequency, N is the bits number of phase accumulator, K is the frequency control word. The design uses the programmable NCO. By changing the frequency control word can change the output frequency of the NCO. Moreover it can be used to adjust the frequency of the carrier. Therefore, it has a great deal of flexibility.

The carrier signals generated by NCO are divided into two roads S_1 and S_2 . S_1 is directly transferred to alternative selector, S_2 is also sent to alternative selector after the phase inverter.

Phase inverter is used to change the carrier signal generated by NCO to π phase waveform. In FPGA implementations, it only requires a inverter. So the structure is very simple.

In the actual digital communication, the baseband signal is random. In FPGA implementation, the design uses m sequence generator to generate a pseudo-random sequence as the digital base band signal source. m sequence is the longest linear feedback shift register sequence for short. It is the longest cycle sequence generated by a linear feedback shift register. The system uses shift register overflowed (highest) and lowest bit to take exclusive-or (XOR) operation. Then the result is sent to the lowest level for the next cycle, resulting in m-sequence.

The control side of alternative selector with control-side is controlled by the input baseband signal. When the input digital signal is "0", the output signal is S_1. When the input digital signal is "1", the output signal is S_2.

III. THE DESIGN OF THE BPSK DEMODULATION

A. The basic principle of BPSK demodulation

In software defined radio system, demodulation uses digital coherent demodulation method generally. Because the error rate in coherent demodulation, detection threshold and the output signal to noise ratio (SNR) and so on have obvious advantages compared with non-coherent demodulation. The demodulator block diagram is shown in Figure 4.

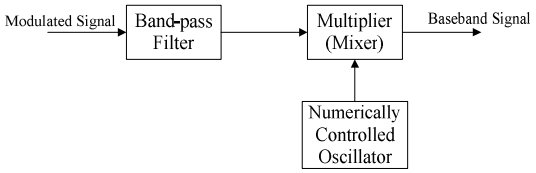


Figure 4. Diagram of BPSK Demodulation

Where, NCO generates local carrier signals. And only when the frequency and phase of local and sender carrier are the same, that is, when implementing carrier synchronization, we can achieve the correct demodulation. In practice, because the signal in the communication is influenced by some uncertain factors, there is certain some of the frequency offset and phase error between the received modulation signal and the local carrier. So the demodulation output would be severely distorted. Therefore, the implementation of carrier synchronization at the receiver side is the key to achieve proper coherent demodulation. Costas loop is a specialized method for BPSK demodulation. In order to realize the coherent demodulation correctly, the

paper uses the Costas phase-locked loop approach to achieve carrier synchronization. And the paper has improved the traditional phase module detection module of Costas loop, using arc tangent phase detector take the place of the traditional multiplier phase detector to implement the function of phase detection.

B. The FPGA implementation of carrier synchronization loop

The Digital Costas Loop is mainly made up of the following four modules: Numerically Controlled Oscillator (NCO), Low-pass Filter (LPF), Phase Detector (PD) and Loop Filter (LF). The schematic diagram is shown in figure 5.

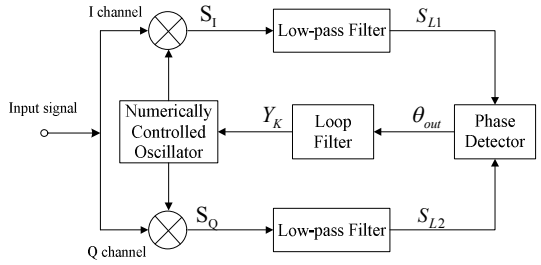


Figure 5. The block diagram of Costas loop

Where phase detector is used to extract the phase error signal between the input signal of the loop and the local carrier signal. Loop filter is to adjust and smooth the phase error. Then adjusted phase error is used to control NCO in order to generate the corresponding frequency carrier. When the carrier frequency and phase generated by NCO are coincident with the transmitter carrier frequency and phase, the demodulated signal can be extracted from the in-phase branch. The flowchart of the Costas loop extracting carrier synchronization and implementing BPSK demodulation is shown in Figure 6 below:

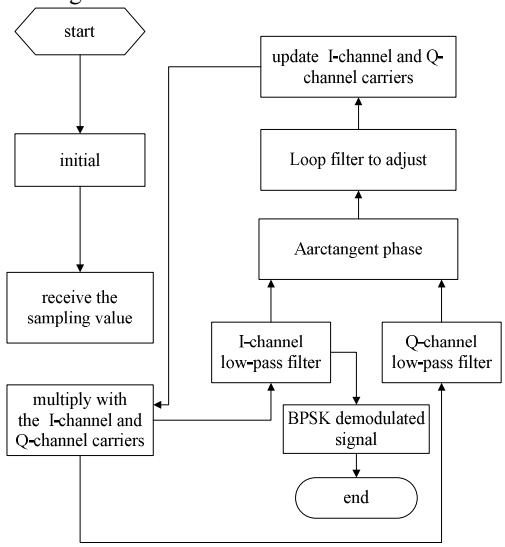


Figure 6. The flow diagram of BPSK demodulation implementation using Costas loop

The design of Phase discriminator (PD) module. Phase detector is a device which is used to compare the phase. Its performance directly decides on the wobble of Costas loop in the condition of white noise. According to the comparison for several common phase detecting methods in the literature [6], this may show that the arctangent phase detecting method is the only method which could keep linear in the half (+ 90 °) interval of input error range. And its output is the phase difference, not approximation, so the precision of phase detecting is higher.

In this paper, the CORDIC algorithm is used to achieve arctangent. CORDIC is an iteration algorithm of arithmetic calculations. The basic idea is to use a series of fixed and associated with the operation base angles deflect continually so as to keep close to the desired rotation angle. Traditionally, calculating trigonometric functions are generally used look-up table method, polynomial expansion method and similar method. But these methods can not take into account the speed, accuracy, simplicity and other requirements. CORDIC algorithm is designed to solve this problem. Starting from the algorithm itself, complex algorithms are decomposed into some of the basic algorithms which are easy to implement in hardware, such as addition, shift and so on. Thus these algorithms can be better realized in hardware. Therefore, the CORDIC algorithm is very suitable for application in large scale programmable logic devices.

The quantify model of CORDIC algorithm is adopted in this paper to realize the arctangent. The Specific implementation steps are as follows:

Step 1 Assign initial value, $x_0 = S_{L1}(t)$, $y_0 = S_{L2}(t)$, $z_0 = 0$, $i = 1$;

Step 2 If $z_i < 0$, then $d_i = -1$; otherwise, $d_i = +1$;

Step 3 Iteration as follows:

$$x_{i+1} = x_i - y_i d_i 2^{-i}$$

$$y_{i+1} = y_i + x_i d_i 2^{-i}$$

$$z_{i+1} = z_i - d_i \arctan(2^{-i})$$;

Step 4 i add 1, if $i < n$, you enters step 2 to continue to carry out, otherwise end the cyclic process.At the end of the calculation, the value of z_{i+1} is the output of phase detector, that is, the value of phase difference θ . Where n is the number of iterative calculation of CORDIC algorithm.

In the realization of hardware circuit, this paper uses the pipeline architecture. Every level pipeline only needs one coefficient memory, two shift registers and three adders. The structure is very simple. It only need simply add pipeline unit to improve its accuracy, so it has good extensibility. After the establishment of n clock time, at intervals of a clock will output a result of the operation. Therefore, the design can realize real-time processing of high-speed data. It is quite suitable for applying in SDR digital receiver.

The design of Loop filter (LF) module. Loop filter plays a key role in Costas loop [7]. Its main functions are filter out the high frequency phase detector leakage component and adjust the parameters of Costas loop. A variety of commonly used loop filter performance is analyzed in detail in [6]. Because the second-order digital loop filter in the case of direct current (DC) gain is infinite and the frequency offset is a constant, is still can be able to achieve a steady state. In addition, the implementation difficulty is appropriate and the performance is superior to other loops. So the system uses the second-order digital loop filter. The structure is shown in figure 8.

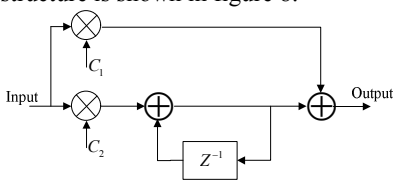


Figure 8. The frequency domain model of second-order digital loop filter

The Z domain transfer function of second-order digital loop filter can be expressed as:

$$F(z) = C_1 + C_2 \frac{1}{1 - z^{-1}} \tag{3}$$

The corresponding time-domain model is shown in Figure 9.

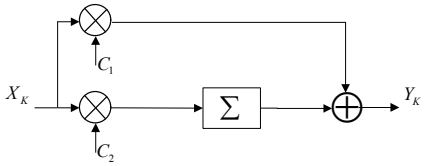


Figure 9. The time domain model of second-order digital loop filter

Then, the time domain difference equation is obtained as:

$$Y_K = C_1 X_K + C_2 \sum_{l=0}^{K} X_l \tag{4}$$

Where X_K is the input values of loop filter, that is, the value of phase difference of phase detector. C_1 and C_2 is the coefficients of loop filter. The two coefficients of the Costas loop is important and difficult. It determines the performance of all loop. C_1 and C_2 can be expressed as follows [8]:

$$C_1 = \frac{1}{K_0 K_d} \frac{8\xi\omega_n T}{4 + 4\xi\omega_n T + (\omega_n T)^2} \tag{5}$$

$$C_2 = \frac{1}{K_0 K_d} \frac{4(\omega_n T)^2}{4 + 4\xi\omega_n T + (\omega_n T)^2} \tag{6}$$

Where ξ is the damping coefficient. In the engineering, the general value of the ξ is selected 0.707. ω_n is the natural angular frequency of the loop. And it can be expressed as follows:

$$\omega_n = \frac{8\xi B_n}{4\xi^2 + 1} \tag{7}$$

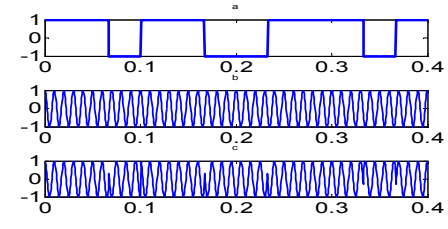
Where B_n is the equivalent noise bandwidth, and the general value meets with the relation $B_n \le 0.1 R_b$. Where R_b is the information data rate. $K_0 K_d$ is the loop gain.

From the expression (5) and (6), it can be seen that the different values of the loop equivalent noise bandwidth B_n are directly affect the value of C_1 and C_2. If the B_n is smaller, C_1 and C_2 are smaller, then the track time of the loop is longer and the noise immunity is better. Increase the bandwidth B_n can reduce the capture time, but the filtering performance will decline. Therefore, in the actual project, you need to select the appropriate values C_1 and C_2 based on your specific project so as to meet the system requirements.

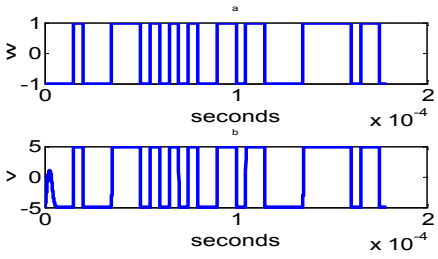
IV. Simulation and Analysis

A. MATLAB Simulation

In order to verify the feasibility of this system, the paper uses MATLAB to realize the simulation for the designed BPSK modem improved Costas loop. First of all, the paper makes the simulation of a BPSK modulator. If the carrier frequency is too large, too dense wave is not easy to observe the results. Therefore, the selected carrier frequency in this paper is 100Hz and the baseband signal frequency is 30Hz. The simulation result is shown in Figure 9 (a). And then the paper makes the simulation of a BPSK demodulator. There is a 200KHz frequency difference between the local carrier of the receiver and the transmitter carrier. Through the adjustment of the Costas carrier synchronization loop, when the Costas loop is locked, the demodulator simulation result is shown in Figure 9 (b).



(a)



(b)

Figure 9. The MATLAB simulation diagram of BPSK modem

In the figure (a), graph a shows randomly generated baseband signal, graph b is the carrier signal generated by NCO, graph c shows BPSK modulated waveform. From figure (a), it is can be seen that when the polarity of the baseband signals change, the modulator can achieve a good phase change, thus complete modulation.

In the figure (b), graph a shows the transmitted baseband signal, graph b shows the recovery baseband signal after a BPSK demodulator. From figure (b), it is can be seen that after 0.01ms, Costas loop eliminates the frequency difference and recovers the correct baseband signal.

B. Modelsim Simulation

The system uses Verilog HDL language to complete the design and the simulation tool is Modelsim SE 6.5 [9]. Then the FPGA Virtex5 series chip of Xilinx Company is used to implement the design. Figure 10 shows the BPSK modem simulation in Modelsim.

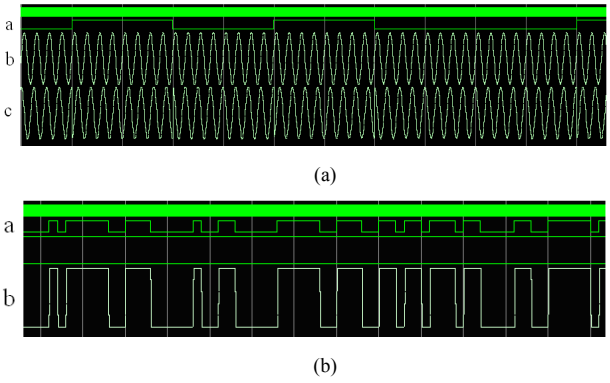


Figure 10. The Modelsim simulation diagram of BPSK modem

In the figure (a), graph a shows randomly generated baseband signal, graph b is the carrier signal generated by NCO, graph c shows BPSK modulated waveform. In the figure (b), graph a shows the transmitted baseband signal, graph b shows the recovery baseband signal after a BPSK demodulator. The simulation results show that, the design of BPSK modem on the FPGA platform can achieve the proper modulation and demodulation.

V. CONCLUSION

In SDR communication system, modulation and demodulation technology is the core content of SDR technology. This paper researched the BPSK modulation and demodulation algorithm based on software defined radio. Algorithm was verified by MATLAB software, used the Verilog hardware description language for hardware implementation. And the paper detailed on how to implement a BPSK modem on the FPGA platform. Among the system, the demodulation part used the Costas loop to realize carrier synchronization. Moreover the loop used the high accuracy arctangent phase detector and the good stability of second-order digital loop filter. Thus the Costas loop takes up fewer hardware resources as a whole, and the stability is better. The simulation results show that the loop can good to eliminate frequency offset, thereby complete the demodulation correctly. Because the system is completed on the FPGA platform, so the system has great versatility and portability. Therefore, it is applicable to SDR for high speed and high precision digital modulation and demodulation.

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