Single-Step Module for the 65C02

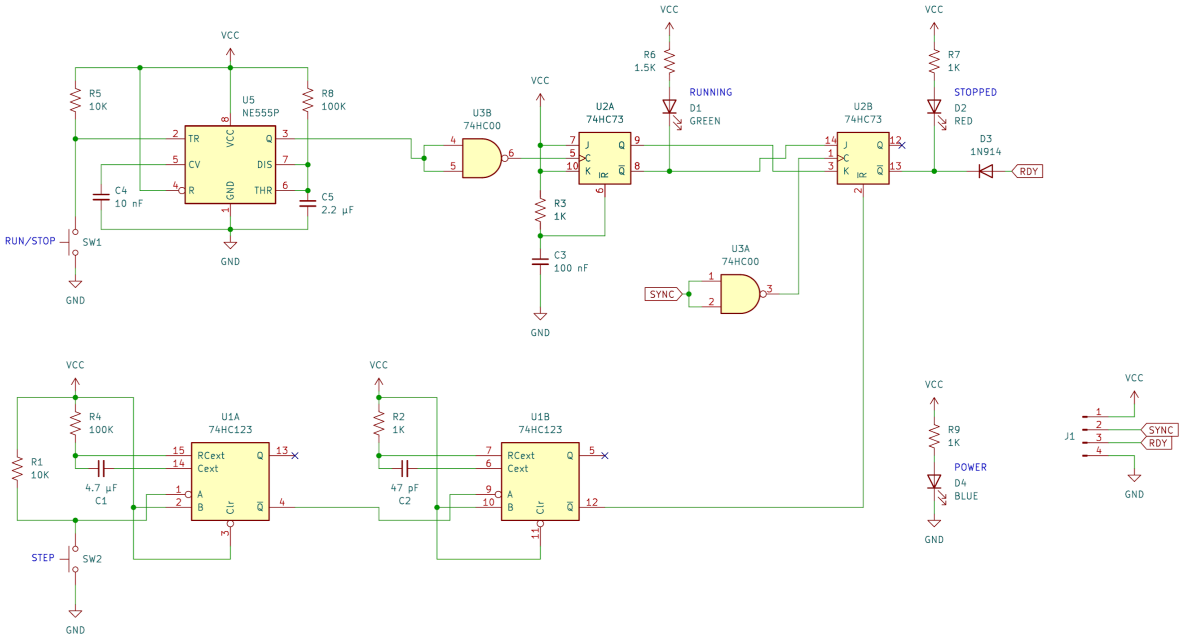
The WDC 65C02 processor provides a SYNC signal that can be used in conjunction with the RDY signal to single step the processor. From the relevant section of the processor data sheet, here's a brief explanation of the mechanism.

> ***3.13 SYNChronize with OpCode fetch (SYNC)***
> *The OpCode fetch cycle of the microprocessor instruction is indicated with SYNC high. The SYNC output is provided to identify those cycles during which the microprocessor is fetching an OpCode. The SYNC line goes high during the clock cycle of an OpCode fetch and stays high for the entire cycle. If the RDY line is pulled low during the clock cycle in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.*

This document describes a single step module that makes use of the facility described above.

The user interface for the single step module consists of two momentary contact buttons, along with LEDs to indicate the state of the controls. One of the buttons (RUN/STOP) is used to toggle between the free running mode and single step mode. The other button (STEP) is used to step to the next instruction when operating in single step mode. The buttons are easily distinguished by size — the larger button is the STEP function. A blue LED provides power on status. A green LED indicates that the processor is in free run mode. A red LED indicates that the processor is stopped and will resume when the STEP button is pressed.

The module is connected to the system under test via a pin header (J1) that provides VCC and ground, as well as the processor's SYNC and RDY signals.



In the circuit, an NE555 timer is used to debounce the RUN/STOP button. As configured, it outputs a positive-going pulse with a minimum duration of about 250 milliseconds, which prevents the button from triggering multiple times over a short interval.

The output of the NE555 is inverted using a NAND gate (U3B) and the resulting signal is used to clock a JK-type flip-flop (U2A) configured in toggle mode. When this flip-flop contains a logic one, the processor will run freely. A logic zero in this flip-flop will cause the processor to enter single-step mode. The button simply toggles the flip-flop between these two states which correspond to the RUN and STOP modes.

The output of flip-flop U2A provides the input to a second JK flip-flop (U2B) that is used to control the state of the processor's RDY input. The (inverted) SYNC signal from the processor clocks the input to this flip-flop. On the rising edge of SYNC, if the J input is high (STOP mode) the RDY signal will be pulled low, causing the processor to stop on the next rising edge of the system clock. When the K input is high (RUN mode) the RDY signal is never driven low.

Note that diode D3 prevents flip-flop U2B from driving RDY high. This ensures that the single-step circuit will not interfere with other peripherals that need to use the RDY signal. It also implies that RDY must be pulled up to VCC through a resistor as recommended in the processor datasheet.

The rest of the circuit is responsible for allowing execution to continue for a single instruction in single-step mode. This is accomplished using the asynchronous reset input of flip-flop U2B. When the reset input is triggered, the inverted Q output of the flip-flop goes high. Assuming that no other device is driving RDY low, the pull-up resistor on the processor's RDY input will cause RDY to rise. The processor will observe the ready state at the next rising edge of the system clock and will continue execution at the next falling edge.

The critical timing consideration is the length of the pulse used to reset flip-flop U2B. It must be shorter than the minimum interval of time after RDY goes high before the SYNC signal could rise again. The worst case is a sequence of two consecutive single byte instructions. In this case, the SYNC signal will go high on the next falling edge of the system clock after RDY has been observed in the high state — i.e. this interval will be one half of the clock period.

One unit of a 74HC123 dual monostable multivibrator (U1A) is used to debounce the STEP button. The output is a negative going pulse of about 210 milliseconds duration, sufficient to prevent the button from triggering repeated short pulses. The output of U1A provides the trigger input to a second monostable timer (U1B) configured to produce a negative going pulse of approximately 200 nanoseconds duration. The 74HC123 was selected for this application because the output pulse width is not extended by the input pulse width.

The output of U1B is used as the reset input of flip-flop U2B. Assuming that the system clock is no greater than 2 MHz, the duration of the reset pulse is less than one quarter of the system clock and therefore the reset action will be completed significantly prior to the next point in time at which the SYNC signal could rise.