

SBOS073B-SEPTEMBER 1997-REVISED NOVEMBER 2007

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

	VALUE	UNIT
Supply Voltage	5.5	V
Signal Input Terminals		
Voltage ⁽²⁾	(V ₋) – 0.5 to (V ₊) + 0.5	V
Current ⁽²⁾	10	mA
Output Short-Circuit ⁽³⁾	Continuous	
Operating Temperature	–55 to +125	°C
Storage Temperature	–55 to +125	°C
Junction Temperature	+150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
- (3) Short-circuit to ground, one amplifier per package.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER ⁽²⁾	TRANSPORT MEDIA, QUANTITY
Single						
OPA340NA	5-Lead SOT-23-5	DBV	–40°C to +85°C	A40	OPA340NA/250 OPA340NA/3K	Tape and Reel
OPA340PA	8-Pin DIP	P	–40°C to +85°C	OPA340PA	OPA340PA	Rails
OPA340UA	SO-8 Surface-Mount	D	–40°C to +85°C	OPA340UA	OPA340UA OPA340UA/2K5	Rails ⁽³⁾
Dual						
OPA2340EA	MSOP-8 Surface-Mount	DGK	–40°C to +85°C	A40A	OPA2340EA/250 OPA2340EA/2K5	Tape and Reel
OPA2340PA	8-Pin DIP	P	–40°C to +85°C	OPA2340PA	OPA2340PA	Rails
OPA2340UA	SO-8 Surface-Mount	D	–40°C to +85°C	OPA2340UA	OPA2340UA	Rails ⁽³⁾
Quad						
OPA4340EA	SSOP-16 Surface-Mount	DBQ	–40°C to +85°C	OPA4340EA	OPA4340EA/250 OPA4340EA/2K5	Tape and Reel
OPA4340UA	SO-14 Surface Mount	D	–40°C to +85°C	OPA4340UA	OPA4340UA OPA4340UA/2K5	Rails ⁽³⁾

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Models with /250, /2500, and /3K are available only in tape and reel in the quantities indicated (e.g., /250 indicates 250 devices per reel). Ordering 3000 pieces of OPA340NA/3K will get a single 3000 piece tape and reel.
- (3) SO-8 and SO-14 models also available in tape and reel.

ELECTRICAL CHARACTERISTICS: $V_S = 2.7V$ to $5V$

BOLDFACE limits apply over the specified temperature range, $T_A = -40^{\circ}C$ to $+85^{\circ}C$. $V_S = 5V$.

At $T_A = +25^{\circ}C$, $R_L = 10k\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER	CONDITIONS	OPA340NA, PA, UA OPA2340EA, PA, UA OPA4340EA, UA			UNIT
		MIN	TYP ⁽¹⁾	MAX	
OFFSET VOLTAGE					
Input Offset Voltage V_{OS}	$V_S = 5V$		± 150	± 500	μV
vs Temperature dV_{OS}/dT			± 2.5		$\mu V/^{\circ}C$
vs Power Supply PSRR	$V_S = 2.7V$ to $5.5V$, $V_{CM} = 0V$		30	120	$\mu V/V$
Over Temperature	$V_S = 2.7V$ to $5.5V$, $V_{CM} = 0V$			120	$\mu V/V$
Channel Separation, dc			0.2		$\mu V/V$
INPUT BIAS CURRENT					
Input Bias Current I_B			± 0.2	± 10	pA
Over Temperature				± 60	pA
Input Offset Current I_{OS}			± 0.2	± 10	pA
NOISE					
Input Voltage Noise, $f = 0.1kHz$ to $50kHz$			8		μV_{rms}
Input Voltage Noise Density, $f = 1kHz$ e_n			25		nV/\sqrt{Hz}
Current Noise Density, $f = 1kHz$ i_n			3		fA/\sqrt{Hz}
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range V_{CM}		-0.3		$(V+) + 0.3$	V
Common-Mode Rejection Ratio CMRR	$-0.3V < V_{CM} < (V+) - 1.8V$	80	92		dB
	$V_S = 5V$, $-0.3V < V_{CM} < 5.3V$	70	84		dB
	$V_S = 2.7V$, $-0.3V < V_{CM} < 3V$	66	80		dB
INPUT IMPEDANCE					
Differential			$10^{13} \parallel 3$		$\Omega \parallel pF$
Common-Mode			$10^{13} \parallel 6$		$\Omega \parallel pF$
OPEN-LOOP GAIN					
Open-Loop Voltage Gain A_{OL}	$R_L = 100k\Omega$, $5mV < V_O < (V+) - 5mV$	106	124		dB
Over Temperature	$R_L = 100k\Omega$, $5mV < V_O < (V+) - 5mV$	106			dB
	$R_L = 10k\Omega$, $5mV < V_O < (V+) - 50mV$	100	120		dB
Over Temperature	$R_L = 10k\Omega$, $5mV < V_O < (V+) - 50mV$	100			dB
	$R_L = 2k\Omega$, $200mV < V_O < (V+) - 200mV$	94	114		dB
Over Temperature	$R_L = 2k\Omega$, $200mV < V_O < (V+) - 200mV$	94			dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product GBW	$G = 1$		5.5		MHz
Slew Rate SR	$V_S = 5V$, $G = 1$, $C_L = 100pF$		6		$V/\mu s$
Settling Time, 0.1%	$V_S = 5V$, 2V Step, $C_L = 100pF$		1		μs
Settling Time, 0.01%	$V_S = 5V$, 2V Step, $C_L = 100pF$		1.6		μs
Overload Recovery Time	$V_{IN} \bullet G = V_S$		0.2		μs
Total Harmonic Distortion + Noise THD+N	$V_S = 5V$, $V_O = 3V_{pp}^{(2)}$, $G = 1$, $f = 1kHz$		0.0007		%

(1) $V_S = +5V$.

(2) $V_{OUT} = 0.25V$ to $3.25V$.

ELECTRICAL CHARACTERISTICS: $V_S = 2.7V$ to $5V$ (continued)

BOLDFACE limits apply over the specified temperature range, $T_A = -40^{\circ}C$ to $+85^{\circ}C$. $V_S = 5V$.

At $T_A = +25^{\circ}C$, $R_L = 10k\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER	CONDITIONS	OPA340NA, PA, UA OPA2340EA, PA, UA OPA4340EA, UA			UNIT
		MIN	TYP ⁽¹⁾	MAX	
OUTPUT					
Voltage Output Swing from Rail ⁽⁴⁾	$R_L = 100k\Omega$, $A_{OL} \geq 106dB$		1	5	mV
Over Temperature	$R_L = 100k\Omega$, $A_{OL} \geq 106dB$			5	mV
	$R_L = 10k\Omega$, $A_{OL} \geq 100dB$		10	50	mV
Over Temperature	$R_L = 10k\Omega$, $A_{OL} \geq 100dB$			50	mV
	$R_L = 2k\Omega$, $A_{OL} \geq 94dB$		40	200	mV
Over Temperature	$R_L = 2k\Omega$, $A_{OL} \geq 94dB$			200	mV
Short-Circuit Current I_{SC}			± 50		mA
Capacitive Load Drive C_{LOAD}		See Typical Characteristics			
POWER SUPPLY					
Specified Voltage Range V_S		2.7		5	V
Operating Voltage Range			2.5 to 5.5		V
Quiescent Current (per amplifier) I_Q	$I_O = 0$, $V_S = +5V$		750	950	μA
Over Temperature	$I_O = 0$, $V_S = +5V$			1100	μA
TEMPERATURE RANGE					
Specified Range		-40		+85	$^{\circ}C$
Operating Range		-55		+125	$^{\circ}C$
Storage Range		-55		+125	$^{\circ}C$
Thermal Resistance θ_{JA}					
SOT23-5 Surface Mount			200		$^{\circ}C/W$
MSOP-8 Surface Mount			150		$^{\circ}C/W$
SO-8 Surface Mount			150		$^{\circ}C/W$
DIP-8 Surface Mount			100		$^{\circ}C/W$
SSOP-16 Surface Mount			100		$^{\circ}C/W$
SO-14 Surface Mount			100		$^{\circ}C/W$

(3) $V_S = +5V$.

(4) Output voltage swings are measured between the output and power supply rails.

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, and $R_L = 10\text{k}\Omega$ connected to $V_S/2$, unless otherwise noted.

**OPEN-LOOP GAIN/PHASE
vs FREQUENCY**

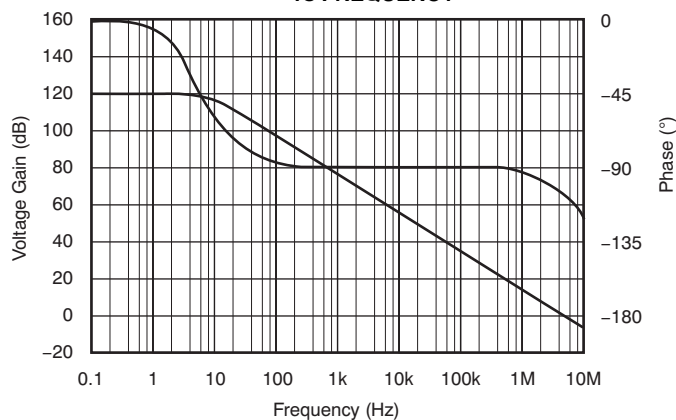


Figure 1.

**POWER-SUPPLY AND COMMON-MODE REJECTION
vs FREQUENCY**

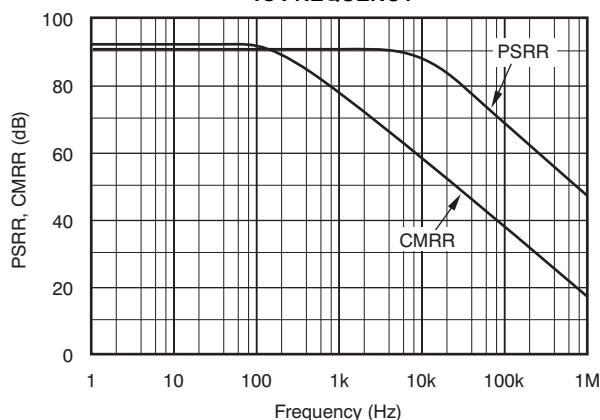


Figure 2.

**INPUT VOLTAGE AND CURRENT NOISE
SPECTRAL DENSITY vs FREQUENCY**

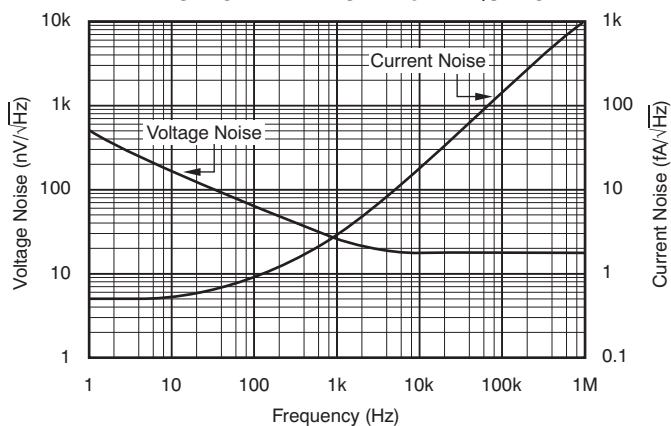


Figure 3.

CHANNEL SEPARATION vs FREQUENCY

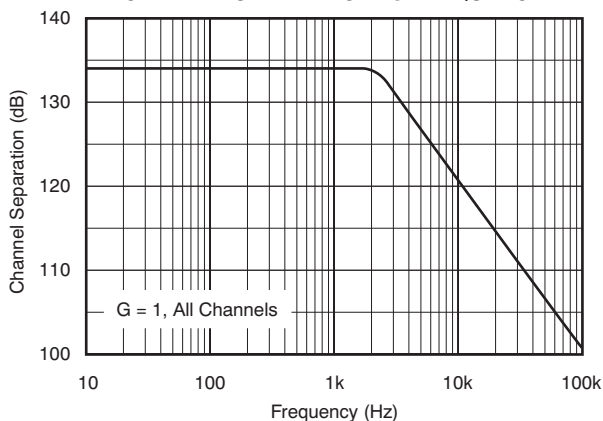


Figure 4.

**TOTAL HARMONIC DISTORTION + NOISE
vs FREQUENCY**

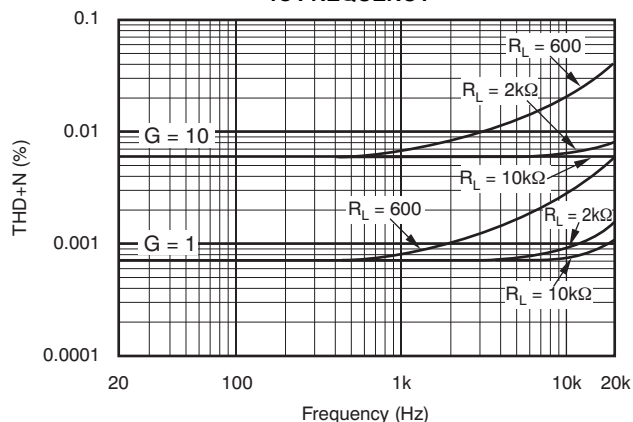


Figure 5.

**CLOSED-LOOP OUTPUT IMPEDANCE
vs FREQUENCY**

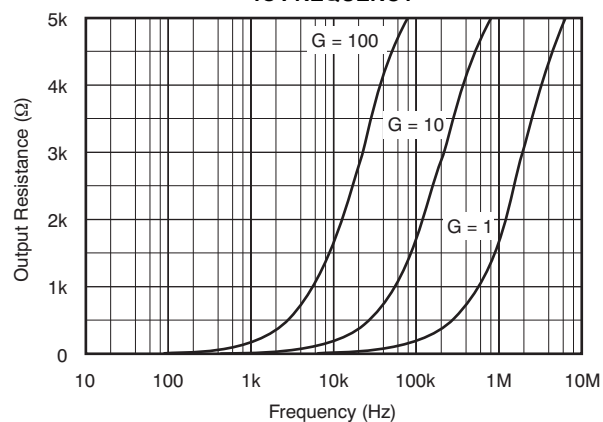


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, and $R_L = 10\text{k}\Omega$ connected to $V_S/2$, unless otherwise noted.

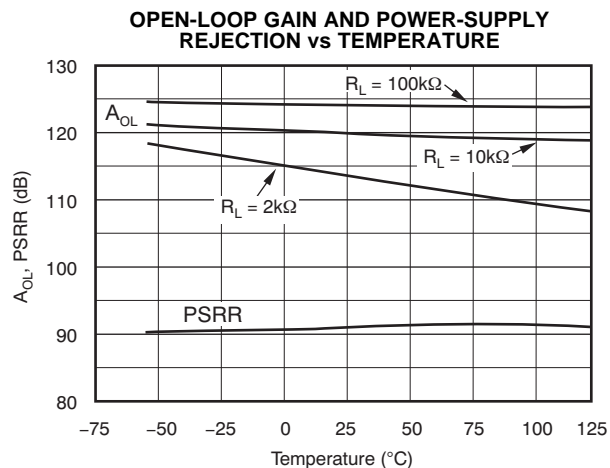


Figure 7.

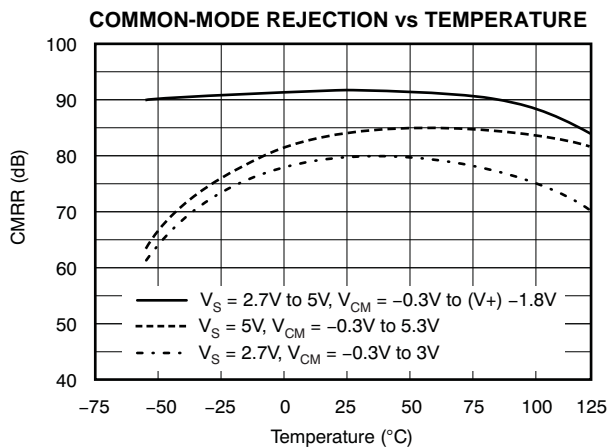


Figure 8.

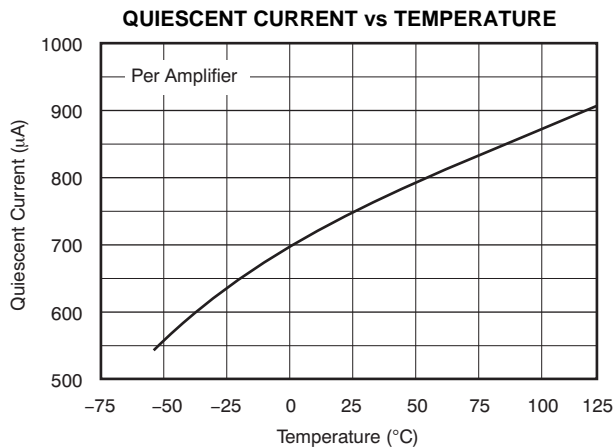


Figure 9.

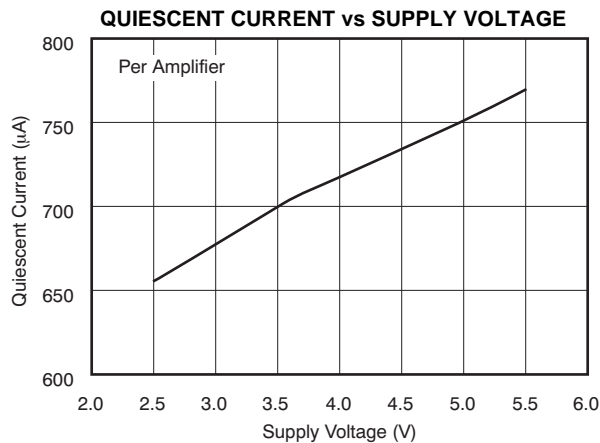


Figure 10.

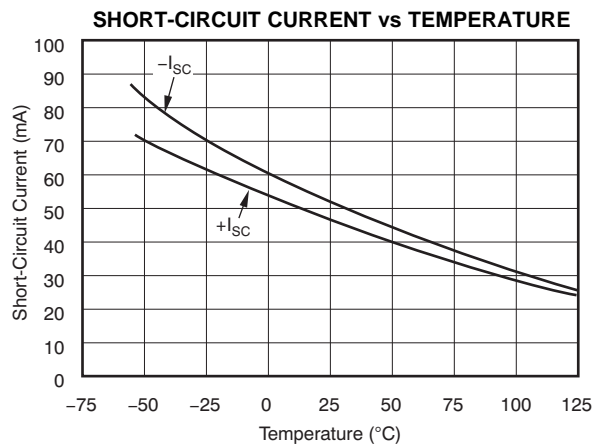


Figure 11.

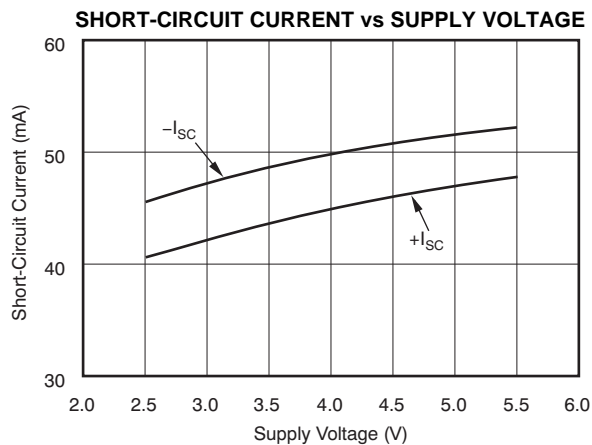


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, and $R_L = 10\text{k}\Omega$ connected to $V_S/2$, unless otherwise noted.

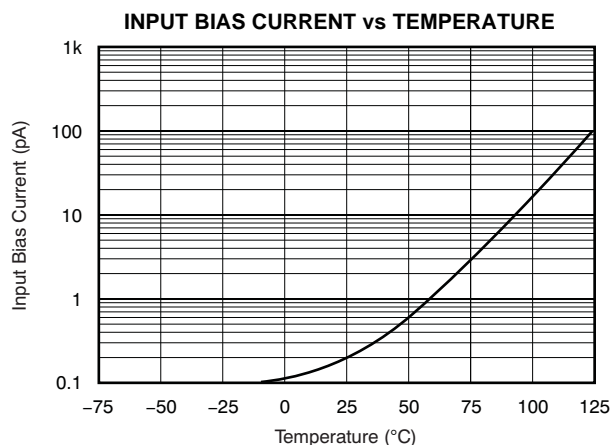


Figure 13.

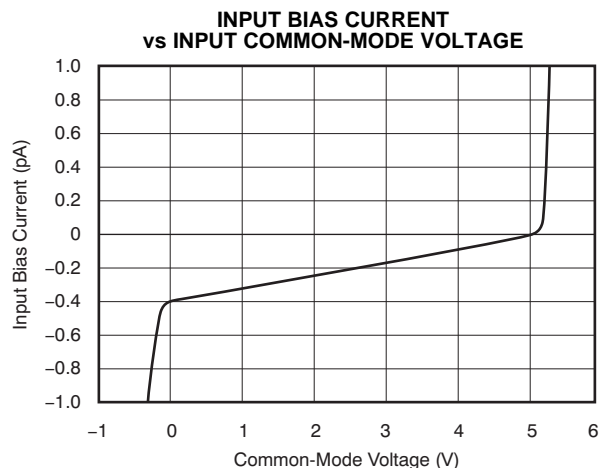


Figure 14.

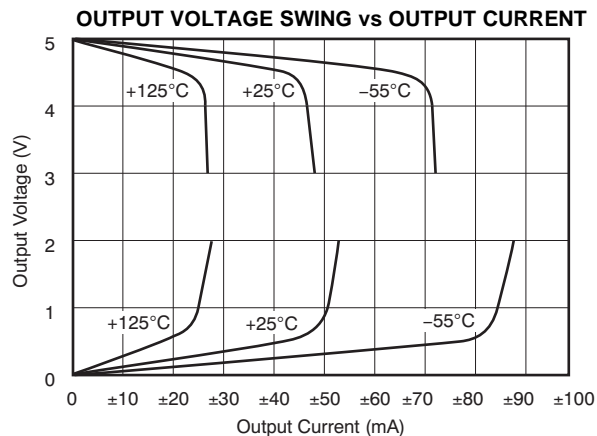


Figure 15.

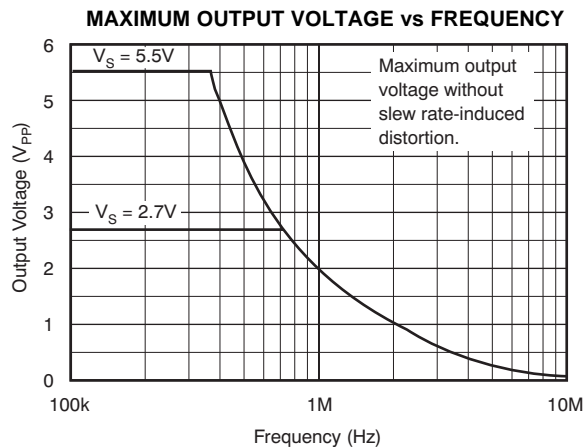


Figure 16.

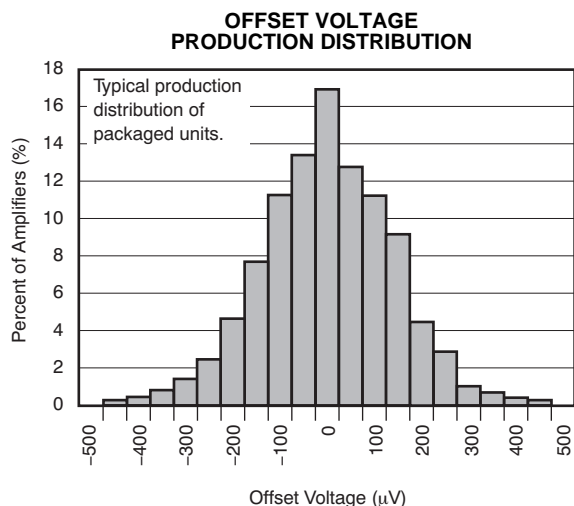


Figure 17.

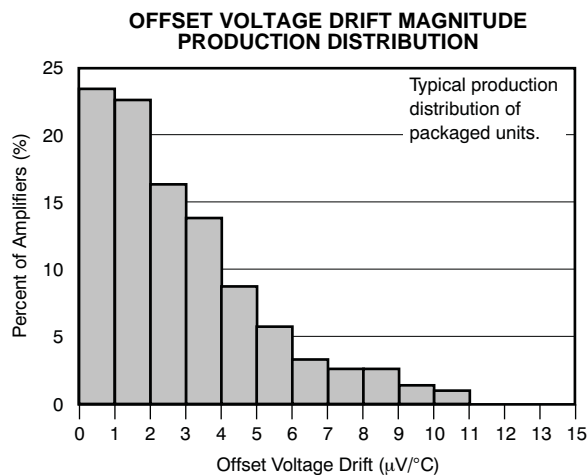


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, and $R_L = 10\text{k}\Omega$ connected to $V_S/2$, unless otherwise noted.

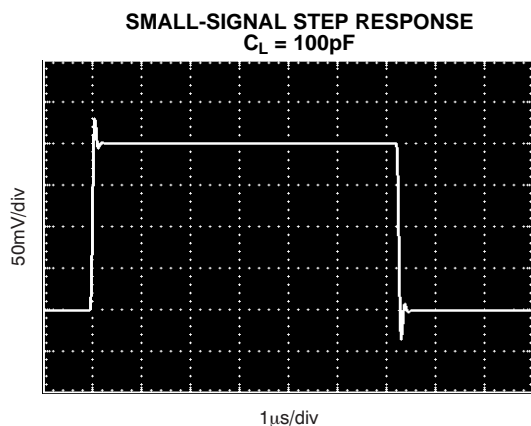


Figure 19.

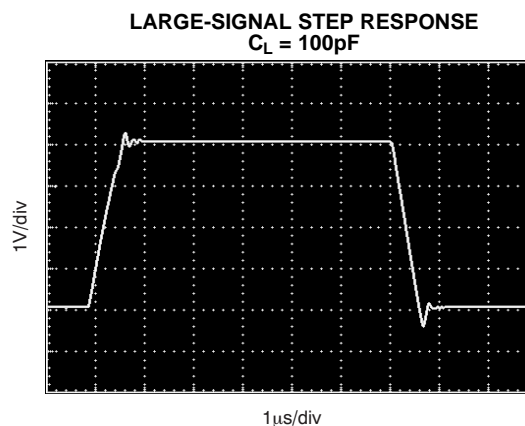


Figure 20.

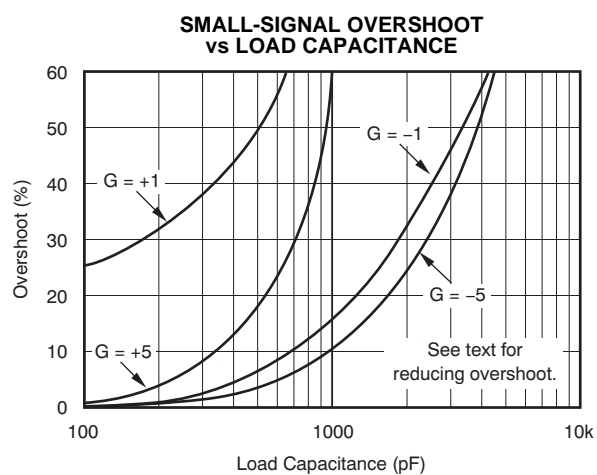


Figure 21.

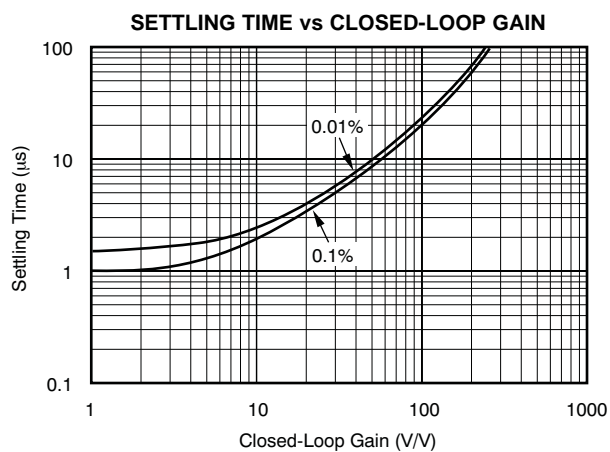


Figure 22.

APPLICATIONS INFORMATION

OPA340 series op amps are fabricated on a state-of-the-art, 0.6 micron CMOS process. They are unity-gain stable and suitable for a wide range of general-purpose applications. Rail-to-rail input/output make them ideal for driving sampling A/D converters. In addition, excellent ac performance makes them well-suited for audio applications. The class AB output stage is capable of driving 600Ω loads connected to any point between V+ and ground.

Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. Figure 23 shows the input and output waveforms for the OPA340 in unity-gain configuration. Operation is from a single +5V supply with a 10kΩ load connected to $V_S/2$. The input is a 5V_{PP} sinusoid. Output voltage is approximately 4.98V_{PP}.

Power-supply pins should be bypassed with 0.01μF ceramic capacitors.

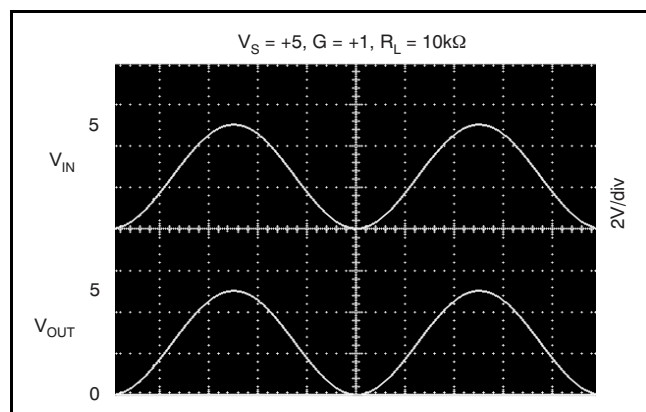


Figure 23. Rail-to-Rail Input and Output

OPERATING VOLTAGE

OPA340 series op amps are fully specified from +2.7V to +5V. However, supply voltage may range from +2.5V to +5.5V. Parameters are ensured over the specified supply range—a unique feature of the OPA340 series. In addition, many specifications apply

from –40°C to +85°C. Most behavior remains virtually unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltages or temperature are shown in the [Typical Characteristics](#).

RAIL-TO-RAIL INPUT

The input common-mode voltage range of the OPA340 series extends 500mV beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair (as shown in Figure 24). The N-channel pair is active for input voltages close to the positive rail, typically $(V+) - 1.3V$ to 500mV above the positive supply, while the P-channel pair is on for inputs from 500mV below the negative supply to approximately $(V+) - 1.3V$. There is a small transition region, typically $(V+) - 1.5V$ to $(V+) - 1.1V$, in which both pairs are on. This 400mV transition region can vary ±300mV with process variation. Thus, the transition region (both stages on) can range from $(V+) - 1.8V$ to $(V+) - 1.4V$ on the low end, up to $(V+) - 1.2V$ to $(V+) - 0.8V$ on the high end.

OPA340 series op amps are laser-trimmed to the reduce offset voltage difference between the N-channel and P-channel input stages, resulting in improved common-mode rejection and a smooth transition between the N-channel pair and the P-channel pair. However, within the 400mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage. Normally, input bias current is approximately 200fA; however, input voltages exceeding the power supplies by more than 500mV can cause excessive current to flow in or out of the input pins. Momentary voltages greater than 500mV beyond the power supply can be tolerated if the current on the input pins is limited to 10mA. This is easily accomplished with an input resistor, as shown in Figure 25. Many input signals are inherently current-limited to less than 10mA; therefore, a limiting resistor is not required.

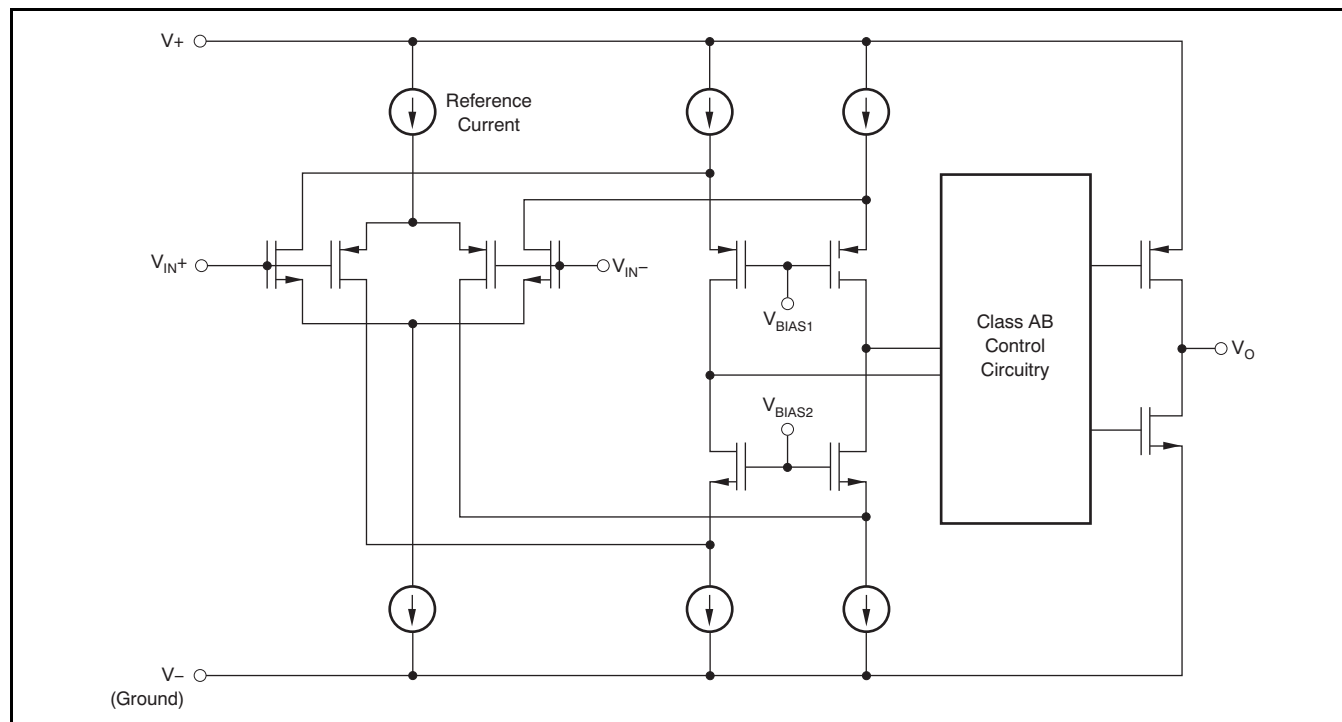


Figure 24. Simplified Schematic

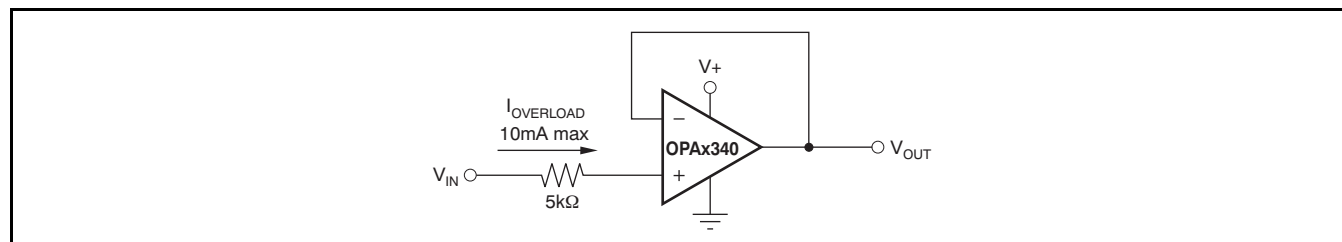


Figure 25. Input Current Protection for Voltages Exceeding the Supply Voltage

RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For light resistive loads ($> 50\text{k}\Omega$), the output voltage is typically a few millivolts from the supply rails. With moderate resistive loads ($2\text{k}\Omega$ to $50\text{k}\Omega$), the output can swing to within a few tens of millivolts from the supply rails and maintain high open-loop gain. See the typical characteristic curve [Output Voltage Swing vs Output Current](#).

CAPACITIVE LOAD AND STABILITY

OPA340 series op amps can drive a wide range of capacitive loads. However, all op amps under certain conditions may become unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An op amp in unity gain configuration is most susceptible to the effects of capacitive load. The capacitive load reacts with the op amp's output resistance, along with any additional load resistance, to create a pole in the small-signal response which degrades the phase margin. In unity gain, OPA340 series op amps perform well, with a pure capacitive load up to approximately 1000pF . Increasing gain enhances the amplifier's ability to drive more capacitance. See the typical performance curve [Small-Signal Overshoot vs Capacitive Load](#).

One method of improving capacitive load drive in the unity gain configuration is to insert a 10Ω to 20Ω resistor in series with the output, as shown in [Figure 26](#). This significantly reduces ringing with large capacitive loads. However, if there is a resistive load in parallel with the capacitive load, it creates a voltage divider introducing a dc error at the output and slightly reduces output swing. This error may be insignificant. For instance, with $R_L = 10k\Omega$ and $R_S = 20\Omega$, there is only about a 0.2% error at the output.

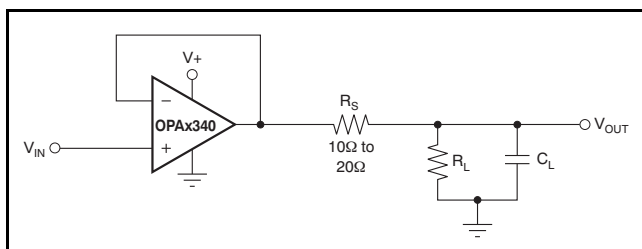


Figure 26. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive

DRIVING A/D CONVERTERS

OPA340 series op amps are optimized for driving medium speed (up to 100kHz) sampling A/D converters. However, they also offer excellent performance for higher speed converters. The OPA340 series provides an effective means of buffering the A/D's input capacitance and resulting charge injection while providing signal gain. [Figure 27](#) and [Figure 28](#) show the OPA340 driving an [ADS7816](#). The [ADS7816](#) is a 12-bit, micro-power sampling converter in the tiny MSOP-8 package. When used with the miniature package options of the OPA340 series, the combination is ideal for space-limited and low-power applications. For further information consult the [ADS7816 data sheet](#). With the OPA340 in a noninverting configuration, an RC network at the amplifier's output can be used to filter high-frequency noise in the signal (see [Figure 27](#)). In the inverting configuration, filtering may be accomplished with a capacitor across the feedback resistor (see [Figure 28](#)).

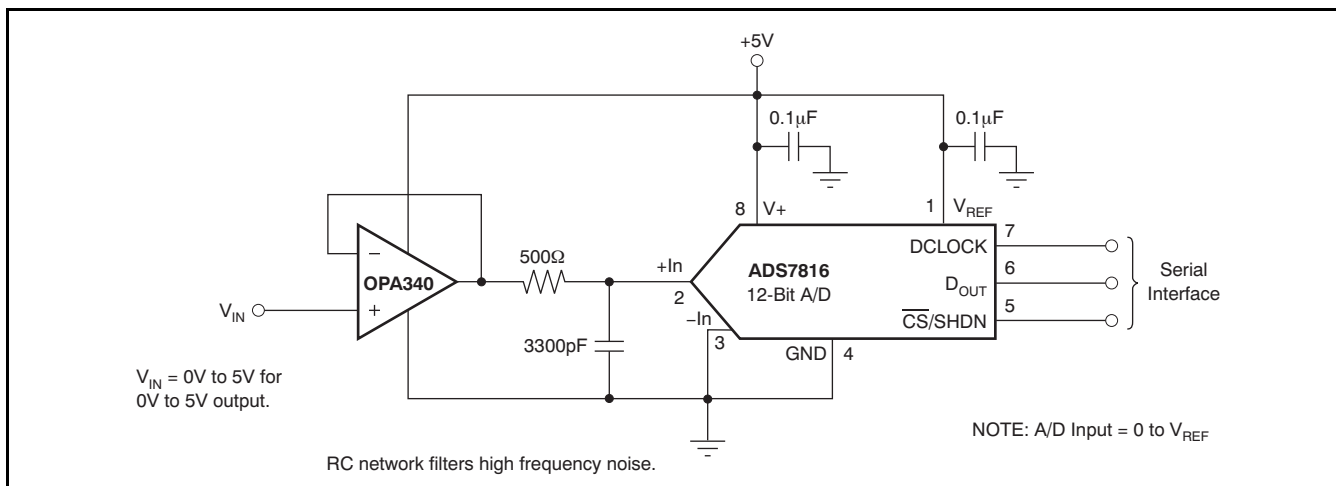


Figure 27. OPA340 in Noninverting Configuration Driving ADS7816

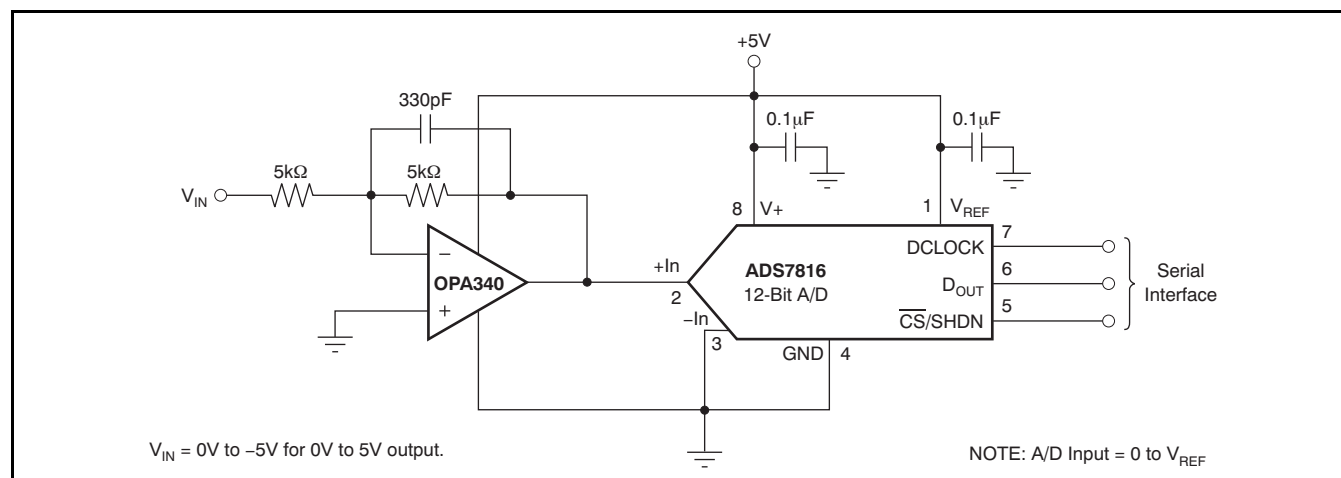


Figure 28. OPA340 in Inverting Configuration Driving ADS7816

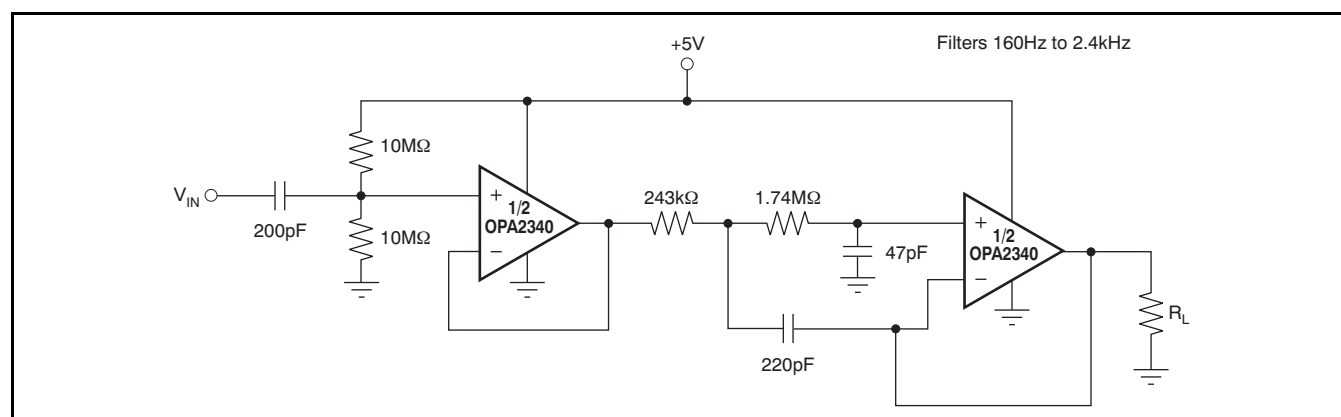


Figure 29. Speech Bandpass Filter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2340EA/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		A40A	Samples
OPA2340EA/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		A40A	Samples
OPA2340EA/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		A40A	Samples
OPA2340EA/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		A40A	Samples
OPA2340PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2340PA	Samples
OPA2340PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2340PA	Samples
OPA2340UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2340UA	Samples
OPA2340UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 2340UA	Samples
OPA2340UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		OPA 2340UA	Samples
OPA2340UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2340UA	Samples
OPA340NA/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A40	Samples
OPA340NA/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A40	Samples
OPA340NA/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A40	Samples
OPA340NA/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A40	Samples
OPA340PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA340PA	Samples
OPA340PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA340PA	Samples
OPA340UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 340UA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA340UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 340UA	Samples
OPA340UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 340UA	Samples
OPA340UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 340UA	Samples
OPA4340EA/250	ACTIVE	SSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4340EA	Samples
OPA4340EA/250G4	ACTIVE	SSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4340EA	Samples
OPA4340EA/2K5	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4340EA	Samples
OPA4340EA/2K5G4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4340EA	Samples
OPA4340PA	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	-40 to 85		
OPA4340UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4340UA	Samples
OPA4340UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4340UA	Samples
OPA4340UA/2K5G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4340UA	Samples
OPA4340UAG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA4340UA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF OPA340 :

- Enhanced Product: [OPA340-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2340EA/250	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2340EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA340NA/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA340NA/250	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA340NA/3K	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA340NA/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA4340EA/250	SSOP	DBQ	16	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4340EA/2K5	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4340UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2340EA/250	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2340EA/2K5	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA340NA/250	SOT-23	DBV	5	250	195.0	200.0	45.0
OPA340NA/250	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA340NA/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA340NA/3K	SOT-23	DBV	5	3000	195.0	200.0	45.0
OPA4340EA/250	SSOP	DBQ	16	250	210.0	185.0	35.0
OPA4340EA/2K5	SSOP	DBQ	16	2500	367.0	367.0	35.0
OPA4340UA/2K5	SOIC	D	14	2500	367.0	367.0	38.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

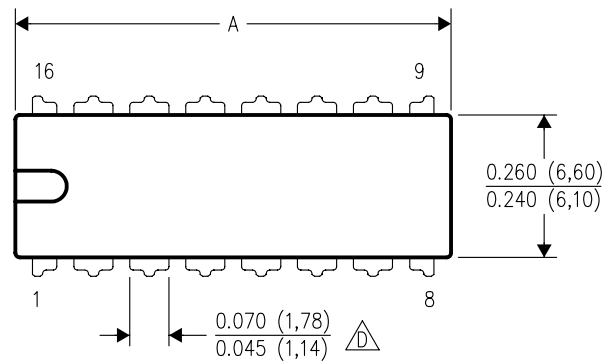


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

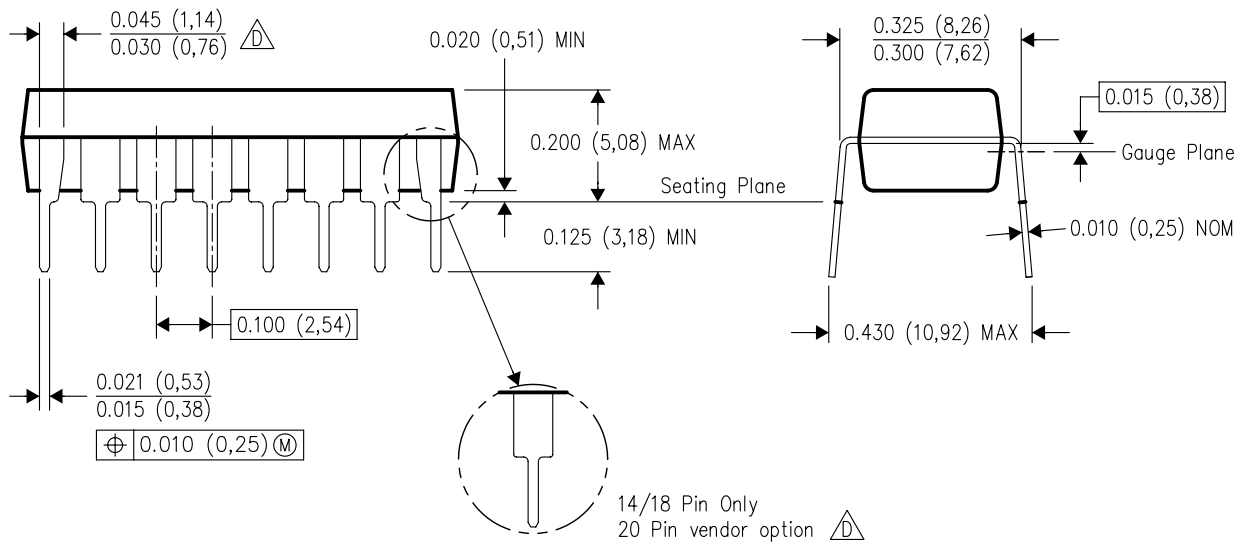
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



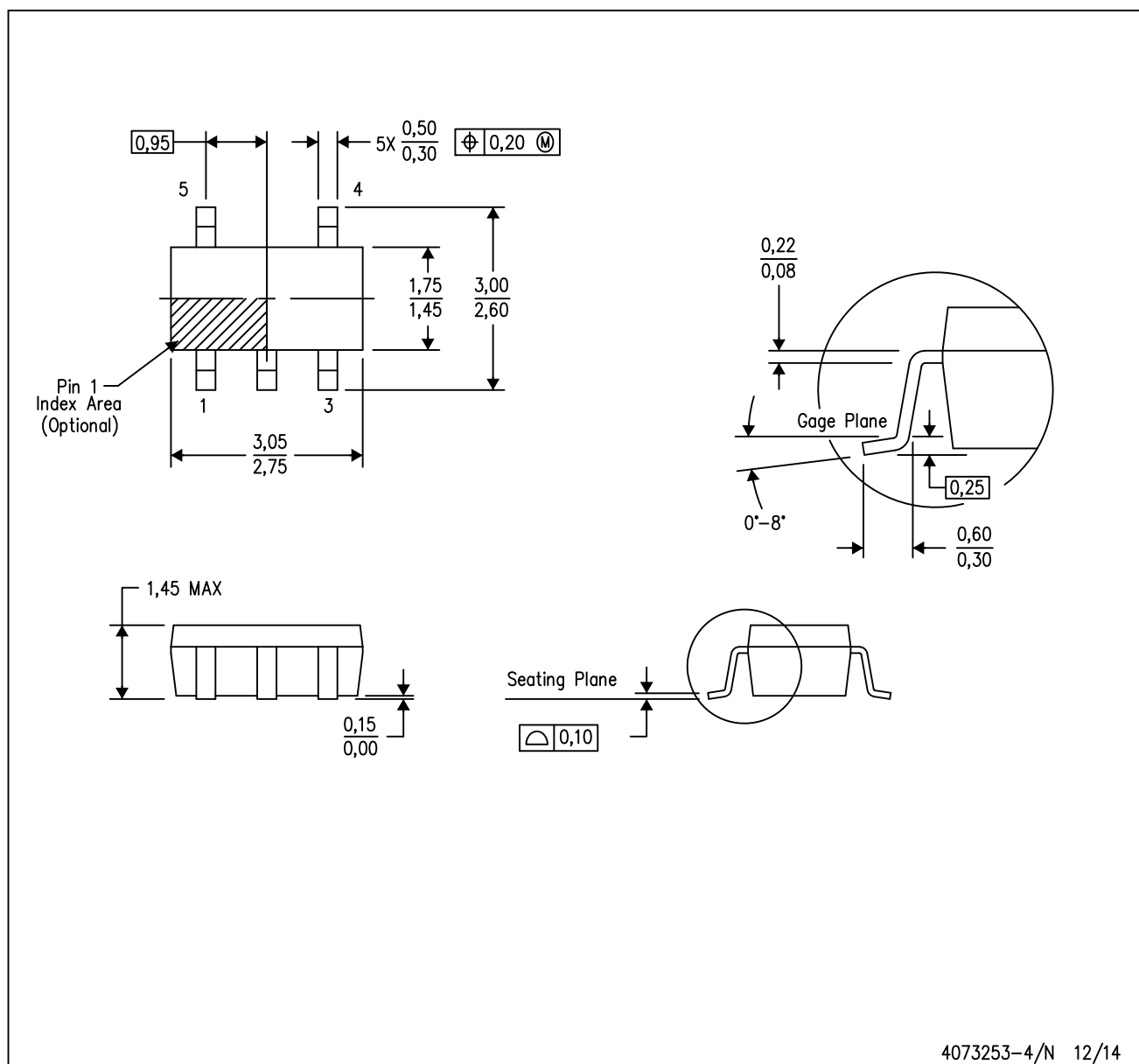
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

DBV (R-PDSO-G5)

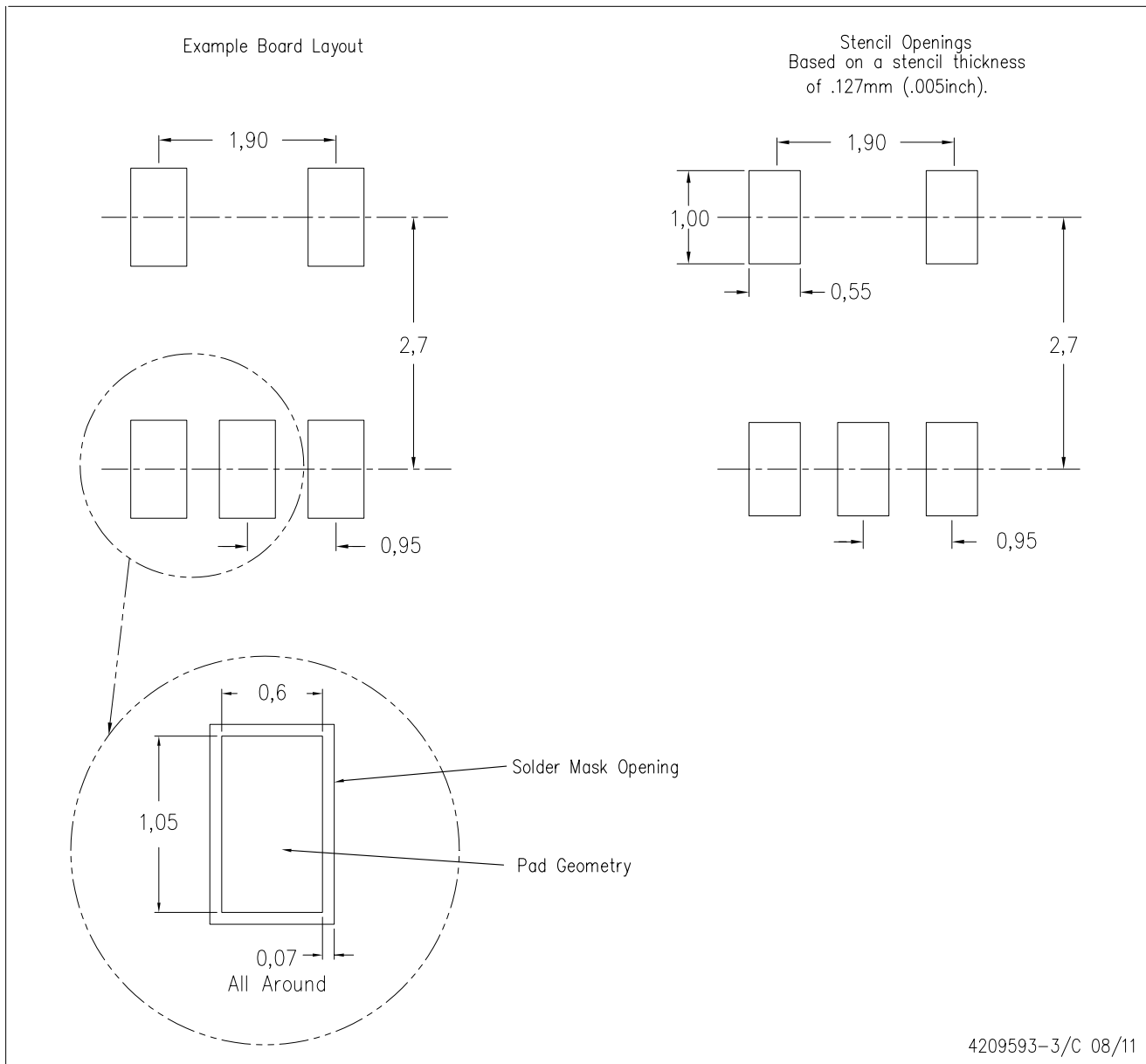
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

D GK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

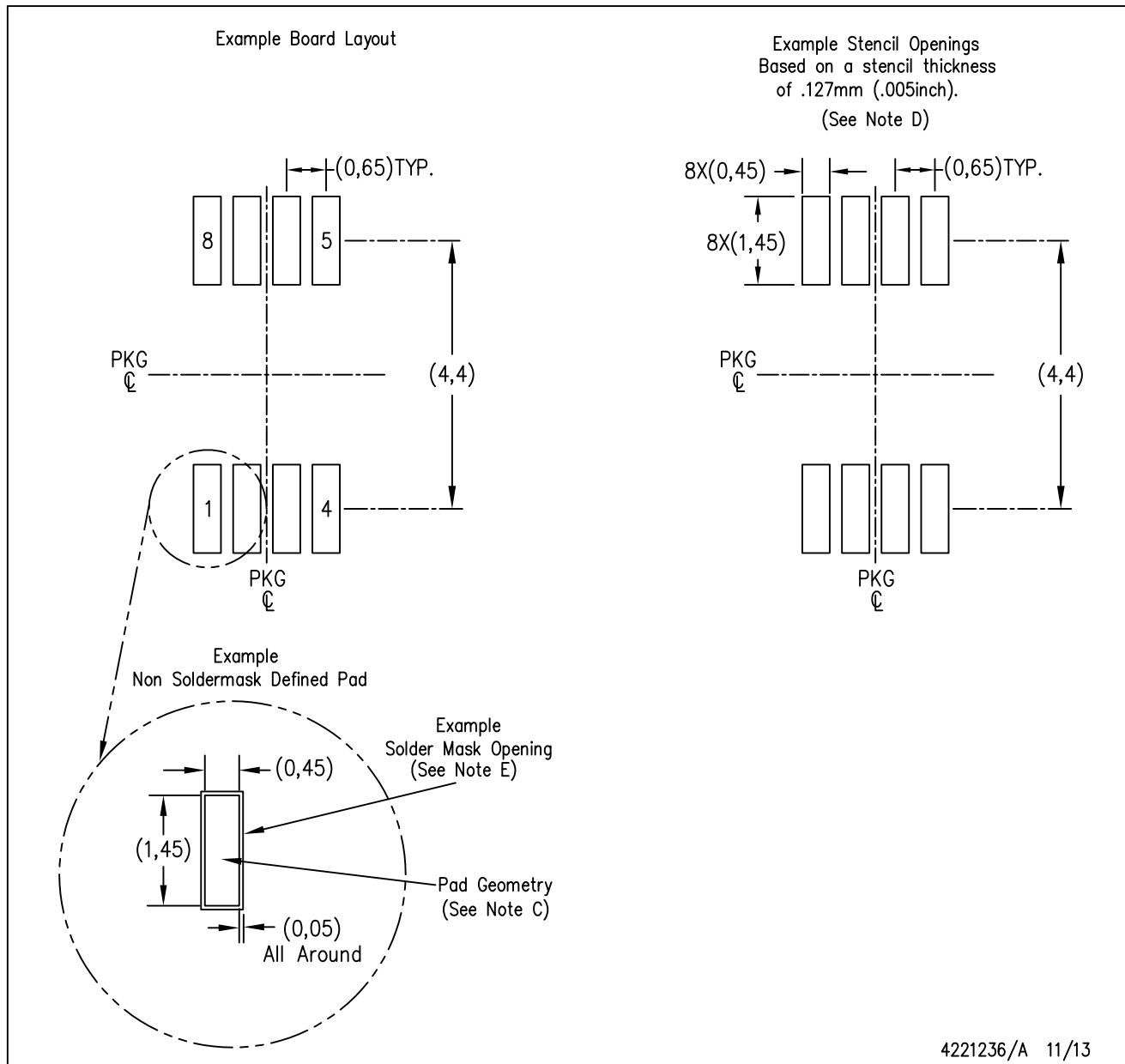


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- ☒ C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- ☐ D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

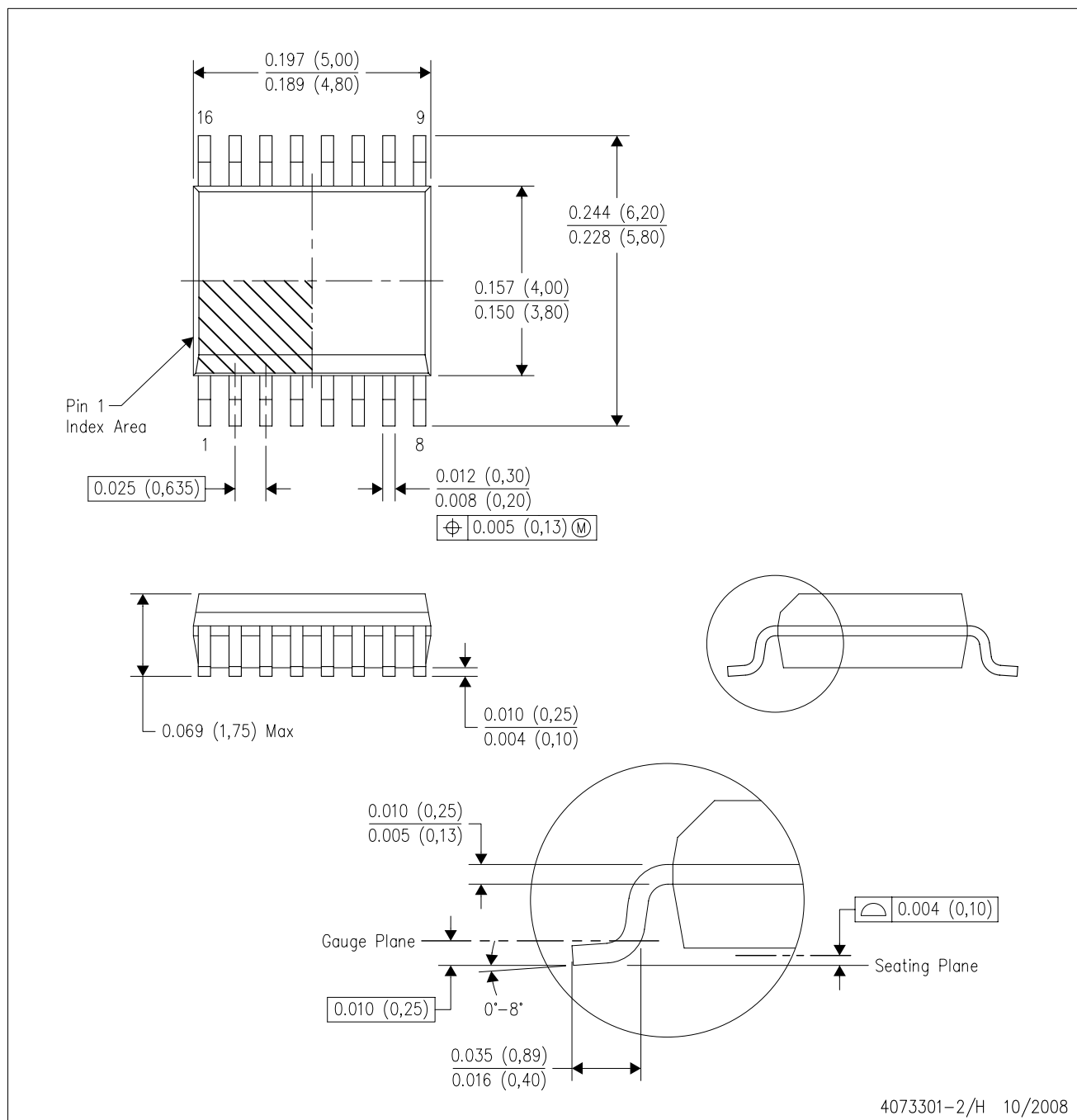
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R-PDSO-G16)

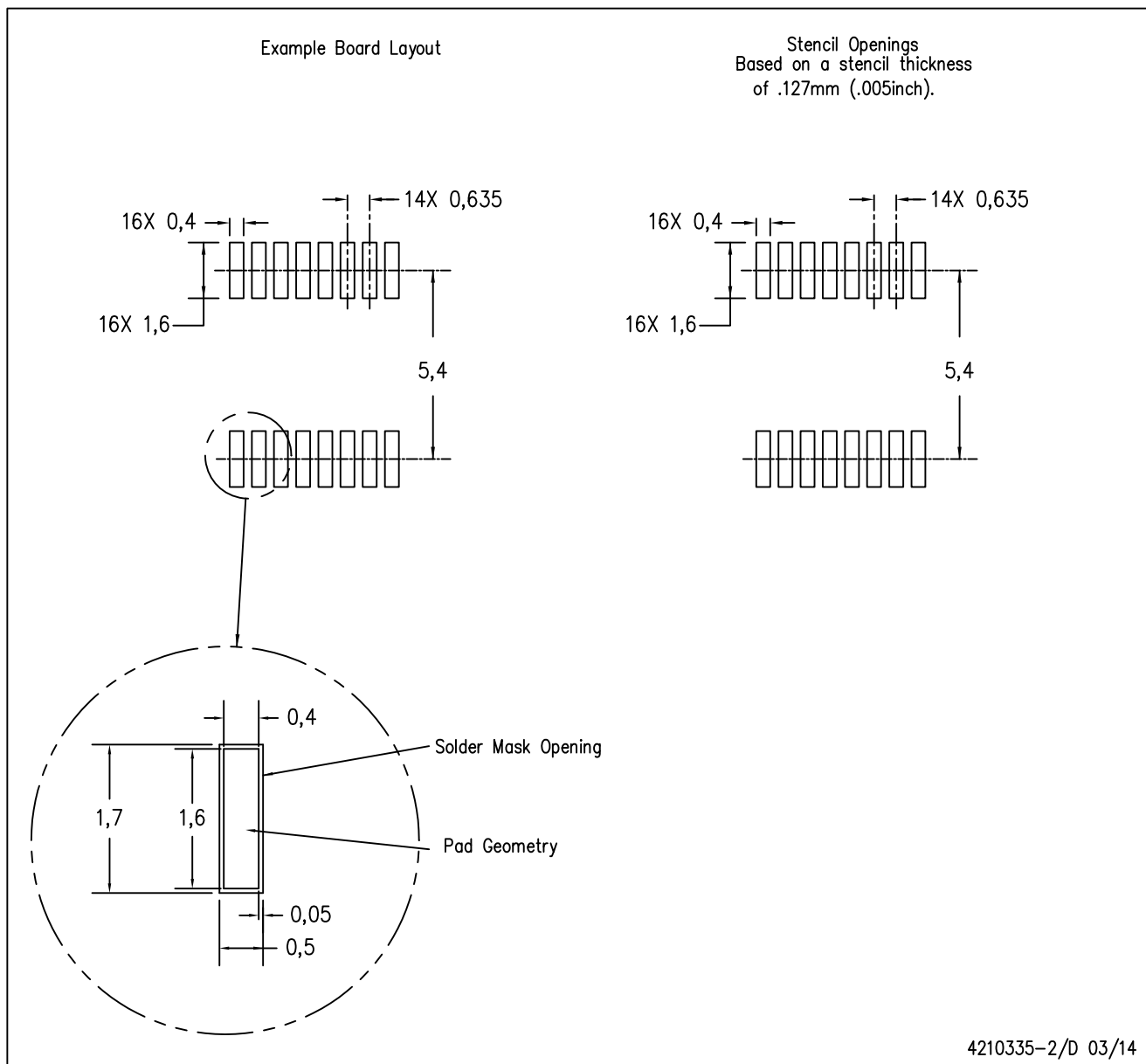
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AB.

DBQ (R-PDSO-G16)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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