ECE 3829: Advanced Digital System Design with FPGAs
C Term 2018

Lab 2- VGA display and Light Sensor interface
Report due at start of class Monday February 5th

Use the provided Ambient Light Sensor module and a VGA Monitor to create a light sensor monitor on the Basys3 board.

This project involves the design of a number of interfaces to peripheral devices. It drives the VGA display using a controller, and reads the light sensor using an SPI interface. The lab involves the use of multiple sequential circuits (counters, shift registers, etc.), the Xilinx Core Generator (for the Mixed Mode Clock Manager, MMCM), and use of existing IP (the Digilent VGA controller) but it is not necessary to develop any new state machines for this lab. There are multiple parts to this project and it will require the full two weeks to complete. To be successful, this lab will require a good design and debugging approach. Progress step-wise making simpler projects that you can test and debug separately and then combine them together (i.e. hierarchical design).

This lab (and report) can be completed individually or with a lab partner (recommended). It will be worth 30% of your course lab grade.

Lab Sign-off: During a lab section or posted help session or office hour, demonstrate what you have working to a member of the course staff for sign-off. You should get sign-offs as your go along instead of waiting to get them all at once. Please BRING your VERILOG listings for the TAs to check (they will return these to you to hand in with the report). The lab report is due in class on Monday February 5th.

Description

Preliminary:

- Modify the simple seven segment display from lab 1 to create a seven_seg module that can display a value from "0000" to "FFFF" on the four seven segment displays. The input to the module should be a 16-bit wide bus, with four bits used to indicate the value to be displayed on each of the seven segments. You will also need a clock to cycle through the four digits. You may want to review ECE2029 Lab 4 for guidence.
- *Make this a separate module* – you will use this module in this and later projects.
- Test this out by using the slide-switches to enter various numbers.

Part 1: VGA display

- Use a Mixed Mode Clock Manager to create a 25MHz clock required for the VGA pixel clock.
    - See the MMCM tutorial for how to add this IP to your design.
    - Note: connect only the 100MHz FPGA clock to the MMCM (nothing else)
    - Add a period constraint to your XDC to match the Basys3 board 100MHz clock frequency.
    - Use this 25MHz clock signal for all the sequential logic in this lab

- Create a VGA display using the VGA controller provided by Digilent (just the 640 by 480 version) – see information at end of this document.
- Use the slide-switches to select and display one of the four the following patterns
    - A completely green display
    - Eight horizontal color bars on the monitor, filling the display
    - A black screen with a yellow block 32 pixels wide by 32 pixels in top center of the screen
    - A black screen with a yellow block 32 pixels wide by 32 pixels in the center of the screen with its vertical position (top to bottom) determined by the value from the light sensor (you can test using other digital IO prior to using light sensor)

  (These should be relatively easy once you start working with the VGA controller provided by Digilent – don't forget to include the 'blank' signal)

Part 2: Light Sensor Interface

- Create an SPI interface to be able to read the 8-bits of light sensor information from the PmodALS module provided.
- Use the 25MHz clock with a counter and clock enable signal to generate the ADC SCLK at 1MHz
- Use a counter or shift register to create the ADC CS signal.
    - Verify the SCLK and CS signals are correct with an oscilloscope.
- Capture a new light sensor value every 200ms (5Hz)
    - Use a shift register to read in the 8-bits of ADC data
- Display the light sensor value in hexadecimal on two right-most digits of the seven-segment displays (i.e. 00 to approx. FF).
    - Display zeros on the other two seven-segment displays
- Capture an SPI ADC 16-bit transfer using an oscilloscope (show the CS, SCLK, and SDO signals on the scope capture) and include this in your report along with a description
    - Note: For all 'scope pictures, preferably take a screen capture with a USB flash drive rather than a camera picture. You should be able to clearly see all the signals and the time base.

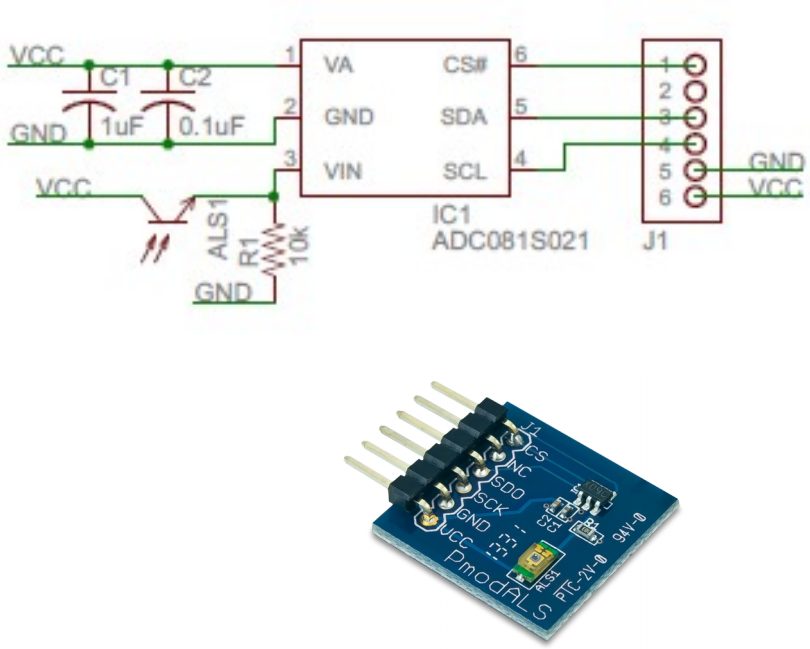
Extra credit

Up to 10% lab bonus points for any good improvements or enhancements to your design (must demo on board **and** describe in your report). For example make a system that can create a "sun set" changing both the position and color of block based on light sensor reading or print your first name on the VGA monitor!

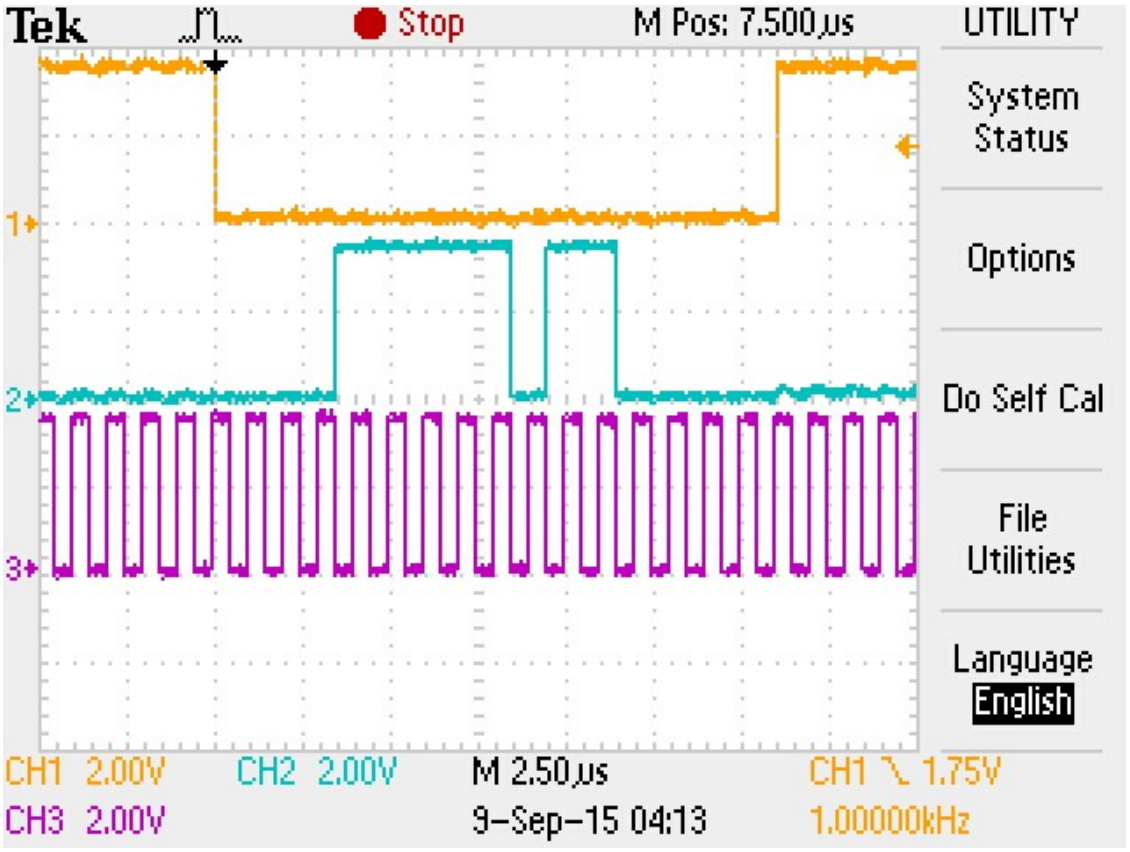
Reference Material

Read the *Seven Segment and VGA Port* section in the Basys3 Reference Manual.

Read the Digilent PmodALS Reference Manual and the Texas Instruments ADC081S021 ADC data sheet.



PmodALS schematic and module from Digilent



CS, SDO, SCK example SPI transfer (with CSK at 1MHz) - bright sensor value (0xFB)

Notes:

Your final design should combine Parts 1 and 2.

Print the sign-off sheet and demonstrate your system during one of your lab sessions or posted course office hours before the due date. ***BOTH PARTNERS MUST BE PRESENT AT ALL SIGN-OFFS!*** Have printed copies of your Verilog source files ready so they can be checked during the demo (don't forget to includes header blocks with names, description, and comments).

Write a report including: *an introduction, a description of your design including good block diagrams showing how you implemented the design, a section describing how many flip-flops your design used and why. Include the part of the synthesis file that displays warnings – explain these. Do not include the entire synthesis file. Include a conclusion describing any problems or issues you had and any lessons learned. You must include your original sign-off sheet and your HDL source files in an appendix.*

Your lab should be written in a professional style. It should be an electronically prepared technical document like what you would submit to a fellow engineer or your boss. The report should include:

Introduction = 1-2 paragraphs (1/2 page tops) succinctly stating the objectives of the lab and giving an overview of what you accomplished.

Discussion and Results = As many pages as it takes (without padding!). In this section you should thoroughly discuss what you did in each part of the lab. You should describe the approach you took to solving any problems. Again, this is a technical document. It should present your work in a clear and concise fashion. Results should also be thoroughly discussed. Any measurements should be tabulated, questions should be stated as given in the assignment and answered completely (in complete sentences).

Be SURE to clearly indicate your answers to all questions asked in the lab assignment. The TA can't give you credit if they can't find your answer!

Summary and Conclusion = 1-2 paragraphs (1/2 page tops). Wrap-up and summarize what you accomplished in the lab. This should be a "bookend" to the introduction.

Appendices = Include sign-off sheet, grading sheet, Verilog source code and any relevant raw data sheets (or links to them).

Grading Guidelines

- [50 pts] Implementation
    - [50 pts] Design works on board and meets requirements
- [20 pts] Source Code – Verilog in Appendix
    - Code style and comments (well-commented, with header blocks and tab-indented code!)
    - Use of *case* vs. *if*, structured vs. spaghetti code, etc.
    - Recognizable implementation of "standard" elements (counters, shift registers, clock dividers, decoders, state machines, etc.)
    - Good modular design
    - No latches or other synthesis problems
- [30 pts] Lab Report
    - [5 pts] Brief Introduction / Problem Statement
    - [15 pts] General overview of approach to solution and description (include good diagrams with descriptions) and oscilloscope pictures with explanations
    - [5 pts] FPGA resource usage (# flip-flops with explanation) and listing and explanation of warning messages. DO NOT copy all the Xilinx reports – just the relevant sections and comment on them to fully explain what they show.
    - [5 pts] Conclusions
        - Problems faced in implementation
        - Solutions used to solve problems
        - Lessons learned from the project
        - Suggestions for further improvements and extensions
- [10 pts] Extra points
    - Possible extra points for good additional features or capabilities. Impress us!. Must demonstrate on BASYS3 board and include description in report)

ECE 3829: Lab 2 sign-off sheet

Name: _____ ECE Box #: _____

Name: _____ ECE Box #: _____

BOTH PARTNERS MUST BE PRESENT AT ALL SIGN-OFFS!

Preliminary (not required to be shown)

The seven segments display works (0000 to FFFF) _____

Part 1 (VGA)

Display shows a green screen _____

Display shows 8 horizontal color bars _____

Display shows a yellow block at top _____

Display shows a yellow block (vertical position determining by light sensor value) _____

Part 2 (Light Sensor)

The light sensor displays the correct value on the seven segment displays (00 to FF, dark to light) – zeros on other digits _____

All combined

All parts are combined into one project _____

Extra Credit (describe)

Example: Text on screen _____

_____