ECE 3829: Advanced Digital System Design with FPGAs - C Term 2018

DAC Waveform Generation and Moving Block
Report due start of class Monday February 19th

This lab exercise involves using a DAC module to generate a sine wave and the VGA controller to generate a moving block. You will also use the seven segment display module from the previous lab for testing and display (you should not need to modify it).

Lab Sign-off: During a lab section or posted help session or office hour, demonstrate what you have working to a member of the course staff for sign-off. You should get sign-offs as your go along instead of waiting to get them all at once. Please BRING your VERILOG listings for the TAs to check *and sign* (they will return these to you to hand in with the report). The lab report is due in class on Monday February 19th.

Description

Part 1: DAC – waveform generation

- Read the AD703 Serial Input, Dual 8-bit DAC data sheet
- Use the PMOD DA1 Module provided during lab
  - Just use the first AD7303 and only DAC1 A (ignore the other 3 DACs)
  - (Use a value of 0 for the 8 control bits)
- Implement the DAC SPI interface with a *shift register* and *state machine*
  - Use a 10MHz SPI clock
  - Update the DAC at a 100KHz rate with new 8-bit data values See data sheet for message format (Use continuous 16-bit write shown in Fig 1).
- Verify the DAC interface is working by first using a constant value to drive the DAC (use 8 of the slider switches to enter the 8-bit code).
  - You should see a constant voltage out of the DAC (in the range 0 to 3.3V) that changes as you modify the slider switches
  - Display the 8-bit data value you send to the DAC on two of the seven-segment displays
- Create a 3.125 kHz saw-tooth waveform whose value is updates every 10 us (i.e. at 100KHz rate). How many steps per per cycle will be needed? *Explain in your report.*
- Use an oscilloscope to capture pictures of the saw-tooth wave and the SPI interface
  - For all ‘scope pictures, preferably take a screen capture with a USB flash drive rather than a camera picture. You should be able to clearly see all the signals and the time base.

Part 2: Moving Block

- Assume the VGA monitor screen is divided into blocks, with each block 24 pixels high by 32 pixels wide, and the top left corner block is at block x,y position (0,0) and the bottom right block is at x,y position (19, 19)

- Create a cyan block and place it at center of the screen. What is it's coordinates (x,y)?.
- Use four push buttons to move the block either up, down, left or right one block position at a time when the push button is pressed (you will need to debounce the push button switches so the block only moves one position for each button press)
- When the colored block hits the outside edge of the display it should stop (not wrap around)
- Display the current x,y position of the cyan block using the seven segment displays (00 00 to 19 19)

Part 3: Simulation and Testing (not required as part of demonstration and sign-off but required for lab report)

- Create a test bench to show the following:
  - An SPI cycle showing voltage code data being transferred to the DAC
- Important – describe and annotate the simulation waveforms

Reference Material

Review the PmodDAC module datasheets

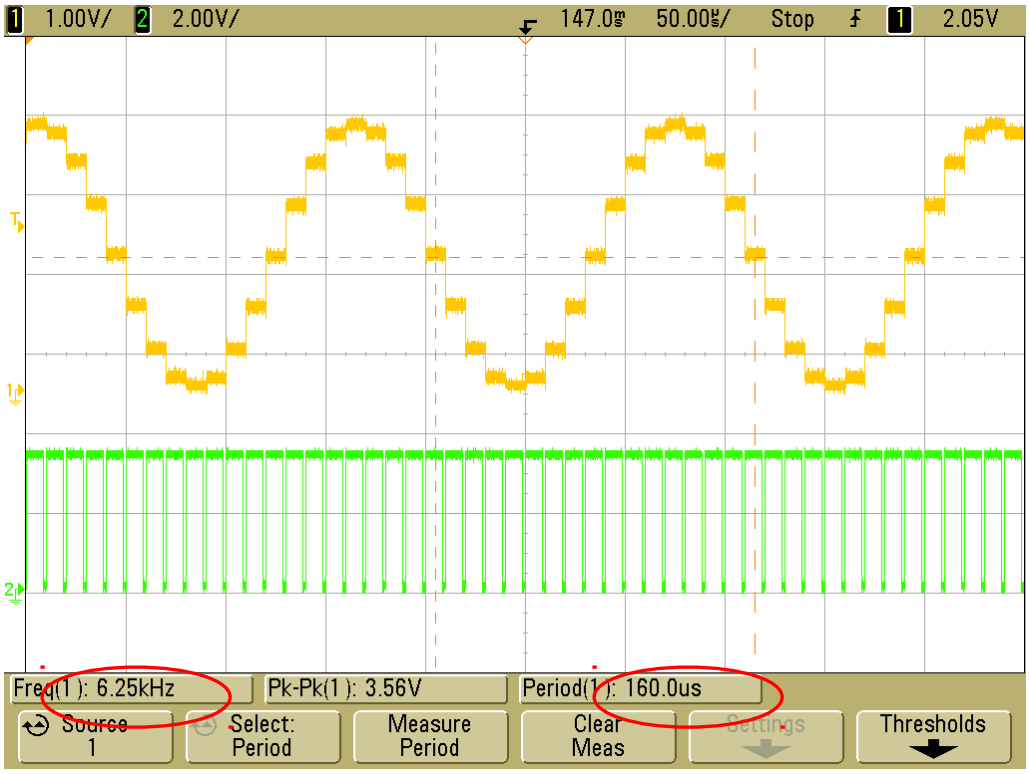
Notes:

Your final design should combine parts 1 and 2.

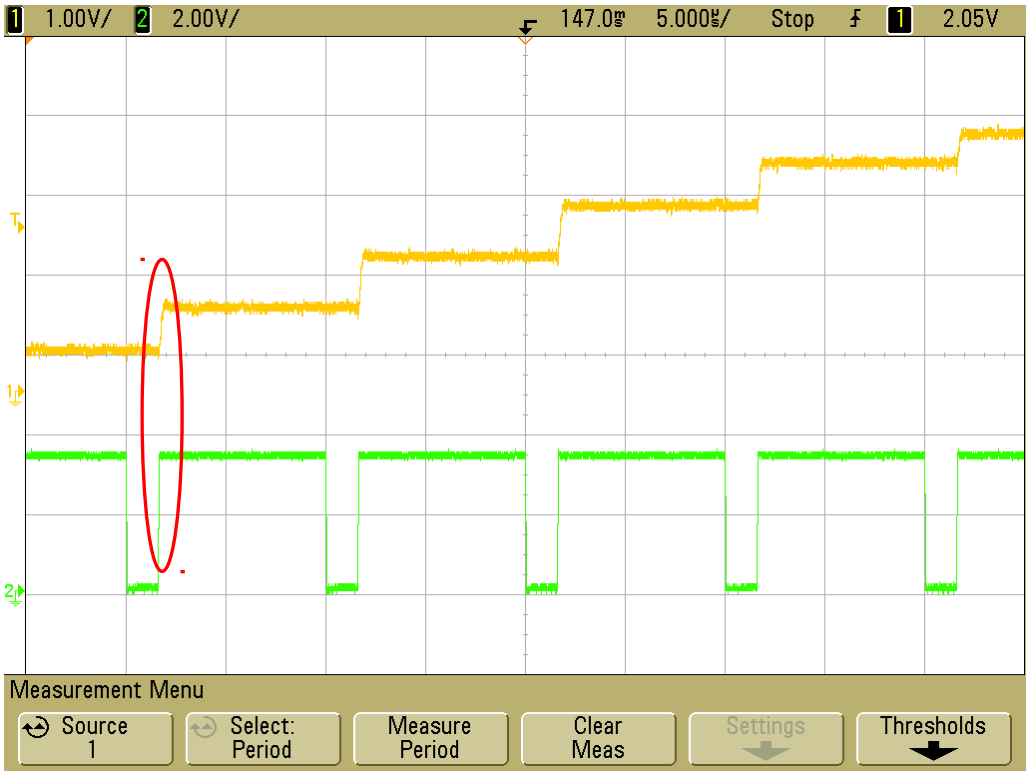
Prepare a sign-off sheet and demonstrate your system during one of your lab sessions or during posted course office hours before the deadline. ***BOTH TEAM MEMBERS MUST BE PRESENT FOR ALL SIGN-OFFS!*** Have your printed Verilog source files ready so they can be checked and signed during the demo (don't forget to header blocks for your Verilog modules including names, description, and comments).

Write a report including: an introduction, a description of your design including good block diagrams showing how you implemented the design, a section describing how many flip-flops your design used and why? Include scope pictures of your DAC waveform and SPI interface. Include a conclusion describing any problems or issues you had and any lessons learned. Include your signoff sheet and your source files in an appendix.

Up to 10% lab bonus points for any good, original improvements or enhancements to your design (must demonstrate on board and describe and document in the report).



An example of 6.25KHz Sine Wave with DAC Sync pulses



100KHz (10us) DAC updates – new analog voltage output after each update

Grading Guidelines

- [40 pts] Implementation
  - [40 pts] Design works on board and meets requirements
- [15 pts] Source Code – Verilog in Appendix
  - Code style and comments (well-commented and tab-indented code!)
  - Use of *case* vs. *if*, structured vs. spaghetti code, etc.
  - Recognizable implementation of "standard" elements (state machines, counters, shift registers, clock dividers, decoders)
  - Good modular design
  - No latches or other synthesis problems
- [45 pts] Lab Report including Test Bench
  - [5 pts] Brief Introduction / Problem Statement
  - [15 pts] General Overview of approach to solution and description and (include Block and State Diagrams with descriptions). Include oscilloscope picture of DAC waveform.
  - [5 pts] FPGA Resource usage (# flip-flops with explanation) and listing and explanation of warning messages (don't copy all the Xilinx reports – just the relevant sections)
  - [15 pts] Test bench description and simulation waveforms (don't just copy the waveforms - annotate and explain well)
  - [5 pts] Conclusions
    - Problems faced in implementation
    - Solutions used to solve problems
    - Lessons learned from the project
    - Suggestions for further improvements and extensions
- [10 pts] Extra points
  - Possible extra points for good additional features or capabilities (need to demo on board and include description in report) – for example, generate different, selectable waveforms at different frequencies. Make max amplitude selectable from slide switches.

ECE 3829: Lab 3 sign-off sheet

Name: _____ ECE Box #: _____

Name: _____ ECE Box #: _____

BOTH TEAM MEMBERS MUST BE PRESENT FOR ALL SIGN-OFFS!

Part 1 (DAC produces constant voltage and sine waveform)

The DAC produces the correct voltage output _____
(verify range 0 to 3.3V when slider switches change)

The DAC produces the correct saw-tooth waveform _____
(verify period and waveform shape)

Part 2 (VGA displays moving block)

The VGA controller produces the correct display: _____

The block moves correctly and seven segment displays show current x,y position _____

Other (describe)

All combined

All parts are combined into one project _____

Extra Credit (describe)

_____