ECE 3829: Advanced Digital System Design with FPGAs - C Term 2018

Lab 1: Combinational Logic Design

Report with Sign-offs Due Monday 22 January 2018

Lab exercise 1: (worth 10% of total lab grade)

This lab is to remind you how to use the Xilinx Vivado Design Suite tools and the Basys3 board to implement a simple combinational logic design. This should be review from ECE2029.

This lab is to be completed individually. All students must submit their own implementation, sign-offs and report. Future labs may be completed in teams of two, if desired.

Background Review

First, complete the Decoder tutorial (in Verilog) - you may find it helpful to also look at the Counter tutorial which shows how to instantiate a lower level module.

Description

Part 1:

- Create a new module called '`seven_seg`' in a separate file. This should allow for four digits (each one 0 to F) to be displayed on the four seven-segment displays. This module should have the following ports:
  - Four 4-bit inputs (`a`, `b`, `c`, and `d`) and two 1-bit inputs (called `sel0`, `sel1`)
  - A 7-bit output to drive the seven-segment cathodes and four 1-bit anodes to drive the four anodes
- Connect 4 consecutive slider switches (e.g. sw3, sw2, sw1 and sw0) to each of the `a`, `b`, `c`, and `d` inputs of the `seven_seg` module.
- Connect the `sel` inputs to the left and right push-button switches.
- When no push-buttons are pressed, display the value of the lower slider switches on seven-segment display #1 (the right most). *Is this* `a` *or* `d`*? Specify in your report*.
- When the right push-button is pressed, display the value of the next lower 4-bits of the slider switches on seven-segment display #2
- Do the same with other push-button combinations to allow the remaining slider switches to be displayed on seven_segment display #3 and #4 (the left most).
- Build this project and download to your Basys 3 board. *Demonstrate Part 1 to the course staff for Sign-off before proceeding with Part 2*

Part 2:

- Create a new top_level module called '`lab1_top`' in a second file that has inputs connected to all the slider switches and push buttons, and outputs connected to the seven segment display.
- Instantiate the `seven_seg` module from Part 1 into the top level module using named association. *Define "named association" in your report. How is it different from ordered or "positional association"?*

- Add additional Verilog statements to the top level module to add the following functionality (use the Up and Down push button switches for selecting among the four functions):

  00 – show the values of the various 16-slider switches on the four seven-segment displays (basically the same as Part 1)

  01 – display '3829'

  10 – display your mail box number (for example '0123')

  11 – display the result of the addition of slider switches [7:0] added to slider switches [15:8]

  (*Note*: You will still need to use the same '`sel`' push-buttons to control anodes as in Part 1 in order to show the value on the four even-segment displays, one at a time. This is a wholly combinational design, no clocks are required.)

  Demonstrate Part 2 to the course staff for sign-off.

Report requirements

Your report is due at the beginning of class on the due date. Attach your original sign-off sheet, a hard (printed) copy of your TWO Verilog files and your XDC constraints file in an appendix. *Make sure each module includes a header with your name, date, a description of its functionality plus inputs and outputs.* Your code should be well commented. Make print outs using notepad++ or similar to get a good, formatted Verilog listing. You will lose points if your listing is unformatted, does not include a proper header for each module or is hard to read.

Your lab should be written in a professional style. It should be an electronically prepared technical document like what you would submit to a fellow engineer or your boss. The report should include:

Introduction = 1-2 paragraphs (1/2 page tops) succinctly stating the objectives of the lab and giving an overview of what you accomplished.

Discussion and Results = As many pages as it takes (without padding!). In this section you should thoroughly discuss what you did in each part of the lab. You should describe the approach you took to solving any problems. Again, this is a technical document. It should present your work in a clear and concise fashion. Results should also be thoroughly discussed. Any measurements should be tabulated, questions should be stated as given in the assignment and answered completely (in complete sentences).

Be SURE to clearly indicate your answers to all questions asked in the lab assignment. The TA can't give you credit if they can't find your answer!

Summary and Conclusion = 1-2 paragraphs (1/2 page tops). Wrap-up and summarize what you accomplished in the lab. This should be a "bookend" to the introduction.

Appendices = Include any relevant raw data sheets, or links to them.

******Remember, this lab must be completed individually and each student must submit a report.***

Reference Material

Complete the decoder tutorial (on the class website).

Review the counter tutorial to see how to instantiate a lower-level module using named association.

```
// instantiate copy of display module using named association
// counter_10 signal is connected to the digit port
// seg signal is connected to the seven_seg port
display disp1 (.digit(counter_10), .seven_seg(seg));
```

Read the Seven Segment section in the Basys3 Reference Manual.

Note: If you want to eliminate the two warning messages during the implementation phase add the following to your XDC file (also shown in the counter tutorial XDC file):

```
# Configuration bank voltage select (CFGBVS) must be set to VCCO or GND,
# and CONFIG_VOLTAGE must be set to the correct configuration voltage,
# in order to determine the I/O voltage support for the pins in bank 0.
set_property CFGBVS VCCO [current_design]
# where value1 is either VCCO or GND
set_property CONFIG_VOLTAGE 3.3 [current_design]
# where value2 is the voltage provided to configuration bank 0
```

Grading Guidelines

- [25 pts] Implementation
  - [25 pts] Designs work on board and meets requirements
- [5 pts] Source Code – Verilog in Appendix
  - Code style and comments (well-commented and tab-indented code!)
  - Use of *case* vs. *if*, structured vs. spaghetti code, etc.
  - Recognizable implementation of "standard" elements (decoders, etc.)
  - Good modular design
- [20 pts] Lab Report including Test Bench
  - [5 pts] Brief Introduction / Problem Statement
  - [15 pts] General Overview of approach to solution and description. Clearly answer all questions posed in lab assignment. Include block diagrams of your projects.
  - [5 pts] Conclusions
    - Problems faced in implementation
    - Solutions used to solve problems
    - Lessons learned from the project
    - Suggestions for further improvements and extensions

ECE 3829: Lab 1 sign-off sheet

Name: _____ ECE Box #: _____

Part 1:

7 segment displays displaying digits from slider switches in response to `sel` push-buttons _____

Part 2:

New top module instantiating 7 segment display and displaying 1 of 4 messages/values based on push-buttons _____