

**CMPE 160 Laboratory Exercise 04**  
**Analysis and Simulation of Sequential Circuits**

Christopher Larson  
Performed: 7 March 2018  
Submitted: 21 March 2018

Lab Section: L3  
Instructor: Mr. Dominguez  
TA: TA Andrew Ramsey  
TA Matthew Millar  
TA Madeline Mooney

Lecture Section: 01  
Professor: Professor Beato

By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables or graphs, or using previous student reports as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

Your Signature: \_\_\_\_\_

# Abstract

The objective of this exercise was to analyze and simulate sequential circuit-4 bit shift register. The exercise was helpful in the understanding of the design and operation of sequential circuits. A 4-bit shift register was designed and tested against a testbench to ensure the correctness of the design. The minimum clock period and maximum clock frequency were also recorded. A 4-bit register was also designed but the AND-OR gates network was replaced with tri-state buffers.

## Design Methodology

The schematic diagram that was designed represented a 4-bit shift register, as shown in Figure 1.

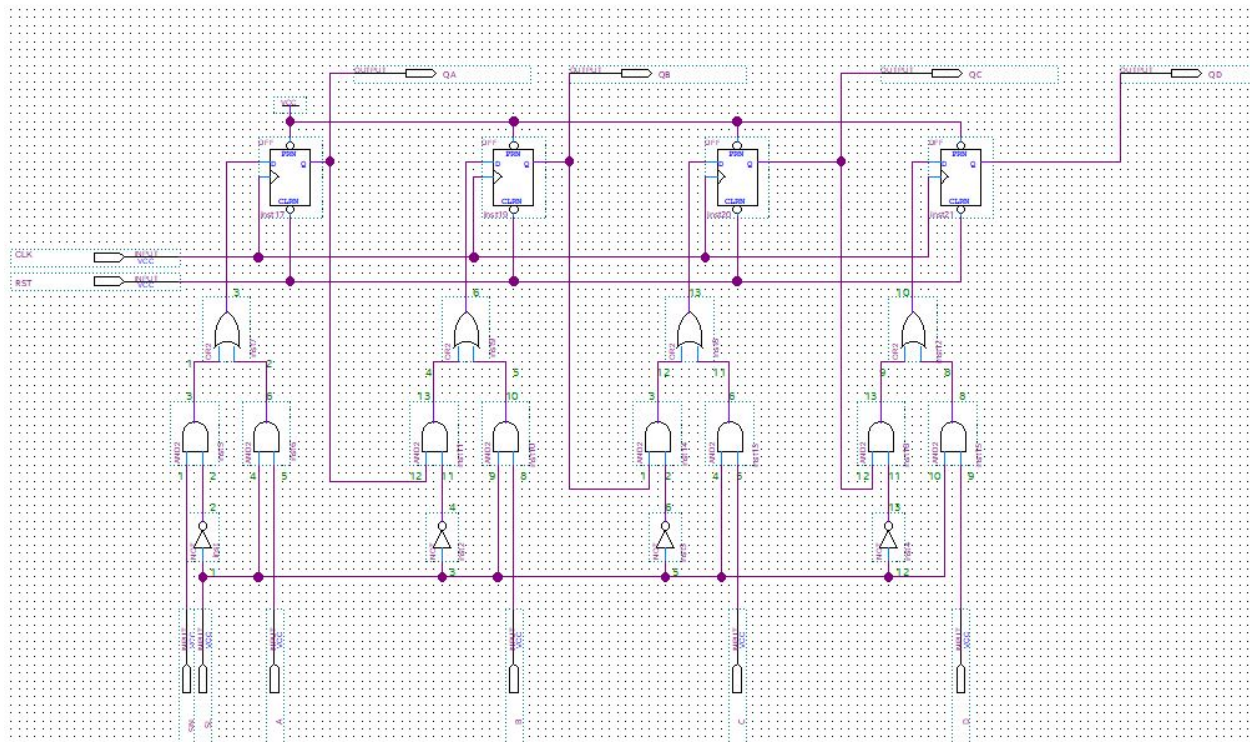


Figure 1: 4-bit shift register

Figure 1 shows the diagram of a 4-bit shift register that was used to create the waveform. The 4-bit shift register with tri-state buffers was also designed and tested against a testbench as well as the waveform was compared to the first waveform to ensure that the two diagrams worked the same. The 4-bit shift register diagram is shown in Figure 2.

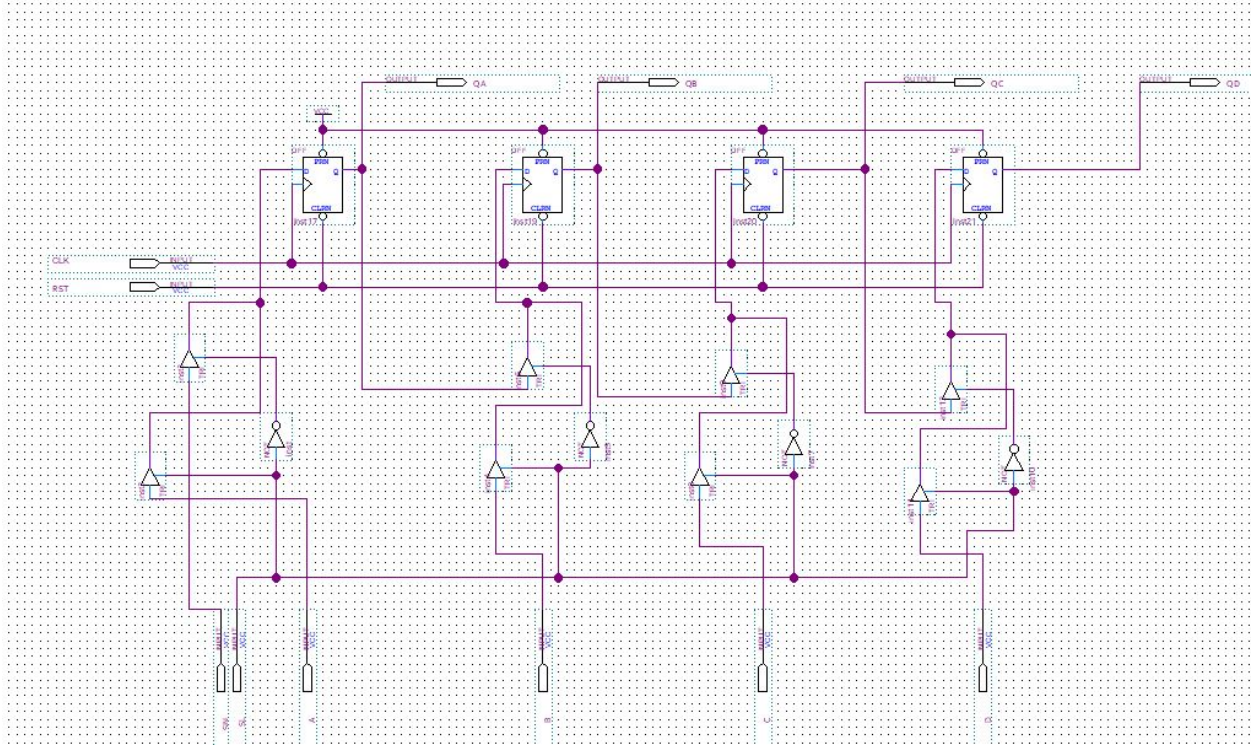


Figure 2: 4-bit shift register with tri-state buffers

## Results and Analysis

The waveform for both the 4-bit shift register and 4-bit register with tri-state buuffers is shown below. There is only one waveform because the two waveforms were the exact same since the two shift registers are functionally the same. The two waveforms were compared to each other to confirm the correctness of the diagrams.

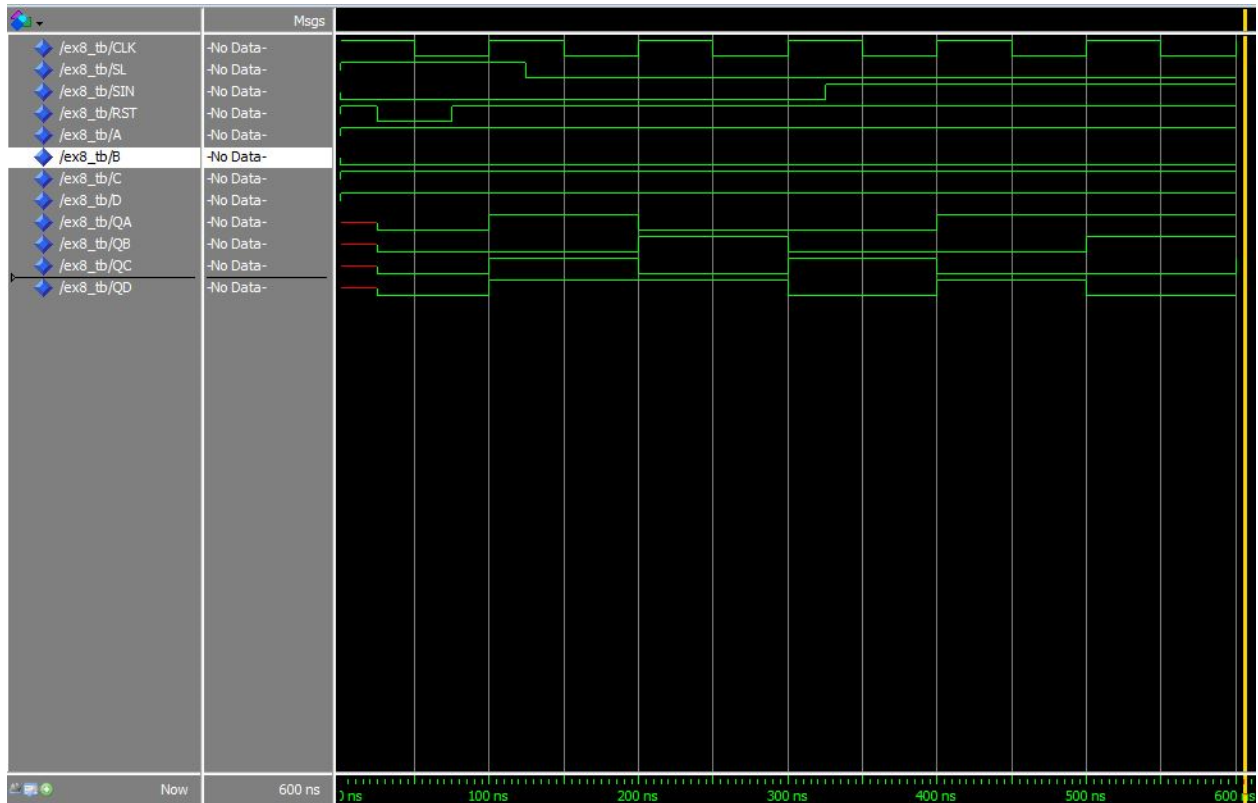


Figure 3: 4-bit shift register waveform

## Conclusion

The exercise was helpful in understanding the design and operation of sequential circuits, like shift registers. There are multiple ways to design the same sequential circuit as shown by the waveforms of the two shift registers having the same waveforms. The schematic diagrams in the exercise were designed correctly as confirmed by the testbench and the waveform of the diagrams being the same.

## Questions

1. The arithmetic operation that occurs was division by two without the remainder of the operation.
2. The arithmetic operation that occurs was multiplication by two.
3. It is not a good idea to change the input signals at exactly the same time as the rising edge because this creates an unpredictable race-situation which might not work as intended.