CMPE 160 Laboratory Exercise 06

Sequential Circuit Elements

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Performed: 28 February 2018
Submitted: 6 March 2018

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Abstract

The objective of this exercise was to design, and implement an active-low enable D latch and a rising edge-triggered, master-slave D flip-flop. An active-low D latch is used to control the output while the enable is low and to leave the output as the last input when the enable is high. A D flip-flop is made by combinining two D latches together and using a controlled CLK signal that changes on a timed interval. A rising edge-triggered flip-flop has two states, one between the rising edges of the clock wave where D changes and one where D remains the same across two rising edges of the clock. A schematic for both the D latch and D flip-flop were designed and tested to see if the design was correct by comparing the waveforms to Table 1 for the D latch and Table 2 for the rising edge-triggered D flip-flop.

Table 1: Active-low enable D latch

En	D	Q	Qn
0	0	0	1
0	1	1	0
1	X	Q	Qn

Table 1 is a D latch with an active-low enable.

Table 2: Rising edge-triggered D flip-flop

CLK	D	Q	Qn
↑	0	1	0
↑	1	0	1
Otherwise	X	Q	Qn