CMPE 160 Laboratory Exercise 05

Combinational Logic Circuit Design Using Boolean Algebra Simplification

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Abstract

The objective of the exercise was to apply combinational logic design to the implementation of two different equations. The two equations used in the exercise were found using Karnaugh Maps to simplify a Boolean expression into the POS and SOP form. The POS and SOP forms were then used as a guideline to build a circuit, the waveforms of this circuit was compared to the waveforms of a given testbench. The use of a testbench was important to validating the correct of the circuit, the circuit was found to be correctly built as the waveforms of the testbench and the circuit were identical.

Design Methodology

The Boolean expression used to create the sum of products and product of sums expressions was $F = \Sigma_{ABCD}(0, 2, 3, 4, 6, 7, 13, 14, 15)$. The Karnaugh map representations of the expressions are shown in Figure 1 for the F_{SOP} and Figure 2 for the F_{POS}. For the SOP expression the "1"s in the K-map are circled and for the POS expression the "0"s are circled.

AB \ CD	00	01	11	10
00	1	0	1	1
01	1	0	1	1
11	0	1	1	1
10	0	0	0	0

Figure 1: K-map of F_{SOP}

The equation given from the K-map in Figure 1 is shown in Equation 1. This is the sum of products equation with the minimal amount of terms.

$$F_{SOP} = \overline{A}C + BC + \overline{A}\,\overline{D} + ABD \tag{1}$$

AB \ CD	00	01	11	10
00	1	0	1	1
01	1	0	1	1
11	0	1	1	1
10	0	0	0	0

Figure 2: K-map of F_{POS}

The equation given from the K-Map in Figure 2 is shown in Equation 2. This is the product of sums equation with the minimal amount of terms.

$$F_{POS} = (A + C + \overline{D})(\overline{A} + B)(\overline{A} + C + D) \tag{2}$$

Using Equations 1 and 2, a circuit diagram was drawn to represent both equations of expression F. This circuit diagram is shown in Figure 3, both expressions use the same inputs but go to different outputs represented as F_{SOP} and F_{POS}.

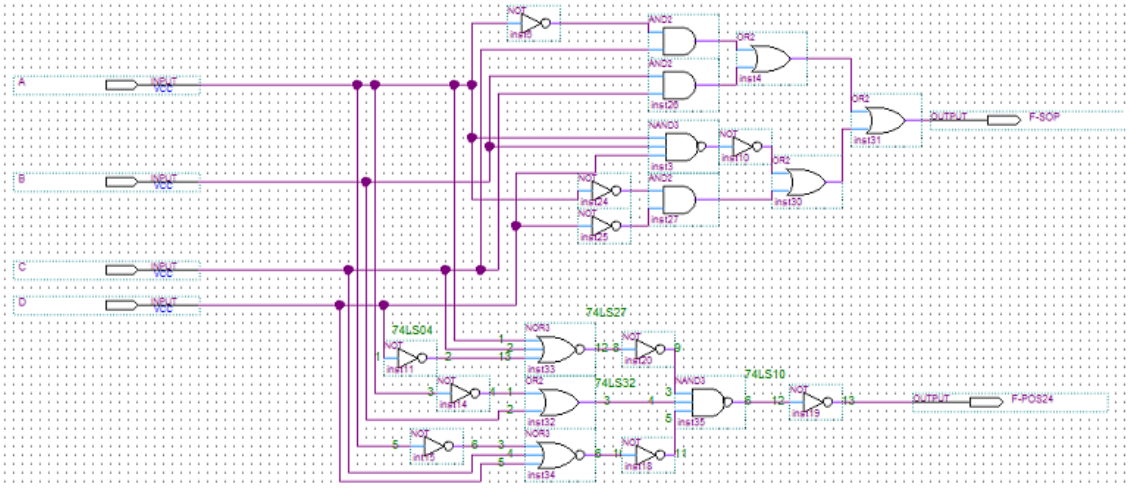

Figure 3: The circuit diagram for the SOP and POS forms of the function F

The circuit diagram in Figure 3 was used to model the waveform of the equation with the least amount of chips and the least amount of EGC, or equivalent gate count. The equation with the least was the POS equation, with a total of 9 EGC and the use of 4 chips.

Results and Analysis

The waveform in Figure 4 matched the waveform in the test bench exactly and shows the circuit design was correct. Since the POS and SOP equations were derived from the same expression and are equal to each other, the waveforms of the two are identical. The waveform also confirms that the equations were derived correctly, and that the circuit diagram was constructed correctly.

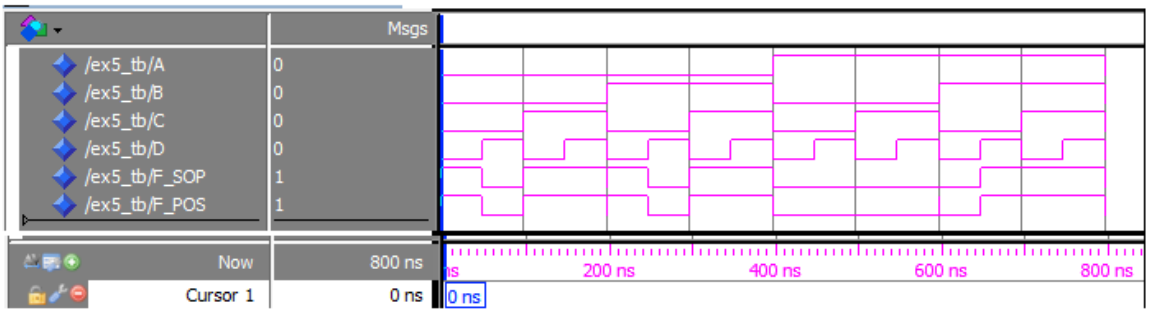

Figure 4: The ModelSim representation of function F

Conclusion

The use of K-maps to simplify an expression into the minimal POS and SOP equation is helpful when trying to create a circuit that uses the least amount of chips and the lowest equivalent gate count. It is important to simulate the simplified equations to ensure that the outputs are equivalent to the original Boolean expression and to each other. The exercise proved successful as the testbench, POS and SOP waveforms were all identical.

Questions

1.

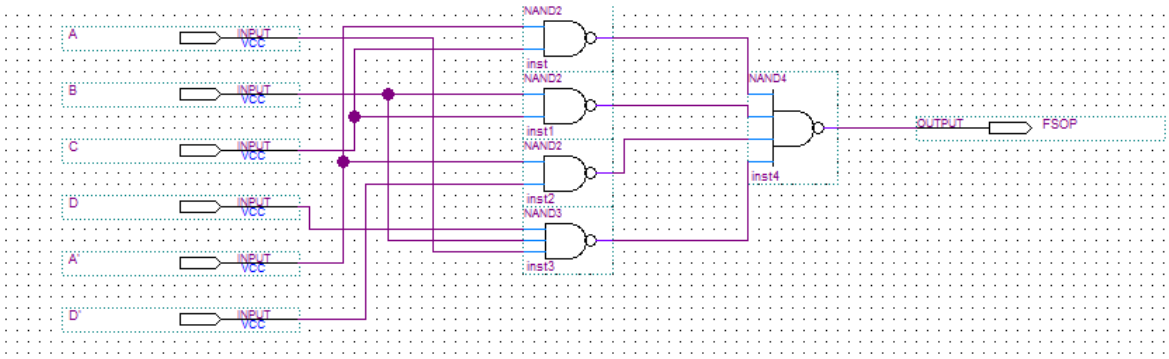

Figure 5: Question 1: 2-level NAND-NAND implementation

2.

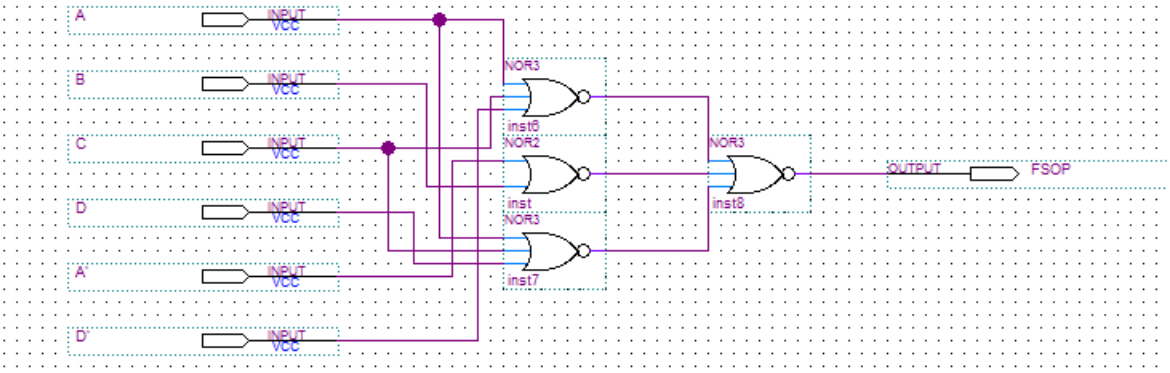

Figure 6: Question 2: 2-level NOR-NOR implementation