Course: Computer Architecture, Spring-2021

Quiz 3

Name:

Partial credit for incorrect answers can be earned only if you show your work. Errors on multiple part questions will be carried though your answer only if work is provided.

1. Unroll the given loop two times – your code should perform the equivalent of two loop iterations. Schedule it to minimize the number of both stall cycles and instructions executed; note which loop (A, B, or any combination thereof) each instruction corresponds to. You may assume the loop will be executed an even number of times and that there are sufficient operational units for all instructions. Registers F2, F4, and F6 are constants set prior to the loop. Register R1 is a variable set prior to the loop. Use the table below for latencies. Don't forget to indicate the locations of the stalls. (6 points)

Code: 91011	12 13 14 15 16 17 3 45 6 7 8 Cons	FP Latencies:		
3 DIV.D 3 MUL.D 3 ADD.D	F8, F5, F2 F7, F4, F5 F3, F8, F6 F0, F7, F3 F0, 16(R1)	Producer of result FP ALU op FP ALU op Load double Load double	Consumer of result FP ALU op Store double FP ALU op Store double	Latency 3 2 1 0
	R1,R0,LOOP	Branch delay slots:	1	

```
Loop: L.D F5, 0 (R1)
    L.D F9,-32(R1)
     ADD.D F8, F5, F2
    ADD.D F12, F9, F2
    DIV.D F7, F4, F5
     DIV.D FII, FY, F9
     MUL.D F3, F8, F6
    MUL.D Flo, Fla, FG
     Stall
     Stall
     ADD.D FO,F7,F3
     ADD.D F9, F11, F10
     PADDUI RI, #64
      SD F0,16(R1)
      BNE RI, RO, LOOP
      S.D F9,16(R1)
```

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2. Complete the dependency graph for the following code. Points will be deducted for missing dependencies, extra dependencies, and incorrect notation. (4 points)



