Extended Temperature Range Supplement

2102/2102L 1024 x 1 Static RAM

MOS Memory Products

Description

The 2102 family consists of 1024-word by 1-bit static Random Access read/write Memories (RAM) that require a single 5 V supply, have fully TTL-compatible inputs and output, and require no clocking or refresh. Chip Select (CS) permits a 3-state output allowing the outputs to be wired-OR.

The 2102 and 2102L are manufactured using the n-channel Isoplanar process and are available in a 16-pin dual in-line package or flatpak.

- FAST ACCESS-250 ns
- SINGLE +5 V SUPPLY
- TTL-COMPATIBLE INPUTS AND OUTPUT
- TOTALLY STATIC—NO CLOCKS OR REFRESH
- 3-STATE OUTPUT
- **LOW POWER (2102L)**
- **FULLY EXPANDABLE**
- **FULLY DECODED**
- 16-PIN DUAL IN-LINE PACKAGE
- TWO TEMPERATURE RANGES

Pin Names

 $\begin{array}{ccc} {\rm A_0^-A_9} & {\rm Address\ Inputs} \\ {\rm D} & {\rm Data\ Input} \\ {\rm R/W} & {\rm Read/Write} \end{array}$

CS Chip Select (active LOW)

Q Data Output

Absolute Maximum Ratings

Any Pin with Respect

to V_{SS}
Storage Temperature
Operating Temperature

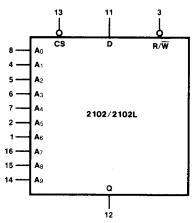
-0.5 V to +7.0 V
-55°C to +150°C

DL: -55°C to +85°C

DM: -55°C to +125°C

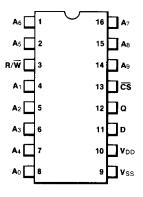
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



V_{SS} = Pin 9 V_{DD} = Pin 10

Connection Diagram 16-Pin DIP



(Top View)

Package	Outline	Order Code			
Ceramic DIP	6Z	D			
Flatpak	II	F			

Note

The Flatpak has the same Pin number to function correspondence as the DIP.

DC Requirements Over full operating temperature range unless otherwise specified

Symbol			2102 DL/D	M, 2102L DL/DM		
			С			
	Characteristic, Note		Min	Max	Unit	Condition
VIH	Input HIGH Voltage	H,F,1	2.0	V _{DD}	1,,	
		2	2.2	V _{DD}	v	
VIL	Input LOW Voltage	H,F,1	-0.5	0.8		
		2	-0.5	0.65	v	
V _{DD}	Power Supply Voltage		4.5	5.5	v	

DC Characteristics V_{DD} = 5.0 V \pm 10%, V_{SS} = 0 V, over full operating temperature range unless otherwise specified

Symbol	Characteristic	2102 DL/	M, 2102L DL/DM		
		Min	Max	Unit	Condition
Voн	Output HIGH Voltage	2.2		V	$I_{OH} = -100 \mu\text{A}$
V _{OL}	Output LOW Voltage		0.45	V	I _{OL} = 2.1 mA
IN	Input Leakage Current		10		V _{IN} = 5.5 V
Юн	Output HIGH Leakage Current		10	μΑ	V _{OUT} = V _{OH(Min)} CS = V _{IH(Min)}
IOL	Output LOW Leakage Current		-50	μΑ	V _{OUT} = V _{OL(Max)} CS = V _{IH(Min)}
loo	Power Supply Current 2102 2102L		60 30	mA	Inputs = 5.5 V D _{OUT} open, T _A = -55°C

AC Requirements Over full operating temperature range unless otherwise specified

Symbol	Characteristic	2102H 2102LH DL/DM	2102F 2102LF DL/DM	21021 2102L1 DL/DM	21022 2102L2 DL/DM	Unit	Condition
		Min	Min	Min	Min		
tcyc	Read or Write Cycle Time	250	350	450	650	ns	V _{SS} = 0 V See DC Requirements for Conditions on V _{DD}
t _{AW}	Address to Write Time	20	20	20	200	ns	
twp	Write Pulse Width	170	170	200	350	ns	
twR	Write Recovery Time	0	0	0	50	ns	
tDS	Data Set-up Time	170	170	200	350	ns	
tDH	Data Hold Time	0	0	0	20	ns	
tcw	Chip Select to Write Time	170	170	200	400	ns	
twc	Write to Chip Select Time	0	0	0	50	ns	

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2102/2102L

Symbol	Characteristic	2102H 2102LH DL/DM		2102F 2102LF DL/DM		21021 2102L1 DL/DM		21022 2102L2 DL/DM					
		Min	Max	Min	Max	Min	Max	Min	Max	Unit	Condition		
tA	Read Access Time		250		350		450		650	ns	V _{SS} = 0 V See DC Requirements for Conditions on V _{DD}		
tco	Chip Select to Output Time		130		170		200		400	ns			
t _{OH1}	Data Valid after Address	40		50		50		50		ns			
t _{OH2}	Previous Data Valid after Chip Deselect	0		0		0		0		ns			
CIN	Input Capacitance		5		5		5		5	ρF	V _{IN} = 0 V, V _{SS} = 0 V		
Cout	Output Capacitance		10		10	İ	10		10	рF	f = 1 MHz, TA = 25°C		

For block diagram, functional description and timing diagrams refer to standard 2102 data sheet, Section 3.