Complete system testbech

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1 Report contents

This report contains a brief explanation of the different part in our project.

2 Structure

The overall structure of the system is seen in Figure 1.

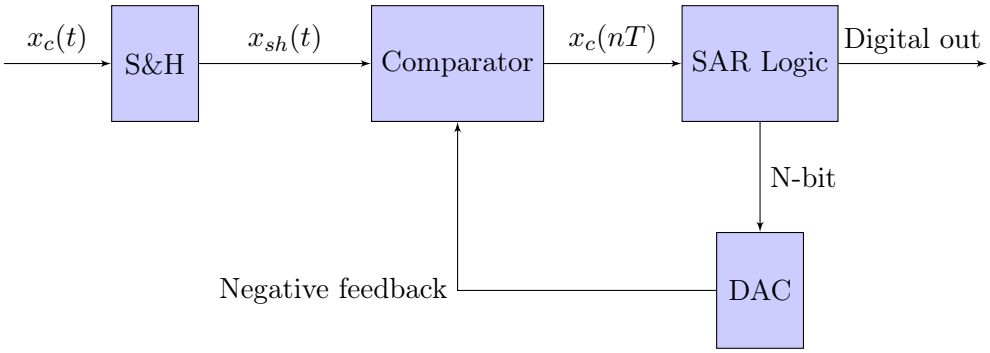

Figure 1: Block diagram

3 Schematic

We have not completed our resarch in circuits to use in this project. We have created schematics for some simple circuitis but we expect that some (or all) of the circuits is going to change.

Schematic: SAR_system

The SAR_system is the complete schematic for the whole system. It consists of a sample and hold block, a comarator block, the SAR logic and the

digital-to-analog converter block. Figure 2 shows the schematic that has been created.

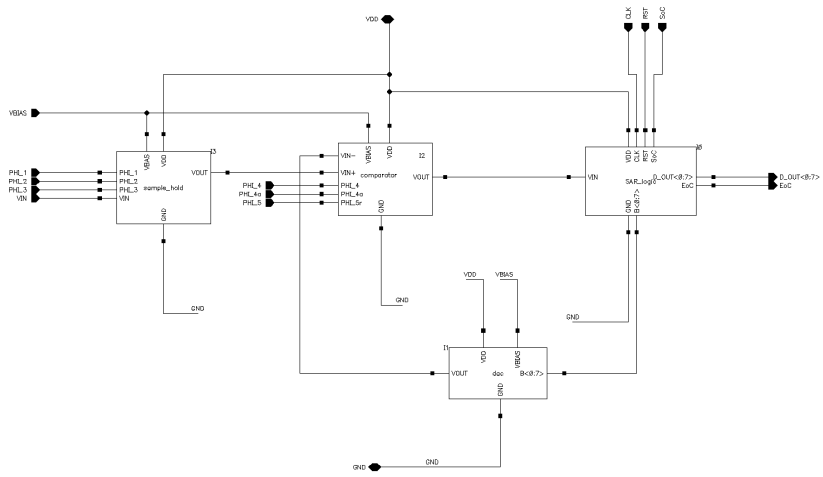

Figure 2: SAR_system

Schematic: sample_hold

The sample and hold (S/H) is based on a circuit provided by R. Jacob Baker in the book CMOS Mixed-Signal Circut Design **[CMOS-baker]**. The implementation is a single-ended S/H implementation. When ϕ_1 and ϕ_2 is high, ϕ_3 is low, and the bottom plate of the hold capacitor is charged by the input signal, while the top plate is held to ground by the feedback around the op amp. When the ϕ_2 is turned off, its charge will be injected into the low impedance input, VIN, since the impedance looking into the left of the ϕ_2 switch is large.

This implementation has not yet beed tested, and may therefor be changed during the project.

Schematic: comparator

The design of the comparator is based on a design in the book Analog Integrated Circuit Design by Carusone, Johns and Martin **[Analog-integrated]**.

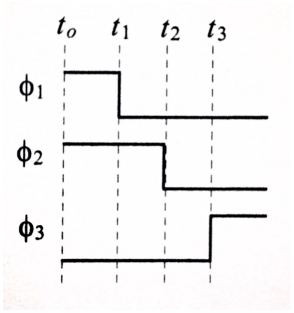

Figure 3: Single-ended S/H opartion [**CMOS-baker**]

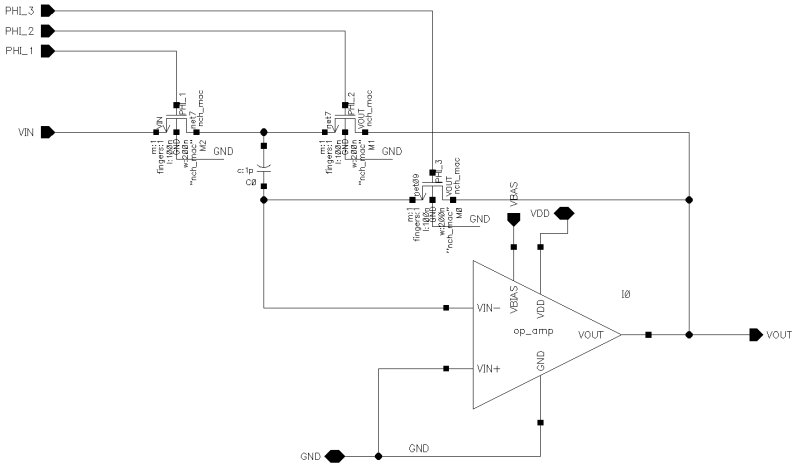

Figure 4: Sample and hold

Schematic: SAR_logic

Schematic: dac

This DAC circuit is based on the R-2R ladder from the book Analog Integrated Circuit Design by Carusone, Johns and Martin [**Analog-integrated**].

Schematic: op_amp

The op-amp circuit is ....

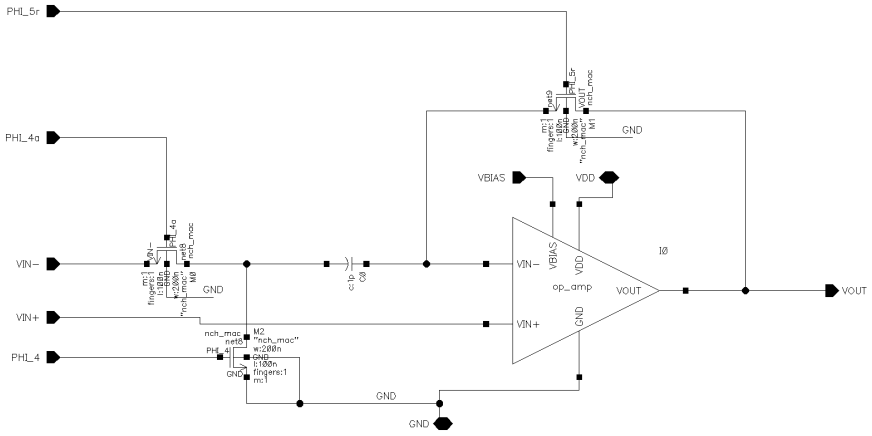

Figure 5: Comparator

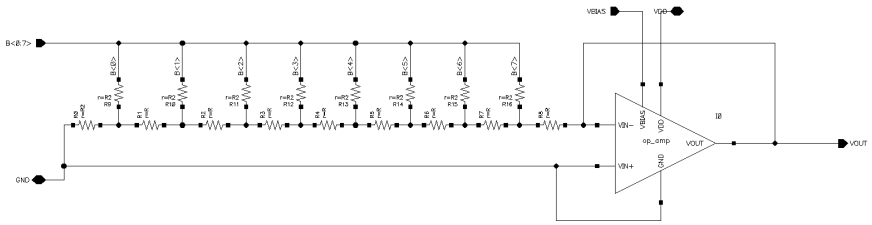

Figure 6: DAC

4 Test bench

In this section a short overview of the different test-beches for our components is presented.

Schematic: SIM_system

This is a complete system test bench. Here all the different components come together to form the full SAR-DAC architechture. Testing on a system level is nessesary to enshure that the circuit performes according to the interface the circuit provides to the outside world. This test senario is quite hard to set up since many signals have to be timed to each other. The verification of the circuit is also challanging since many signals has to be considerd. In order to manage this test we need to generate a test procedure with the spesified stimuli and check the results to a expected pattern.

Schematic: SIM_sample_hold

Schematic: SIM_comparator

Schematic: SIM_SAR_logic

Schematic: SIM_dac

Schematic: SIM_op_amp