A 12-bit 104-MS/s SAR ADC in 28nm CMOS for Digitally-Assisted Wireless Transmitters

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***Abstract*—A 12b 104MS/s successive approximation register analog-to-digital converter (SAR ADC) is presented for a digitally-assisted wireless transmitter system for use in cellular applications. A power-on calibration technique is implemented to correct capacitor DAC mismatch and reduce capacitor size, thereby relaxing the current consumption of the input buffer and reference generator. The total capacitor size is reduced to 0.6pF from 3.6pF required for 12-bit matching. The ADC analog core area is 0.003mm^2. After calibration, this work achieves 88dB SFDR at 26MHz sampling rate and 76.2dB SFDR at 104MHz sampling rate. Measured DNL and INL are 0.5LSBs and 1.1LSBs respectively. The ADC achieves both high speed and low power by combining several techniques: digital calibration, redundancy, asynchronous bit-cycling, monotonic switching, 25% duty-cycle sampling period, 3dB input gain, and a fully dynamic comparator The power consumption from 1.2V/1.1V supplies is 0.88mW for a single ADC core and 6.1-mW for the entire I/Q ADC, including the reference generator and input buffers. The ADC is fabricated in 28nm CMOS.**

Keywords—Successive approximation resigster analog-to-digital converter; SAR ADC; digital calibration SAR ADC; non-binary search SAR ADC; reference generatort

I. INTRODUCTION

In a typical cellular system, the wireless transmitter typically dominates the system power. Fig. 1 illustrates several techniques that can be used to increase power efficiency: Envelope Tracking (ET), Antenna Tuning (AT) and Digital Pre-Distortion (DPD). As shown in Fig. 1, the RF signal can be sensed, down-converted, digitized, and fed back to the digital baseband to enable closed-looped calibration. Traditional factory calibration reuses the downlink I/Q ADC for digitization, but this requires an extra analog multiplexor and extensive time and effort to characterize the different RF components under various operating conditions, especially over temperature. On-the-fly calibration is one solution and has the advantage of reducing the time and effort needed, but at the cost of extra feedback paths. Meanwhile, ET and DPD require higher linearity than is required in the transmitter signal path, in order to keep uplink performance. It is especially important to maintain high linearity over a frequency span from 2 to 3 times that of the baseband signal bandwidth since harmonics are key information to be extracted for digital baseband processing. Therefore, a low power, high linearity, and wide bandwidth ADC in the baseband feedback path is demanded. The SAR ADC is well known for its high speed, fully digital operation, state-of-the-art power efficiency,

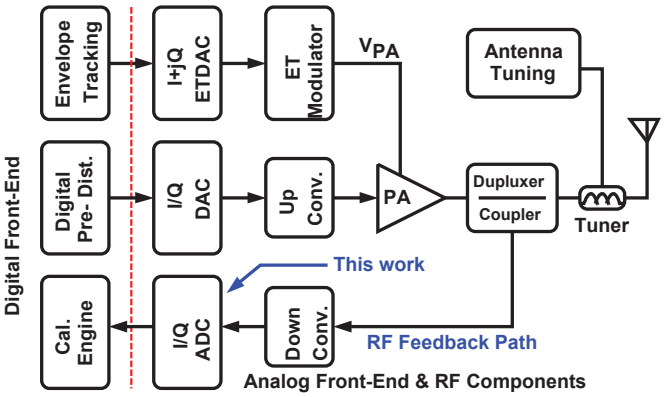

Fig. 1. Highly digitally-assisted wireless transmitter system

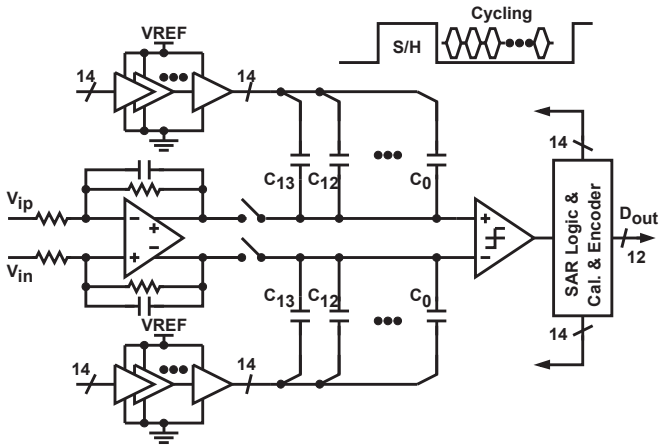

Fig. 2. SAR ADC architecture

and easy scaling to advanced process nodes. For these reasons, a SAR ADC is adopted in this application.

The remaining sections are organized as follows. Section II introduces the ADC architecture. Section III describes the low power techniques that are used, and Section IV shows measurement results and conclusions.

II. ADC ARCHITECTURE

Fig. 2 shows the single channel SAR ADC, including the input buffer, SAR core, and digital logic. The input buffer is composed of a class-AB amplifier with active RC low pass filter configuration. It also functions as an anti-alias filter to reduce RF noise folding into baseband. Moreover, the filter

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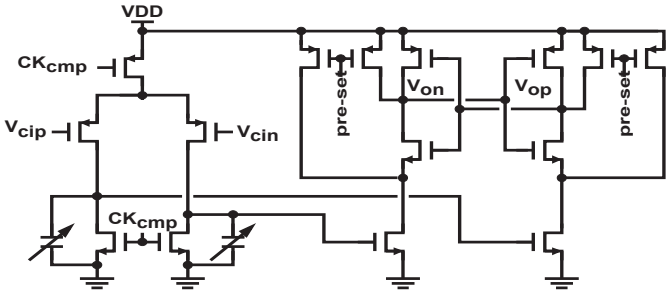

Fig. 3. Comparator with offset trimming.

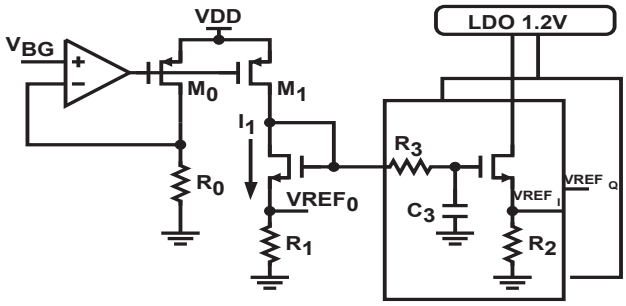

Fig. 4. Voltage reference generator

can prevent kick-back noise of the sampling switch from interfering to the RF band. A 3dB gain is provided by the input buffer to amplify the 1.2Vpp input swing to 1.7Vpp at the SAR input. As a result, the comparator noise requirement can be relaxed, which leads to lower power in the comparator.

The input buffer drives the capacitor DAC (CDAC) during the sampling interval via boot-strapped sampling switches. The sampling period is designed to occupy 25% of one clock period. This gives fully 75% of the clock period for the SAR conversion, easing the stringent timing for asynchronous bit-cycling, comparator metastability and reference settling. With this timing arrangement, power can be further optimized by minimizing the drive strengths of the digital SAR logic. During the sampling phase, the top-plates of the CDAC are connected to the sampling switch and the bottom-plates are connected to VREF. In the bit cycling phase, the bottom-plates are sequentially and monotonically switched to GND with each comparator bit decision [1].

As shown in Fig. 3, a dynamic pre-amplifier is used in the comparator, as it is more power efficient and faster than a static biased pre-amplifier. However, without a static pre-amp, the comparator kick-back noise which injects to the CDAC through Cgs and Cgd of the input differential pair presents a limiting factor for 12-bit resolution. Therefore, the device sizes of the dynamic pre-amplifier must be minimized, which induces large input referred offset. To overcome this, the comparator is designed with input offset trimming as part of the overall calibration procedure.

For a 104MS/s sample rate, one bit-decision period must be less than 500ps, which requires a very high speed reference voltage generator to satisfy CDAC settling. An open loop source follower architecture is used, as shown in Fig. 4. Since the ADC input full scale is determined by this reference voltage, it needs to be insensitive to temperature drift. In Fig. 4, $VREF_0$ is determined by I_1*R_1, so we choose the ratio of R_0/R_1 and PMOS M_0/M_1 to yield $VREF_0$=0.9V. $VREF_I$ and $VREF_Q$ are replicated from $VREF_0$, which tracks the band gap voltage, and are therefore insensitive to temperature and process variation. R3 and C3 form a low pass filter to isolate I and Q channels. Each source follower branch consumes 600uA and is supplied from a dedicated 1.2V LDO.

III. LOW POWER TECHNIQUES

A. Non-Binary SAR ADC

As mentioned in section II, in order for the CDAC to settle to a voltage smaller than 1LSB during single bit cycling, a very fast and power-hungry reference generator is required.

Although the CDAC is reduced to 600fF by the proposed mismatch calibration technique, analysis shows that the reference generator still has to burn 1.8mA in its output stage for a single channel, assuming a binary search algorithm is used. To reduce the required reference generator current, this work uses a non-binary search algorithm [2]. The non-binary algorithm introduces redundancy range for every decision step. If a decision error occurs at a certain step, the redundancy allows the error to be corrected in subsequent steps. Incomplete CDAC settling, reference generator ripple, and circuit noise can all cause a decision error. The error voltage should be well controlled within the redundancy range to guarantee correction capability in subsequent steps. Assuming the redundancy range of the *k-th* step is *r(k)* and the *k-th* CDAC output weight is *w(k)*, then the redundancy range can be expressed as $r(k)= w(k+2) + w(k+3) + ...+w(N) – w(k+1)$, where N is the last decision. A decision error occurring at the *k-th* step makes CDAC to output a wrong *w(k+1)*, which is then corrected by appropriate weighting of the following steps.

TABLE I. CAPACITOR WEIGHTS AND REDUNDANCY RANGE

decision step	Cap Weight	sum	redundancy (LSBs)	Redundancy (%)
0	2048	4335	319	15.6
1	984	2287	199	20.2
3	552	1303	95	17.2
3	328	751	71	21.6
4	176	423	55	31.3
5	96	247	23	24.0
6	64	151	15	23.4
7	36	87	7	19.4
8	22	51	1	4.5
9	14	29	n/a	0.0
10	8	15	n/a	0.0
11	4	7	n/a	0.0
12	2	3	n/a	0.0
13	1	1	n/a	0.0

In this work, 14 decision steps are used to achieve 12-bit accuracy with proper redundancy range. Table I shows the redundancy range in each decision step. MSB bit cycling will switch the heaviest weighted capacitors, resulting in the largest ripples at the reference generator output. Therefore, this work plans redundancy range in the 0 *to* 8^{th} steps. After amplification by the input buffer, the real input swing to the 12-bit ADC is 1.7Vpp, which maps to a digital code of 4095. The ADC requires a reference voltage of 0.85V for 1.7V input swing; however, using an even higher reference voltage will increase the speed of the capacitor drivers. Therefore, in this work, the full scale digital code is 4335 with a 0.9V reference voltage.

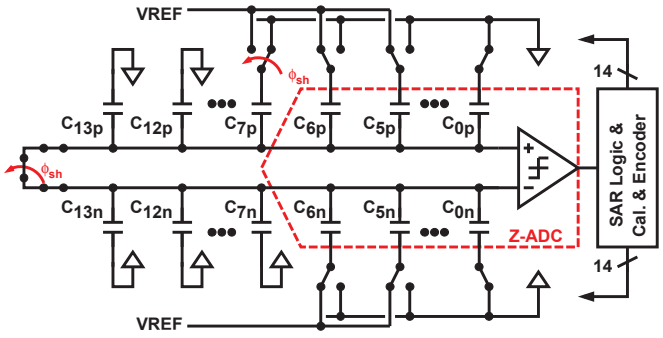

Fig. 5. SAR ADC configuration for calibration mode.

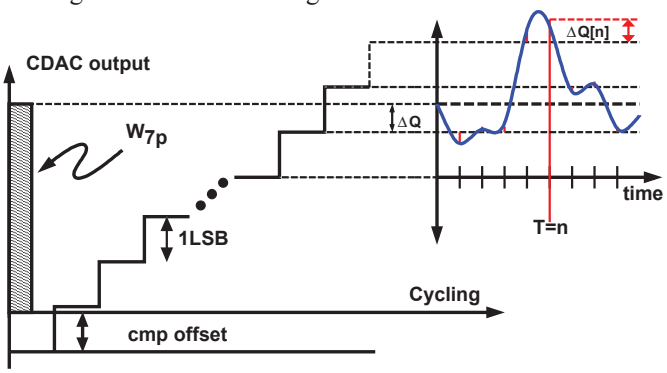

Fig. 6. Quantization noise spreading.

B. Capacitor Mismatch Calibration

If the CDAC were sized according to matching data, a 1.76fF unit capacitance and 7.2pF total capacitance are required to guarantee 3-sigma DNL of 1LSB at 12-bit resolution. With the proposed mismatch calibration, the unit capacitance size is relaxed to 0.29fF and is finally limited by the thermal noise requirement and difficulty in laying out tiny metal capacitors. The CDAC capacitance is reduced from 3.6pF to 0.6pF single-ended. Thus, the reference generator output driving current can be reduced to 600uA from 3mA, an 80% reduction. Furthermore, the capacitor reduction also reduces the current consumption of the input buffer by 72%.

In [3], a digital background capacitor mismatch calibration is used to overcome PVT sensitivity of some analog circuits, such as the residue amplifier. Thanks to the mostly digital circuits of the single stage SAR ADC in this work, only the comparator offset has a temperature dependency, and this would be cancelled at the system level. A simple, cost and power effective foreground digital calibration is adopted and performs well enough for the application. The hardware overhead is less than that of [3]. The hardware overhead for calibration only requires a multiplexor to force capacitors to be tied to VREF or GND, and a very simple averaging function in the digital engine. The calibration configuration is shown in Fig. 5. Even though the unit capacitor matching is relaxed, the CDAC 3-sigma estimated DNL caused by C_{0p}~C_{6p} and C_{0n}~C_{6n} is within 1LSB. That means calibration is not necessary for the LSB CDAC. As a result, the back-end ADC (called Z-ADC), that comprises only C_{0p}~C_{6p} and C_{0n}~C_{6n}, can be used to extract the real weights of C_{7p}~C_{13p} and C_{7n}~C_{13n}. The first capacitor to be calibrated is C_{7p}. The calibration forces C_{7p} to be connected to GND and shorts the two input nodes of sampling switches during the sampling phase. The Z-ADC capacitors are connected to VREF as in normal operation and the other MSB capacitors are fixed to GND. When sampling is finished, the other MSB capacitors are kept tied to GND while C_{7p} is switched to VREF. The CDAC output is determined by weight of C_{7p}, called w_{7p} as illustrated in Fig. 6. The Z-ADC digitizes the real value of w_{7p}. The real weight of C_{7n} is determined next by the same method and the results are saved in a look up table. The same method is then used to extract the weights of C_{8p} and C_{8n}, with the Z-ADC now comprised of C_{0p}~C_{7p} and C_{0n}~C_{7n}. After all the MSB capacitor weights are extracted, the ADC goes back to normal operation and the encoder will adjust the final digital output by the real capacitor weights.

Each capacitor weight extraction is repeated 512 times and averaged. In the absence of noise, the quantization noise (ΔQ in Fig. 6) would be the same each time and averaging 512 times would not increase the resolution of the Z-ADC. The method we use to increase the resolution of the Z-ADC to greater than 12-bit is to inject a white noise (blue line in Fig. 6) which spreads ΔQ[n]. This white noise is uncorrelated to ΔQ[n]; therefore, zero mean white noise is cancelled after averaging and quantization noise becomes close to zero. The white noise comes from intrinsic circuit noise.

Comparator input referred offset is also included in the Z-ADC output. The calibration extracts C_{7p} and C_{7n} and both of them include comparator offset. When we calculate the difference of C_{7p} and C_{7n}, the offset is cancelled. The calibration assumes that the weight summation of decision steps 7^{th}~13^{th} (87 shown in Table I,) must be larger than the weight of step 6^{th} (64 shown in Table I,). On the other hand, CDAC output plus comparator offset in Fig. 6, must be higher than w_{7p} after Z-ADC bit cycling is finished. Large comparator offset may cause calibration out of range and hence the comparator offset must be well controlled. Sizing the input pair larger will create serious SNR degradation by kick-back noise, however. Instead, offset is auto-trimmed before mismatch calibration in this work. At first, the pre-amplifier differential inputs are shorted; the output loading capacitance of pre-amplifier is then trimmed according to the 32 comparator outputs. Offset trimming effectively minimizes offset and kick-back noise simultaneously.

IV. Experimental Results

Fig. 7, shows the measured DNL and INL. The DNL is improved to 0.5LSBs from 1LSB and the INL is improved to 1.1LSBs from 4LSBs by calibration. Because of the monotonic switching procedure, the CDAC switching is not fully differential as the input goes away from mid-scale towards plus and minus scale. Due to this, noise sources, such as comparator kick-back, will now become signal dependent and the resulting DNL will show as bow tie shape. Fig. 8 shows the measured spectra at 26MS/s for the verification of the calibration with minimum dynamic interference. The results show a SFDR of 88.3dB after calibration, a 23.4dB SFDR improvement and a 3.7dB improvement in SNDR. With the ADC operating at 104MS/s, Fig. 9 shows the SNDR is 60.5dB and SFDR is 76.2dB after calibration. As the input frequency increasing to 12.6MHz, the SNDR becomes 57.7dB and SFDR is 72.1dB. The measured SNDR and SFDR are shown in Fig. 10. The input buffer bandwidth has been optimized for LTE uplink application, from DC to 3 times the baseband signal bandwidth.

The SNDR degradation is dominated by the insufficient close-loop gain of the input buffer at high frequency. Fig. 11, shows the die photo of the I/Q channel ADCs including the ADC cores, input buffers, reference generator, LDO, bias generator, and digital circuit. The ADC analog core occupies 0.003mm^2 and the total area is 0.047mm^2 including all the circuits.

The ADC performance summary and comparison with state-of-the-art is shown in Table II, including the performance of the ADC with input buffer and reference generator, the ADC core only (including the digital encoder power), and the ADC with just the reference generator. The power consumption of a single channel input buffer, ADC, and reference is 3.1mW. The FoM is 34fJ/conversion. The power consumption of a single channel ADC with reference is only 1.6mW resulting in a FoM of 13.2fJ/conversion. This work shows a compact area and comparable performance to [4], and [5].

TABLE II. PERFORMANCE COMPARISON

	This Work (One Channel)			[4]	[5]
	Buf. + ADC + Ref.	ADC	ADC + Ref	ADC + Ref	ADC + Ref
Technology	28nm			28nm	28nm
Resolution	12b			15b	14b
Sample Rate	104MS/s			100MS/s	80 MS/s
Supply(V)	1.2/1.1	1.1	1.2/1.1	1/1.8	1/1.8
Swing(Vpp)	1.2	1.7	1.7	2	1.4
Power(mW)	3.06	0.88	1.6	8	1.5
Peak SNDR(dB)	60.5	63	63	71	68
Area(mm^2)	0.024	0.003	0.007	0.1	0.14
FoM(fJ/conv.)	34	7.3	13.2	27.6	9.1

V. CONCLUSION

This work demonstrates a 12-bit 104MS/s SAR ADC with low power consumption achieved by a 3dB buffer gain, low kick-back dynamic comparator, monotonic switching, redundancy, and mismatch calibration. The calibration improves static linearity to 88dB SFDR. The techniques used reduce reference generator power by 80%, input buffer current by 72%, and capacitor size by 83%. This work is a very compact ADC for mobile application, and fabricated in 28nm CMOS technology. The FoM of the entire ADC is 34fJ/conversion and 7.3fJ/conversion for ADC core alone.

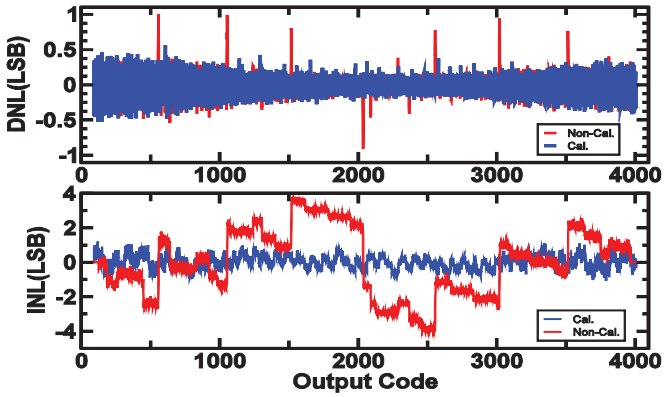

Fig. 7. Measured DNL/INL Calibrated and Non-Calibrated.

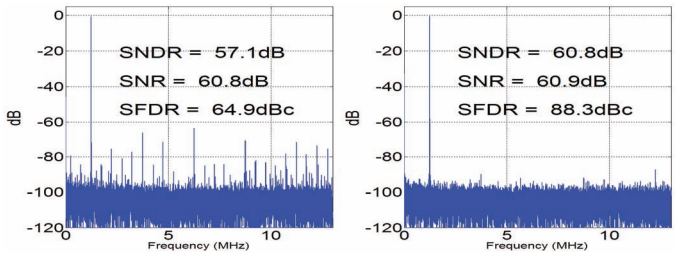

Fig. 8. Measured spectra before and after cal. at 26MS/s

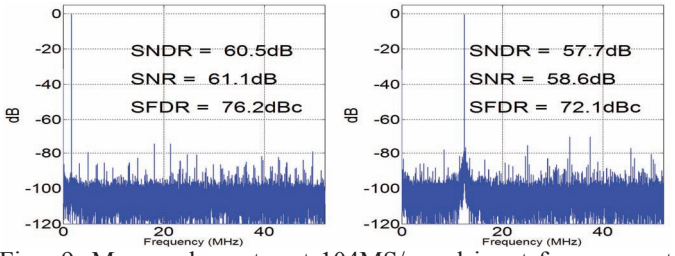

Fig. 9. Measured spectra at 104MS/s and input frequency at 1.6MHz and 12MHz.

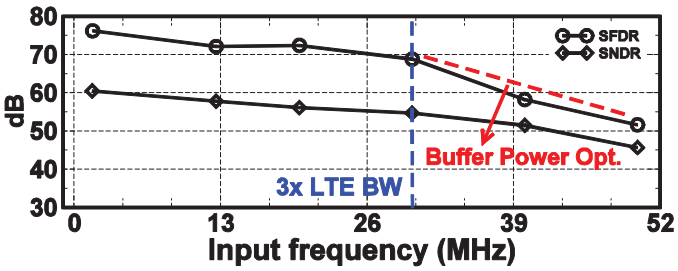

Fig. 10. SNDR and SFDR versus input frequency.

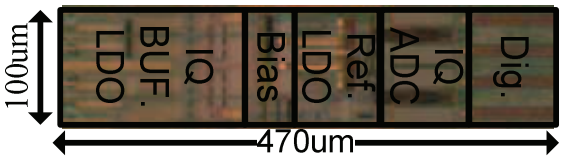

Fig. 11. Die Photo

VI. ACKNOWLEDGEMENT

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