ANALYSIS AND DESIGN OF SUCCESSIVE APPROXIMATION ADC AND 3.5 GHz RF TRANSMITTER IN 90nm CMOS

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ANALYSIS AND DESIGN OF SUCCESSIVE APPROXIMATION ADC AND 3.5 GHz RF TRANSMITTER IN 90nm CMOS

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LIST OF SYMBOLS AND ABBREVIATIONS

λ	Channel Length Modulation parameter
ℓ	Resistivity
β	Process Conductance
SOC	System on Chip
LO	Local Oscillator
PSRR	Power Supply rejection ratio
SAR	Successive Approximation Register
T&H	Track & Hold
S&H	Sample & Hold
DAC	Digital to Analog Converter
ADC	Analog to Digital Converter
TX FE	Transmitter Front end
IM3	Third order Intermodulation Distortion
P1dB	Gain Compression point
NF	Noise Figure

SUMMARY

The growing trend in wireless communication has lead to crowding of the available frequency bands. With a vast increase in digital media transfer, the focus has shifted towards designing multi-gigabit subsystems in silicon. In order to provide a cost effective solution, circuits designed in CMOS are implemented in a single system on chip.

The 90nm ST Microelectronics Digital CMOS process, optimized for digital circuit design requires a lot of internal compensation for analog circuits to meet the expectation. The three major causes for concern is process, temperature and supply voltage variation. The focus of this thesis is on the design of a feedback control loop, which uses temperature as the sensing element to control output power variation and the design of 3.5 GHz transmitter which acts as a feeder for multiband transmitter systems.

The focus is on two aspects of integrated circuit design. First one is on the challenges faced in the design of the various components of the feedback control loop – Successive approximation ADC, Encoder & Temperature sensor, while the second one is on the design of high linearity, low noise figure mixer and system level simulation leading to optimizing various components to achieve the target specifications.

CHAPTER 1

INTRODUCTION

Most high speed analog integrated circuits are fabricated in digital CMOS technologies. In the past years, the performance of digital CMOS circuit has improved with advances in digital technology. The minimum feature size has been constantly scaled down, which has imparted the capability to build digital circuits with smaller area, high speed and reduced parasitic. But analog circuits are still being made using longer channel length transistors due to the degrading effects of smaller channel length on the circuit performance. Digital circuits are scalable in nature, i.e. with the course of time; the same circuit has been scaled and moved on from older to newer technology. The design of circuits in short channel varies substantially from long channel design.

Motivation

The work presented in this thesis focuses on two aspects. First the design of Successive approximation data converters and their application in feedback control loops and second it focuses on the design of Gilbert cell mixer and System level design of Transmitter at 3.5 GHz. The design of multi-gigabit subsystems in silicon leaves a lot of aspects to be controlled. The output power of a transmitter is generally expected to be a constant parameter with changes in temperature or operating conditions of the chip. This is achieved by using a feedback loop to sense changes in output power and correspondingly control the power amplifier to meet the specifications. The 3.5 GHz transmitter acts as a feeder to 6-40 GHz wideband transmitter. Various parts of the 3.5 GHz transmitter have been revised multiple times to reach the linearity, intermodulation and noise figure requirements.

Organization of Thesis

The thesis is divided into seven different chapters excluding the introduction. The second chapter deals with the problems faced in designing circuits using short channel devices. The circuits developed using long channel devices are much more resilient to early voltage effect, whereas the same cannot be said about the short channel devices. To ensure the advantages of using short channel devices are well utilized and how the defects are overcome by adding additional compensation circuitry forms the focus of this chapter. Various factors affecting the performance in short channel devices has been discussed in detail with certain simulations to illustrate the short channel effects and how they perform when compared with long channel counter parts.

The third chapter focuses on the design of Successive approximation data converter (SAR) and its various components. The design of sample and hold circuit, comparator and SAR logic has been discussed from conceptual to transistor level design. Various forms of SAR Architecture have also been explored in terms of single ended design and fully differential design.

The fourth chapter focuses on the applications of SAR ADC. The temperature sensor based control of Transmitter front end has been discussed in detail along with the design of various components like temperature sensor, sense amplifier, SAR ADC, SPI and DC bias core control. The performance of the transmitter front end with and without feedback has been analyzed.

The fifth chapter focuses on the design of Bandgap reference for sub micron CMOS process. The design of first order bandgap reference to generate a constant bias voltage has been discussed with emphasis on PSRR and Output impedance.

The sixth chapter focuses on the design of upconversion mixer. The mixer design emphasis is on linearity, noise figure and intermodulation performance. The short channel effects pose a significant challenge in mixer design. The effect of transconductance and noise contribution of the devices based on their sizing has been analyzed in detail. Improved image rejection performance has been obtained by modifying the tank circuit and effect of image signal on the expected signal has been analyzed. The various methods to optimize mixer performance for linearity and noise figure performance have been analyzed in detail.

The seventh chapter focuses on the design of 3.5 GHz transmitter. The system level simulation of the 3.5 GHz transmitter and various performance specifications has been analyzed. The design of input buffer and RF filter has been presented and their impact on the overall system performance in terms of linearity and intermodulation performance has been discussed.

The Appendix A presents the verilog code for SAR logic design used in Data converters. The Appendix B presents the Matlab code used to measure DNL and INL for the ADC.

CHAPTER 2

IMPLICATION OF SHORT CHANNEL EFFECTS IN 90NM CMOS

Analog and RF integrated circuits are primarily fabricated on CMOS process optimized for digital design. The advancement in digital CMOS has allowed the device dimensions to shrink to 45nm or smaller. Digital circuit design benefits from reduction of channel length because it offers high speed, lower parasitic, lower area, low voltage and low power operation. Though the digital CMOS process can support extremely small channel lengths, most of the analog circuits are designed with long channel transistors in order to achieve the desired circuit performance. Sometimes the analog circuits are designed with a mixture of short and long channel lengths. Certain factors still form a roadblock to the use of short channel devices in analog design namely:

i. Short channel transistors have pronounced effect of channel length modulation thereby causing drastic variation in source to drain small signal resistance.

ii. Decreasing the channel length causes a decrease in effective channel area below the gate of the MOS transistor. Mismatch and noise are inversely proportional to the effective area and their effect becomes more pronounced with smaller channel lengths.

iii. Smaller channel length transistors are extremely notorious to dc biasing conditions. This introduces non-idealities in conventional biasing schemes like current mirrors. In a current mirror, when the device is operated in strong inversion a large variation in drain current as a function of output voltage is observed. This becomes even worse in weak inversion due to exponential dependence of the drain current on drain voltage.

Conventional analog circuit architectures cannot overcome the short channel effects. New architectures and design techniques are needed to make analog circuits work

properly. A band gap reference designed using short channel devices is described later in this work. The behavior of short channel devices is primarily observed by modeling, simulation and measurement where circuit performance of dc biasing, small signal gain, noise, mismatch and high frequency performance are briefly studied in the following section.

DC Operating Conditions

Proper dc biasing is the first step towards achieving desired performance. Most of the analog circuits are current biased using various current sources and sinks. The current bias does carry an inherent variation based on process, supply voltage and temperature characteristic of the reference generator. It is important to study the effect of smaller channel lengths on the performance of current sink and sources.

In a current sink the output current is expected to remain fairly constant over a wide range of output voltage range, i.e. the output resistance should remain fairly constant. The lower limit of the output voltage range can be referred to as $V_{\min}$, which is the point at which the current sink starts to deviate largely from its ideal behavior. This happens when the mirrored transistor moves from saturation to triode region. Basic current mirror and high swing cascode current mirror are considered and their performance with different channel lengths namely 2um, 1um, 0.7um, 0.25 um and 0.1um are presented.

The most commonly used current mirror and its performance are shown in the Fig. 2.1, works well for long channel devices but degrades with decreasing channel length. With short channel length the drain current suffers large channel length modulation effects.

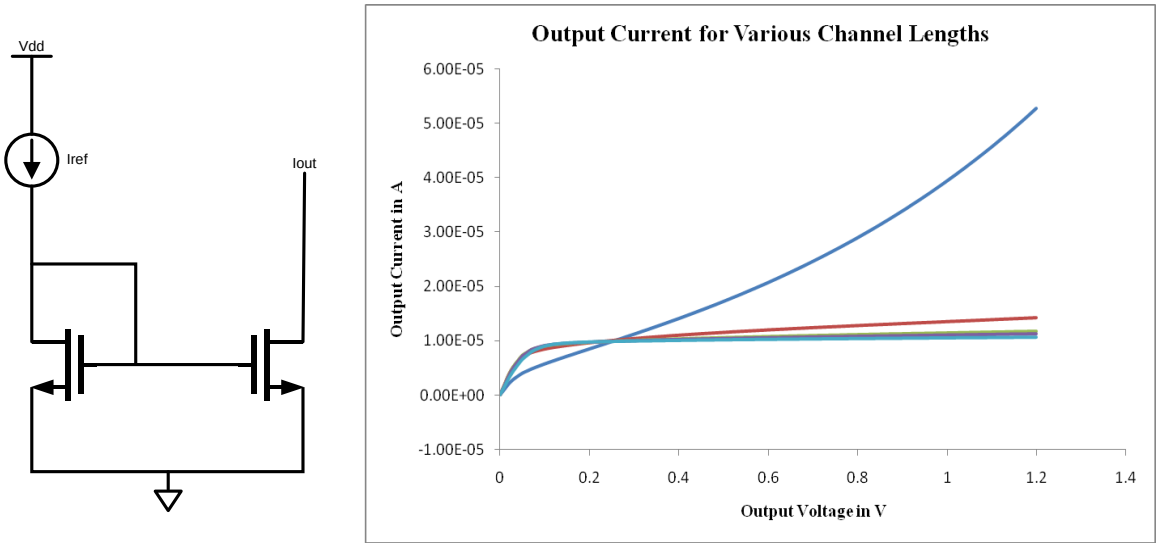

Fig 2.1 – Basic Current Mirror

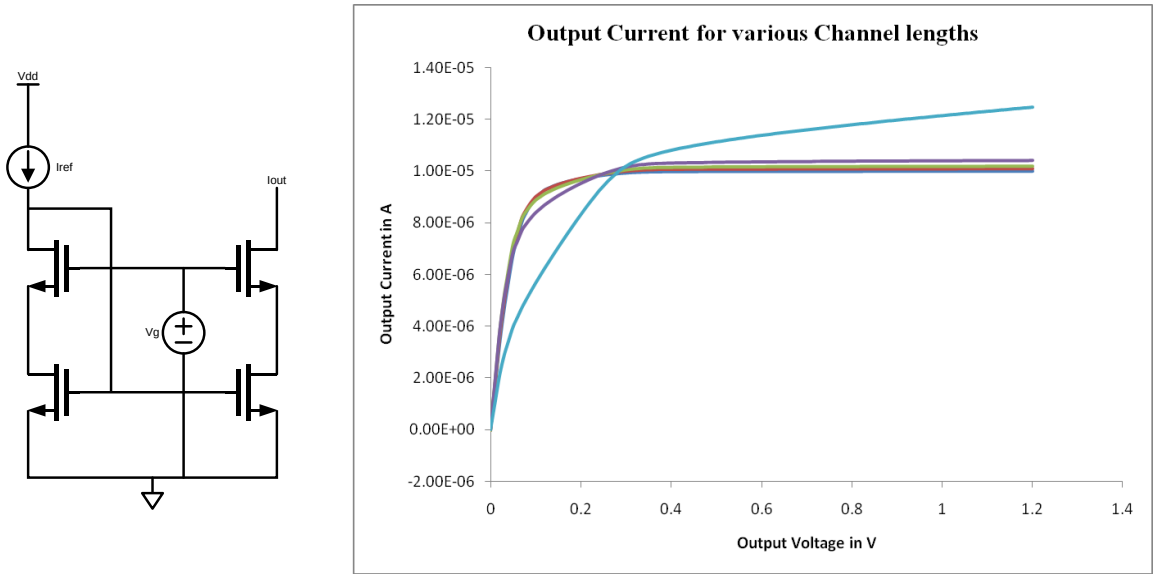

Fig 2.2 – High Swing Cascode Current Mirror

The high swing cascode current mirror and its performance are shown in the Fig. 2.2. It can be observed that with smaller channel length the mirror current remains appreciably constant over a wide output voltage range. The value of $V_{\min}$ is also small. This biasing scheme is the optimal choice for analog design with short channel devices but we have to live with the fact that it needs an additional biasing voltage.

Small Signal Gain

In most of the analog circuits, the small signal ac voltage gain is one of the most important specifications. For long channel devices the forward transconductance in moderate and strong inversion region is given as:

$$g_m = \sqrt{u_n C_{ox} \frac{W}{L} I_d} \tag{2.1}$$

The Eqn. (2.1) assumes square law model, but for smaller channel lengths, the drain current model tends to become linear primarily due to the degradation of mobility with decreasing channel length. While using small channel length, the expression for drain current and the transconductance beomces mathematically intensive and complicated. The reduction in channel length gives rise to large transconductance. The oxide thickness has also decreased causing an increase in transconductance of the device. On the other hand smaller channel length causes variations in output resistance given by drain to source resistance.

$$r_{ds} = V_A \big/ I_d \tag{2.2}$$

The early voltage decreases strongly with smaller channel length causing a decrease in drain to source resistance. The Fig. 2.3 presents a basic differential amplifier whose small signal gain has been measured again four different channel lengths.

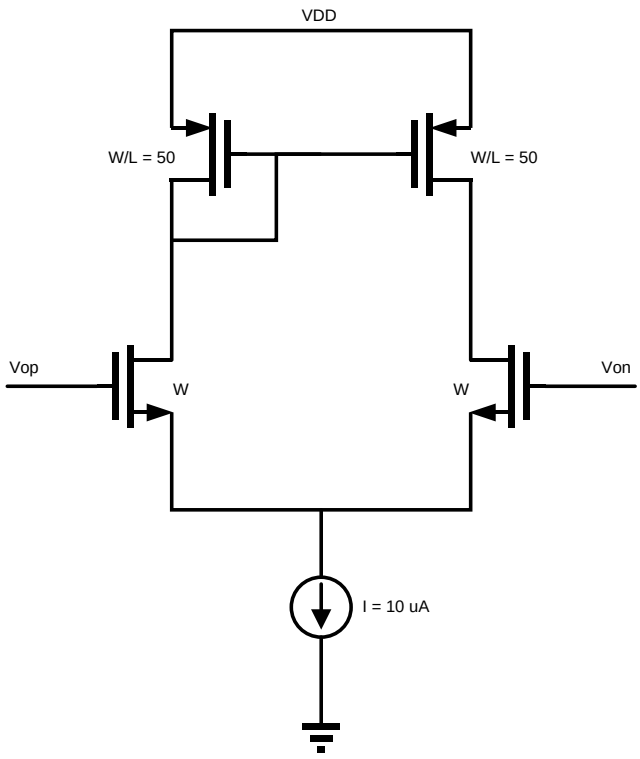

Fig 2.3 – Schematic of Differential Amplifier

Table 2.1 – Simulation results for small signal gain of Differential amplifier.

Channel Length L in um	Gain in dB
1.8	40
0.8	36
0.25	21

Mismatch

In high precision analog circuits transistor mismatch is intolerable. Mismatch in CMOS circuits gives rise to voltage and current offsets that degrade the circuit performance. Mismatch can be classified into two categories process mismatch and mismatch in design. Processing mismatch occurs in fabrication phase, where the devices with identical geometries in design have mismatched geometries after fabrication due to process defects and limitations. Mismatch in design is caused by improper biasing conditions. This gives rise to a systematic offset. An example for mismatch in design is given as follows:

i. In a differential input pair consisting of two identical MOS transistors with equal input voltages, but carry different currents.

ii. In a current mirror circuit, the mirrored and reference current are mismatched.

In most cases, the mismatches in design phase are eliminated with design techniques but the final offsets observed in circuits are caused during processing resulting in mismatch of transistor geometries. The analysis of mismatch in MOS transistors is largely based on analytical equations whose parameters have been extracted from experimental results. The drain current equation for NMOS in saturation with channel length modulation in account is given as:

$$I_d = \frac{u_n C_{ox}}{2} \frac{W}{L} (V_{gs} - V_{Th})^2 (1 + \lambda V_{ds}) \tag{2.3}$$

Where V_{Th} is the threshold voltage and λ is the channel length modulation parameter.

The threshold voltage can be expressed as [2]:

$$V_{Th} = \phi_{MS} + 2 \mid \phi_F \mid + \frac{Q_D}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} \tag{2.4}$$

where, ϕ_{MS} is the metal semiconductor work function, ϕ_F is the Fermi potential of the bulk, Q_D is the average depletion charge density and Q_{SS} is the trapped charge density inside the gate oxide. The average depletion charge per unit gate area can be expressed as

$$Q_D = WL(\sqrt{2\varepsilon_{si} q N_{Sub}}) \tag{2.5}$$

Where, N_{Sub} is the substrate doping density. From the Eqn. 2.3 to 2.5, it can inferred that the mismatch during fabrication will cause

i. Mismatch in threshold voltage of the devices.

ii. Mismatch in process transconductance.

iii. Mismatch in drain current.

The variance of *threshold voltage mismatch* is given as expressed in [2]

$$\sigma_{V_T}^2 = \frac{A_{W_T}^2}{WL} + \frac{A_{2V_T}^2}{WL^2} + \frac{A_{3V_T}^2}{W^2 L} \tag{2.6}$$

for smaller values of L, the second term in R.H.S of Eqn. (2.6) will cause a large variance in threshold voltage. The third term in R.H.S of Eqn. (2.6) will cause a reduction in the variance of the threshold voltage with increasing channel width. In general, it is found that the effect of the second term is much larger than the third term when the geometries are varied. Thus, it can be summarized that

(a) For large values of W and L , the variance of the threshold voltage reduces to

$$\sigma_{V_T}^2 = \frac{A_{W_T}^2}{WL} \propto \frac{1}{Area} \tag{2.7}$$

(b) For large W and extremely small channel lengths, the variance of the threshold voltage becomes

$$\sigma_{V_T}^2 = \frac{A_{W_T}^2}{WL^2} \propto \frac{1}{L^2} \tag{2.8}$$

Generally, the standard deviation of the threshold voltage mismatch is inversely proportional to square root of the device area. In [7], based on experimental results with smaller channel lengths, it was found to vary inversely with three quarters of the area. The smallest threshold voltage mismatch can be obtained for large *L* and small *W*. But this condition may not be suitable for the design requirements where mostly higher aspect ratios (W/L) are needed for larger transconductances. In [4], it is suggested that the threshold voltage mismatch can be optimized using the condition $W_{drawn}/L_{drawn} = DW/DL$ where *DW* and *DL* are the lateral out-diffusions along the channel width and the channel length respectively during processing. This condition will make the aspect ratios for the transistors constant, and it might not agree with the design requirements.

β mismatch: β can be expressed as

$$\beta = \mu C_{ox} \frac{W_{eff}}{L_{eff}} \tag{2.9}$$

The variation in β is primarily caused by variations in the mobility and the device dimensions. The effect of mobility variation (caused by dopant variation) is the most dominant. In general, β mismatch follows the same trend as the threshold voltage mismatch.

Drain current mismatch: In [9], the relationship between drain current mismatch and mismatches in V_T and β was derived as

$$\frac{\sigma^2(\Delta I_D)}{I_D} = \frac{\sigma^2(\Delta\beta)}{\beta^2} + 4\frac{\sigma^2(\Delta V_T)}{(V_{GS} - V_{Th})^2} \tag{2.10}$$

Mismatch in drain current will result in “systematic offset”. The improvement in drain current matching requires improved matching for both V_T and β. The conditions for

better V_T and β matching are the same: larger channel lengths have better matching than smaller channel lengths, and larger device area improves matching. There is another aspect of matching related to back-gate bias for MOS transistors in weak inversion [3,5]. The source-to-substrate bias can play an important role in matching of the drain current. The minimum feature size studied in [3,5] was 1.2 μm. In this study, the following were shown for weakly inverted MOS devices through experimental data:

(a) Reversed-biased source-to-substrate junction degraded matching in the drain currents.

(b) Forward biased source-to-substrate junction improved matching of the drain currents.

This study showed that forward biasing the bulks can yield better matching, but it imposes problems of latch-up, and the magnitude of forward-biased current through the source-to-bulk diodes need to be controlled for proper circuit operation. The actual matching performance of different device geometries can be studied through experimental data as done in [2-10]. It can also be studied through design for different channel lengths. When designing circuits using minimum feature-size channel lengths, the following conclusions can be drawn about matching,

- Small channel lengths worsen matching. With smaller channel lengths, the widths need to be made larger to achieve some improvement in matching due to larger device area. Larger widths will tend to make the device operate in weak inversion.
- Transistors, when operated in weak inversion can have improved matching with forward biasing of source-to-substrate junction diodes.

Limits on Supply Voltage

The current state of the CMOS technology has allowed tremendous downscaling in geometry, but it has also scaled down the limits of the power supply voltages. In most of the current CMOS processes, the maximum allowable supply voltage is less than 1.8

volts. Using a first-order approximation, the maximum supply voltage in a process can be approximated as 10 times the minimum feature size in that process. Application of higher supply voltages can result in higher reversed-biased diode junction voltages (like across the drain substrate junction), and it can cause avalanche breakdown of the junctions. The Gate oxide thickness has also decreased causing an increase in the electric field inside the oxide. For higher gate bias voltages, the electric field inside the gate oxide can exceed the maximum value of the critical electric field for oxide breakdown causing large tunneling gate current. With smaller channel lengths, the distribution of potential near the drain end becomes steeper, and the derivative of the potential (electric field) near the drain end is large. This causes hot carrier degradation due to the generation of hot electrons and holes. Thus, the performance of the smaller channel length devices will get degraded further with technology scaling.

Noise

The limits of supply voltage are being scaled down with the scaling of the CMOS technology. The output swing levels of the circuits are dependent on the supply voltage, which are also getting scaled down with technology. For most of the analog circuits, dynamic range is an important specification. The upper limit of the dynamic range is dependent on the maximum output swing level, and the lower limit is dependent on the noise floor. Since the upper limit of the dynamic range is getting scaled down due to downscaling of the supply voltage, there is tremendous need to reduce the noise floor to achieve appreciable dynamic range. So, circuits designed in minimum channel lengths should have low noise. In CMOS circuits, the various sources of noise can be visualized as [11]:

- Flicker or $1/f$ noise: This noise is due to the random generation and recombination of carriers at the interface. The generation and recombination lifetime of these carriers is

large, thus this kind of noise is very dominant in lower frequency, and it is negligible in higher frequencies. In a MOS transistor, flicker noise can be expressed as

$$i_n^2 = \left[\frac{\frac{KF}{2K'WLC_{ox}}}{f} \right] \Delta f \qquad (2.11)$$

Where, *KF* is the noise factor, and *f* is the frequency. This is the dominant source of noise at low frequencies. With technology scaling, the values of K' and C_{ox} are increasing, which will lower the flicker noise, but the use of smaller channel lengths will cause more noise due to decrease in area as suggested by Eqn. (2.11). So, when designing circuits at minimum channel length, larger widths should be used to reduce flicker noise. The flicker noise can also be reduced by switched-biased techniques [12-14]. If a switching pulse waveform is used to periodically switch the circuit from *on* to *off* state, then the flicker noise is present only in the *on* cycle when the carriers are present in the channel. In the *off* state, the channel is depleted of carriers, and the flicker noise is negligible. Using a 50% duty cycle of the switching waveform, the flicker noise can be reduced by a factor of 2. This technique is specially suited for oscillators whose phase noise can be reduced using this technique. In [12,13], it is also reported that larger reduction of the flicker noise can be achieved by turning *off* the device from strong inversion to strong accumulation. The reduction in the flicker noise is directly proportional to how much the device is pushed from inversion into accumulation. This reduction in the flicker noise is also inversely proportional to the switching frequency.

When using smaller channel lengths, the most viable way to reduce the flicker noise is to increase the width of the input transistors and maintain very high gain from the input to the output. Thus, the input stage will become the dominant source of noise, and the gain will reduce the noise contributions from various other elements in the following

stages of the circuit. In Fig. 2.4, simulation results for the flicker noise at 1 Hz are presented. The channel length of the devices was fixed at 0.1 μm. The widths of the input transistors were varied to study their effect on the flicker noise. As expected, the flicker noise decreased with increase in the channel width.

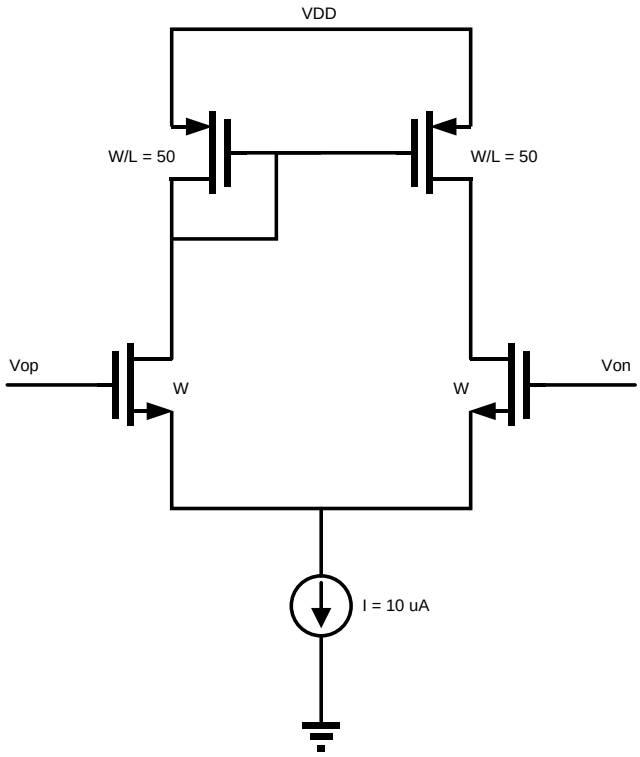

Fig 2.4 – Schematic of Differential Amplifier with L = 0.1 um.

Table 2.2 – Simulation results for Flicker Noise @ 1 Hz with various widths

Input Transistor Width W (um)	Flicker Noise @ 1 Hz (uV/sqrt(Hz))
6.25	16.64
25	8.89
100	5.15

- Thermal noise of the channel: Thermal noise is caused by the carriers in the channel. The channel acts as a resistor when inverted, and it gives rise to thermal noise. The classical noise model for drain thermal noise is given by

$$i_d^2 = 4kT\gamma(g_m + g_{mb} + g_{ds})\Delta f \tag{2.12}$$

Is a bias dependent parameter. The parameter, $\gamma = 2 / 3$ in saturation and $2 / 3 < \gamma < 1$ in the triode region. This noise model is valid only for long channel devices. In small geometry devices, most of the carriers travel with saturation velocity, and they cause more thermal noise in the channel. Various new thermal noise models have been proposed in [12,15,16] for smaller geometries, where the thermal noise was modeled as

$$i_d^2 = 4kT \frac{\mu_{eff}}{L_{eff}^2} Q_{inv} \Delta f \tag{2.13}$$

Where, μ_{eff} is the effective carrier mobility in the channel, Qinv is the inversion channel charge per unit area, and $L_{eff} = L - \Delta L$. L is the channel length, and ΔL is the reduction in the channel length caused in saturation due to extension of the drain depletion region into the channel. In small channel length devices operated in saturation, the thermal noise in the channel is very large due to smaller value of L_{eff} . Much of the increase in noise may be attributed to large channel length modulation and drain-induced barrier lowering effects. The thermal noise in the channel can be kept low with smaller values of Q_{inv}, which will correspond to smaller drain currents. Using back gate reversed-biased technique, the thermal noise in the channel can be reduced for devices with small channel lengths and large widths. Experimental results also show that the thermal noise in the channel is directly proportional to the drain current [15].

- Gate resistance noise: This noise is due to the thermal noise generated by the gate resistance, which is caused by the finite gate contact resistance and finite sheet resistance of the gate material. The gate resistance can be given by

$$R_g = R_{g,sq}\left(\frac{W}{3L}\right) \tag{2.14}$$

Where $R_{g,sq}$ is the sheet resistance of the gate. It is desired to have low sheet resistance and small aspect ratio to reduce the gate resistance noise. For MOS devices with polysilicide gates, this noise becomes insignificant.

- Induced gate noise: This noise is due to the thermal noise generated by the carriers in the channel, which capacitively gets coupled on to the gate as a gate current. This noise is highly correlated to the thermal noise in the channel. It is dependent on the value of the gate oxide capacitance. With shrinking technology, the gate oxide capacitance has increased, which has decreased the gate capacitive reactance. Thus, at lower frequencies, more capacitive coupling of thermal noise takes place from the channel to the gate. Smaller gate dimensions will reduce this noise effect due to reduction in the gate oxide capacitance, but this will tend to increase other noise effects.

In summary, the flicker noise can be reduced by using larger channel widths and switched-biasing techniques. Decreasing the drain current can reduce the thermal noise, but it will affect the circuit performance. The induced gate noise can be reduced with smaller device area, which generally is not a good choice.

High Frequency Performance

One of the major reasons for using smaller device dimensions is to achieve higher bandwidth. The bandwidth of a circuit is either limited by the external load capacitance, or the internal parasitic capacitances of the nodes. For smaller output load capacitances, decrease in the width and the length of the devices will cause a decrease in the parasitic capacitances, which will improve the bandwidth. In CMOS processes, a figure of high frequency limitation is given by the "*transition frequency*" parameter f_T, which is estimated as

$$f_T = \frac{g_m}{C_{gs}} \tag{2.15}$$

It is evident that transition frequency will increase as the device dimensions are scaled down because the transconductance of the MOS device increases with decrease in the channel length, which also causes a decrease in gate source capacitance. Overall, from Eqn. (2.15), smaller channel lengths will result in a higher transition frequency.

Distortion

One of the major reasons for using smaller device dimensions is to achieve higher bandwidth. Distortion is an important performance specification in most of the analog circuits. It is often given by THD (total harmonic distortion), which is a ratio of the power in the fundamental component to the combined power of all the higher order harmonics of the non-linear circuit. The power in the fundamental component is dependent on the linear gain of the circuit. In CMOS circuits, this linear gain is often the product of g_m and r_{ds} of the MOS devices. Small channel length devices tend to show linear transfer characteristics, i.e., their drain current varies almost linearly with the gate bias. This inherently makes the g_m almost constant with variations in the gate bias, which is an essential requirement for good distortion performance. On the other hand,

smaller channel length devices have poor r_{ds} due to large channel length modulation effects, and it varies appreciably with change in V_{ds} . This has a major effect on the reduction of the linear gain of the circuit, and it strengthens the harmonics. This causes a decrease in the power of the fundamental frequency component, which in turn degrades the THD performance.

Technology-Dependent Circuit performance

The various implications of using small channel length devices were discussed in the previous sections. In this section, various aspects related to the dependence of the circuit performance on the technology are discussed. The drain current equation of a MOS transistor in saturation is given by

$$I_D = K' \frac{W}{L} \frac{(V_{GS} - V_{Th})^2}{2} (1 + \lambda V_{DS}) \tag{2.16}$$

Eqn. (2.16) is valid only for long channel length devices, and it is an approximation for smaller channel lengths. In the Eqn. (2.16) K', V_{Th} , and λ can be seen as the *technology-dependent* parameters. Across different technologies, these 3 parameters will vary causing a change in the drain current. This will change the biasing conditions of the circuit and affect the circuit performance. The drain current is dependent on the *technology-dependent* parameters. Also, for smaller channel lengths, the drain current given by Eqn. 2.16 is an approximation. Various drain current models for short channel lengths have been proposed; the most popular being the BSIM models. For simplicity, the drain current equation for long channel devices is given by Eqn. (2.17)

$$I_D \propto (V_{GS} - V_{Th})^2 \tag{2.17}$$

For small channel length devices, the drain current can be approximated as

$$I_D \propto (V_{GS} - V_{Th}) \tag{2.18}$$

It can be concluded that the drain current is not only dependent on the *technology dependent* parameters but also on the channel length. To develop a scalable architecture, the circuit performance needs to be made independent of the design equations, because these equations are sensitive to both the *technology-dependent* parameters as well as the channel length. A unified approach needs to be developed that will yield technology as well as channel length insensitive circuits. One way to achieve this is by expressing the performance specifications of the circuit as ratios, which will result in the same performance across different technologies as well as channel lengths. The op amp has been chosen as an example circuit to study scalability and the impact of small channel lengths. In the following sections, some sample simulations of two commonly used op amp topologies will be presented for understanding the affect of the technology on the circuit performance.

A simple, two-stage, Miller-Compensated op amp is shown in Fig. 2.5. It is one of the most widely-used versions of the op amp. In this section, the performance of this circuit will be verified across two different CMOS technologies. The importance of this exercise is to understand the effect of *technology-dependent* parameters on the circuit performance. If the transistors of this op amp were scaled as-it-is into different technologies, then its performance will be affected. Simulations were performed on this op amp in 0.13 μ*m* CMOS and a 90 n*m* CMOS technology. The same circuit (with the same device sizes) was used in both the technologies. Their performance is compared in Table 2.4.

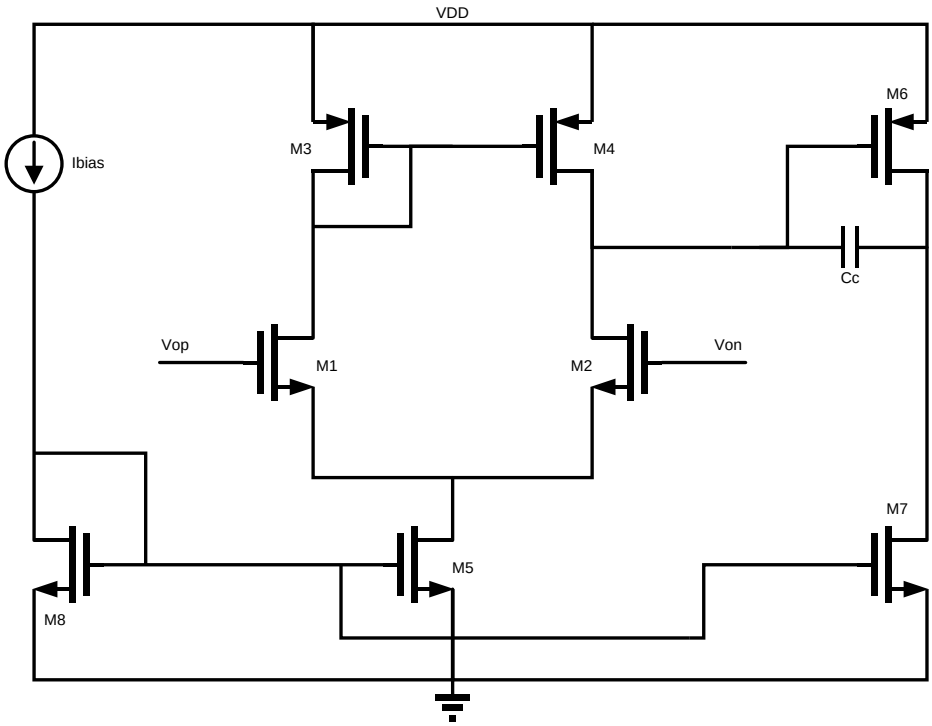

Fig. 2.5 – Schematic of Two Stage Operational amplifier with Current mirror load.

Table 2.3. Component values for Two Stage Operational Amplifier

Parameter	**Value**
Ibias	10 uA
M1 = M2 = (0.5) M5 = (0.5) M8	10
M3 = M4	10
M6	100
M7	100
Cc	0.5 pF

Table 2.4. Comparison of performance summary of Two Stage Operational Amplifier in 90 nm & 0.13 um CMOS with a Load capacitance of 1 pF.

Parameter	0.13 um CMOS	90 nm CMOS
Vdd	1.8 V	1.2 V
Small Signal Gain	73 dB	67 dB
Unity Gain Bandwidth	20 MHz	38 MHz
Phase Margin	56 deg	68 deg
Slew rate	20 V/uS	22 V/uS
ICMR	0.4 – 1.8 V	0.35 – 1.2 V
CMRR	81 dB	75 dB
PSRR	83 dB	71 dB
Input referred noise	8.2 uV/sqrt(Hz) @ 1 Hz	3.5 uV/sqrt(Hz) @ 1 Hz
Idd	80 uA	86 uA

Summary

It can be summarized that the performance of analog integrated circuits is affected by technology as well as channel length. The small and large signal parameters of the MOS transistors are dependent on the *technology-dependent* parameters, which vary largely across different technologies. Thus, when migrating from one technology to another, the aspect ratios need to be re-designed to maintain the desired performance. The channel length of the devices also affects the circuit performance. Circuit performance degrades with shrinking channel lengths. Thus, if the devices are scaled while migrating across different technologies, the circuit performance will depend on the scaled value of the device channel length, and most of the devices have to be re-designed for their aspect ratios to achieve the desired performance.

CHAPTER 3

SUCCESSIVE APPROXIMATION DATA CONVERTERS

Successive approximation ADC operates with medium conversion speed, moderate circuit complexity and high conversion accuracy. SAR ADC is one of the most popular Nyquist rate data converters. The terms “Divided reference algorithm” and “Binary search algorithm” can be used to best describe the basic principles of SAR data converter.

SAR Architecture

Successive approximation employs a binary search algorithm in a feedback loop including a 1 bit A/D converter. The Fig. 3.1 illustrates this architecture which consists of a front end track & hold circuit, comparator, DAC and SAR logic. SAR logic is basically a shift register combined with decision logic and decision register. The pointer points to the last bit changed in the decision register and the data stored in this register is the result of all comparisons performed during conversion period. During binary search, the circuit halves the difference between the sampled signal (V_{IN}) and DAC output (V_{DAC}). The conversion first sets MSB as 1 so that the DAC produces midscale at analog output. The comparator is then strobed to determine the polarity of $V_{IN} - V_{DAC}$. The pointer and the decision logic direct to logical output of the comparator to the MSB. If $V_{IN} > V_{DAC}$, the MSB of the register is maintained at 1 or else set to 0. Subsequently the pointer is set to choose the bit penultimate to MSB as 1. After the DAC output has settled to its new value, the comparator is strobed once again and the above sequence is repeated.

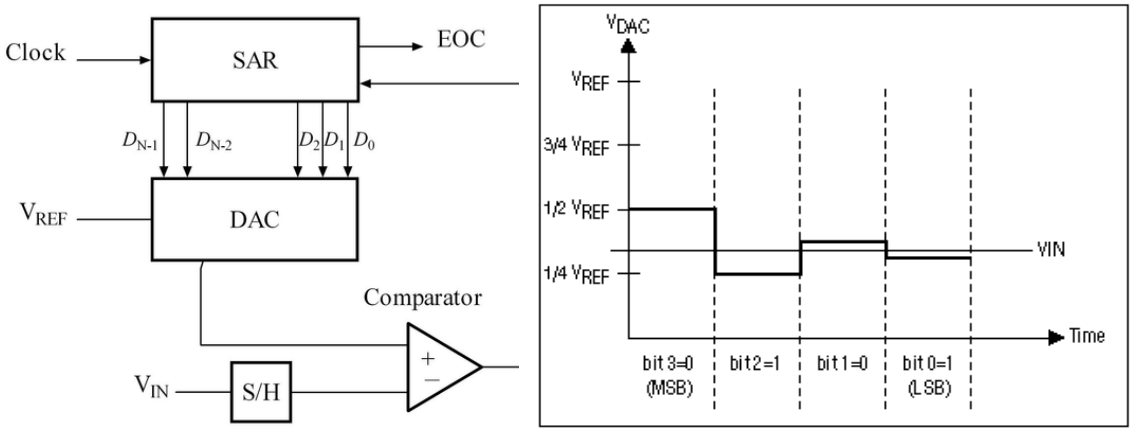

Fig 3.1 Block diagram of SAR ADC & DAC Output Waveform

For a resolution of M bits, the successive approximation architecture is at least M times slower than the full-flash configurations, but it offers several advantages.

- The comparator offset voltage does not affect the overall linearity of the converter because it can be represented as a voltage source in series with Sample & hold output, indicating that offset voltage simply adds to analog input and hence appears as an offset in the overall characteristics. Consequently the comparator can be designed for high speed operation in high resolution systems.
- This architecture does not require an explicit subtractor which is an important advantage for high resolution applications
- The circuit complexity and power dissipation are in general less than that of the other architectures.

If the Sample & hold circuit provides the required linearity, speed and comparator input referred noise is small enough, and then the converter's performance depends primarily on the DAC. In particular differential and integral non linearities of the converter are given by those of the DAC, and the maximum conversion rate is limited by its output settling time. In the first conversion cycle, the DAC output must settle to maximum resolution of the system so that the comparator determines the MSB correctly.

If the clock period is constant, the following conversion cycles will be as long as the first one, implying that the conversion rate is constrained by the speed of the DAC.

Track & Hold

A sample-and-hold (S/H) or track-and-hold (T/H) circuit is frequently required to capture rapidly varying signals for subsequent processing by slower circuitry. The function of the S/H circuit is to track/sample the analog input signal and to hold that value while subsequent circuitry digitizes it. Although an S/H refers to a device which spends an infinitesimal time acquiring signals and a T/H refers to a device which spends a finite time in this mode, common practice will be followed and the two terms will be used interchangeably throughout this discussion as will the terms *sample* and *track*.

The function of a track-and-hold circuit is to buffer its input signal accurately during track mode providing at its output a signal which is linearly proportional to the input, and to maintain a constant output level during hold mode equal to the T/H output value at the instant it was strobed from track to hold by an external clock signal. Fig. 3.2 shows the waveforms of a practical sample-and-hold circuit.

Several parameters describe the speed and accuracy with which this operation is performed. The *track mode* is the state when the T/H output follows the T/H input. The *hold mode* refers to the period when the T/H output is maintained at a constant value. *Track-to-hold transition* is the instant when the circuit switches from the track mode to the hold mode and the *hold-to-track transition* refers to the switch from hold mode back to track mode. The time between successive *track-to-hold transitions* is the *sample period* that's reciprocal is the *sample rate*.

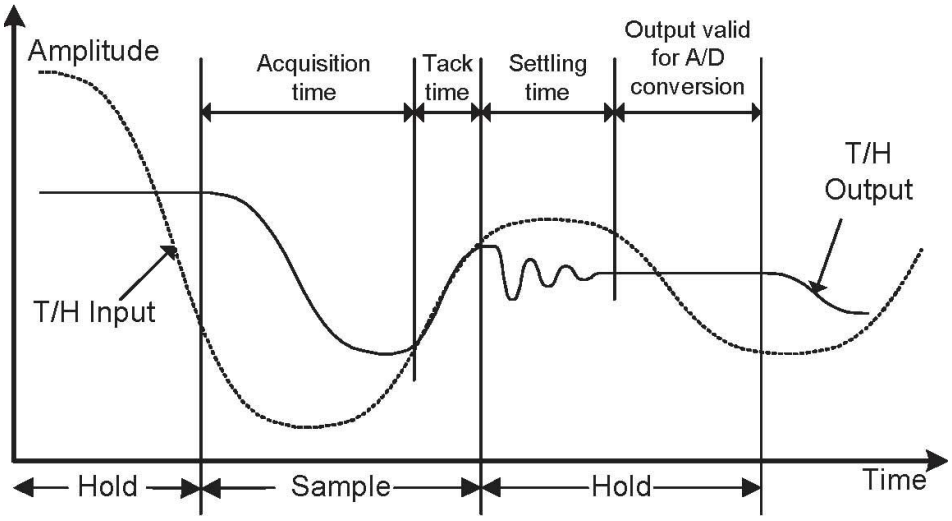

Fig. 3.2 – Track & hold terminologies

In track mode, the T/H functions as a simple buffer amplifier. While in the hold mode two effects are of primary importance. The first is *droop* which describes the decay of the output signal as energy is lost from the storage element (usually a capacitor) within the T/H circuit. This is usually not a problem for CMOS amplifiers which have infinite DC input impedance. The second important aspect of hold mode performance is *feedthrough*, which describes the unwanted presence at the T/H output of a signal component proportional to the input signal. The *signal feedthrough* is usually described as the ratio of the unwanted output signal to the input signal amplitude.

The *acquisition time*, is the time during which the sample-and-hold circuit must remain in the sample mode to ensure that the subsequent hold mode output will be within specified error band of the input level that existed at the instant of the sample and hold conversion. The acquisition time assumes that the gain and offset effects have been removed. The remainder of time during the track mode exclusive of acquisition time is called the *track time* during which the T/H output is a replica of its input.

The *settling time*, is the time interval between the sample-and-hold transition command and the time when the output transient and subsequent ringing have settled to within a specified error band. Thus, the minimum sample-and-hold time is equal to the sum of acquisition time and settling time. The remainder of the time during the hold mode represents the maximum time available for A/D conversion if the T/H is used for that purpose. *Conversion time* of an A/D converter is the interval between the convert command and the instant when the digital code is available at the ADC output. Therefore, the minimum sample period of a practical A/D converter system is the sum of acquisition time, settling time, and conversion time.

The track-to-hold transition determines many aspects of sample-and-hold performance. The *delay time* is the time elapsed from the execution of the external hold command until the internal track-to-hold transition actually begins. In practical circuits this switching occurs over a non-zero interval called the *aperture time* measured between initiation and completion of the track-to-hold transition. Practical circuits do not exhibit precisely the same sample period for each sample. This random variation from sample to sample is caused by phase noise on the incoming clock signal and further exacerbated by electronic noise within the sample-and-hold itself. The standard deviation of the sample period is termed the *aperture jitter*. The time jitter causes an amplitude uncertainty, which depends on the rate of rise of the signal at the sample point. Finally, at the track-to-hold transition, circuit effects frequently give rise to a perturbation at the sample-and-hold output. This effect which manifests itself as a discontinuity in the sample-and-hold output waveform called *hold jump* or *hold pedestal* can depend on the input signal giving rise to distortion.

A large number of Sample & Hold limitations originate from non-idealities of the sampling switch. Aperture jitter, nonlinearity, pedestal error, feed through and SNDR of these circuits are strongly influenced by the sampling switch performance.

A MOS transistor can be used as an analog switch with its gate voltage controlling the resistance between its source and drain. The ON resistance of the device is given by

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \tag{3.10}$$

For a fixed sampling capacitor, the acquisition time can be decreased only by lowering the ON resistance. In a given CMOS process the mobility and oxide capacitance are normally constant and gate-source voltage cannot exceed the supply voltage leaving only the aspect ratio of the device as the control variable. In addition to finite channel resistance, the MOS switches exhibit channel charge injection and clock feedthrough. When MOS is on, it carries certain amount of charge in its channel that, under strong inversion conditions can be expressed as

$$Q_{ch} = WLC_{ox}(V_{GS} - V_{TH}) \tag{3.11}$$

When the device turns off, this charge leaves the channel through the source and drain terminals, introducing an error voltage on the sampling capacitor. This error appears as an offset if Q_{ch} is constant, a gain error if Q_{ch} is linearly proportional to the input signal, or a nonlinear term if Q_{ch} has a nonlinear dependence on the input signal. While the first two types of errors can be tolerated when data converters used in digital signal processing applications while third type limits linearity of the sample and hold and contributes to harmonic distortion. The nonlinear component in Q_{ch} arises primarily from the nonlinear dependence of threshold voltage on the input voltage through body effect. The fraction of charge injected into the source and drain terminals also depends on the impedance seen at

the nodes and clock transition time. In practice, it is difficult to accurately predict these variables or apply the error figures measured for a given topology to another circuit.

Another source of error in MOS switches is clock feed through, caused by the finite overlap capacitance between the gate and source or drain terminals. The control voltage applied to the gate of the device changes state to turn the switch off, C_{ov} (Gate to drain junction capacitance) conducts the transition and changes the voltage stored on holding capacitor by an amount equal to

$$\Delta V = \frac{C_{ov}}{C_{ov} + C_H} V_{CK} \tag{3.12}$$

Where V_{CK} is the amplitude of the control signal. This clearly indicates that clock feed through is independent of the input signal if C_{ov} is constant and thus appears as an offset in the input/output characteristic. A frequency dependent nonlinearity error in MOS sampling circuits arises from the variation of the switch on-resistance with the input voltage. For high frequency inputs this variation introduces input-dependent phase shift and harmonic distortion.

Another error that appears in high speed MOS sampling circuit stems from the input dependent sampling instant. Since the MOS switch turns off only when its gate source voltage has fallen below V_{Th}, the time at which the device turns off depends on the instantaneous level of input. If we assume an nMOS device, the circuit enters hold mode when the input signal is near the ground potential than when it's higher. This introduces jitter and harmonic distortion and it becomes noticeable when the clock transition time is comparable with the input signal slew rate. For a sinusoidal input with amplitude A and frequency f_{in}, the expression for Signal to Distortion ratio (SDR) of the Sample & Hold is given as

$$SDR_{\max} = 20\log_{10}\frac{V_{CF}}{Af_{in}t_F} - 4 \tag{3.13}$$

Where V_{CF} and t_F are the clock amplitude and fall time respectively. The sampling switch input and output range can also limit the full scale voltage swing of a sampling circuit. For a supply voltage of V_{DD}, simple NMOS based sample and hold circuit has a full scale range of $V_{DD} - V_{TH}$, where V_{TH} includes the body effect where appropriate. This can be overcome by using a transmission gate, which ensures rail to rail output swing.

The circuit implementation of the Sample & Hold circuit is given in the Fig. 3.3. The simple sample and hold circuit suffers with the problem of substantial charge injection, which is encounter by adding a dummy device M_2 with half the width of the sampling switch M_1 and is driven with complementary clock.

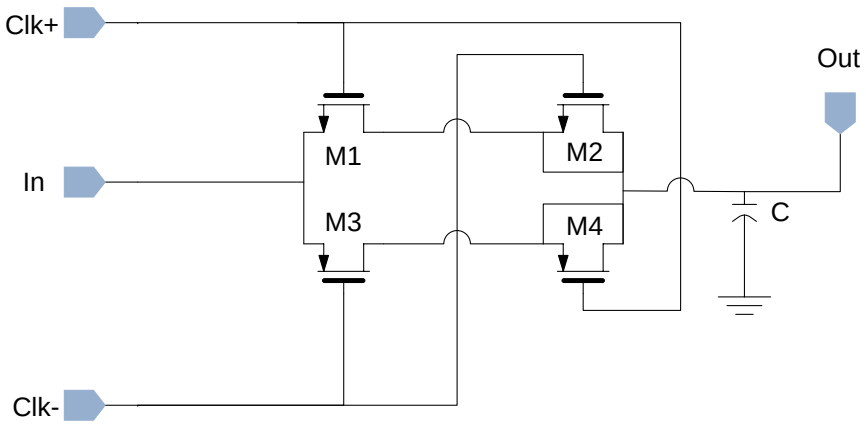

Fig. 3.3. Schematic of Sample & Hold circuit.

In the circuit when M1 turns off and injects charge onto holding capacitor C_H, M2 turns on and absorbs charge from the capacitor. Hence it is exactly half of the M1 channel charge is injected onto C_H, then complete cancellation occurs and the held voltage on C_H is not corrupted by charge injection. A pair of the same circuit can be used in differential fashion for Differential SAR ADC.

Comparator

The comparator can be basically defined as a quantizer where in the quantization noise forms the crux of the ADC design. A *quantizer* is a device that converts a continuous range of input amplitude levels into a finite set of discrete digital code words. Theoretically an *analog-to-digital conversion* process comprises a sampling and quantization processes. A/D converter system usually consists of a quantizer along with other signal conditioning circuitry such as amplifiers, filters, sample-and-hold circuits etc. Despite this difference, the terms quantizer and A/D converter are often used synonymously.

A quantizer can be uniquely described by its transfer function or quantization characteristic, which contains two sets of information: the first includes the digital codes associated with each output state, and the second includes the *threshold levels* which are the set of input amplitudes at which the quantizer transitions from one output code to the next.

Fig. 3.4 shows the transfer characteristic of an ideal 3-bit quantizer. The analog input voltage normalized to full scale (FS) is shown on the horizontal axis. The digital output code is given on the vertical axis. The quantizer has been designed so that the output digital word changes when the analog input is at odd multiples of FS/16. The LSB of the digital output code changes each time the analog input changes by FS/2*n* where *n* is equal to the number of digital bits. A change of $FS / 2^n$ in the analog input is called an LSB. In Fig. 3.4, an LSB is the length of the horizontal part of the stairstep, or FS/8. The ideally quantized ranges of the analog input are shown just above the horizontal axis on Fig. 3.4. These ranges are centered about even multiples of FS/16 except for the rightmost and leftmost, which have no right or left limits, respectively.

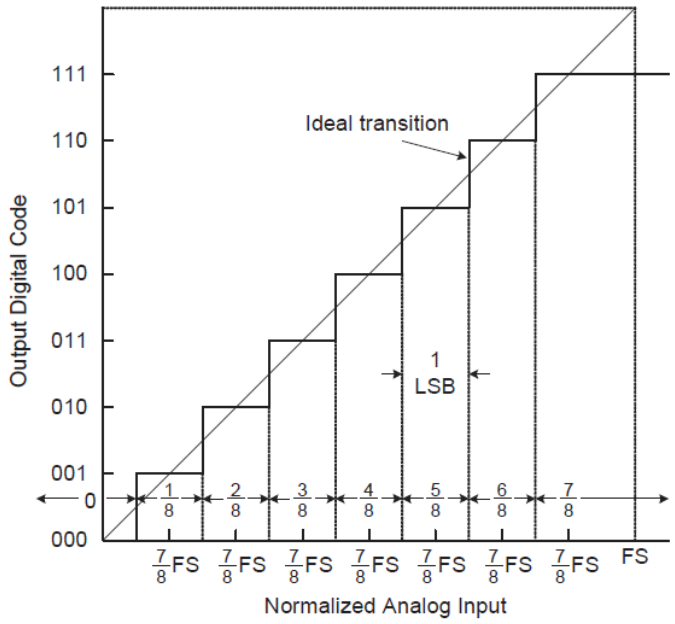

Fig. 3.4 – Ideal input output characteristics for a 3 bit quantizer

Graphically, the quantizing process means that a straight line representing the relationship between the input and the output of a linear analog system is replaced by a transfer characteristic that is staircase-like in appearance. The quantizing process has a two-fold effect: (i) the peak-to-peak range of input sample values is subdivided into a finite set decision levels or decision thresholds that are alighted with the "risers" of the staircase, and (ii) the output is assigned a discrete value selected from a finite set of representation levels or reconstruction values that are aligned with the "treads" of the staircase. The transfer characteristic of uniform quantizer is shown in Fig. 3.5(a) for midtread type and in Fig. 3.5(b) for midriser type. The separation between the decision thresholds and the separation between the representation levels of the quantizer have a common value called the *step size* Δ.

An ADC's actual threshold levels are denoted by *Tk* where the index *k* ranges from 0 to *M* giving a total of *M*+ 1 value. Correspondingly, ideal thresholds levels are

denoted. For an *N*-bit bipolar quantizer, a midtread characteristic has *M* = 2^*N* thresholds and has one quantization level with value zero. A midriser characteristic has *M* +1 = 2*N* +1 thresholds, one of which has value zero. By convention, T0 = −∞ and TM= +∞ *and* for each characteristic so only *M* −1physical thresholds actually exist. Based on the locations of thresholds, quantizers can be divided to two categories: uniform and non-uniform (Fig. 3.5). The thresholds of uniform quantizers are evenly distributed while in non-uniform quantizer's thresholds locations match the probability density function of the incoming signal (such as human speech). Uniform quantizers are most commonly used and will be dealt with exclusively here.

The *Full-Scale Range*, *FSR*, of a quantizer represents full scale input range. The length of adjacent intervals is called the *quantization step* or simply Δ. For an *N*-bit quantizer, the relationship between the Full-Scale Range and the quantization step can be described by $\Delta = \frac{FSR}{2^N}$.

A term related to Full-Scale Range is *Full-Scale*, *FS*, which is the magnitude of the Full-Scale Range's maximum excursion from the transfer function origin. For a bipolar quantizer with origin located at the center of full-scale range, *FS* = *FSR* / 2. For a unipolar quantizer, *FS* = *FSR*.

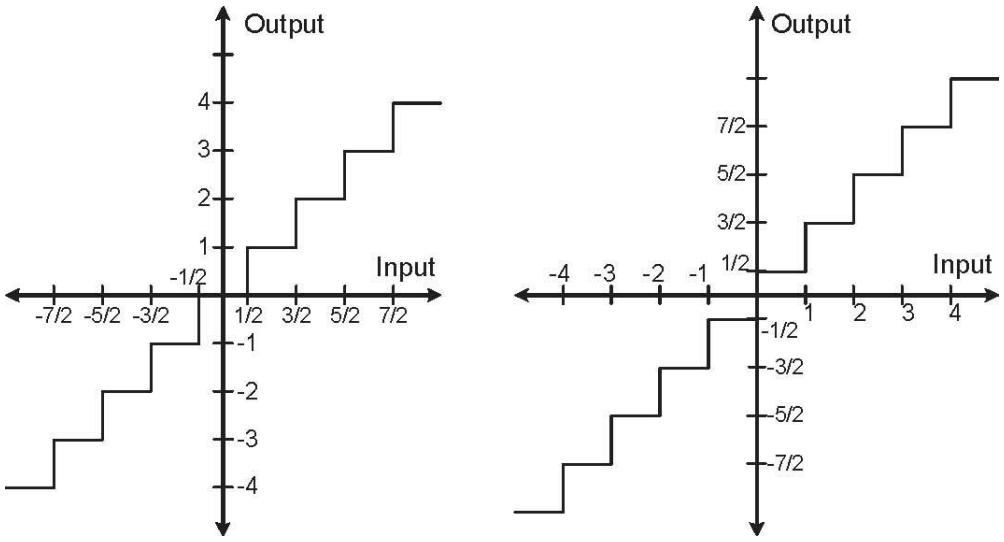

Fig. 3.5 Ideal quantizer transfer characteristic (a) midtread (b) midriser

Real quantizer transfer functions fall short of the ideal because imperfections in fabrication cause actual thresholds to deviate from their desired placement. Such nonidealities can be expressed in several ways (Fig. 3.6). An error which causes all thresholds to shift from their ideal positions by an equal amount is called an *offset* (V_{off}). Non-ideality which results in an erroneous quantizer step size, Δ, is called *gain error*. Δ can be defined as a function of FSR.

The step size Δ can be assigned the value which minimizes threshold errors as calculated by linear regression. In the latter case FSR and Δ relationship still holds, but FSR is a function of Δ instead of vice-versa. *Linearity error* refers to the deviation of the actual threshold levels from their ideal values after offset and gain errors have been removed. Excessive linearity error results in *missing codes*, a condition wherein a valid output code say Δ_i, never occurs because its defining interval $[T_i, T_{i+1}]$ has become vanishingly small, $T_{i+1} \leq T_i$. Linearity error is quantified by the *threshold level errors*

$$\varepsilon_k = T_k - V_{off} - T_k^* \tag{3.14}$$

Where k is defined for the thresholds 0 through M but has meaning only for the real thresholds 1 through M-1. This array of error terms, also called Integral nonlinearity or simply INL. Here, INL is defined for each digital word, but one should be aware that sometimes the term "INL" is defined as the maximum magnitude of the INL values. Related to INL is the Differential non linearity or DNL

$$d_k = T_k - T_{k-1} - \Delta \tag{3.15}$$

Since DNL is defined by a first-order difference equation, it is valid only for the range $1 \le k \le M$ and only has physical meaning over $2 \le k \le M - 1$. The element array of DNL values is also frequently described by its statistical properties such as peak and rms. The terms integral and differential arise when describing the above two error measures because DNL can be defined as the first-order difference of the INL sequence.

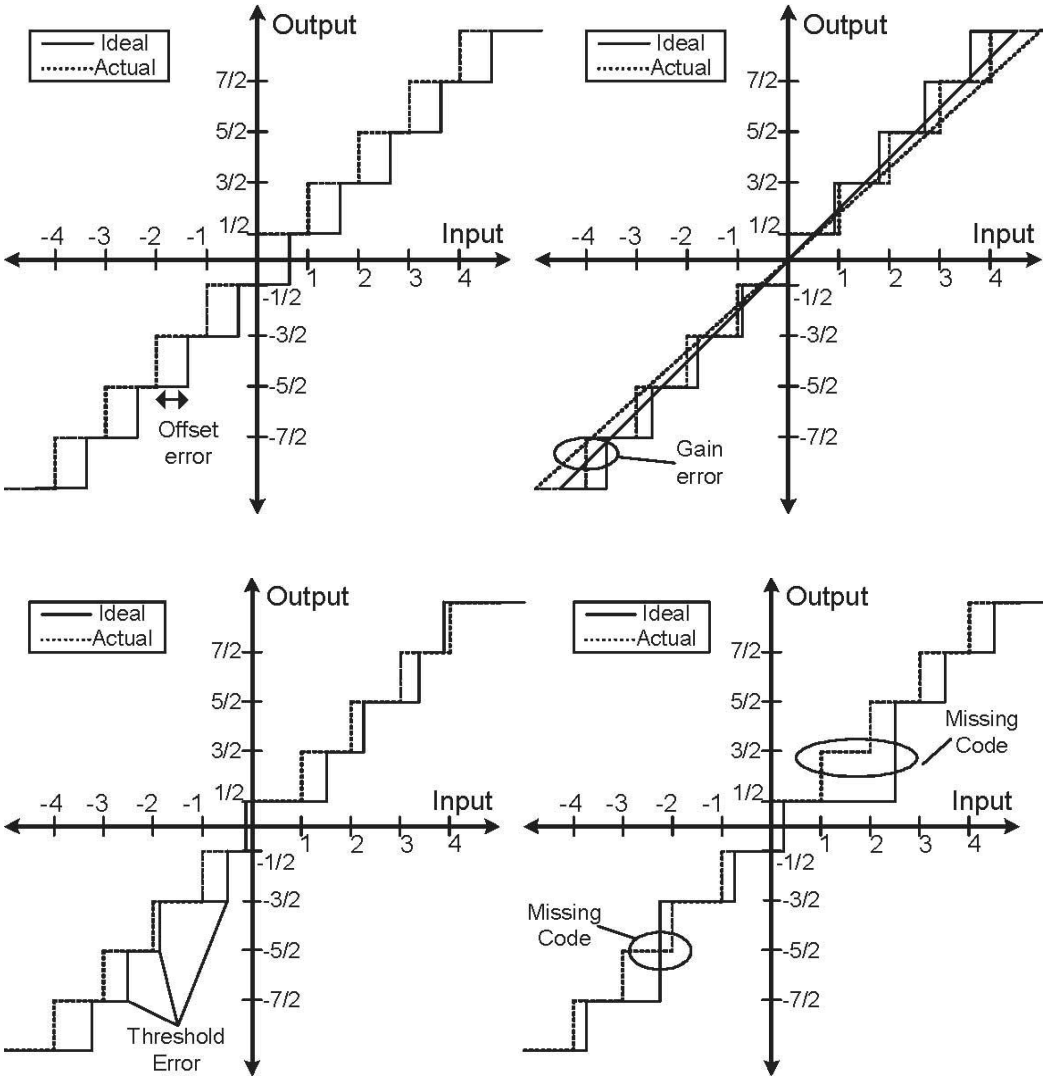

Fig. 3.6 Quantization transfer functions including error sources (a) Offset error. (b) Gain error. (c) Linearity error. (d) Missing codes

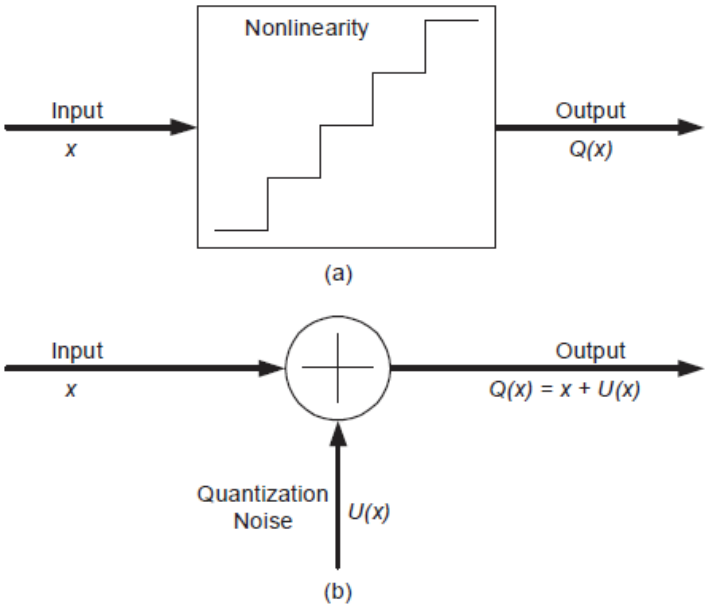

Fig. 3.7 Quantizer models. (a) nonlinear deterministic model (b) statistic model

$$d_k = T_k - T_{k-1} - \Delta$$
$$d_k = T_k - T_{k-1} - (T_k^* - T_{k-1}^*)$$
$$d_k = (T_k - T_k^* - \Delta) - (T_{k-1} - T_{k-1}^* - \Delta)$$
$$d_k = \varepsilon_k - \varepsilon_{k-1}$$

Several terms are commonly used to describe the relative power of the analog input to an A/D converter. The *loading factor*, LF, expresses the RMS amplitude of the input waveform relative to the quantizer FSR

$$LF = \frac{V_{rms}(Input)}{FSR/2} \tag{3.16}$$

Quantization Noise can be described by a nonlinear input–output transfer function as depicted in Fig. 10. The quantized output signal, $Q(x)$, is the sum of the original input signal, x, and a quantization error, where

$$U(x) = Q(x) - x \tag{3.17}$$

Here $U(x)$ is the error resulting when the input signal, x, is quantized with finite resolution. This quantization error, as shown in Fig. 3.8, is a deterministic function of the input signal, x. However, subject to certain simplifying constraints it can be approximated as a random noise component. The constraints necessary to justify this statistical model are:

• $U(x)$ is a stationary process

• $U(x)$ is uncorrelated with x

• The elements of are $U(x)$ uncorrelated with each other

• The probability density function of $U(x)$ is uniform over $(-\Delta/2, \Delta/2)$

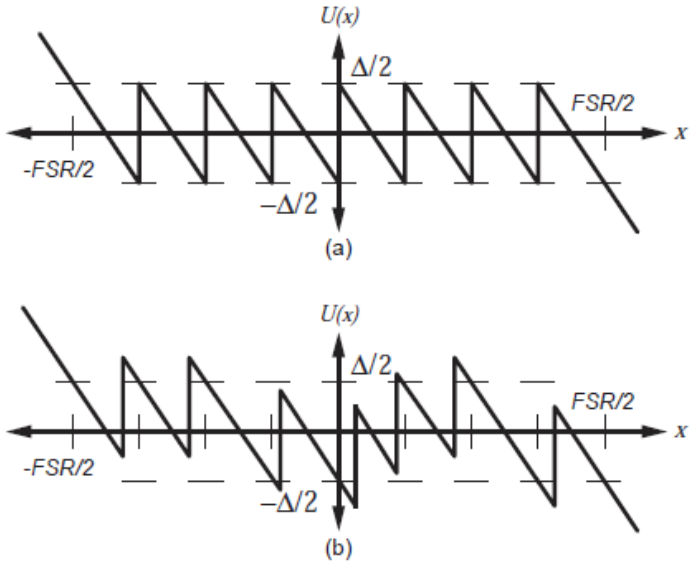

Fig. 3.8 Quantization noise models. (a) Ideal quantizer (b) quantizer with threshold level errors.

Under these constraints $U(x)$ is often modeled as a uniformly distributed random variable thereby simplifying the analysis of quantizer performance. Quantizer operation is frequently characterized by signal-to-noise ratio (*SNR*), which expresses (usually in decibels) the ratio of the output signal power to the output noise power. Since the

quantization noise is assumed to be uniformly distributed on $(-\Delta/2, \Delta/2)$ the output noise power can be easily calculated as

$$\sigma^2(\Delta) = \frac{\Delta^2}{12} \tag{3.18}$$

The power of the full swing sinusoidal input signal is

$$P_S = \frac{(2^N \Delta)^2}{8} \tag{3.19}$$

The quantizer SNR is therefore given by

$$SNR_Q = 6.02N + 1.76(dB) \tag{3.20}$$

Where the subscript *Q* modifying SNR refers to quantization noise as distinct from thermal noise or other deleterious error sources which compromise overall signal to noise ratio. Eq. (3.20) is a frequently used equation for predicting optimum A/D performance. For a 7-bit converter maximum SNR is 43.9 dB, and for an 8-bit converter the maximum SNR is 49.92dB. Eq. (3.20) can be used to assess the performance of any quantizer relative to the ideal. Replacing the maximum achievable SNR by the actual SNR and solving for the equivalent resolution, *N*, a figure of merit called the Effective-Number-Of-Bits (ENOB) is derived.

$$ENOB = \frac{SNR - 1.76}{6.02} \tag{3.21}$$

The effective number of bits is a commonly used metric for summarizing the performance of non-ideal quantizers. In practice, A/D converters encounter inputs which are more complicated than simple sinusoids. Under conditions with such complicated signal environments, the A/D converter may have different achievable maximum SNR.

Comparison is in effect a binary phenomenon that produces a logic output of one or zero depending on the polarity of the input. The Fig. 3.10 depicts the input output characteristic of an ideal comparator, indicating an abrupt transition at $V_{in1} - V_{in2} = 0$.

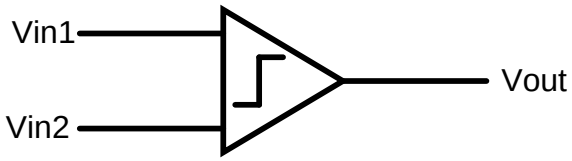

Fig 3.9 – Symbol of Comparator

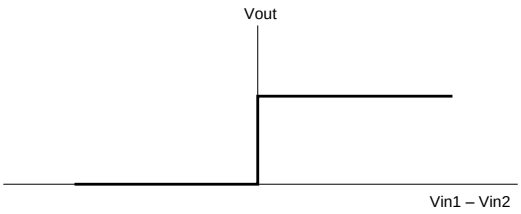

Fig 3.10 – Ideal Characteristics

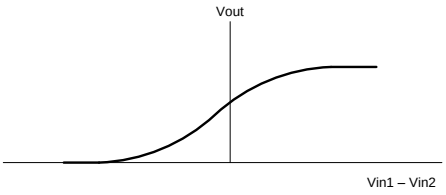

Fig 3.11 – Observed Characteristics

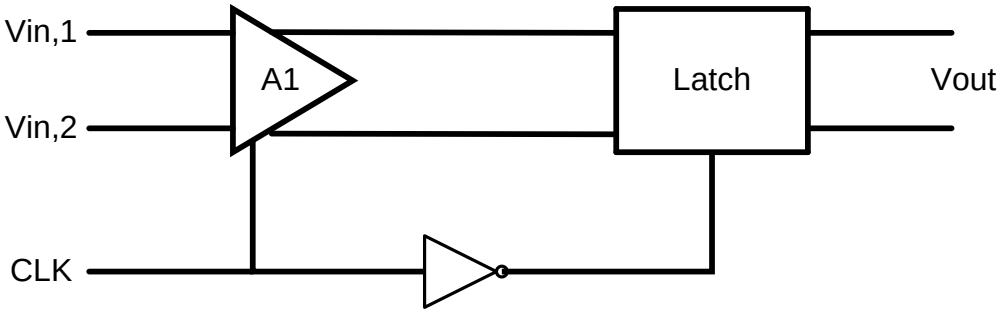

Fig 3.12 – Typical Comparator architecture

This nonlinear characteristic can be approximated with a high gain amplifier wherein the slope of the characteristic is small signal gain in its active region. The output of the high gain amplifier would reach saturation if $V_{in1} - V_{in2}$ is sufficiently large. If the saturation voltage or maximum output voltage is defined as V_H then the minimum voltage difference that the amplifier can detect is given as V_H / A_v.

As a consequence high resolution can be obtained only by increasing the voltage gain (A_v) because the logical output V_H cannot be reduced. The amplifiers used in comparators need not be linear, rather they should be capable to pick out even minimal

voltage difference between the two inputs, and so positive feedback is incorporated. However there is a problem of latch up in positive feedback, in order to avoid this comparators are split into two stages. The first stage is the preamplifier and the second stage is the latch. Typical comparator architecture as in Fig. 3.12 with a preamplifier and latch has two operating modes: tracking and latching. In the tracking mode the preamplifier is enabled to amplify the input difference, hence its output tracks the input while the latch is disabled. In the latching mode, preamplifier is disabled and the latch is enabled so that the instantaneous output is regeneratively amplified by and logic levels are produced at the output. The use of latch to perform sampling and amplification of a voltage difference entails an important issue related to the output response in the presence of small inputs: metastability. If a comparator is given a finite time to regeneratively produce a logic-level output, then for some range of differential input values near zero, the comparator output will not be large enough to be unambiguously interpreted by succeeding encoding logic. This logic can therefore produce erroneous output codes which increase the noise power in the comparator output waveform thereby diminishing SNR. They are generally known as conversion errors, rabbit errors, sparkle codes and metastability errors. The nature of the digital output produced under the conditions of metastability errors depends greatly on the output coding format used. If gray coding is used rather than binary, metastability errors manifest themselves as a single bit error in an otherwise accurate output word.

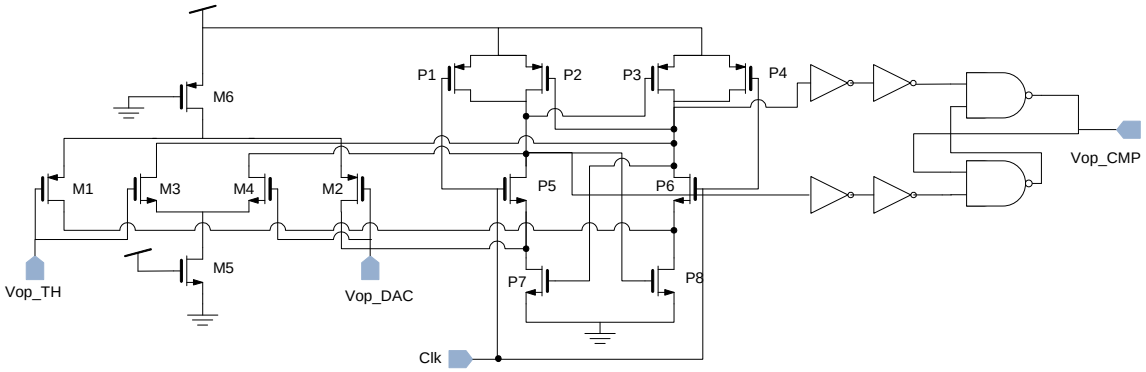

Fig 3.13 – Schematic of Comparator

The comparator circuit presented in Fig 3.13 is a clocked comparator with power consumption of 30uW. The input stage has been designed to facilitate any common mode voltage from 0 to 1.2 V. The output stage of this circuit consists of SR latch which provides the Comparator decision value to the SAR Digital logic. The positive terminal of the comparator is driven by the output of the track and hold circuit. Here we have presented the comparator with appropriate connections for the Positive going signal.

To accommodate the complete input common mode range NMOS differential pair (M3 & M4) and PMOS differential pair (M1 & M2) is used. The P2, P3, P5, P6, P7 and P8 can be imagined as a clocked inverter with cross coupling to achieve positive feedback. P1 and P4 are driven by the clock which can pull up the output nodes to V_{DD}. This leaves the output nodes at a dynamic state. The dynamic output nodes are converted into static nodes by using a RS latch. Use of RS latch also eliminates metastability errors. An inverted based driver is placed at the output if necessary to ensure that it can drive the required capacitivie load.

Positive terminal accepts the time varying input and compares the reference voltage applied on the Negative terminal. A decision is made and applied to the Output terminal of the comparator. Another comparator with Input terminals of Von_TH, Von_DAC and Output terminal of Von_CMP is used where the functionality of these terminals are exactly the same as the one mentioned above. The comparator has a rise time of 1 ns. This slewing is necessary to ensure it doesn't create a race condition by changing the Output state along with the rising edge of the clock. More details on this problem and its solution have been presented in the SAR Digital logic section.

SAR Logic

The SAR logic for the ADC is a state machine which takes the Clock signal as input. The clock signal is divided by 8 to generate the clock required for Sample & Hold circuit. 6 clock cycles are required for one complete conversion. Two additional clock cycles are for Start of Conversion and End of Conversion.

1. The Start of Conversion (SOC) – 1st Clock cycle is used to reset all the registers in the logic block.
2. The 2nd Clock cycle – Comparator performs comparison between Input data and reference voltage and generates a 1 or 0. The data is stored in the registers and applied to the DAC. The DAC sets the reference voltage for the next conversion cycle. The same process is repeated for 2nd to 7th clock cycle to complete conversion process.
3. The End of Conversion (EOC) – 8th Clock cycle latches the output data to the data bus.

The SAR logic operated over an 8 clock cycle period, with 2 cycles allotted for SOC & EOC and 6 clock cycles for digital data. A 6 bit conversion scheme is used to divide the entire voltage head room of 0 to 1.2 V into 64 levels. If observed closely it will be found that the signal in the range of 300 to 600 mV occupies the digital data in the range of 01XXXX where XXXX varies from 0000 to 1111. This XXXX component is the 4 bit data of interest. This ensures the input signal is split into 16 levels of each 18.75 mV and an accurate digital conversion data is produced. Each level is separated by 18.75 mV which is adequate to combat the variations in DAC output voltage due to process corner variations. In addition, the SAR logic also provides the clock signal to the analog sample and hold circuit as the clock out signal. This clock is based upon the SPI clock, which is divided down by a factor of eight. This is done with a counter, producing a 50% duty cycle clock. Clock out is held high for 1 cycle of the standard clock and is then held

low for 7 cycles of the standard clock. The rising edge of clock out is synchronized with the beginning of the sample state.

Table 3.1. Description of various states of the SAR logic.

State	Description	Next state	Duration
Sample	Registers are reset, sample and hold takes sample	Convert_1	1 clock period
Convert_1	Apply 10000 to DAC	Convert_2	1 clock period
Convert_2	Latch in comparator result as C_1; Apply $C_1$10000 to DAC	Convert_3	1 clock period
Convert_3	Latch in comparator result as C_2; Apply $C_1C_2$1000 to DAC	Convert_4	1 clock period
Convert_4	Latch in comparator result as C_3; Apply $C_1C_2C_{31}$00 to DAC	Convert_5	1 clock period
Convert_5	Latch in comparator result as C_1; Apply $C_1C_2C_3C_4$10 to DAC	Convert_6	1 clock period
Convert_6	Latch in comparator result as C_1; Apply C_1 $C_2C_3C_4C_5$1 to DAC	End of Conversion	1 clock period
End of Conversion	Latch in comparator result as C_6; Do bounds checking and place result on output.	Sample	1 clock periods

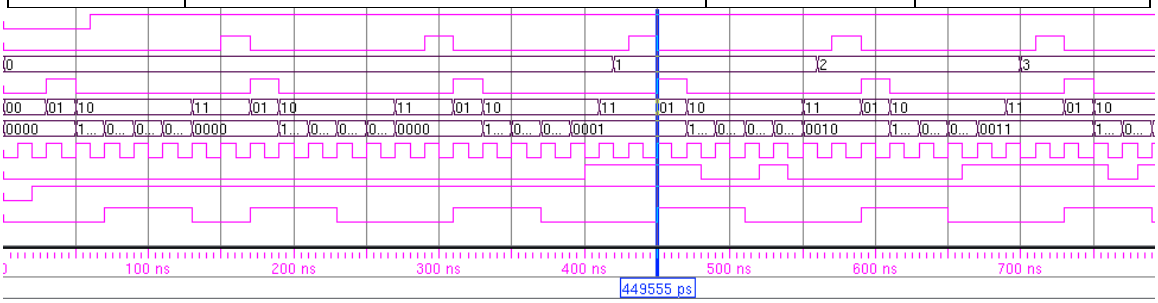

Fig 3.14 – Timing diagram for SAR Logic (10 Clk cyles for conversion)

SOC (Start of Conversion) is the first waveform which initializes the ADC into operation by moving into Logic High. EOC (End of Conversion) is the second waveform which flips from Logic low to Logic high presenting a Clock cycle. The Output Data ports are read at this time which gives out the Final Digital data. Result is the third waveform which shows the Digital data for each bit along the conversion process starting from MSB and moves towards LSB. Sample is the fourth waveform used to indicate the state of SAR logic, 0 – Sample Mode and 1 – Hold Mode. State is the fifth waveform which shows the state of the SAR logic 00 – Reset, 01 – Sample Mode, 10 – Conversion mode, 11 – Conversion complete. Vref_Mask is the sixth waveform which is applied to the DAC to change the reference voltage level for the Comparator for every clock cycle. Clock is the seventh waveform of Standard Clock of 27 MHz used in conversion logic. Cmp_Decision is the eighth waveform which shows the digital input to the SAR logic from the Comparator's output terminals. Reset_N is the ninth waveform which is used to reset all the gates to in the Digital block to logic low. Clk_Out is the last waveform which is used for testing the ADC in Cadence.

The SAR logic is developed for multiple applications like Temperature sensor, RSSI and CCA. In order to cater to the needs of temperature sensor, the previously described SAR logic was designed with 10 cycles to perform a single conversion. For RSSI and CCA applications the SAR logic was designed to perform the conversion in 8 clock cycles and the clock frequency was also changed. The Fig. 3.15 gives the modified SAR logic timing diagram for RSSI / CCA applications.

The first waveform is the Clock, which is followed by Comparator decision waveform. The third waveform is the conversion counter which counts the number of conversion cycles. The fourth waveform is end of conversion, which indicates from that clock cycle the converter data is available. The fifth waveform is the reset waveform

which is used to reset the SAR logic when one complete conversion is finished. The sixth waveform is the 6 bit output. The seventh waveform is start of conversion which indicates that the first conversion is about to happen. The eighth waveform is the reference voltage mask which is applied to the DAC to set the reference voltage for the comparator. The SAR logic was designed in verilog and it was synthesized in Synopsys design compiler. To generate the layout for the SAR logic, first floor planning is done followed by adding power grids. Then an initial estimate of placing the cells and data path routing is done. After routing filler cells are added and ports are added to the layout. The Fig. 3.16, 3.17, 3.18, 3.19 and 3.20 shows the various steps of synthesis

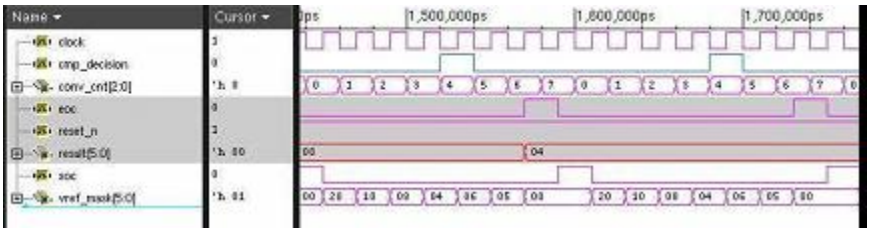

Fig 3.15 – Timing Diagram for SAR logic (8 Clk cycles for conversion)

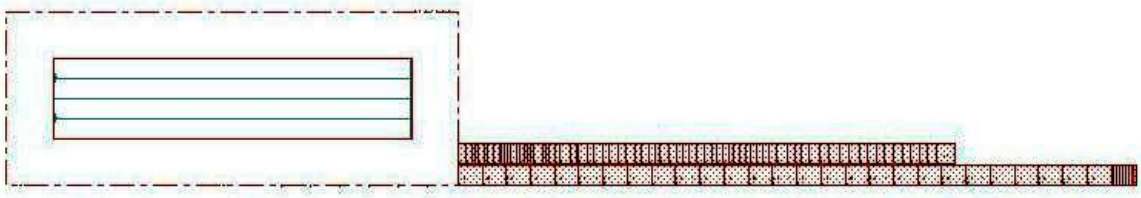

Fig 3.16 – Floor planning

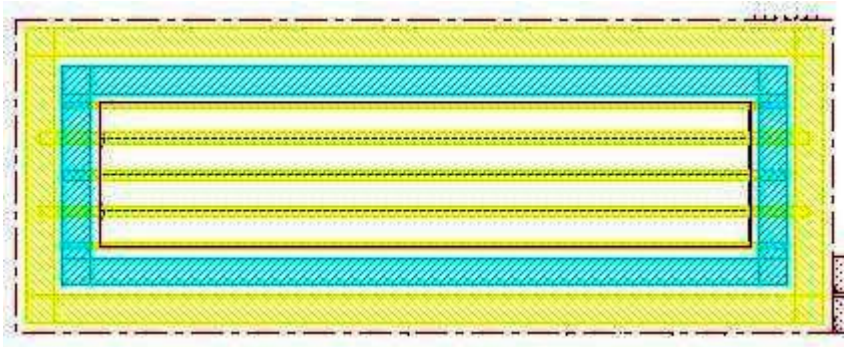

Fig 3.17 – Power Grid

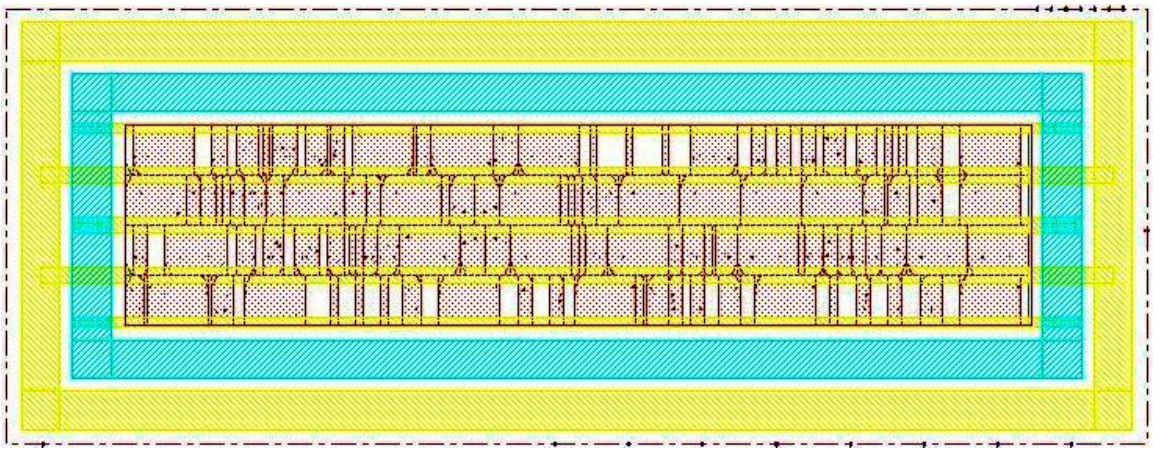

Fig 3.18 – Place components of SAR logic on layout

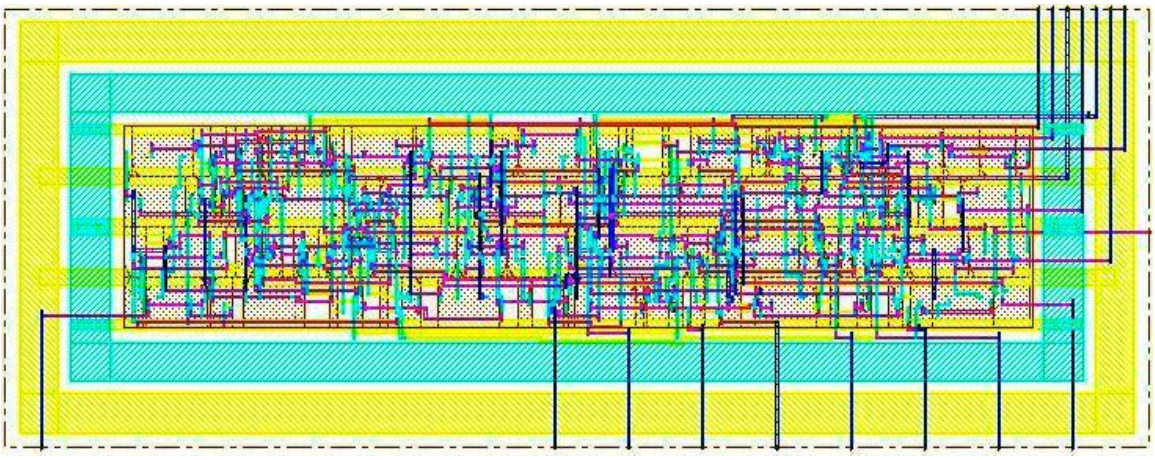

Fig 3.19 – Routing of data path of SAR logic on layout

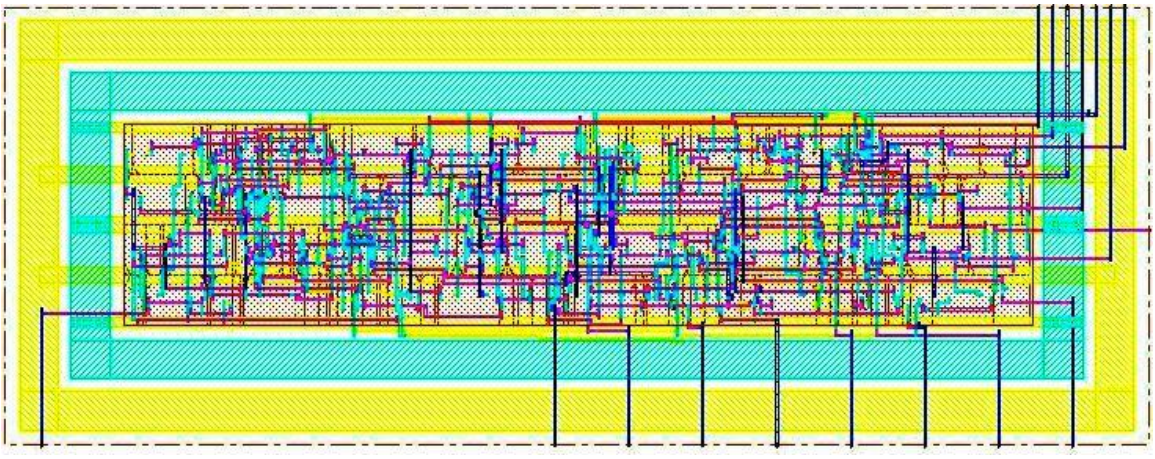

Fig 3.20 – Adding filler cells and port assignment

Digital to Analog Converter

DAC is the component in SAR ADC which determines the overall linearity of the ADC. The basic purpose of the DAC is to generate analog output proportional to digital code. Each digital code contains a certain fraction of reference which multiplied or divided, where the reference may be one of the three electrical quantities: voltage, current or charge. The accuracy of this function determines the linearity of the DAC, while the speed at which each reference can be selected and established gives the conversion rate of the DAC. The linearity and SNDR of D/A converters depend on the accuracy of the reference multiplication or division employed to generate the output levels. The resistor ladder based DAC is on voltage division, where a given reference voltage V_{ref} can be divided into N equal segments using a ladder composed of N identical resistors $R_1 = R_2 .... = R_N$. An n-bit DAC theoretically requires about 2^n resistors, manifesting exponential growth of the number of resistors as a function of resolution. An important aspect of resistor ladder is integral and differential non-linearities they introduce when used in SAR ADC. These errors result from mismatches in the resistors comprising of the ladder. The resistors do not exhibit linear gradient rather random mismatch. This type of mismatch originates primarily from the uncertainities in geometry definition during processing, as well as random variations in contact resistance. Consider two resistors lay out with identical geometry and dimensions. In the ideal case, the value of the resistor can be expressed as

$$R = \frac{\rho L}{Wt} + 2R_C \tag{3.22}$$

Where ρ is the resistivity, L, W and t are the length, width and thickness of the resistors, respectively and R_C represents additional resistance due to each contact. In reality the resistors suffer from several mismatch components: resistivity mismatch, width, length and thickness mismatch and contact resistance mismatch. In a typical process, width and

length mismatch results from limited edge definition capability in lithography and etching or deposition of the resistor material, the variation in thickness arises from gradients across the die and contact resistance mismatch caused by random variations in the finite resistance at the interface of the resistor and the interconnect. Taking the total differential the overall mismatch between two resistors can be given as

$$\Delta R = \frac{L\Delta\rho}{Wt} + \frac{\rho\Delta L}{Wt} - \frac{\rho L\Delta W}{W^2 t} - \frac{\rho L\Delta t}{Wt^2} + 2\Delta R_C \tag{3.23}$$

The value can be normalized to the mean value of the resistors, R to yield the relative mismatch. Since the contact resistance decreases as the resistor width increases we can write $R_C = r/W$, where r is the proportionality factor. Thus the above Eqn. 3.23 can be modified as

$$\frac{\Delta R}{R} = \frac{\Delta\rho}{\rho} + \frac{\Delta L}{L} - \frac{\Delta W}{W} - \frac{\Delta t}{t} + 2\frac{t\Delta r}{\rho L} \tag{3.24}$$

In a typical process, ρ and t are given, leaving L, W and R as the only variable under designer's control. To minimize the overall mismatch, each of these parameters must be maximized. Large dimensions lead to high parasitic capacitance between the resistor and substrate as well as large chip space.

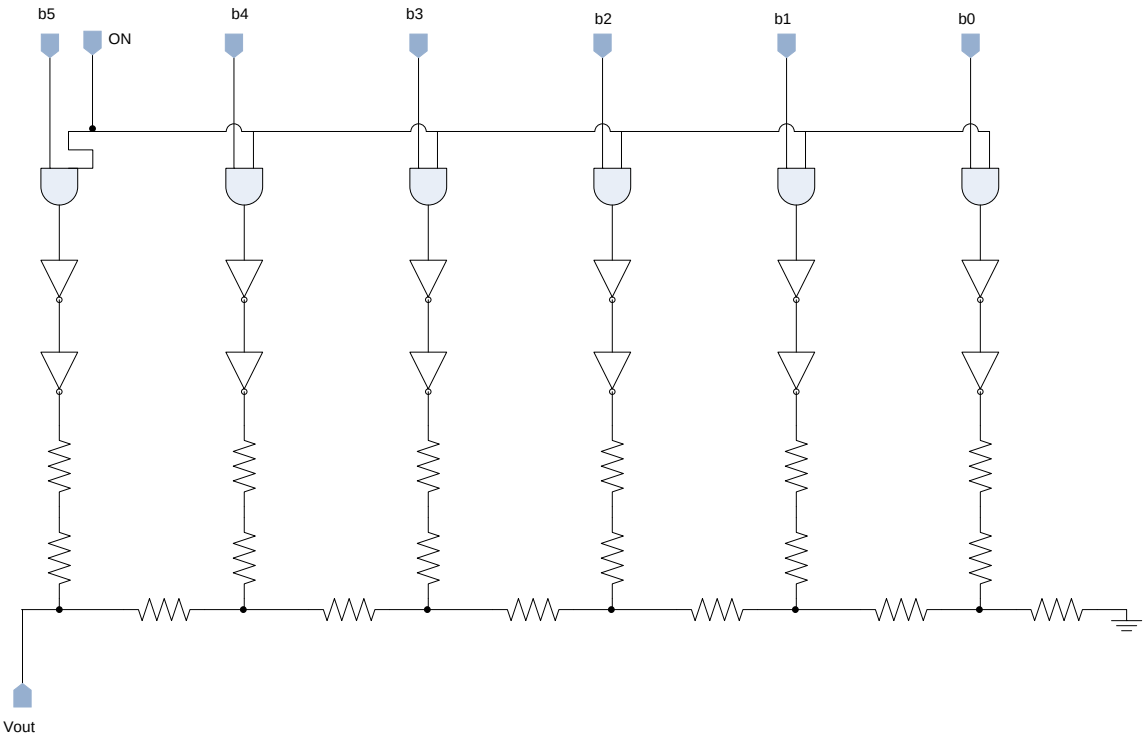

Fig. 3.21 - R-2R ladder based DAC

Resistor ladder networks provide a simple, inexpensive way to perform digital to analog conversion (DAC). The most popular networks are the binary weighted ladder and the R/2R ladder. Both devices will convert digital voltage information to analog, but the R/2R ladder has become the most popular due to the network's inherent accuracy superiority and ease of manufacture. Fig. 3.21 is a diagram of the basic R/2R ladder network with N bits. The "ladder" portrayal comes from the ladder-like topology of the network. Note that the network consists of only two resistor values; R and 2R (twice the value of R) no matter how many bits make up the ladder. The particular value of R is not critical to the function of the R/2R ladder.

The binary weighted ladder shown in Fig. 3.21 requires double multiples of R as the number of bits increase. As the ratios of the resistors become more and more obtuse in a binary weighted network, the ability to trim the resistors to accurate ratio tolerances becomes diminished. More accurate ratios can be obtained in a resistor network with

consistent, similar values as in the R/2R network. The R/2R network provides the most accurate method of digital to analog conversion. The last resistance in the ladder is the termination resistor which is connected to ground. The termination resistor assures that the Thevenin resistance of the network as measured to ground looking toward the LSB (with all bits grounded) is R as shown in Fig. 3.21. The Thevenin resistance of an R/2R ladder is always R, regardless of the number of bits in the ladder. Digital information is presented to the ladder as individual bits of a digital word switched between a reference voltage (Vr) and ground. Depending on the number and location of the bits switched to Vr or ground, Vout will vary between 0 volts and Vr. If all inputs are connected to ground, 0 volts is produced at the output, if all inputs are connected to Vr, the output voltage approaches Vr, and if some inputs are connected to ground and some to Vr then an output voltage between 0 volts and Vr occurs. These inputs (also called bits in the digital lingo) range from the Most Significant Bit to the Least Significant Bit. As the names indicate, the MSB, when activated, causes the greatest change in the output voltage and the LSB, when activated, will cause the smallest change in the output voltage. If we label the bits (or inputs) bit 1 to bit N the output voltage caused by connecting a particular bit to Vr with all other bits grounded is:

$$V_{out} = \frac{V_r}{2^N} \tag{3.25}$$

Where N is the bit number. For bit 1, Vout =Vr/2, for bit 2, Vout = Vr/4 etc. Since an R/2R ladder is a linear circuit, we can apply the principle of superposition to calculate Vout. The expected output voltage is calculated by summing the effect of all bits connected to Vr. For example, if bits 1 and 3 are connected to Vr with all other inputs grounded, the output voltage is calculated by:

$$V_{out} = V_r/2 + V_r/8 \tag{3.26}$$

The R/2R ladder is a binary circuit. The effect of each successive bit approaching the LSB is 1/2 of the previous bit. If this sequence is extended to a ladder of infinite bits, the

effect of the LSB on Vout approaches 0. Conversely, the full-scale output of the network (with all bits connected to Vr) approaches Vr as shown in Eqn. 3.27

$$\lim_{N\to\infty}(V_r)\sum_{i=1}^{N}1/2^i = V_r \tag{3.27}$$

The full-scale output is less than Vr for all practical R/2R ladders, and for low pin count devices the full-scale output voltage can be significantly below the value of Vr. Eqn. 3.28 can be used to calculate the full-scale output of an R/2R ladder of N bits.

$$FSR = (V_r)\sum_{i=1}^{N} 1/2^i \tag{3.28}$$

An R/2R ladder of 4 bits would have a full-scale output voltage of 1/2 +1/4 + 1/8 + 1/16 = 15Vr/16 or 0.9375 volts (if Vr=1 volt) while a 10 bit R/2R ladder would have a full-scale output voltage of 0.99902 (if Vr=1 volt). The number of inputs or bits determines the resolution of an R/2R ladder. Since there are two possible states at each input, ground or Vr, (also designated as “0” or “1” in digital lingo for positive logic) there are 2N combinations of Vr and ground to the inputs of an R/2R ladder. The resolution of the ladder is the smallest possible output change for any input change to the ladder and is given by 1/2N where N is the number of bits. This is the output change that would occur for a change in the least significant bit. For a 10bit R/2R there are 2N or or 1024 possible binary combinations at the inputs. The resolution of the network is 1/1024 or .0009766. A change in state at the LSB input should change the output of the ladder by .09766% of the full scale output voltage. The output accuracy of the R/2R ladder is typically specified in terms of full-scale output ± some number of least significant bits. R/2R ladders are usually specified with output accuracies of ±1 LSB or ±1/2 LSB. For example, a ±1/2 LSB specification on a 10 bit ladder is exactly the same as ±0.04883% full-scale accuracy.

Fully Differential SAR Architecture

The fully differential SAR architecture is very similar to the standard SAR architecture. The difference comes in the way SAR logic is implemented. The positive going signal and negative going signal are converted into digital signal into two separate assembly of sample and hold circuit, comparator, DAC and SAR logic. The two digital signals are subtracted to obtain a fully differential digital equivalent of the analog signal.

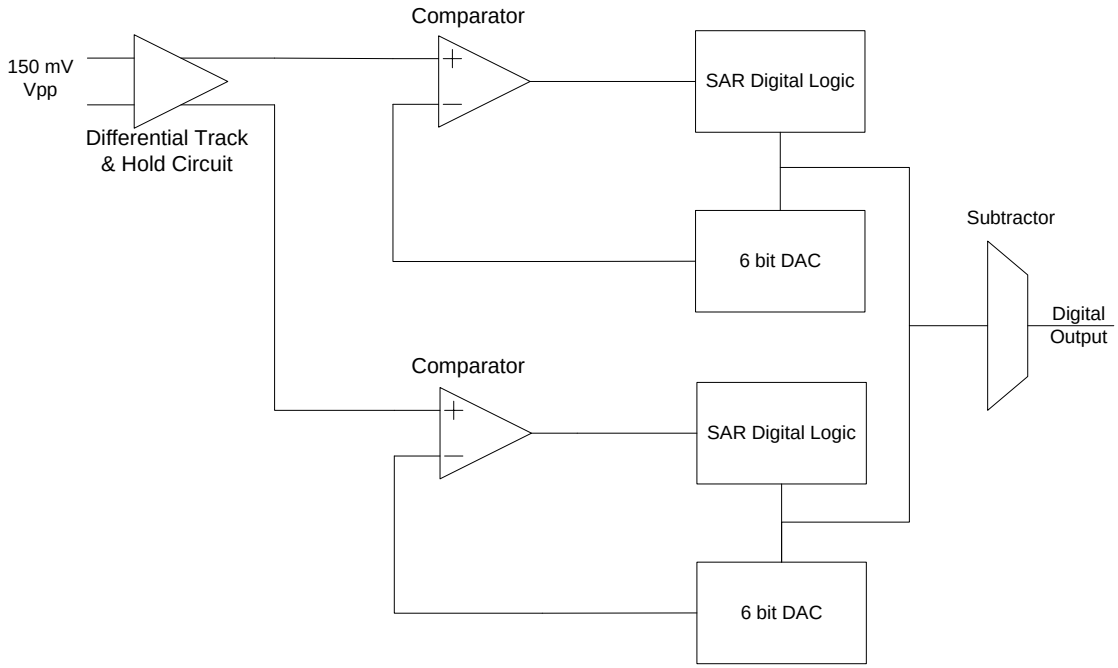

Fig 3.22 – Architecture of the Fully Differential SAR ADC

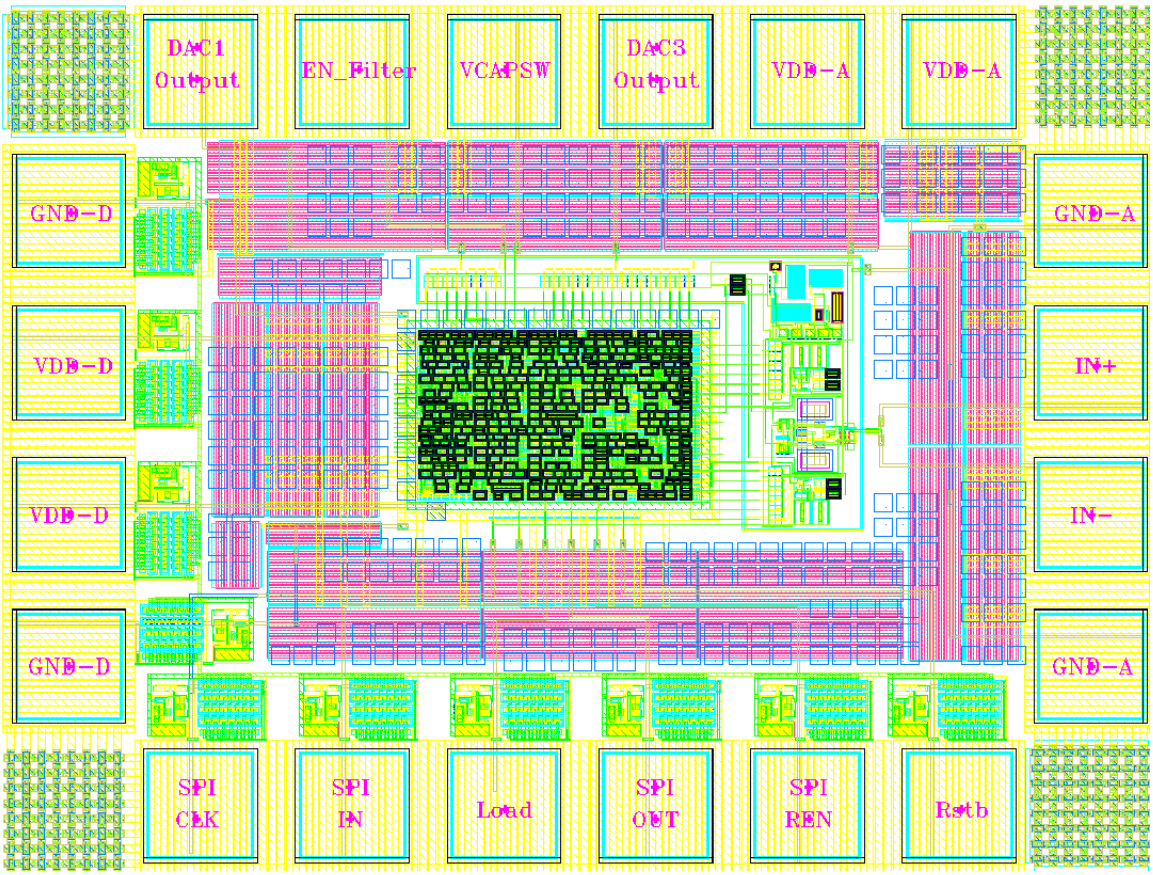

Fig 3.23 – Test Structure for SAR ADC with Serial Peripheral Interface

The fully differential ADC test structure is shown in Fig 3.23. The ADC contains a first order band gap reference circuit to provide the necessary voltage and current bias for the system. The SAR logic, subtractor and SPI are all integrated into a single digital block. The various inputs to the digital block are ESD protected with ESD circuit which can be seen very close to the pads. The ADC architecture and various components have been discussed in detail; let us look into the performance summary of the ADC. The performance summary of the fully differential ADC is given in Table 3.2. The integral and differential non-linearity was computed by extracting the output digital signal and post processing in Matlab. The INL and DNL code is presented in Appendix B.

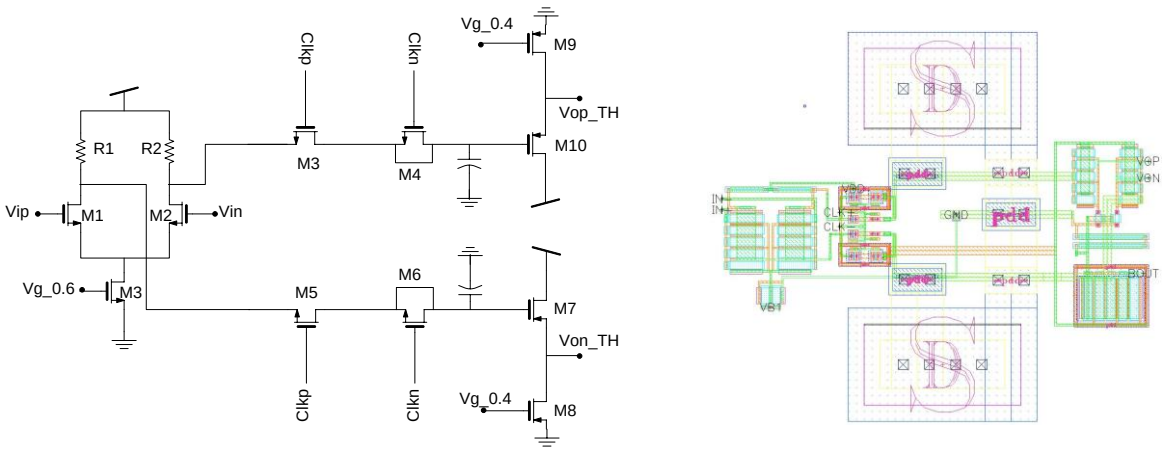

Fig 3.24 – Schematic and Layout of Sample & Hold Circuit

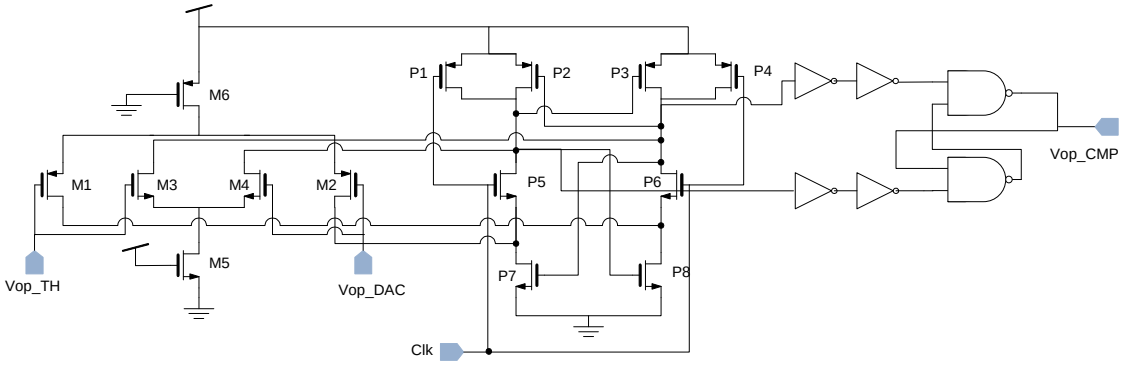

Fig 3.25 – Schematic of Comparator

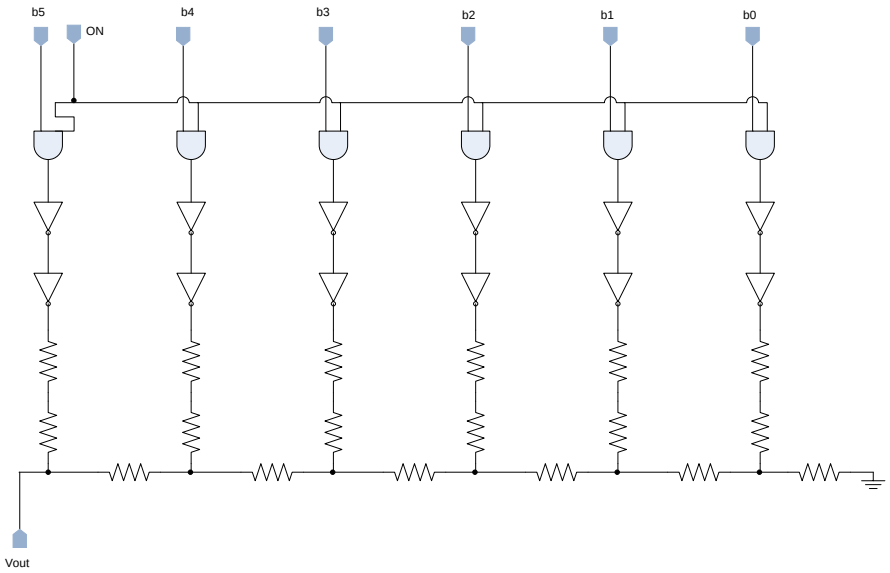

Fig 3.26 – Schematic of 6 bit DAC

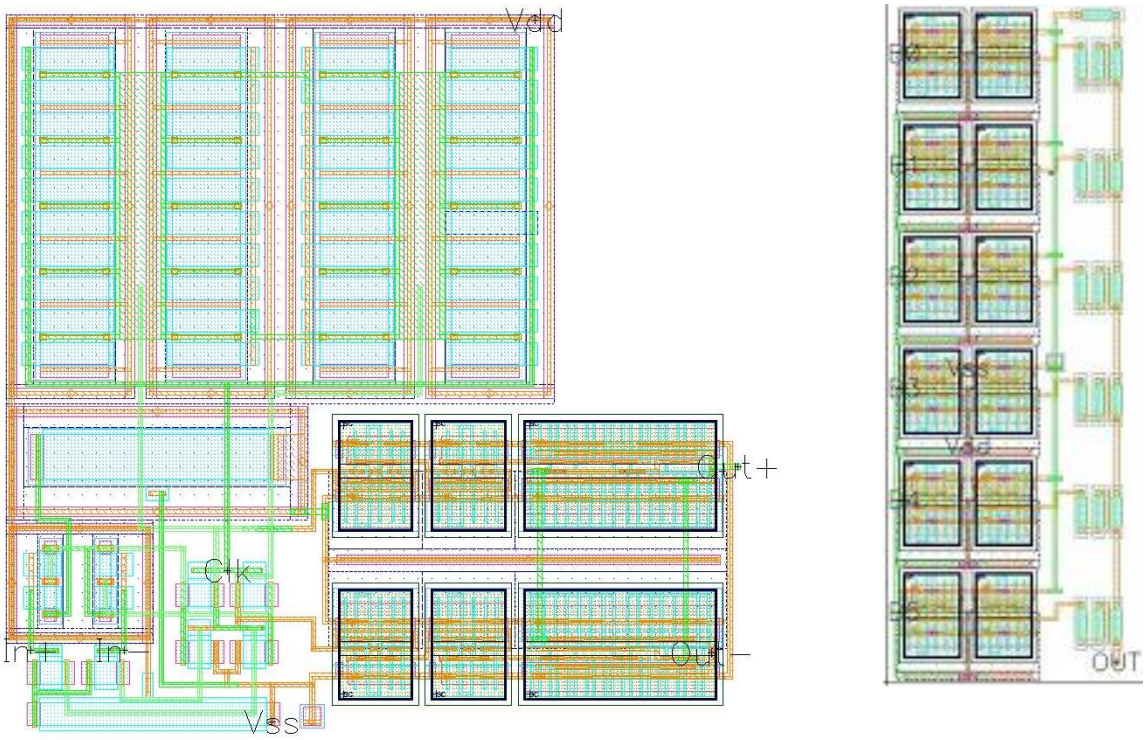

Fig 3.27 – Layout of Comparator and 6 bit DAC

Table 3.2 – Performance Summary of Fully Differential ADC

Parameters	Value
DNL	0.15 LSB
SNR	23 dB
SFDR	27 dB
ENOB	3.5
Clock Frequency	27 MHz
Speed	3.4 MSPS

CHAPTER 4

APPLICATIONS OF SUCCESSIVE APPROXIMATION ADC

Successive approximation data converter operates with medium conversion speed, moderate circuit complexity and high conversion accuracy. SAR ADC is very commonly used in feedback control applications because of high conversion accuracy and medium speed operation. 6 bit SAR ADC is used in feedback loop for precise digital control.

Temperature based sensing control for RF Front End

The output power of a power amplifier varies with temperature. This is contributed by the fact there is ambient temperature variation along with the local heating effect caused by large current flow in the output stages of a power amplifier. The pattern of behavior observed in power amplifier, led to the idea of using a temperature based sensor to detect output power variation.

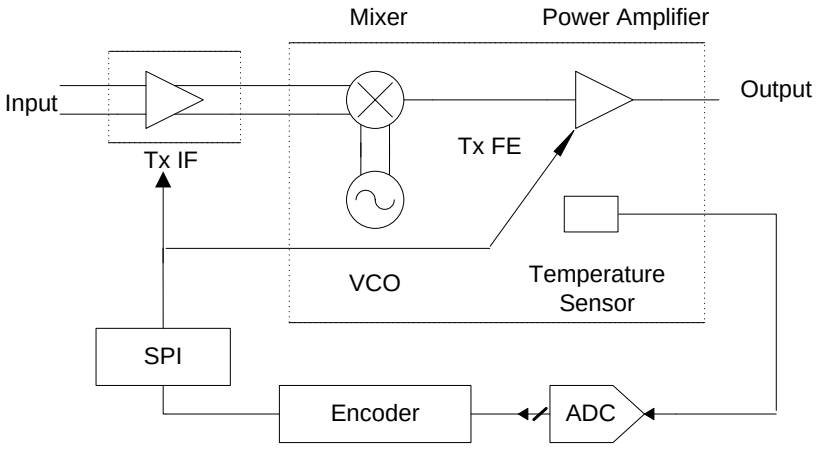

Fig 4.1 – Transmitter Front End with Temperature sensor based feedback control.

The sensor then generates a DC voltage which was converted to a digital equivalent and applied to a bias core. The bias core output is controlled by setting certain

digital input which is used to vary the gate bias applied to the last stage of the power amplifier. The temperature sensor circuit consists of a device which has the same bias point as the device in the last stage of the Power amplifier. The device size is scaled to draw 20 uA current in the test device. A current mirror load is used to mirror the same current into a substrate bipolar junction transistor, which is used as a Remote temperature sensing element. The base emitter voltage versus temperature characteristic of the bipolar device is crucial to generate a sensing voltage. The output of the temperature sensor circuit is then further amplified with an inverting amplifier and buffered before applying to the ADC.

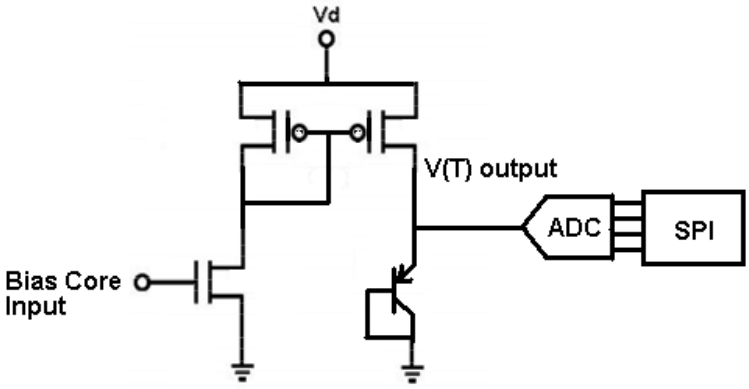

Fig 4.2 – Basic Temperature Sensor circuit

The dynamic range obtained with this sensor is close to 150 mV. In order to improve the dynamic range an operational amplifier based inverting amplifier was used to increase the dynamic range to 600 mV. A plot of the dynamic range is given in Fig 4.4, where the blue curve is the dynamic range observed before the sense amplifier while the red curve is the improved dynamic range with sense amplifier. A voltage buffer is used before applying the sensor output to the data converter. The reason for increasing the dynamic range of the sensor is to make it fit into the full scale range specifications of the data converter. The simulation results for the sensor and measured results for the same are presented in Table 4.1.

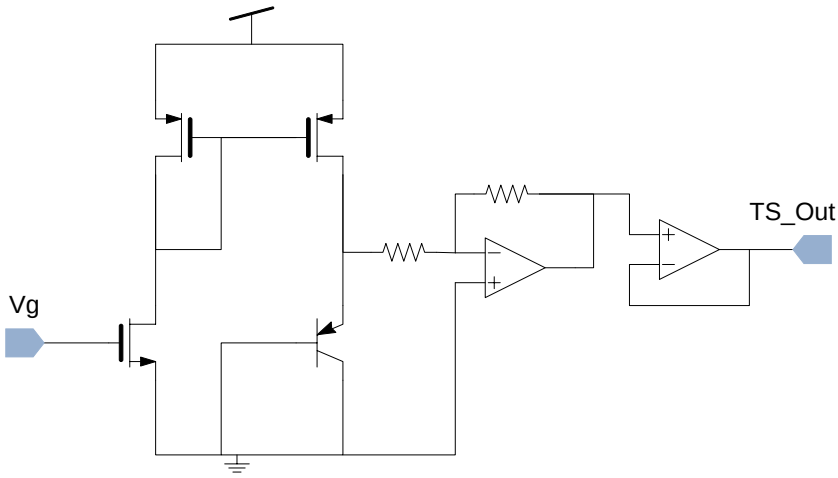

Fig 4.3 – Proposed Temperature Sensor circuit

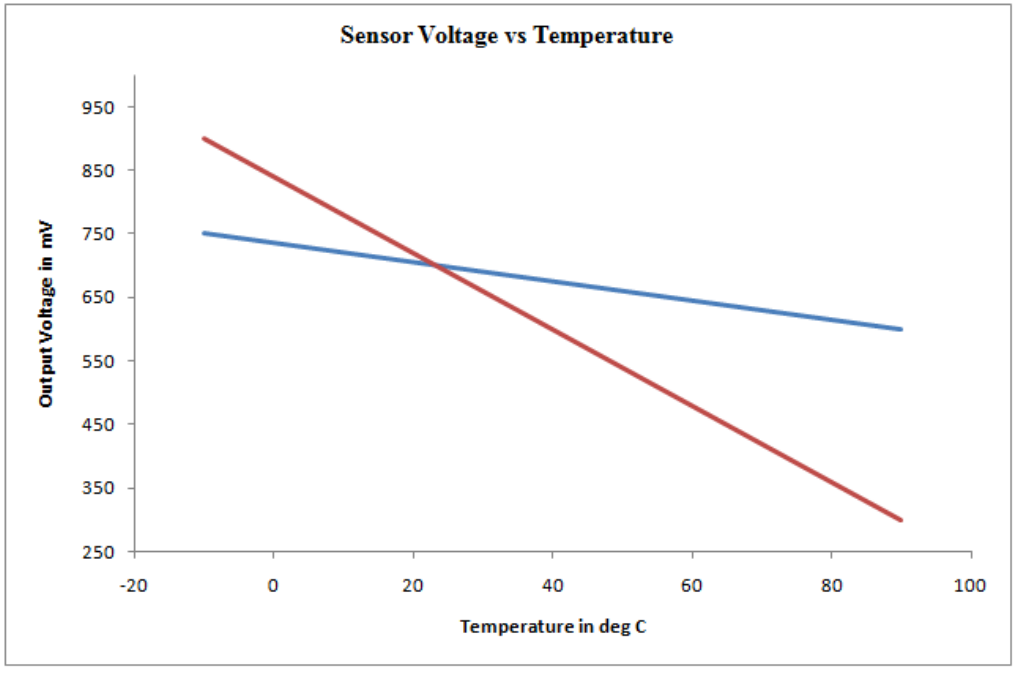

Fig 4.4 – Sensor Output Voltage versus Temperature

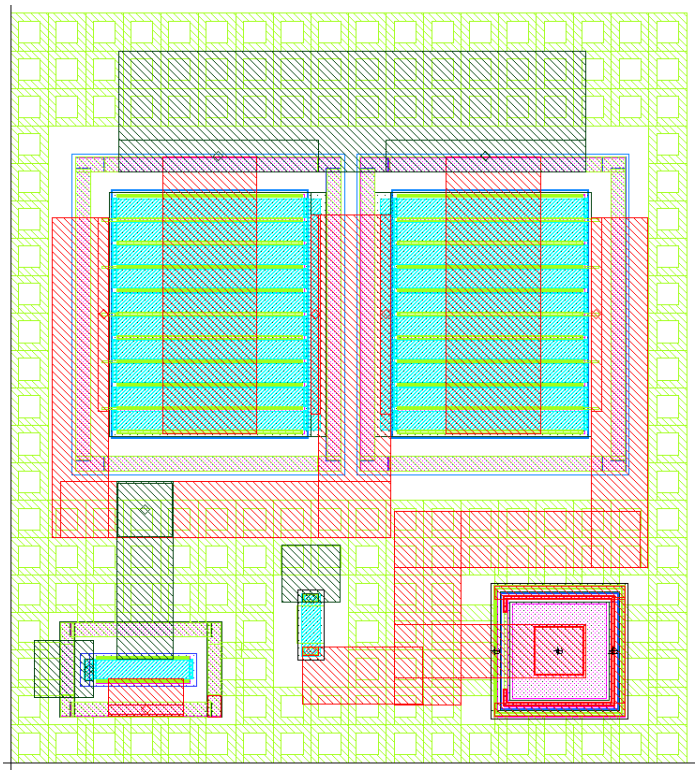

Fig 4.5 – Layout of Temperature Sensor

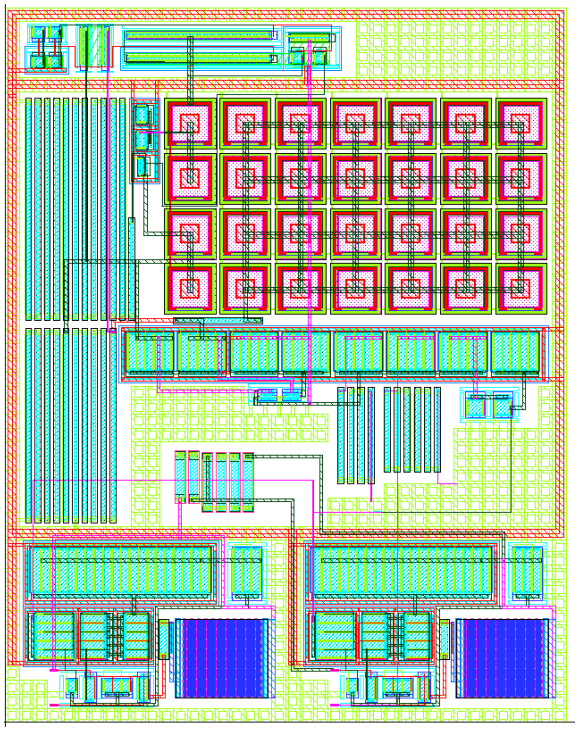

Fig 4.6 – Layout of Sense Amplifier along with Bandgap reference circuit

Table 4.1 – Performance Summary of Temperature sensor across various process corners

Temp in C	TYP	SS	SF	FS	FF
-10	0.8497	0.8555	0.8475	0.8608	0.8608
-5	0.8424	0.8483	0.8402	0.8538	0.8538
0	0.8351	0.8411	0.8329	0.8467	0.8467
5	0.8278	0.8338	0.8256	0.8395	0.8395
10	0.8204	0.8265	0.8182	0.8323	0.8323
15	0.813	0.8192	0.8108	0.8251	0.8251
20	0.8056	0.8118	0.8034	0.8178	0.8178
25	0.7981	0.8044	0.7959	0.8104	0.8104
30	0.7906	0.797	0.7884	0.803	0.803
35	0.7831	0.7896	0.7809	0.7956	0.7956
40	0.7756	0.7821	0.7734	0.7882	0.7882
45	0.7681	0.7746	0.7658	0.7807	0.7807
50	0.7605	0.767	0.7583	0.7732	0.7732
55	0.7529	0.7595	0.7507	0.7657	0.7657
60	0.7453	0.7519	0.7431	0.7582	0.7582
65	0.7377	0.7443	0.7355	0.7506	0.7506
70	0.7301	0.7367	0.7278	0.743	0.743
75	0.7224	0.7291	0.7202	0.7354	0.7354
80	0.7147	0.7215	0.7125	0.7278	0.7278
85	0.7071	0.7138	0.7048	0.7201	0.7201
90	0.6993	0.7062	0.6971	0.7125	0.7125

A single ended version of 6-bit Successive approximation ADC has been used to convert the sensor voltage into a digital equivalent. The schematic and layout of the various components of the ADC are given in Fig 4.8 to 4.16. The ADC error correction circuit comprises three stages. Every stage contains a 6 bit DAC, Comparator and Increment / Decrement control block. The 6 bit DAC takes the ADC output and converts it to equivalent analog voltage. The comparator takes T&H output for reference and generates a decision based on the analog input voltage. If the output of the comparator is 1 the Increment / Decrement control block increments the ADC output by 1, if the output of the comparator is 0 the ADC output is decremented by 1. This system has the ability detect errors on the LSB and LSB + 1.

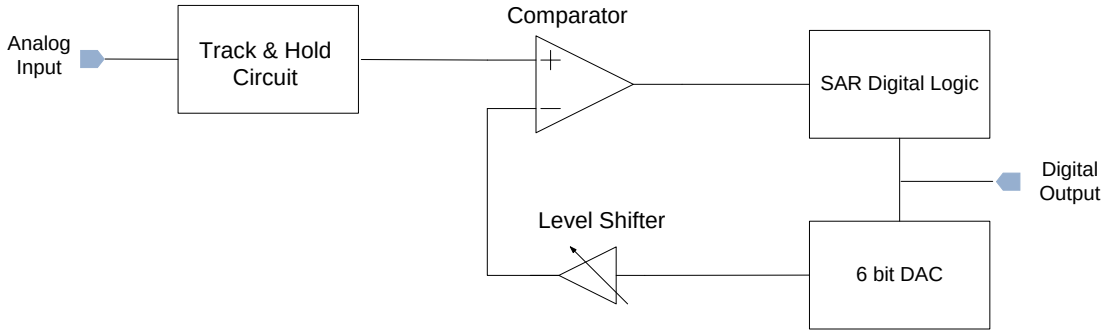

Fig 4.7 – SAR Architecture

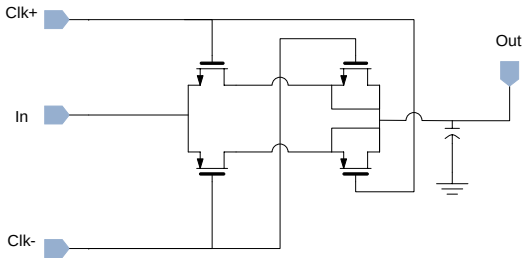

Fig 4.8 – Schematic of Sample & Hold Circuit

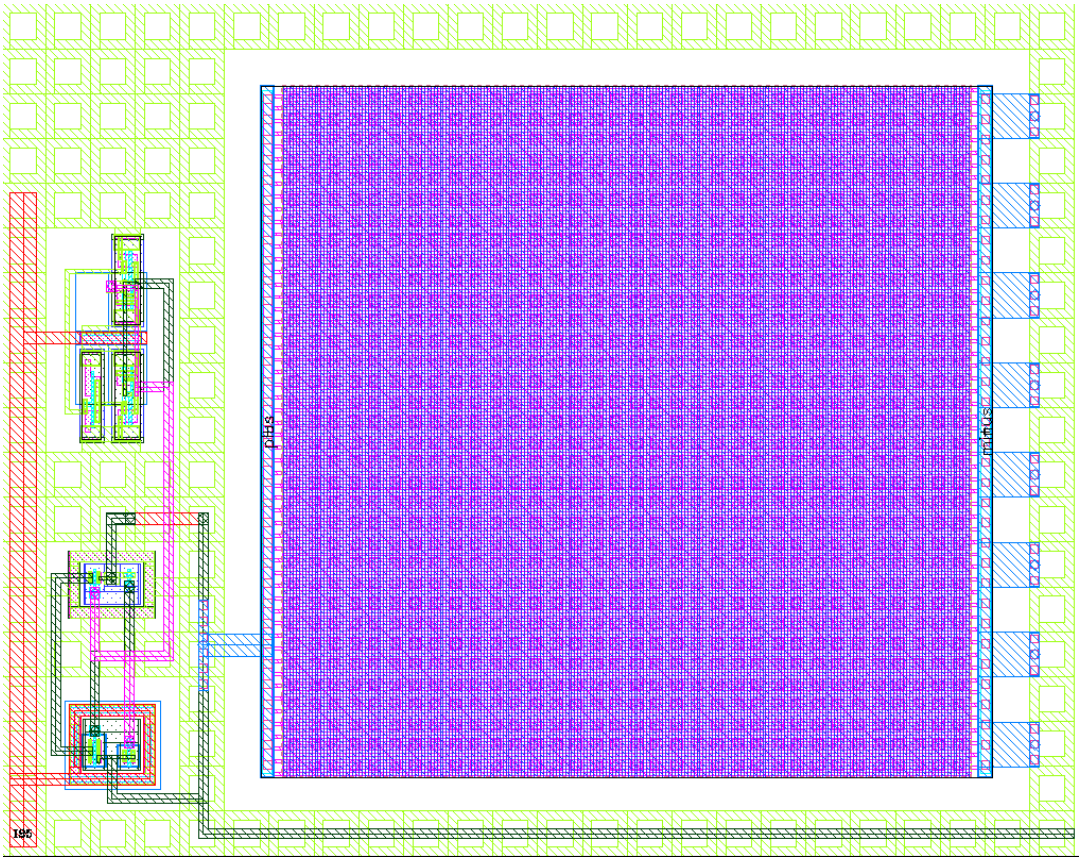

Fig 4.9 – Layout of Sample & Hold Circuit

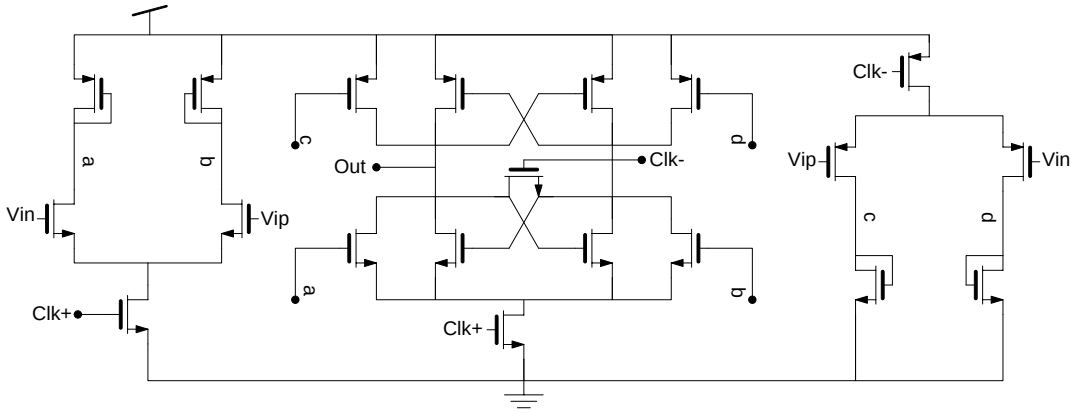

Fig 4.10 – Schematic of Comparator

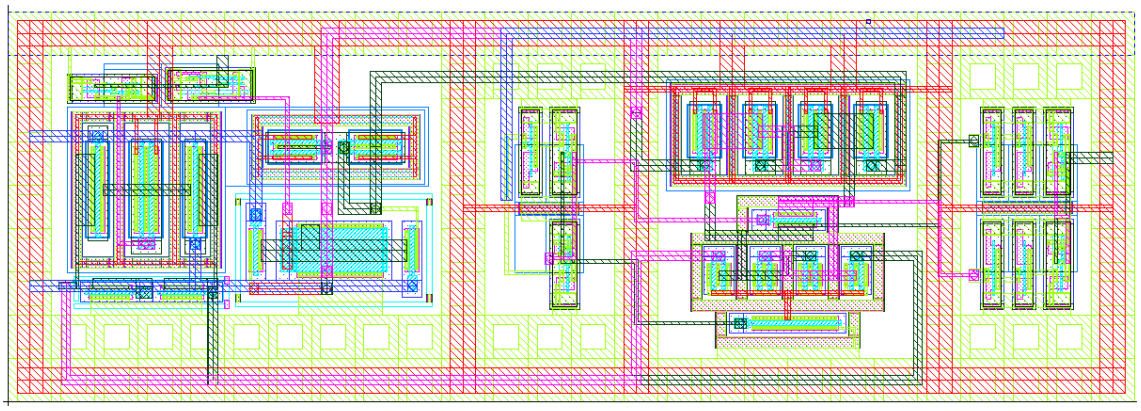

Fig 4.11 – Layout of Comparator

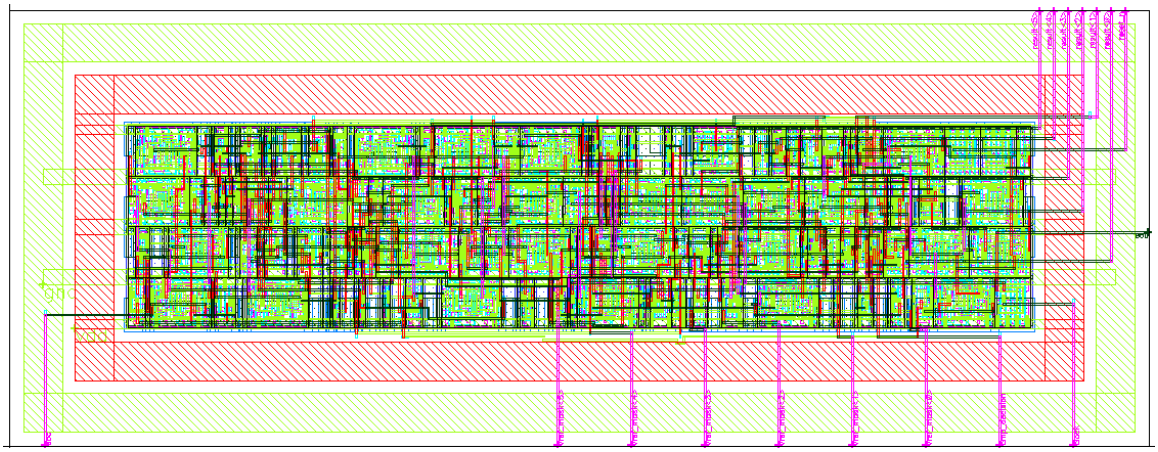

Fig 4.12 – SAR Logic

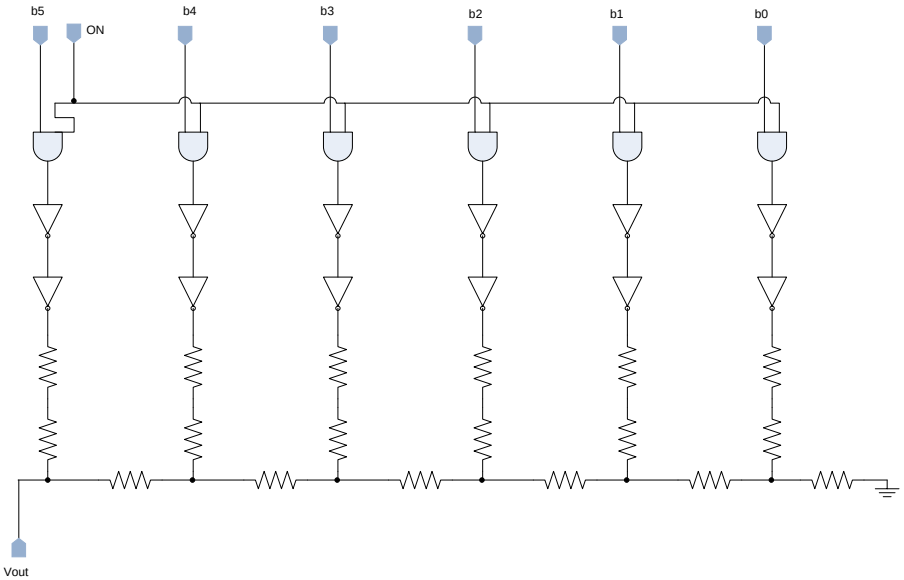

Fig 4.13 – Schematic of DAC

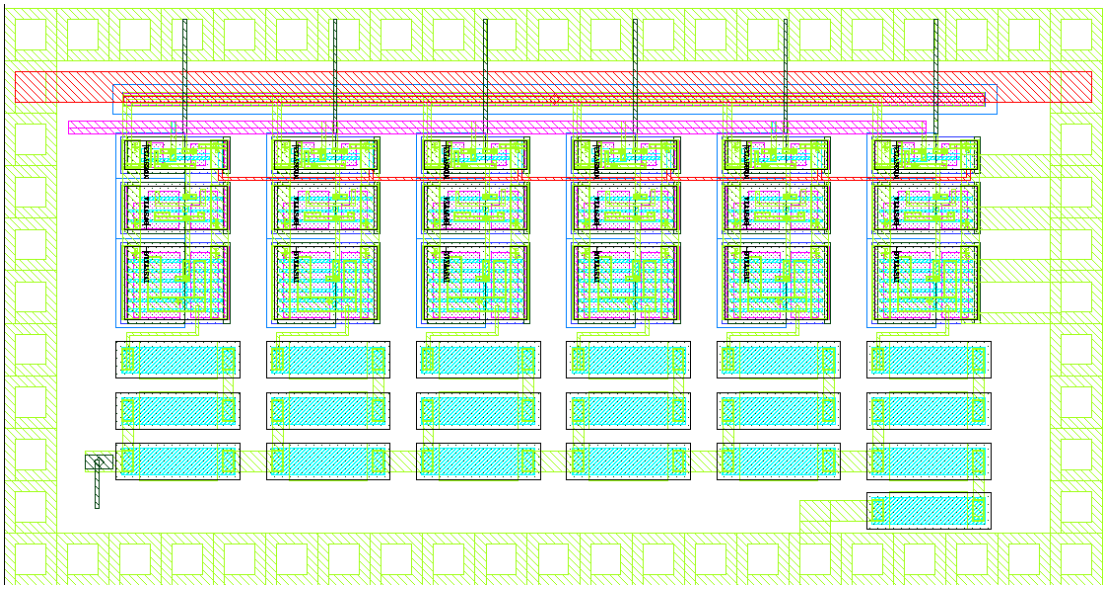

Fig 4.14 – Layout of DAC

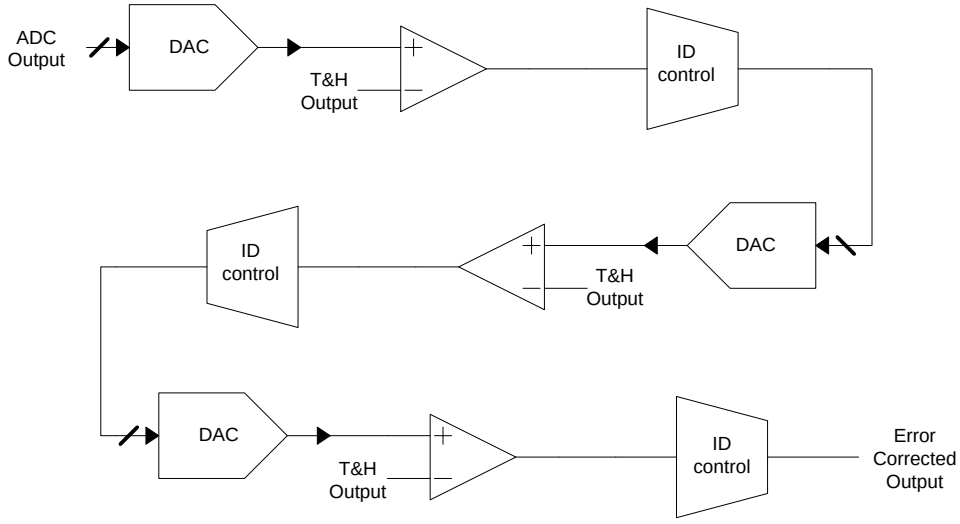

Fig 4.15 – Schematic of the Error Correction Circuit

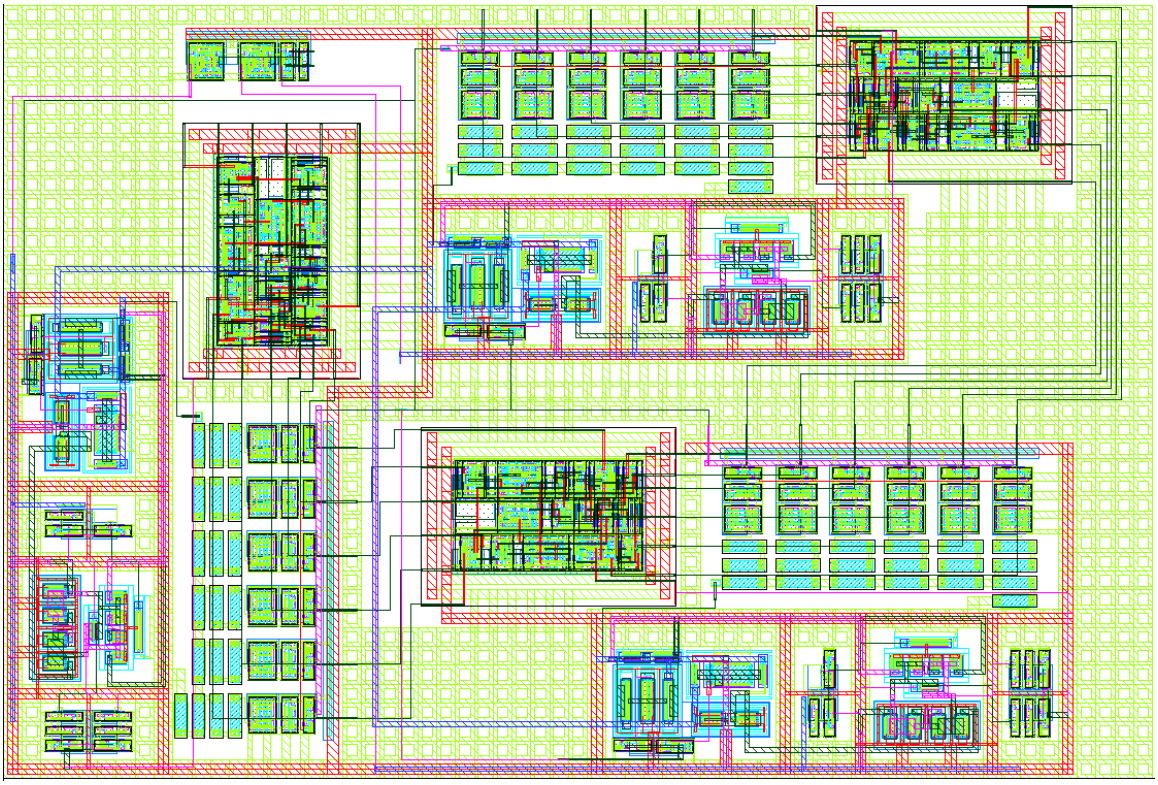

Fig 4.16 – Layout of the Error Correction Circuit

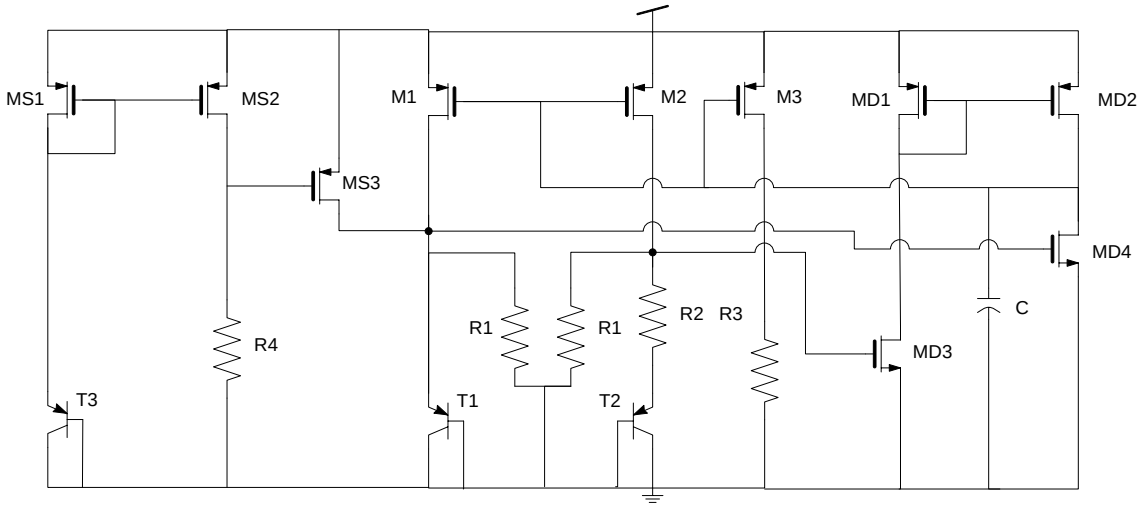

Fig 4.17 – Schematic of Bandgap reference circuit

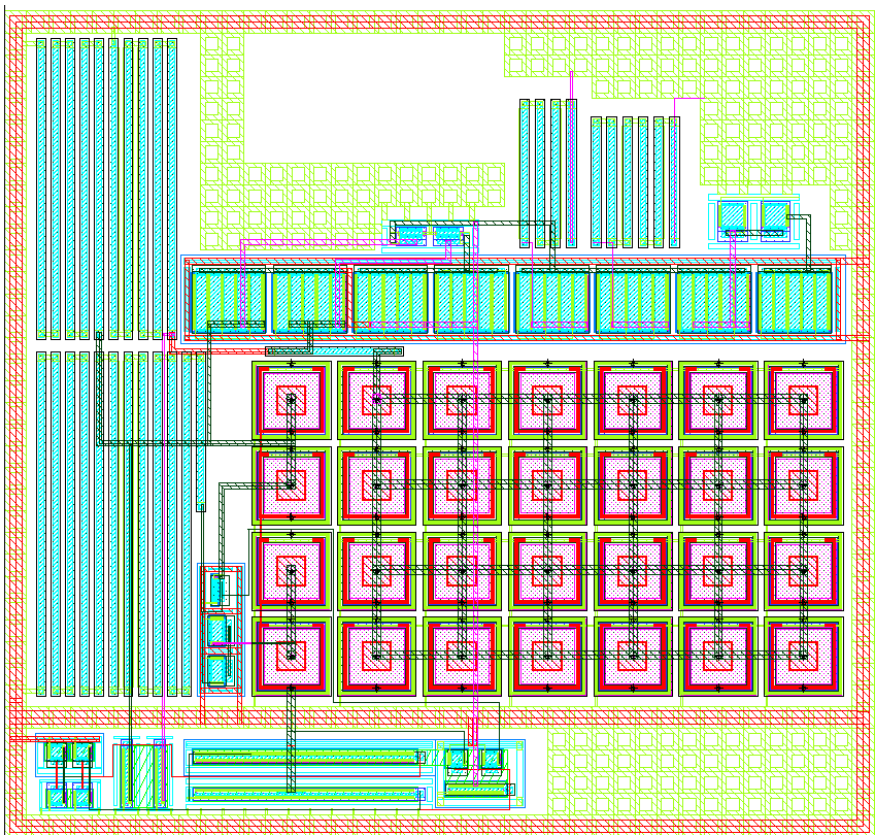

Fig 4.18 – Layout of Bandgap reference circuit

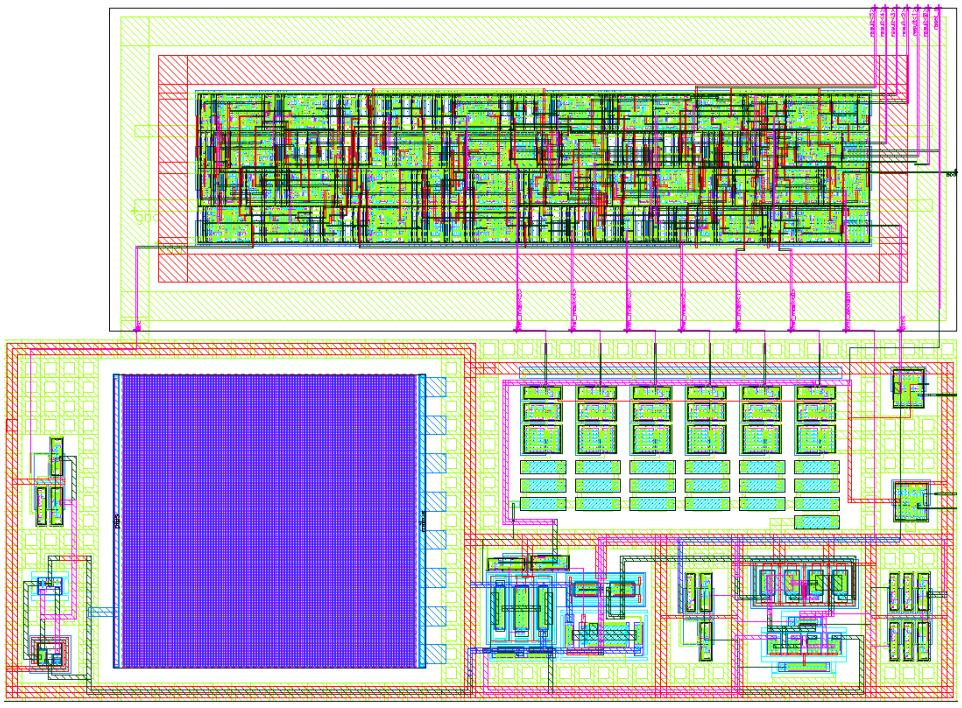

Fig 4.19 – Layout of SAR ADC

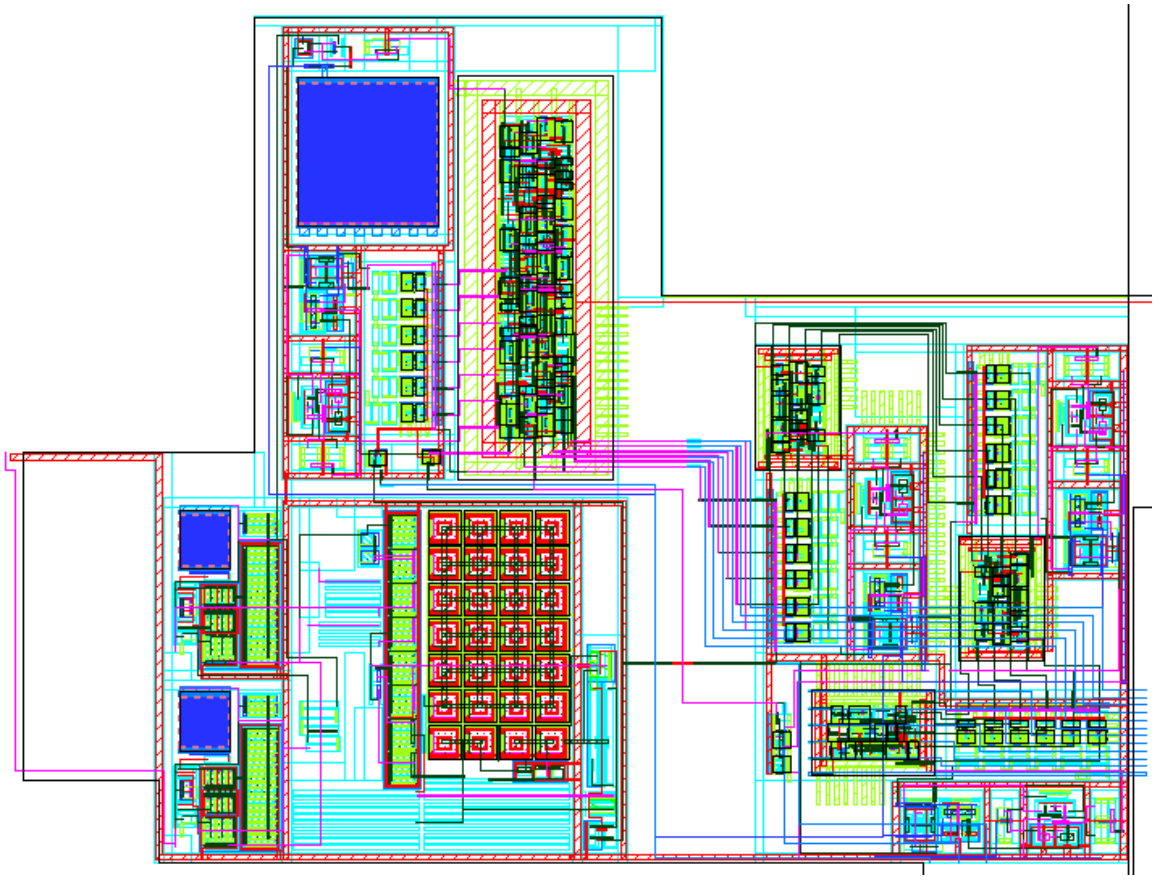

Fig 4.20 – Tx FE feedback control loop

The ADC output is applied to an encoder which looks up for the corresponding logic to be applied for the bias core to ensure proper performance settings in the Tx front end. The transmitter front end suffers from ambient temperature changes and local hot spots. The goal is to sense the temperature changes, calibrate the Gain and Linearity performance in order to maintain a constant output power. The temperature sensor is placed right next to the Power amplifier, hence any change in the temperature of the PA would be reflected as a Voltage output of the temperature sensor.The control signal from the encoder will be used to vary either Gain of the Tx IF block or the Output P1dB of the Tx Front end or even both depending upon the output power requirement. The data is further observed to provide control signals for the IF blocks preceding the transmitter front end.

The idea of control is to maintain a constant output power which can be set at four different states based on user input. The maximum output power of the whole chain defines the upper limit on what the user can extract out of this Tx, which is depicted by the curve identified as “Maximum Setting”. The other curves namely User selected level 1 to 3 basically refers to OP1dB, 2 dB backoff and 4 backoff (from OP1dB) at room temperature.

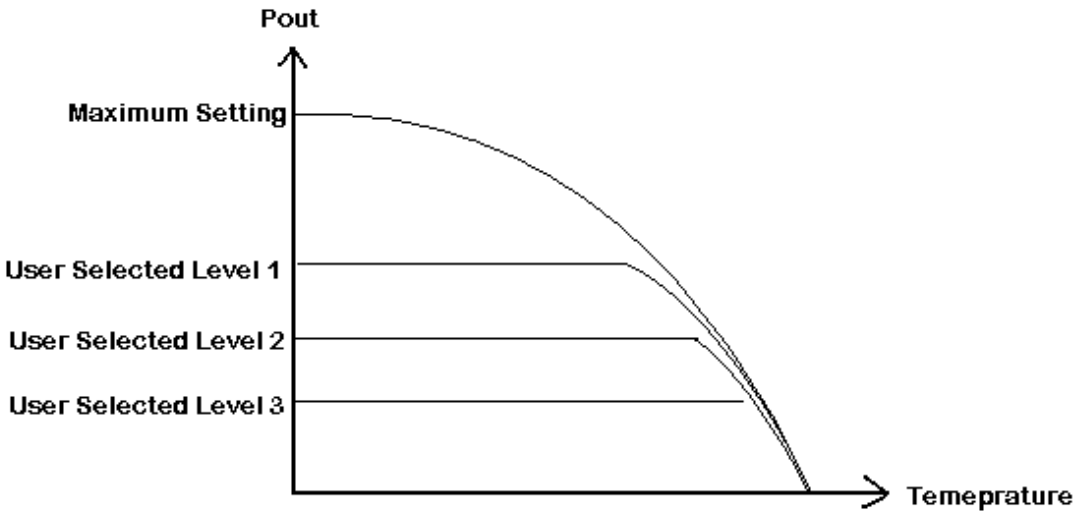

Fig 4.21 – Ideal output power variation with Temperature

The ideal curve has been translated into realistic achievable target curve depicted in Fig 4.22. As we can observe from the Fig. the User selected level 1 is different from the one depicted in Fig 4.22. The idea is to allow Low Output power variation within a specific temperature range. This pattern is repeated until the performance is limited by the “Maximum Setting” curve.

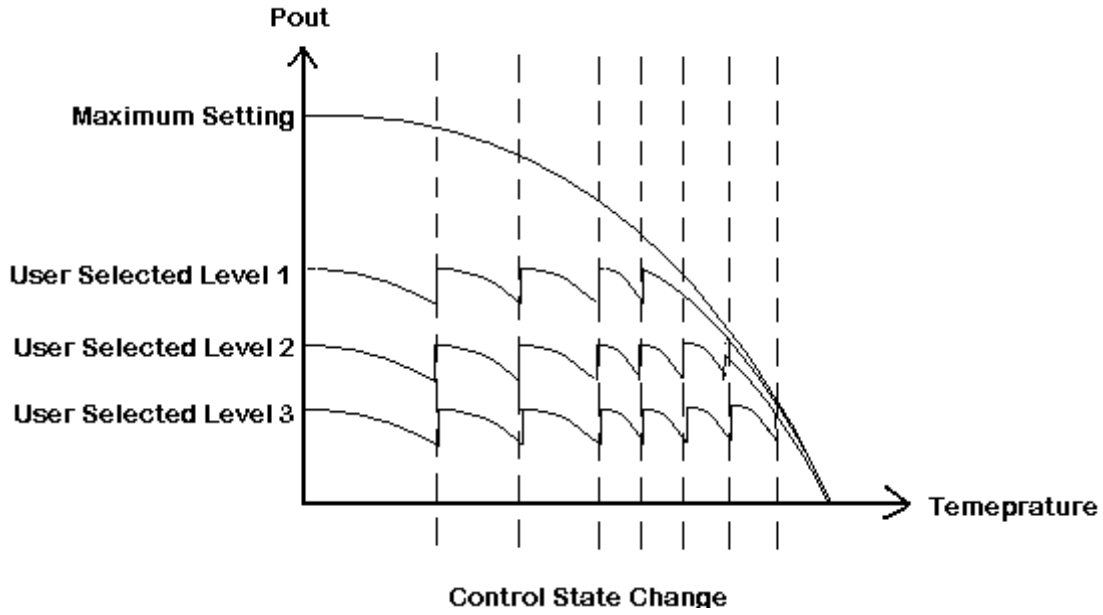

Fig 4.22 – Practical Characterisitcs of Output Power variation with Temperature

Before going into a detailed description we can choose some states for each curve setting. We will follow the following settings for our further discussion, with each state specified at room temperature

Maximum Setting : Saturated Output Power (P_{Sat})

User Selected Level 1 : Power @ Output P1dB point (P_{OP1dB})

User Selected Level 2 : 1 dB backoff from OP1dB
User Selected Level 3 : 2 dB backoff from OP1dB

By utilizing the performance data characterized by Gain, Output power and OP1dB variation with temperature the required control state change for the system with FIR enabled/disabled in the IF stage has been determined. The system has been modeled such that for a variation in output power approx in the range of 2 dB for a specific temperature range requires a control stage change.

A plot of performance from the temperature sensor has been analyzed by selecting a particular performance setting for the Tx Front End. The input power chosen for Tx FE comes from the maximum power output of the Tx IF block. The Table 4.2 shows the variation of Output power of the IF block with temperature and it is followed a graphical plot of the same as shown in Fig 4.23

Table 4.2 – Temperature versus Output power for IF section

Temp (deg C)	Pout (dBm)
-10	8.06
10	6.97
30	6.11
50	5.02
70	4.04
90	3.60

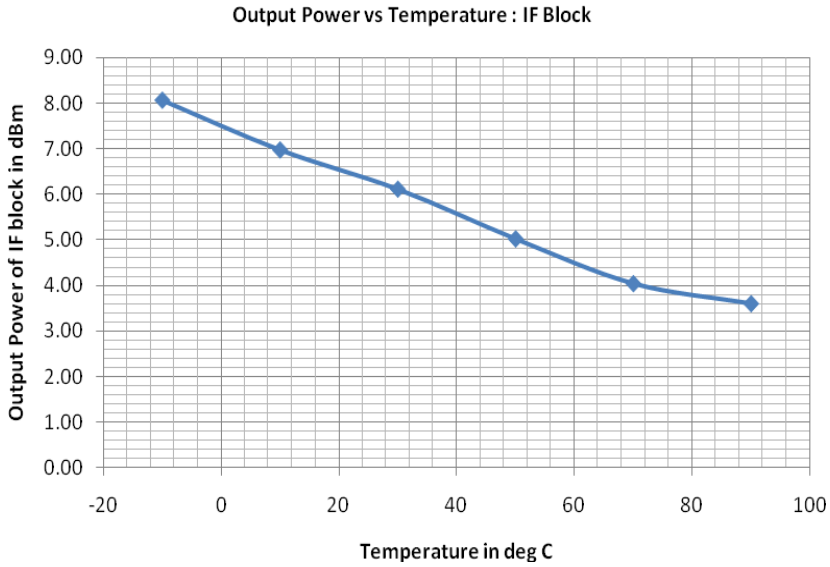

Fig 4.23 – Plot of Output power versus Temperature for IF section

From the Table 4.23 Output power data was applied as the Input power to the Tx Front End and thereby the Overall Gain and Output P1dB of the complete Tx chain were obtained. The details are presented in Table 4.3 and a plot of Output P1dB versus Temperature for Tx FE is given in Fig. 4.24.

Table 4.3 – Input, Output power, Gain and OP1dB variation with Temperature

Temp (deg C)	Input Power (dBm)	Output Power (dBm)	Gain (dB)	OP1dB (dBm)
-10	8.06	12	3.94	7.27
10	6.97	10.5	3.53	5.89
30	6.11	9.24	3.13	4.88
50	5.02	6.83	1.81	3.2
70	4.04	2.25	-1.79	-0.29
90	3.6	-1.91	-5.51	-4.86

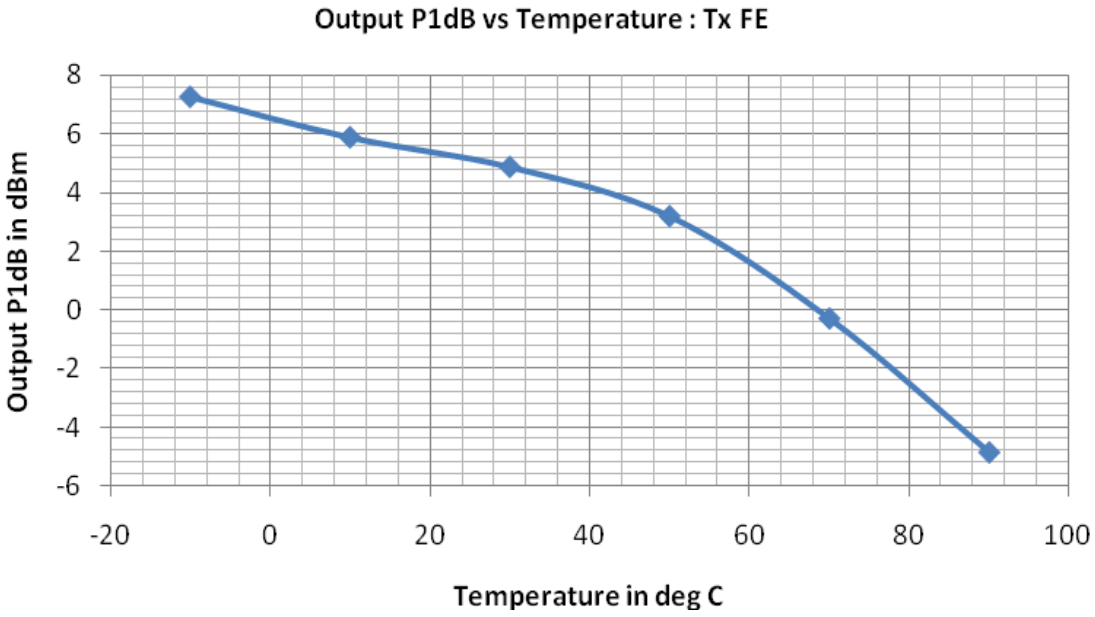

Fig 4.24 – Plot of Output P1dB versus Temperature for Transmitter front end

From the Fig. 4.23 and 4.24 encoder logic has been devised for choosing the temperature for Control state change by checking for Output power variation of around 2 dB. The proposed states are tabulated in Table 4.4,4.5 and 4.6.

Table 4.4 – Tabulation of Output power variation for various states

Temperature (deg C)	Δ Pout (dBm)
-10 to 20	2
20 to 40	1.8
40 to 50	1.4
50 to 60	2.4
60 to 70	1.75
70 to 80	1.85
80 to 90	-2.3

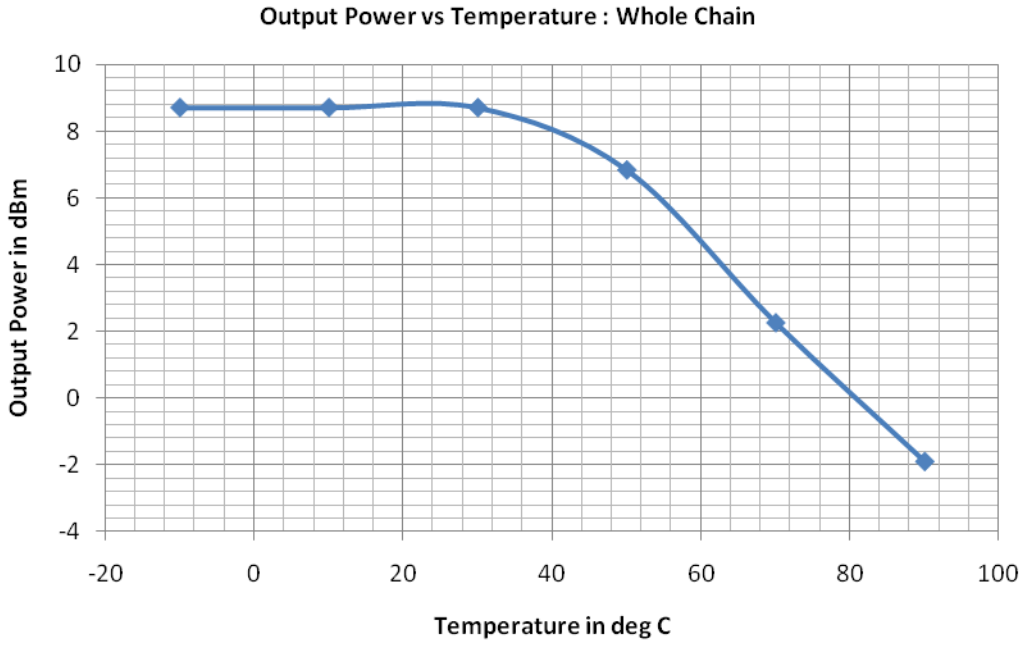

Fig 4.25 – Output Power versus Temperature plot for whole chain.

Table 4.5 – Gain, OP1dB & Saturation Power for various temperatures & control states.

Temp	Gain	OP1dB	Psat	Gain	OP1dB	Psat	Gain	OP1dB	Psat
	State 5			State 4			State 3		
-10	18.5	9	12	18.5	8.9	11	18.5	8.7	10.3
10	17.4	8.15	12	17.4	8.05	11	17.4	7.85	10.3
20	17	8.15	12	17	8.05	11	17	7.85	10.3
30	16.6	8.2	12	16.6	8.1	11	16.6	7.9	10.3
40	16	8.1	12	16	8	11	16	7.9	10.3
50	15.4	8.1	12	15.4	8	11	15.4	7.8	10.3
70	13.2	6.6	11	13.2	6.5	10	13.2	6.3	9.3
90	10	2.6	10	10	2.5	9	10	2.3	8.3

Table 4.6 – Gain, OP1dB & Saturation Power for various temperatures & control states.

Temp	Gain	OP1dB	Psat	Gain	OP1dB	Psat
	State 2			State 1		
-10	18.5	8	9.7	18.5	5.5	8.7
10	17.4	7.15	9.7	17.4	4.65	8.7
20	17	7.15	9.7	17	4.65	8.7
30	16.6	7.2	9.7	16.6	4.7	8.7
40	16	7.2	9.7	16	4.7	8.7
50	15.4	7.1	9.7	15.4	4.6	8.7
70	13.2	5.6	8.7	13.2	3.1	7.7
90	10	1.6	7.7	10	-0.9	6.7

The Fig. 4.26 and Table 4.7 show the performance characteristics of the Tx Front End Gain versus variation in temperature.

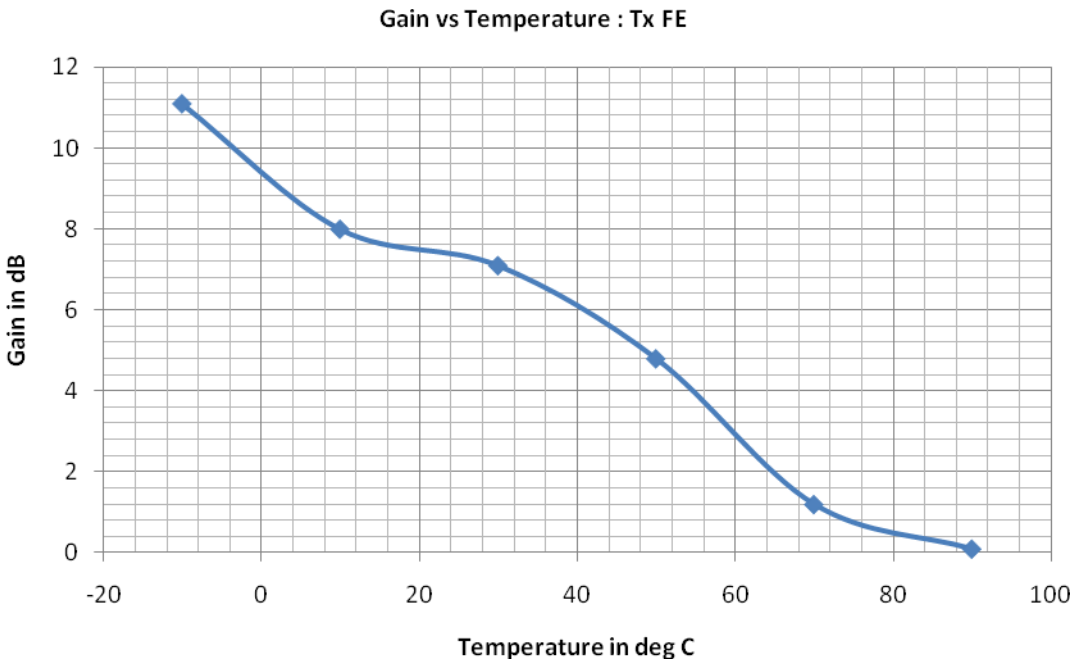

Fig 4.26 – Plot of Gain versus Temperature for Transmitter front end.

Table 4.7 – Tabulation of Temperature and corresponding Gain for Tx Front end.

Temp (deg C)	Gain (dB)
-10	11.1
10	8
30	7.1
50	4.8
70	1.2
90	0.1

The Table 4.7 indicates the temperature range for which the Tx Front End needs to be controlled. The IF Gain control mapping table has been built with both the IF block performance and the Overall lineup in mind. The mapping is provided in the form on Fig. 4.27 and 4.28, which shows the selection logic. Every point on the Fig. 4.27 and 4.28 have been chosen to obtain the highest possible performance state for Output Power and OutputP1dB. Then the 'State' of the Power Amplifier is chosen to fix the OP1dB to a specific value (5 dBm). Once the OP1dB is set the input power to the Tx front end is varied to obtain a constant Output Power (5 dBm). The input to Tx FE is the output of the IF block. The temperature sensor control mapping for RF and IF block is illustrated in Fig. 4.27 and 4.28, and their data points are given in Tables 4.5 and 4.6.

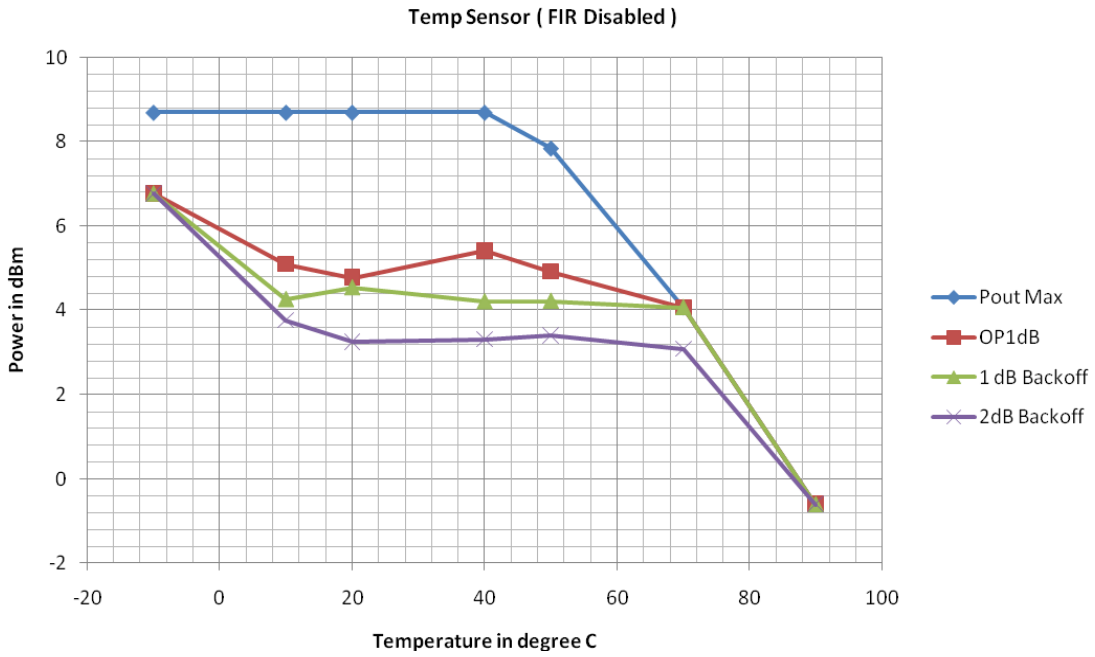

Fig 4.27 – Plot of Output power versus Temperature for FIR Disabled condition

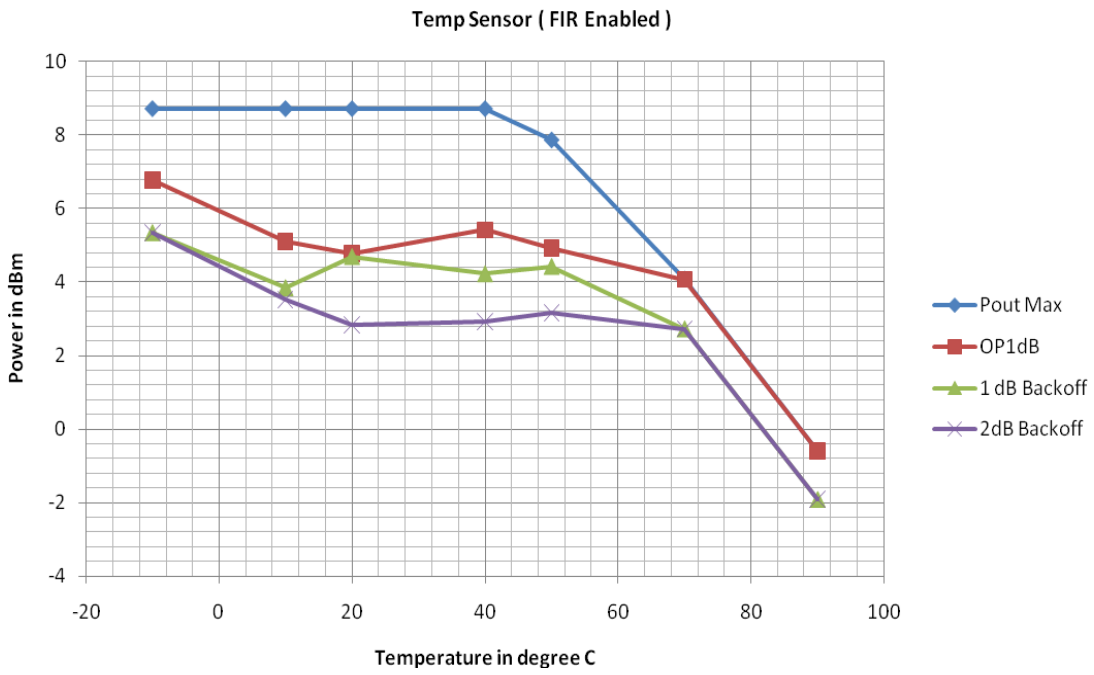

Fig 4.28 – Plot of Output power versus Temperature for FIR enabled condition

Summary

The performance summary of the overall feedback loop is based 0n the overall power consumption and the ability to turn the loop ON and OFF. The feedback loop doesn't need to operate when the transmitter is OFF; hence all circuits ADC, Sensor, band gap reference and error correction circuits have been designed with an option to turn them OFF. In the OFF state the overall current consumption is reduced to 0.4 uA, which is mainly the leakage current from various circuits. The overall power consumption and performance summary of the ADC is given in Table 4.9.

Table 4.8 – Power Consumption split up for the components

Blocks	Power Consumption	
Supply Voltage = 1.2 V	ON State	OFF State
SAR ADC	240 uW	0.8 uW
Temperature Sensor	160 uW	0.2 uW
Sense Amplifier	80 uW	0.2 uW
Total Power Consumption	480 uW	1.2 uW

Table 4.9 – Performance Summary of the SAR ADC

Parameters	Value
Clock Frequency	27 MHz
Speed	3.4 MSPS
DNL	0.15 LSB
ENOB	3.6
SNR	23.45 dB
DC Bias (Vdd / Id)	1.2 V / 200 uA
DC Power consumption	240 uW

CHAPTER 5

BANDGAP REFERENCE

Bandgap reference circuits are used in a host of analog, digital, and mixed-signal systems to establish an accurate voltage standard for the entire IC. The accuracy of the bandgap reference voltage under steady-state (dc) and transient (ac) conditions is critical to obtain high system performance. A constant reference voltage plays a crucial role in many applications such as DAC, Level Shifter and Sample Hold circuits as previously discussed in Chapter 3. The discussion presented here follows from a conventional bandgap reference leading to the new reference circuit designed and the impact of error sources on the design.

Conventional Bandgap reference

An accurate voltage or current reference is an important component of most integrated circuits. As its name suggests, a reference establishes a stable point (either a voltage or current) that the rest of the circuits in the system can utilize for generating reliable and predictable results. Whether used with a regulator to build a power-supply [26], in an operational amplifier to set up a bias point [27], or in an analog-to-digital converter (ADC) to establish a standard to compare voltages against [28], the accuracy of the reference directly impacts and often dictates the overall performance of a system. The bandgap reference circuit has been the most elegant way to fashion an integrated circuit (IC) voltage reference [29]-[30]. The circuit operates on the principle of adding a voltage that decreases linearly with temperature to one that increases linearly with temperature to produce a stable reference voltage with respect to temperature to the first order. Barring a small curvature, the base-emitter voltage of a bipolar transistor in the active region decreases linearly with temperature, i.e., it has a complementary-to-absolute-temperature (CTAT) dependence. The voltage that increases linearly with temperature, i.e., the

proportional-to-absolute-te mperature (PTAT) voltage, is produced through the difference in the base-emitter voltages of two bipolar transistors operating under different current densities (a manifestation of the well-known Gilbert principle [7]). A bandgap reference circuit adds these CTAT and PTAT voltages to produce a temperature-independent voltage VREF, as shown in Fig. 5.1. Conventionally, since the CTAT component is generated from a diode or base-emitter voltage, the value of the reference voltage is close to the bandgap voltage of silicon (≈1.2V). The reason for this is that the diode voltage has various temperature dependent terms and its zero-order or temperature-independent component is the bandgap voltage.

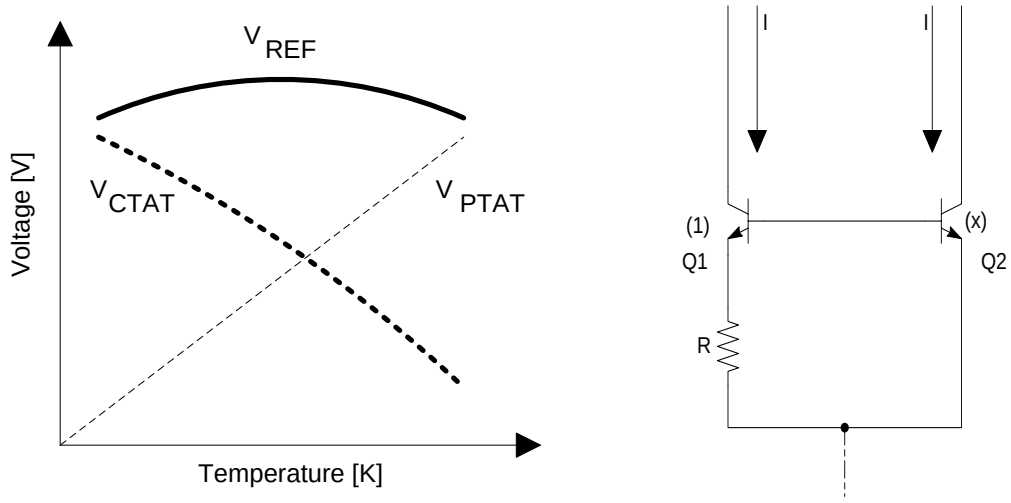

Fig 5.1 Temperature behavior of a typical Bandgap reference circuit

The Brokaw cell [29] shown in Fig. 5.1 forms the building block of most of the state of art bandgap references [26]-[29]. The current mirror forces the same current to both bipolar transistors Q1 and Q2, which have unequal areas and hence different base-emitter voltages. The difference of the base-emitter voltages of transistors Q1 and Q2, when applied to resistor R, produces a PTAT current I_{PTAT} and, consequently, a PTAT voltage V_{PTAT} across resistor R_{PTAT} :

$$V_{BE} = V_T \ln(\frac{I_C}{J_S.Area}) \tag{5.10}$$

$$I_{PTAT} = I_{C_1} = I_{C_2} = \frac{V_T}{R}\ln(C) \tag{5.11}$$

This voltage, having a positive temperature coefficient, is then added to the base-emitter voltage of Q1, which has a negative temperature coefficient to generate the temperature stable reference voltage V_{REF} [31], which is given by

$$V_{REF} = V_{CTAT} + V_{PTAT} = V_{BE_1} + 2I_{PTAT}R_{PTAT} \tag{5.12}$$

$$V_{REF} = V_{BE_1} + 2V_T \ln(C)\frac{R_{PTAT}}{R} \tag{5.13}$$

Note that one possible solution of Eqn. 5.13 occurs when both collector currents are zero, in other words, the bandgap reference is in a zero-current or "off" state. The circuit can be pulled out of this state if a perturbation of sufficient energy is applied – which is why all bandgap reference circuits require a start-up block that supplies this energy and thereby prevent the reference from settling into this undesired yet stable state. In the band gap a start-up block is added which draws current from the low-impedance node when the circuit is in the undesired "OFF" state. This current is then mirrored and forced into the collector of Q1 and the circuit eventually settles into the desired stable state when the branch currents are defined by the non-zero solution of Eqn. 5.13.

The principal role of a bandgap reference circuit is to generate an accurate and reliable reference voltage and most of its key specifications quantify the deviation of this voltage from its ideal value in the presence of various sources of error. These error sources exhibit a diverse behavior – they may be random or systematic in nature, affect the reference under dc or transient conditions, and have a short- or long-term influence on the accuracy of the output voltage. The impact of various error sources on the dc and ac accuracy of bandgap references shall be analyzed in detail in the subsequent chapters.

The initial accuracy of a reference quantifies the effect of random process variations, mismatch, and package stresses on the dc accuracy of the reference voltage. While the systematic component of these error sources can be accounted for through careful calibration, the random component affects each sample uniquely and initial accuracy can therefore only be specified after statistical analysis of a large sample size. It is defined as the ratio of the 3-σ variation ($3\sigma V_{REF}$) of a reference, over a large number of samples, to the mean value (μV_{REF}), and is given by

$$\text{Initial Accuracy} = \pm\frac{3\sigma V_{REF}}{\mu_{V_{REF}}} \tag{5.14}$$

During the design phase, the designer uses simulations on the initial accuracy of the untrimmed reference to determine the number of trim bits required to achieve a given accuracy specification. During the testing phase, the initial accuracy of the reference is measured after trim over several devices that have been obtained, ideally, from multiple wafers and multiple lots. Since trimming is carried out at room temperature for purposes of convenience, the initial accuracy is typically specified at room temperature (27°C).The temperature coefficient (TC) of a reference voltage quantifies the effect of temperature variations on its dc accuracy and is given by

$$TC = \frac{V_{REF-\max} - V_{REF-\min}}{(\frac{V_{REF-\max} + V_{REF-\min}}{2})} \cdot \frac{1}{T_{High} - T_{Low}} \tag{5.15}$$

Where T_{High} and T_{Low} are the upper and lower extremes of the measured temperature range and VREF-max and VREF-min are the maximum and minimum values of the reference voltage in this range. In other words, the TC of a reference is given by the deviation of the output voltage from its mean value in the tested temperature range. A reference in which the first-order temperature coefficient of base emitter voltage has been compensated has an ideal TC of 15-20ppm/°C due to the remaining non-linearity in VBE

(corresponding to roughly 3-4mV deviation on a 1.2V reference over -40°C to 125°C). Random process variations, mismatch, and package stresses alter the TC performance of a reference from its theoretical systematic value by introducing inaccuracies in the CTAT and PTAT components of the reference voltage that affect each sample uniquely. Practically, therefore, TC is specified by the box method, whereby it is calculated by using the absolute maximum and minimum reference voltage among all measured samples across the entire temperature range in Eqn. 5.15.

Bandgap reference for 90nm CMOS

Two components build up the output voltage of a bandgap reference. One is the voltage across a directly biased diode (base–emitter voltage V_{BE}) and the other is a term proportional to the absolute temperature (PTAT). The negative temperature coefficient of the former term compensates for the positive temperature coefficient of the latter. If $V_T = kT/q$ is used to obtain a PTAT voltage, it is well known that we have to multiply V_T by approximately 22 to compensate for the temperature dependence of the diode voltage. If this condition is satisfied, the generated bandgap voltage becomes approximately 1.2 V. Using a supply voltage (Vdd) as low as 1.2 V; we can generate a fraction of 1.2 V with similar temperature features. Since the bandgap voltage is given by

$$V_{BG} = V_{BE} + n\frac{kT}{q} \tag{5.16}$$

A fraction of traditional bandgap voltage is obtained by scaling the both the terms in Eqn. 5.16, using currents proportional to V_{BE} and V_T respectively. These currents are suitably added and transformed into voltage with resistor. We compensate for temperature dependence of the resistors used by fabricating them with the same kind of material. The circuit diagram in Fig 5.2 shows the implementation of the described operation.

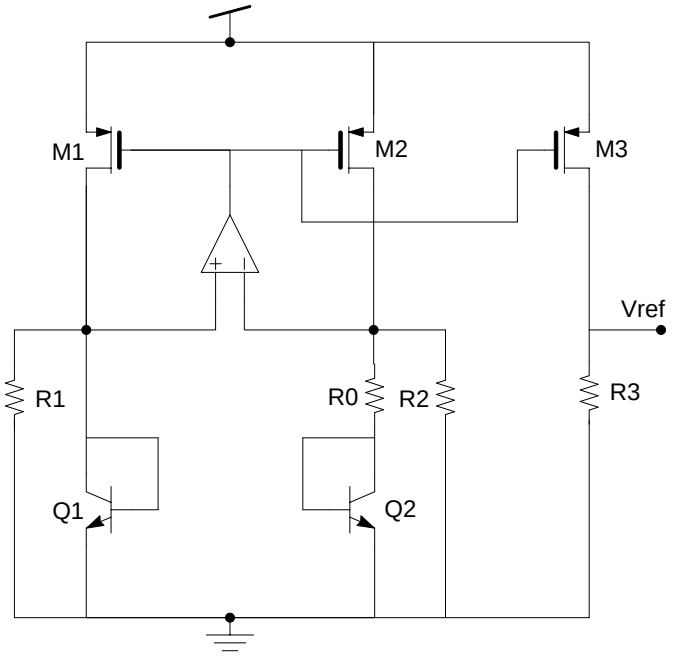

Fig 5.2 Schematic of Bandgap reference w/o curvature compensation

Two diode connected bipolar transistors with emitter area ratio N drain the same current, leading to ΔV_{BE} equal to $V_T \ln(N)$. Therefore the current in R_0 is PTAT. The operational amplifier forces the two voltages V_A and V_B to be equal, thus producing a current in the nominally equal resistors R_1 and R_2 proportional to V_{BE}. As a result, the current in M_1, M_2 and M_3 is given by

$$I_1 = \frac{V_T \ln(N)}{R_0} + \frac{V_{BE}}{R_1} \tag{5.17}$$

The output voltage is given by

$$V_{out} = \frac{R_3}{R_1}\left[\frac{R_1 \ln(N)}{R_0} V_T + V_{BE}\right] \tag{5.18}$$

The compensation of the temperature coefficients of V_T and V_{BE} is ensured by choosing values of N and of the R1/R0 ratio which satisfy

$$\frac{R_1 \ln(N)}{R_0} = 22 \tag{5.19}$$

In particular, to minimize the spread of the resistors, we chose N = 24. Moreover, since transistors M_1, M_2 and M_3 maintain almost the same drain-source voltage V_{DS}, independent of the actual supply voltage, the power supply rejection ratio of the circuit is only determined by the operational amplifier. From the circuit, it is clear that the minimum supply voltage is determined by the base emitter voltage plus the saturation voltage of a p-channel transistor. Therefore 1.2 V is enough to operate the circuit; it must ensure the operational amplifier operates properly which is the true limit of the circuit.

The bandgap reference needs an operational amplifier whose input common mode is around 0.7 V. Moreover, since the output node drives the p-channel current sources, its output quiescent voltage should be below $V_{DD} - V_{Th-p}$. Assuming $V_{DD} = 1.2V$ and $V_{Th-p} = 0.7V$, the output voltage results as low as 0.2 V. Moreover the gain of the operational amplifier must be around 60 dB without any bandwidth constraints. The design condition leads to the following considerations. First input common mode voltage makes it difficult to accommodate an n-channel input differential stage, which requies a level shift of input voltage by 200mV towards the supply rail. Secondly the low output voltage prevents the use of cascode configuration. Finally the required biasing conditions can lead to significant offset, which can become the key limit to the correct operation of the bandgap circuit. The operational amplifier used here consists of basic differential pair with current mirror load. The input pair device size is kept at bare minimum to ensure the current consumption is less than 60 uA. This ensures a flow of 12 uA current in each arm of the bandgap reference cell. The same current is mirrored in another arm with a resistor to compensate for the CTAT performance. The output voltage is 0.6 V.

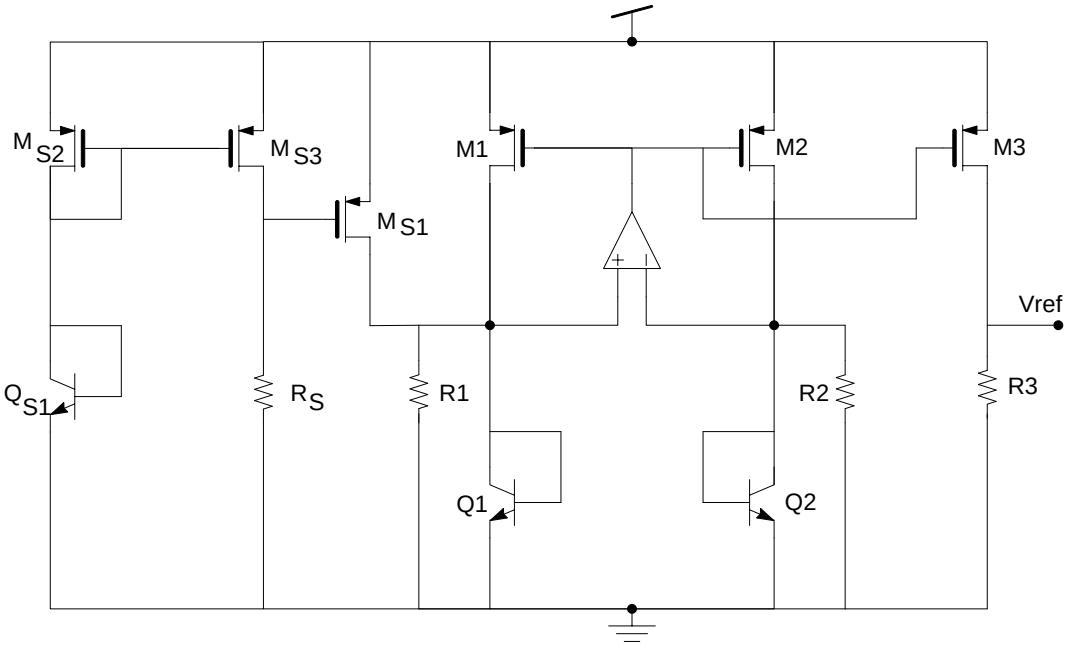

Fig 5.3. Schematic of Bandgap reference with start up circuit

The proposed bandgap reference needs a more effective startup circuit than those usually adopted, consisting of simple pull-up or pull-down resistors. In conventional bandgap architecture the nonlinear I-V relationships of a diode and N times larger diode with a resistance R_0 in series have two well-defined crossing points. Therefore, a very small current flowing for a short period of time in the diodes is sufficient to lead the circuit towards the proper operating point. By contrast, the use of resistors in parallel to the diodes makes the two I-V relationships more linear, and consequently, the crossing points are much less defined. Moreover in order to turn on the diode connected BJT's, a significant amount of current ($V_{BE}/R_{1,2}$) has to flow in the resistors (R_1 and R_2). The startup circuit shown in Fig. 5.5 ensures additional current is continuously provided to diodes and the resistors until the bandgap circuit reaches the proper operating point.

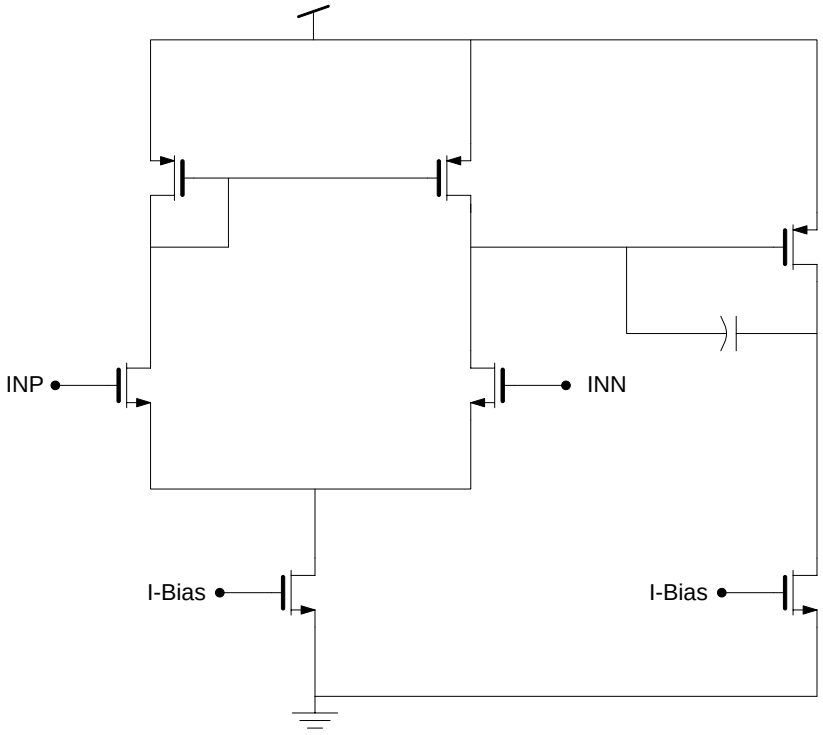

Fig 5.4 Schematic of the Two Stage Operational amplifier

In particular if the current in Q_1 is zero, the current in Q_{S_1} is zero as well and the p-channel sources (M_{S2} and M_{S3}) is off. The gate of M_{S1} is pulled down to ground. Thus injecting a significant current into Q_1 and R_1. At the end of startup phase, when the circuit reaches normal operating conditions, the current in M_{S3} and the value of R_S used brings the gate of M_{S1} close to V_{DD}, thus turning off the startup circuit. A weak startup current in the operational amplifier can be a source of a significant systematic offset, which could lead the bandgap to a metastable operating point. Fortunately this is not the case in the circuit used, because we control the operational amplifier with the same reference current used in the bandgap. Consequently we can achieve an exact tracking of currents in the input differential stage and in the current sources, nulling the systematic offset even during the startup phase.

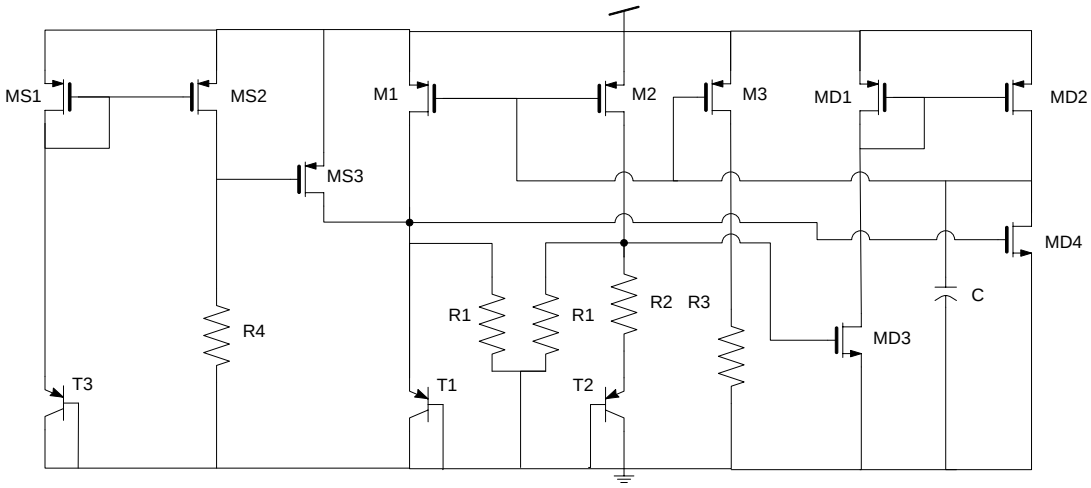

Fig 5.5 - Schematic of Bandgap reference circuit with a Differential amplifier used in place of Operational amplifier to reinforce the Gate of M1 and M2.

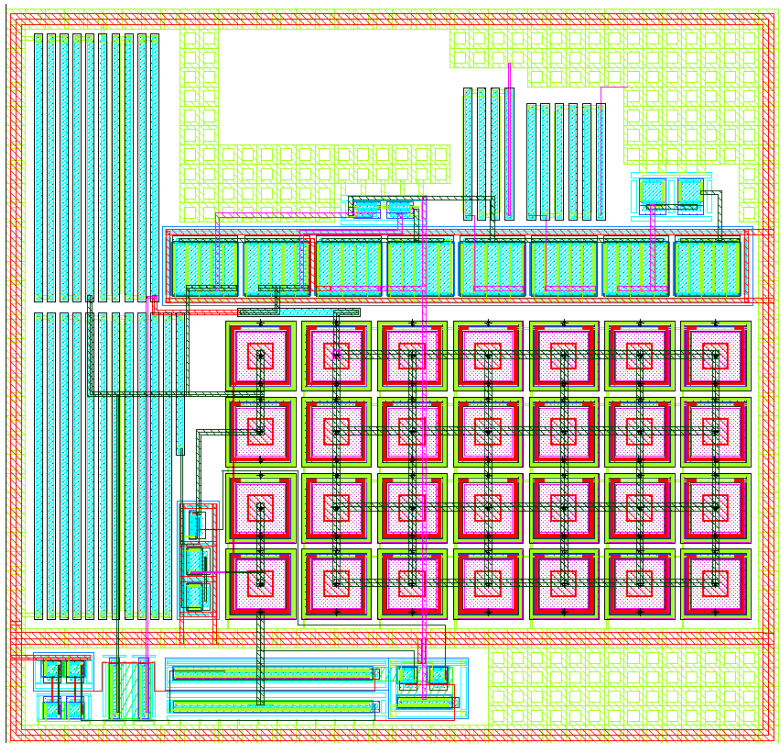

Fig 5.6 – Layout of the Bandgap reference circuit.

Low output impedance enables a voltage reference to shunt noise and source currents and thereby maintain high dc and ac accuracy despite variations in loading conditions. It is evident from a number of datasheets [38]-[41], most of the references used in industry for noise-sensitive sub-system like an analog-to-digital converter or

voltage-controlled oscillators are variations of the regulated references presented in [29], [32]. The low output impedance is achieved in this reference by adding an operational amplifier with n-type input pair. This OTA transforms the high impedance output node to a low impedance output node to provide bias.

Error Sources

A number of factors degrade the accuracy of CMOS bandgap reference circuits,including process variations and mismatch, package stresses, power-supply fluctuations [30]-[34], load variations, and temperature changes. This chapter discusses these various error sources and quantifies their impact on accuracy. Errors due to process variations and mismatch are first analyzed, after which the systematic and random effects of package shift are studied. Next, an intuitive model for predicting the effect of line variations on accuracy is presented. The effects of load variations on the output of a reference are then discussed. Finally, the deviation of the reference voltage due to temperature changes is analyzed. The various error sources discussed here are

a) Process variations and Mismatch.
b) MOSFET mismatch
c) Resistor mismatch
d) Resistor variation
e) BJT mismatch
f) Base emitter voltage variation
g) Power Supply variations
h) Load variations

Conventionally, process variations and mismatch have been considered to be error sources that a circuit designer has no control over. Their harmful effects have therefore been mitigated primarily through careful layout followed by intensive trimming during

the manufacturing process. However, as requirements on initial accuracy rise, raising the level of trimming implies consuming more silicon area and using longer test times to accommodate a higher number of trim bits. Finally, this translates to incurring higher manufacturing costs. Therefore, even though the importance of judicious layout cannot be overstated nor the effectiveness of trimming denied, quantifying process-induced errors is critical to identifying and studying the dominant culprits and, ultimately, exploring alternate strategies for obtaining high accuracy.

The basic topology of the circuit used for analyzing error sources in bandgap references is shown in Fig. 5.7. This is the building block for most bandgap reference circuits and expressions for the error in the reference voltage of this circuit can easily be applied to most practical bandgap implementations. Referring to Fig. 5.7, the reference voltage generated by a conventional first-order bandgap reference is given by

$$V_{REF} = V_{BE1} + 2(\frac{V_T \ln C}{R})R_{PTAT} \tag{5.20}$$

And consequently

$$\Delta V_{REF} = \Delta V_{BE1} + 2\Delta I_{PTAT} R_{PTAT} \tag{5.21}$$

Where VCTAT and VPTAT are the complementary-to-absolute-temperature (CTAT) and proportional-to-absolute-temperature (PTAT) components of the reference voltage, respectively, IPTAT is the PTAT current, and C is the ratio of the current densities of Q1 and Q2. In Eqn. (5.21) and subsequent expressions, the Δ symbol indicates a change in the variable that follows it. The factor of '2' arises since the current through RPTAT is the sum of the PTAT currents flowing through Q1 and Q2 and this value may change from one circuit to another. The magnitude of the error in the reference voltage (ΔVREF) is obtained by comparing the reference voltage of an 'ideal' bandgap reference circuit to that in which the particular error source being studied is artificially introduced.

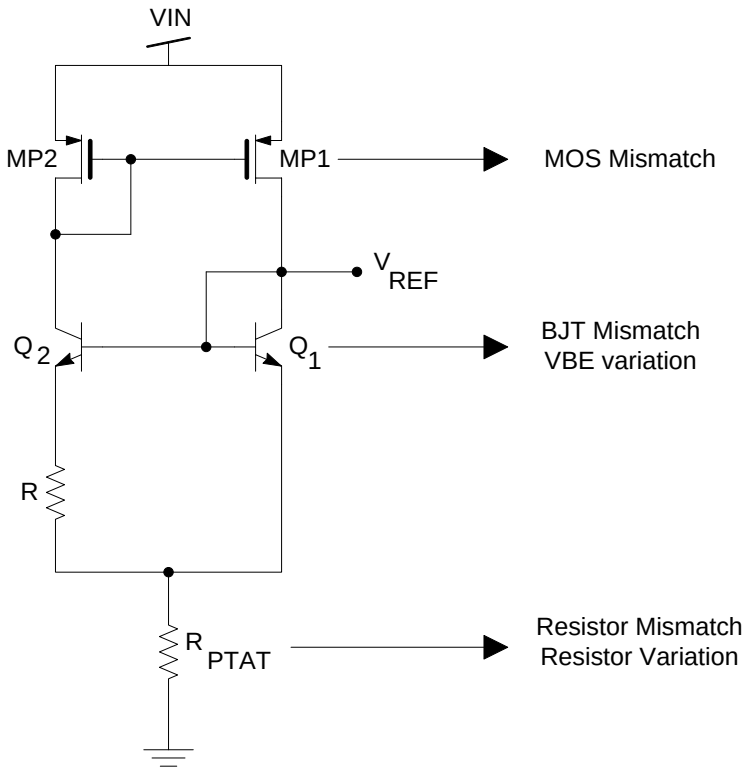

Fig 5.7 Basic band gap reference cell

MOS Mismatch - A mismatch in MOS devices MP1-MP2 leads to a deviation in the desired ratio of the mirror currents. The mismatch may occur due to a disparity in the aspect ratio (W/L) or threshold voltage (VTH) of the MOS pair. Obtaining precisely matched MOS devices, however, is extremely challenging in the noisy, low-voltage environments characteristic of SoCs. Improving dc accuracy through increases in transistor area (for better MOS matching) incurs the penalty of higher parasitic capacitance at the mirror nodes (such as VM in Fig. 5.7). This ultimately leads to a reduction in the reference's bandwidth which lowers its ability to respond to line and load fluctuations in noisy SoC domains and consequently degrades its ac accuracy. Moreover, shrinking supply voltages, characteristic of modern CMOS processes, is imposing stringent constraints on the maximum allowable headroom analog circuits can utilize, thereby making it difficult to generate the large overdrives critical for a high degree of matching performance. Finally, since the threshold voltage of a MOS device has non-

linear temperature dependence, the offset also varies nonlinearly with temperature, making it difficult to compensate, even through trimming. For these reasons, MOS mismatch is the most critical process-induced error source in bandgap reference circuits.

Resistor mismatch - Though resistors can be matched to a high degree of accuracy (typically 1% and 0.1% through meticulous layout), resistor mismatch influences the PTAT voltage, which is a strong function of the ratio of resistors RPTAT and R. In particular, the use of dummy devices at the edges of resistor arrays can reduce mismatch due to etching errors while increasing resistor area spatially averages fluctuations in geometry. Techniques like common-centroid layout and inter digitation spatially average geometry and dopant fluctuations over resistor arrays, leading to a high degree of matching.

Resistor variation - Process variations lead to a large deviation in resistor values (often as large as 20%). This variation changes the VBE component by altering the PTAT current flowing in the circuit. These errors can be reduced by choosing a material for the resistor that does not exhibit significant spread in resistivity over process, voltage, and temperature. Polysilicon resistors, for example, typically exhibit a smaller variation of resistance with voltage and temperature, than n-well resistors. While resistor variations, which occur as a result of deviations in sheet resistance from one die to another, cannot be controlled, they have a minimal impact on the accuracy of the bandgap reference – even a 20% variation generates an error of roughly 5mV, equivalent to a 0.5% error in the reference.

BJT mismatch errors result from a deviation in the desired ratio of the saturation current density J_S of transistors Q_1 and Q_2. If δ_Q is the fractional error in the ratio, the error in the reference voltage is given by

$$\Delta V_{REF} = \frac{V_{PTAT}}{\ln C}\delta_Q \tag{5.22}$$

The mismatch is given by

$$\delta_Q = \frac{\Delta I_S}{I_S} \tag{5.23}$$

Since bipolar transistors can be matched to a high degree of accuracy (e.g. 0.1-1%), BJT mismatch has a small effect on the accuracy of the reference voltage.

Base Emitter Voltage variation - The spread in the base-emitter voltage of the bipolar transistor used to generate the CTAT component can be a considerable source of error because it directly translates to an error in the reference voltage and is dictated entirely by the process used. For the CMOS references proposed in [20]-[23], in which circuit techniques like dynamic element matching and auto-zeroing have been used to eliminate the effect of device mismatch, the residual error in VREF of 3-10mV is primarily due to the spread in VBE. This indicates that substrate PNPs available in standard CMOS technologies exhibit a lower VBE variation than their high-β NPN counterparts in BiCMOS processes, which display a variation of 20-30mV. This performance advantage of substrate PNPs has been attributed to their wider base width which spatially averages dopant variations in the base. This leads to a higher degree of uniformity in base-doping and a more stable saturation-current density.

Power Supply Rejection

Conventionally, the effects of power-supply fluctuations on the reference voltage can be suppressed by adding large external bypass capacitors at the input and output of a discrete bandgap reference IC. As systems undergo higher levels of integration, however, external components increase the bill-of-materials (BoM) and thereby directly impact cost. Simultaneously, higher integration has resulted in the fabrication of switching

digital circuits, which are inherent noise sources, in close proximity to critical analog blocks. The high frequency noise generated by digital circuits can easily couple onto supply lines through crosstalk and subsequently degrades the ac accuracy of a noise-sensitive bandgap reference. Studying the ability of a reference to suppress supply noise across a wide spectrum of frequencies is therefore crucial for a designer to devise economically viable yet effective techniques to improve its Power-Supply Ripple-Rejection or PSRR performance.

A number of analog circuits, including operational amplifiers, linear regulators, and bandgap references employ shunt feedback to regulate their output voltage. As shown in Fig. 5.8, the output in these circuits is typically sampled by an amplifier that uses the error in the feedback voltage and desired voltage to drive the gate (or base) of a MOS (or bipolar) transistor M_0. The transistor M_0 sources (or sinks) an appropriate current into (or from) the impedance at the output to maintain a steady voltage in the presence a varying power-supply. The feedback loop is characterized by gain $A_{OL}\beta$ and is comprised of the error amplifier, which exhibits an output resistance and corresponding pole ($f_{p-oA} \simeq 1/2\pi R_{O-A}C_{O-A}$), and M_0, which has a drain-source resistance and an output pole determined by the output capacitor.

It has been shown that the PSRR of these closed-loop systems is intimately related to the open-loop parameters of their feedback loop [26]-[28], [31], [33]-[34]. While the analytical expressions derived in [29], provide a designer with good estimates for PSRR performance, they do little to provide him/her with an intuitive understanding of how the open-loop response of these circuits influences their ability to reject noise from the power-supply. An intuitive and insightful model for analyzing PSRR is presented in Fig. 5.8. While the model is valid for any circuit that employs shunt

feedback to regulate its output, it shall be discussed here in the context of a regulated band gap reference.

In its simplest form, the PSRR transfer function (a ratio of the output to the supply ripple) can be viewed as the effect of a voltage divider caused by impedance between the supply and the output and impedance between the output and ground. Using this approach, the model consists of an impedance ladder comprising of the channel resistance of output device Mo (rds) and a parallel combination of the open-loop output resistance to ground (zo) and the shunting effect of the feedback loop (zo-ref). Hence, referring to Fig. 5.8, we can see that

$$z_o = z_{co} \parallel R_o \tag{5.24}$$

$$z_{o-ref} = \frac{z_o \parallel r_{ds}}{A_{OL}\beta} \tag{5.25}$$

The error in the reference voltage due to supply voltage changes, in other words, the PSRR performance of the reference, is given by

$$PSRR = \frac{\delta V_{ref}}{\delta V_{dd}} = \frac{z_o \parallel z_{o-ref}}{r_{ds} + z_o \parallel z_{o-ref}} \tag{5.26}$$

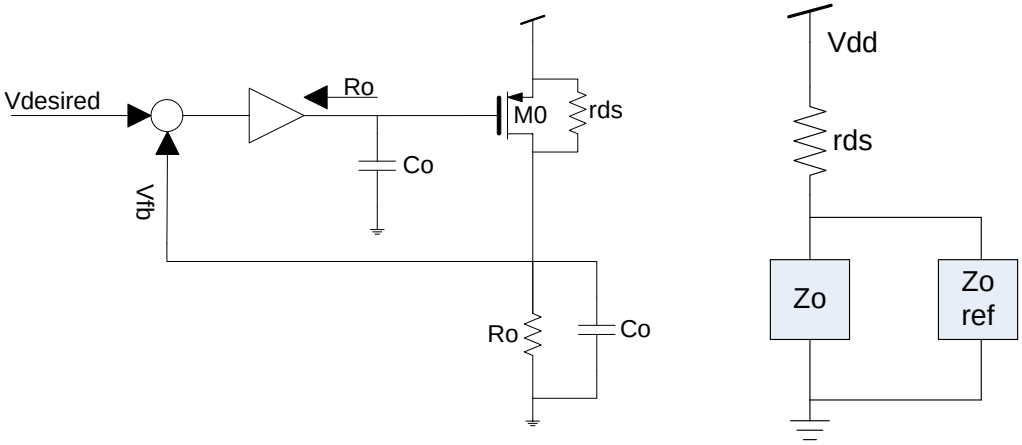

Fig. 5.8 PSRR analysis for a simple resistive divider topology

Fig. 5.9 depicts the sketch of a typical PSRR curve and how the intuitive model is used to determine the PSRR performance of a regulated reference over a large range of frequencies, simply by accounting for the frequency dependence of Z_O (Output impedance) and Z_{O-ref} (Regulated output impedance). The PSRR performance over various frequency bands is given below:

a) PSRR at DC & Low frequencies: At DC / low frequencies the high open loop gain determines the PSRR.

$$PSRR = \frac{1}{A_{OL-dc}\beta} \tag{5.27}$$

b) PSRR at Moderate frequencies: The shunting effect of the feedback loop deteriorates at frequencies beyond the bandwidth of the amplifier, thereby causing an increase in the regulated output impedance. This leads to rise in output ripple and consequently the PSRR expression (transfer function) can be given as:

$$PSRR = \frac{1+\frac{s}{BW}}{(A_{OL-dc}\beta)(1+\frac{s}{UGF})} \tag{5.28}$$

The presence of a pole at Unity gain frequency, as predicted by the Eqn. 5.28 indicates that the PSRR deteriorates due to the absence of increased closed loop resistance at UGF. At this stage the effect of the feedback loop no longer exists and PSRR performance is determined simply by the frequency-independent resistive divider between the channel resistance rds of the output device and resistor Ro. The PSRR is now given by

$$PSRR = \frac{z_o}{z_o + r_{ds}} = \frac{R_o}{R_o + r_{ds}} \approx 1 \tag{5.29}$$

At these frequencies PSRR of the reference is the weakest since the closed loop output resistance is not decreased by the feedback loop and the output capacitor cannot shunt the output ripple to ground because the impedance is still high.

c) PSRR at High frequencies: When the output capacitor starts shunting R_o to ground, a smaller ripple appears at the output, causing an improvement in PSRR performance (since z_o decreases with increasing frequency) and the second PSRR pole. Thus the new PSRR expression can be given as:

$$PSRR = \frac{z_{Co}}{z_o + r_{ds}} \tag{5.30}$$

The effectiveness of the output capacitor at high frequency is minimal, theoretically an ac short. So this gives rise to a zero on the PSRR curve at

$$z_2 = \frac{1}{2\pi Z_o C_o} \tag{5.31}$$

A potential-divider-based model for analyzing the PSRR of bandgap references over a wide range of frequencies was presented. Trace '1' in Fig. 5.9 represents a typical PSRR curve of a conventional reference, as predicted by this model. In particular, PSRR at low frequencies, its dominant zero, and two subsequent poles correspond to the dc open loop gain (Aolβ), the bandwidth of the amplifier (BWA), the unity-gain frequency of the system (UGF), and the output pole (po), respectively. These curves indicate the worst-case PSRR occurs in the vicinity of the UGF of the system, typically in the range of 1-10MHz [29], [31]. Intuitively, the loop gain provides high supply-ripple rejection at low frequencies, while the output capacitor shunts any ripple appearing at the output to ground at very high frequencies. Numerous techniques have been used to improve the PSRR of bandgap references. The simplest solution is to place an RC filter in line with the power-supply to filter out fluctuations before they reach the reference [1], as shown in Fig. 4.2(a). This adds a pole to the PSRR curve at the filter's corner frequency, as shown by trace '2' in Fig. 5.9. However, since circuits in SoCs often operate under low-voltage conditions, the reduction in available voltage headroom caused by the dc current flowing

through this resistor, and the resultant voltage drop, would severely limit its size, pushing the pole to very high frequencies.

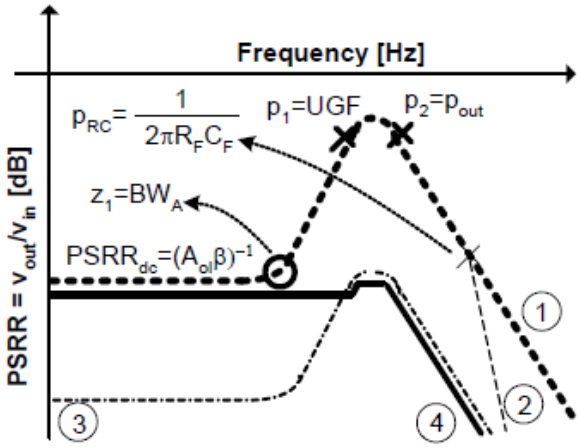

Fig 5.9 Frequency versus PSRR based on Transfer function

1	Conventional Band gap reference
2	With RC Filter on the Supply
3	With pre-regulation
4	Cascode topology with regulation and RC filter

A pre-regulator establishes a ‘pseudo-supply’ for the bandgap reference by forcing a bias current into a small resistance, as shown in Fig. 5.10. This technique improves PSRR performance by increasing the resistance between the input supply and the supply of the reference. While this is a compact and effective technique for achieving

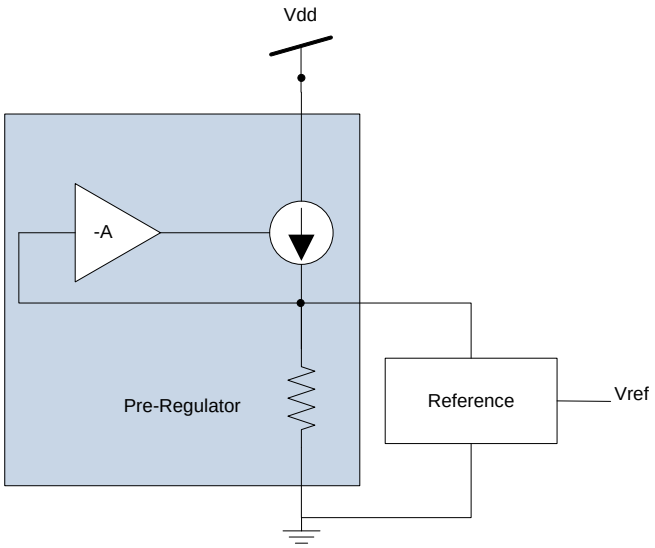

Fig 5.10 – Reference generator with Pre-regulation

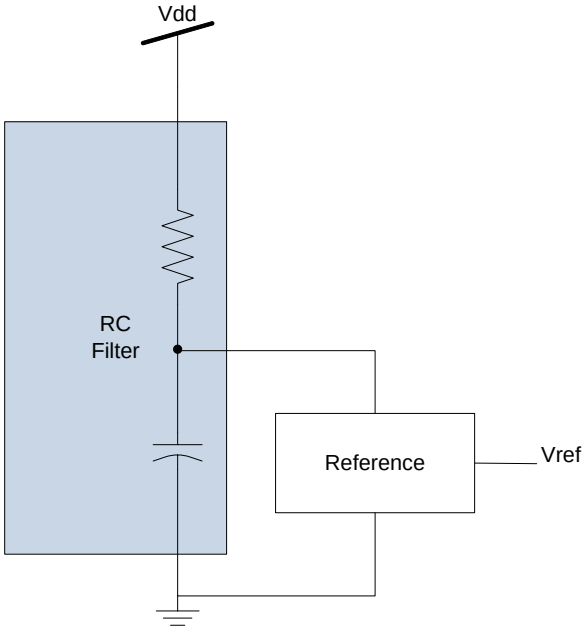

Fig 5.11 – Reference generator with RC filter on the supply

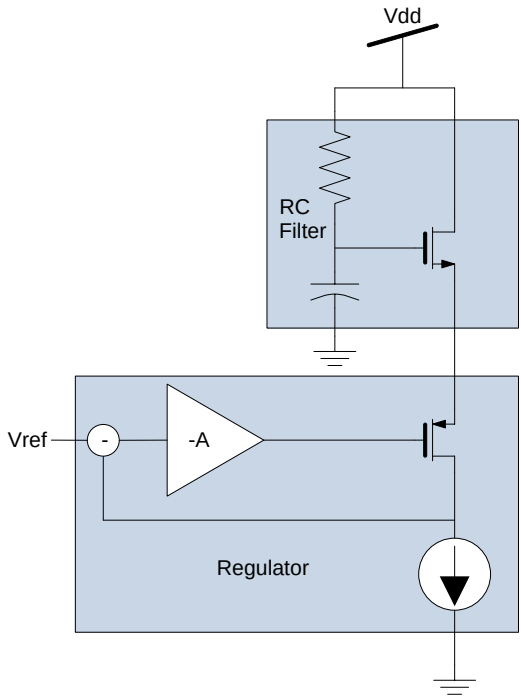

Fig 5.12 – Reference generator with RC filter and Cascode based regulation for high PSRR

high PSRR performance, it has an important drawback: references in SoC solutions need to supply large transient currents to suppress load noise but pre-regulators are limited by their quiescent current in their current sourcing capability. Though this drawback is eliminated by controlling the current source through shunt feedback (as in a linear regulator), the solution proves ineffective to improve PSRR at high frequencies given that the feedback loop of pre-regulator has the same bandwidth limitations as that of the bandgap reference. Another technique to suppress the effect of line fluctuations on the accuracy of the reference voltage, and hence improve PSRR performance, is to use NMOS devices to isolate circuits from the power-supply. In [29], a PSRR of -40 dB over a wide frequency range is achieved using an NMOS device to cascode the PMOS pass device of a Miller-compensated linear regulator, as shown in Fig. 5.12. Due to relatively high voltage headroom (1.8V) the gate of the NMOS cascode is biased through the

supply using a simple RC filter. The high voltage headroom also allows the error amplifier, which is powered directly from the supply (versus through a cascode), to use internal cascodes and gain boosting to improve its PSRR performance, leading to higher dropout and power consumption. Moreover, the circuit uses 1.2nF of on-chip decoupling capacitance that occupies an area that is prohibitively large for many VLSI SoC systems.

Summary

The performance summary of the BGR is summarized in the Table 5.1. Fig. 5.13 shows the variation of output voltage and output current with temperature. The current and voltage curve has a trendline to approximate to a second order polynomial behavior.

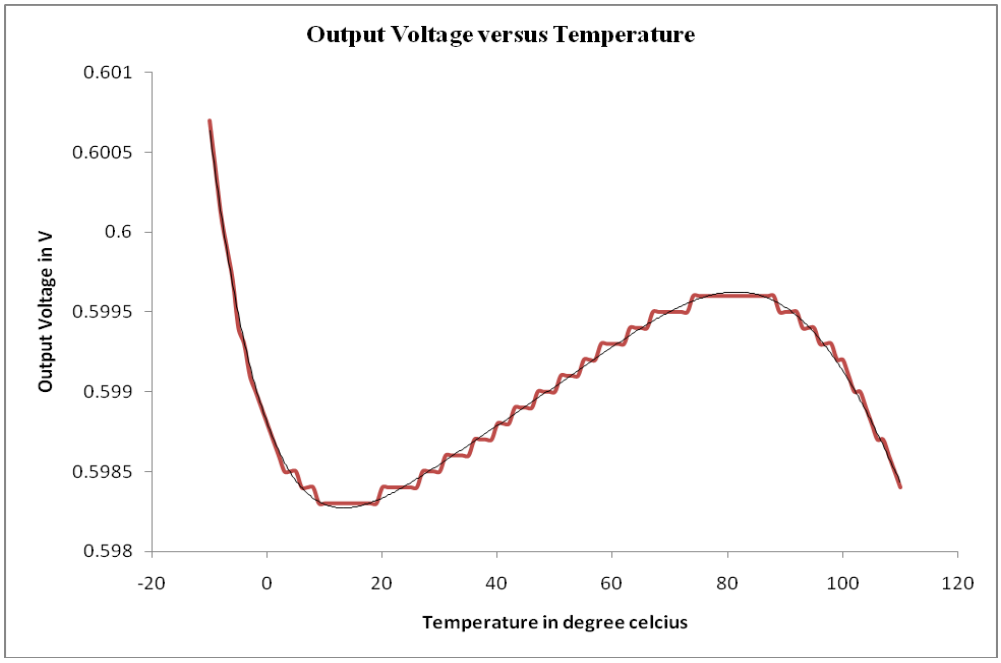

Fig 5.13 – Variation of Output Voltage versus Temperature

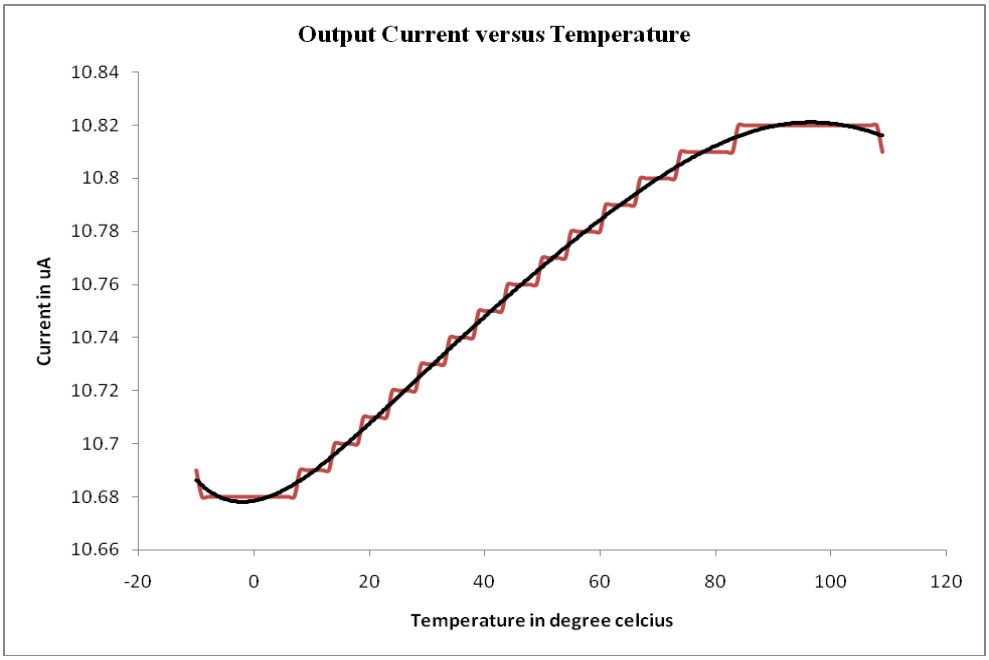

Fig 5.14 – Variation of Output Current versus Temperature

Since this circuit was designed with ON / OFF switching capability, study of the time required for the BGR to reach the steady state value is given in Fig 5.15.

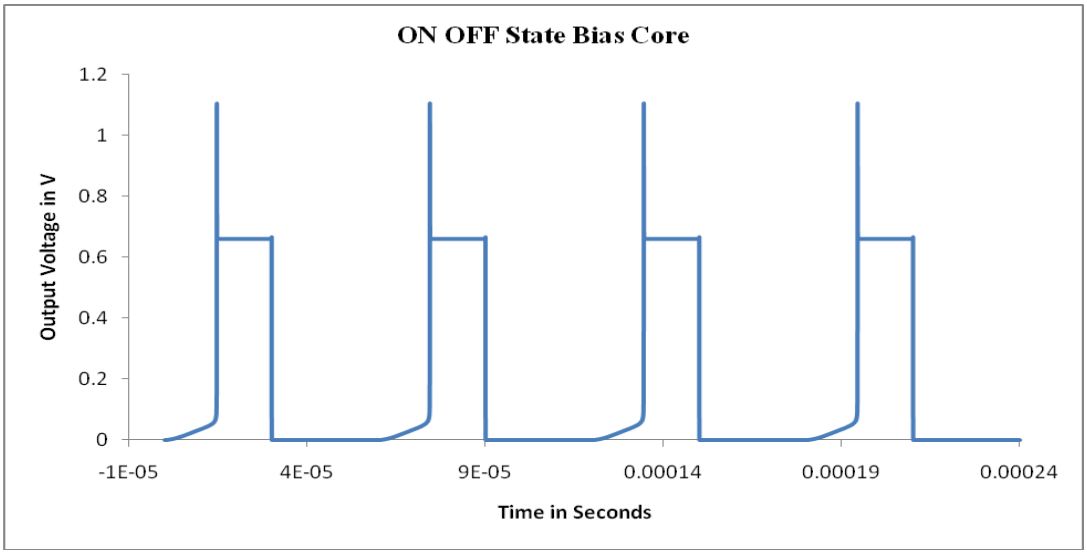

Fig 5.15 – The ON / OFF control for the core takes about 15 us to reach a 10% margin around the Output voltage of 600 mV.

The PSRR performance of the circuit is in accordance with the discussion from the section on PSSR as illustrated in Fig 5.16.

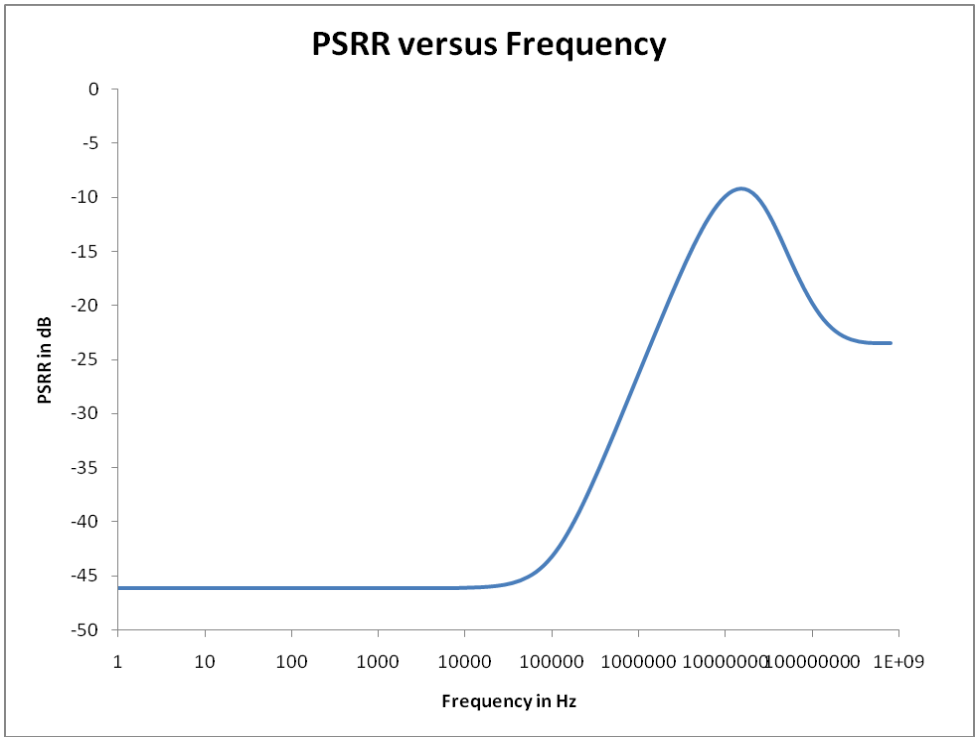

Fig 5.16 – PSRR versus frequency characterestics of the bandgap reference circuit

The output voltage regulation against changes in power supply is given in Fig 5.17.

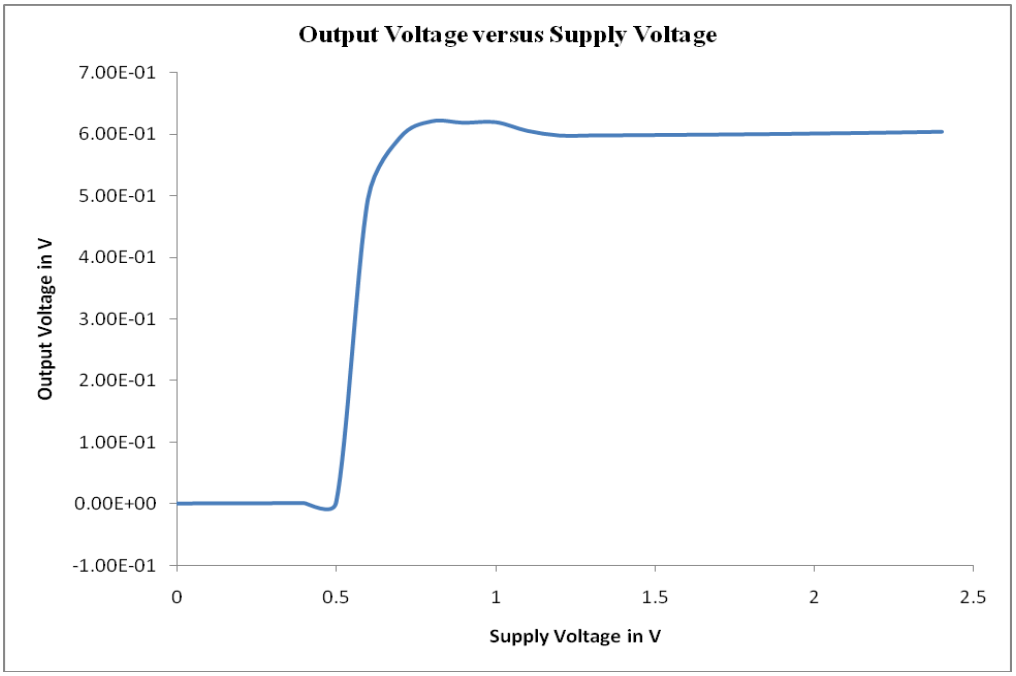

Fig 5.17 – Regulation of Output voltage for varying Supply Voltage.

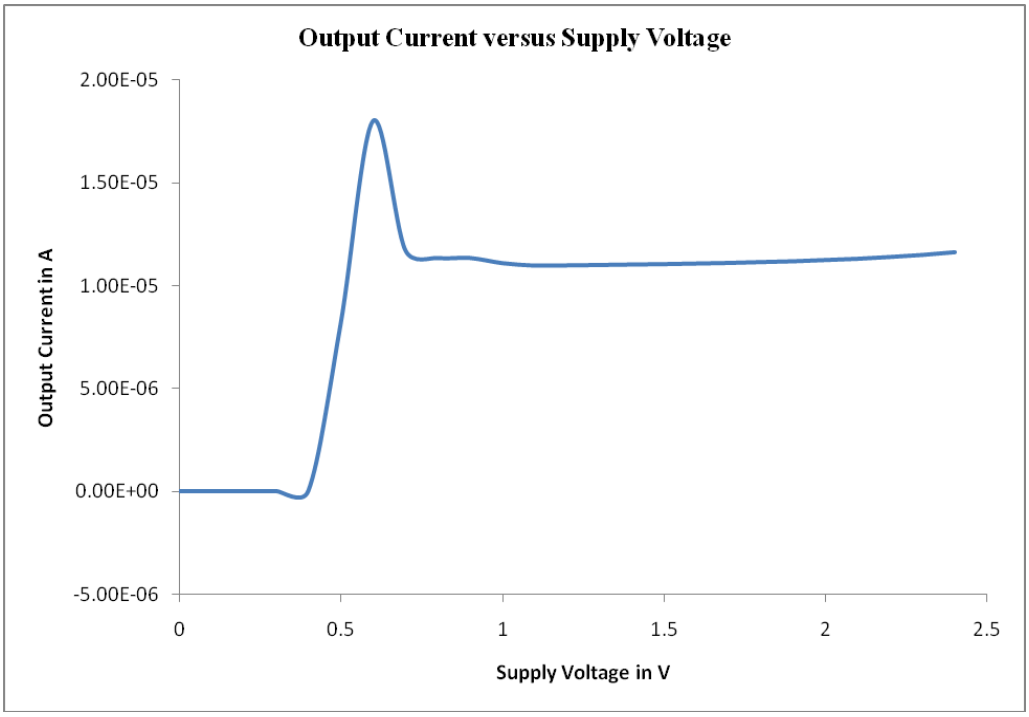

Fig 5.18 – Regulation of Output current for varying supplying voltage.

Table 5.1 – Performance Summary of the Bandgap reference circuit

Parameter	Values
Supply Voltage	1.2 V
Current consumption	80 uA
Output Voltage	600 mV
Output Current	10.69 uA

Studying the various sources of error that degrade the accuracy of the band gap reference is crucial to understanding their diverse characteristics with the ultimate goal of minimizing the detrimental effects. The bandgap reference is generally used to constant bias voltage along with a comparable current source. The current source performance is generally not very close to any other specific current bias circuits, but the possibility of generating current bias from the same bandgap reference can come as an advantage when space constraint is an issue. In modern system on chip solutions the area is always a constraint and hence proper understanding of error sources and power supply rejection is crucial to evaluate whether a first order or second order curvature compensated bandgap reference. Though most applications would prefer to have second order bandgap reference because of its accuracy, it's generally not the case. The idea of having a sub threshold operation for mos devices in second order reference circuits is considered risky, since the whole chip wouldn't perform if the reference circuits are unable to function. Hence most of the RF systems go with a first order bandgap reference in a short channel design.

CHAPTER 6

UPCONVERSION MIXER

Mixers are key components in both receivers and transmitters. Mixers translate signals from one frequency band to another. The output of the mixer consists of multiple images of the mixers input signal where each image is shifted up or down by multiples of the local oscillator (LO) frequency. The most important mixer output signals are usually the signals translated up and down by one LO frequency.

In an ideal situation, the mixer output would be an exact replica of the input signal. In reality mixer output is distorted due to non-linearity in the mixer. In addition, the mixer components and a non-ideal LO signal introduce more noise to the output. Bad design might also cause leakage effects, complicating the design of the complete system. Noise performance and rejection of out-of-band interferers are both critical to the receiver system because they both limit the receiver system's sensitivity. Linearity is important to transmitter performance, where you want an error-free output signal.

Conventional Mixer Design

Devices that exhibit nonlinear or rectifying characterestics are good candidates for designing mixers. Any device used as mixer must have strong non-linearity, low noise, low distortion and good frequency response in the region of interest. The simple nonlinear device for this purpose is a Schottky barrier diode. At microwave frequencies junction diodes are unsuitable because of their poor frequency response. FET is extensively used in mixer design due to their excellent frequency response, low noise properties and the ease of incorporation in radio frequency integrated circuits. Mixers can

be classified as active or passive mixers. Active mixers generally have the conversion gain, whereas passive mixers have conversion loss. Diode mixers are passive mixers, whereas the FET mixers are active mixers since they have potential for achieving conversion gain.

There are several system aspects to be considered while designing a mixer. The mixer conversion gain, G is one of the most important parameters. It characterizes the efficiency at which the input RF signal is converted to the desired IF frequency. It is defined as the ratio of power delivered to the load at IF frequency to the power available at RF frequency.

$$G_C = \frac{P_{IF}}{P_{RF}} \tag{6.10}$$

In an up conversion mixer P_{IF} is the input signal while P_{RF} is the output signal. The conversion gain increases with increase in LO power, until LO power reaches a level that saturates the mixer. Active mixers tend to have conversion gain and the various noise sources that affect FET are from the source, drain and gate resistances. Also traps in the semiconductor material and shot noise due to carrier transport contribute to additional noise in mixer design. A general expression for noise figure can be given as

$$NF = \frac{N_{OUT}}{GN_{IN}} \tag{6.11}$$

Where N_{OUT} the output noise power is N_{IN} is the input noise power and G is the conversion gain. Noise figure definition for a mixer is slightly complicated compared to standard definition because of the contribution by image components. For an upconversion mixer image frequency problem is more relevant since the image is very close to the LO frequency on the higher or lower side. In a simple definition, the frequency conversion from IF to RF along with image components is given by

$$N_{OUT} = Gk(T_O + T_{SSB})B$$
$$N_{IN} = kT_O B \tag{6.12}$$
$$NF_{SSB_1} = (T_O + T_{SSB})/T_O$$

Where k is the boltzman constant, B is the bandwidth, T_O is the IF source temperature, T_{SSB} is the single sideband mixer noise temperature that characterizes noise added by the mixer when converting from IF to RF. The first sideband expression is given in Eqn. 6.12. The double side band noise figure for the upconversion mixer is given by

$$NF_{DSB} = \frac{2T_O + T_{SSB}}{2T_O} \tag{6.13}$$

Diode conversion mixers have conversion loss and this leads to higher system noise, while active mixers have conversion gain and its noise figure cannot be easily related to conversion loss. The bandwidth of the passive mixer is determined by the hybrids and baluns used to couple the IF and LO signal through the diodes where as the active mixer have the device or external circuits which define their bandwidth.

Like other non-resistive networks, a mixer is amplitude-nonlinear above a certain input level resulting in a gain compression characteristic as shown in Fig. 6.1. Above this point the If fails to track the RF input power level – normally a 1dB rise in RF power will result in a 1dB rise in the IF power level. The 1dB compression point is measured by plotting incident RF power against IF power as shown in the Fig. 6.1. Most mixers have the 1dB compression point specified at the input ie the single-tone input signal level at which the output of the mixer has fallen 1dB below the expected output level. For typical double balanced mixers this figure is ~ 6dB below the LO power level. (So performance can be improved by overdriving the LO port).

The 1dB compression point gives rise to the dynamic range of the mixer, which is the difference between the 1dB compression point and the minimum discernable signal

(MDS – this is dependant on the noise floor of the device). These parameters define how much signal leakage will occur between pairs of ports (ie) RF to LO, LO to IF and RF to IF. So if for example RF to IF isolation was specified at 35dB this means that the RF at the IF port will be 35dB lower than the RF applied to RF port.

Intermodulation distortion (IM3) parameter is the same as specified for amplifiers and measured in a similar way. It is measured by applying two closely spaced input tones at frequencies F1 and F2. Third order products from the mixing of these tones with the LO (at frequency FLO) occur at frequencies given by: (2F1±F2) ±FLO and (2F2±F1) ±FLO. In the case of the mixer, the third order products of most interest are (2F1-F2)-FLO and (2F2-F1)-FLO as they fall in, or close to the IF band.

The IM3 performance is often summarised by giving the 3^{rd} Order Intercept point (IM3 Intercept) as shown in the compression characteristic of Fig. 6.2, where the IM3, IM5 plots intersect with the extrapolated gain plot (blue dotted line). As a rule of thumb the IM3 intercept point is approximately 10dB above the 1dB compression point. This figure of merit gives an indication of the mixer's signal handling capability. In particular it provides an indication of the levels of third order products a mixer is likely to produce under multi-tone excitation. The IM3 and IM5 graphs will intercept the fundamental graph at the intercept point. (Note the IM2 intercept point will be different and usually a lot higher). Again, for mixers the measurement is referred to the input ($IP_{3,in}$) and is given by:

$$IP_{n,IN} = \frac{IMR}{(n-1)} + \text{Input power (dBm)} \qquad (6.14)$$

Where IMR = Intermodulation ratio (The difference in dB between the desired output and spurious signal) and n = the IM order. Typically, for double balanced mixers $IM_{3,in}$ is ~

14dB greater than the single tone 1dB compression point and ~ 8dB greater than the LO power.

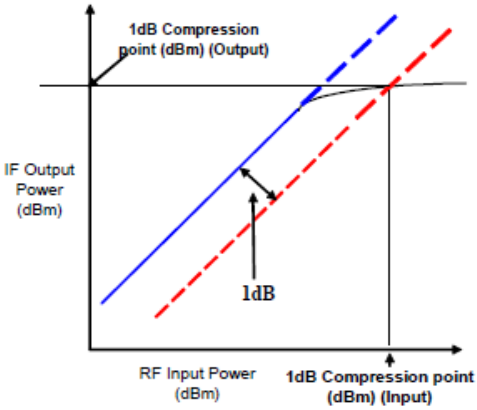

Fig 6.1 Gain compression curve

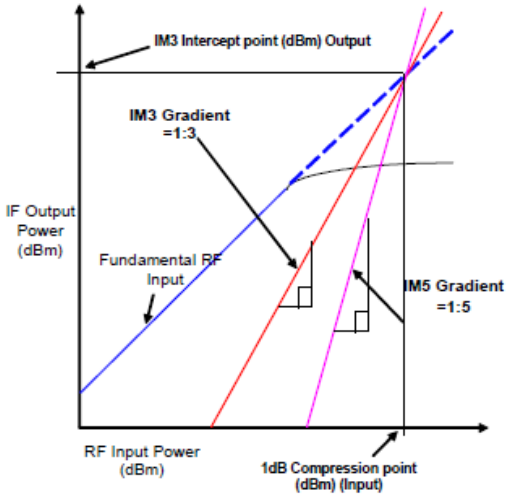

Fig 6.2 IM3 & IM5 characterestics of Mixer

Gilbert Cell Mixer

There are two types of mixers, passive and active. Generally passive types (although have better IM3 performance) have higher conversion losses and hence higher noise figures than active mixers. Additionally, there are single balanced mixers and double balanced mixers. Single balanced mixers are much less complex, but have inferior performance in terms of RF to IF and LO to IF rejection, compared to double balanced mixers. The advantages of a double balanced Gilbert cell mixer are as follows:

a) Both LO and RF are balanced, providing both LO and RF Rejection at the IF output.
b) All ports of the mixer are inherently isolated from each other.
c) Increased linearity compared to singly balanced.
d) Improved suppression of spurious products (all even order products of the LO and/or the RF are suppressed).
e) High intercept points.
f) Less susceptable to supply voltage noise due to differential topography.
g) Ideally doesn't have an LO component at the output.

The disadvantages associated with the Gilbert cell mixer are as follows:

a) Require a higher LO drive level.
b) Require two baluns (although mixer will usually be connected to differential amplifiers).
c) Ports highly sensitive to reactive terminations.
d) A small phase mismatch between the LO+ and LO- leads to significant local oscillator leakage.

The most popular active, double balanced mixer topography in RFIC design is the Gilbert Cell mixer, the circuit of which is shown in Fig. 6.2. This type of mixer exploits symmetry to remove the unwanted RF & LO output signals from the IF by cancellation.

The RF signal is applied to the transistors M2 & M3 which perform a voltage to current conversion. For correct operation these devices should not be driven into saturation and therefore, signals considerably less than the 1dB compression point should be used. Performance can be improved by adding degeneration resistors, on the source terminals of M2 & M3. FET's M4 to M7 form a multiplication function, multiplying the linear RF signal current from M2 and M3 with the LO signal applied across M4 to M7 which provide the switching function. M2 and M3 provide positive and negative RF current and M4 & M7 switch between them to provide the RF signal or the inverted RF signal to the left hand load. M5 & M7 switch between them for the right hand load. The two load resistors form a current to voltage transformation giving differential output IF signals. This is the operation of a down conversion mixer, for an upconversion mixer the RF and IF signal should be interchanged.

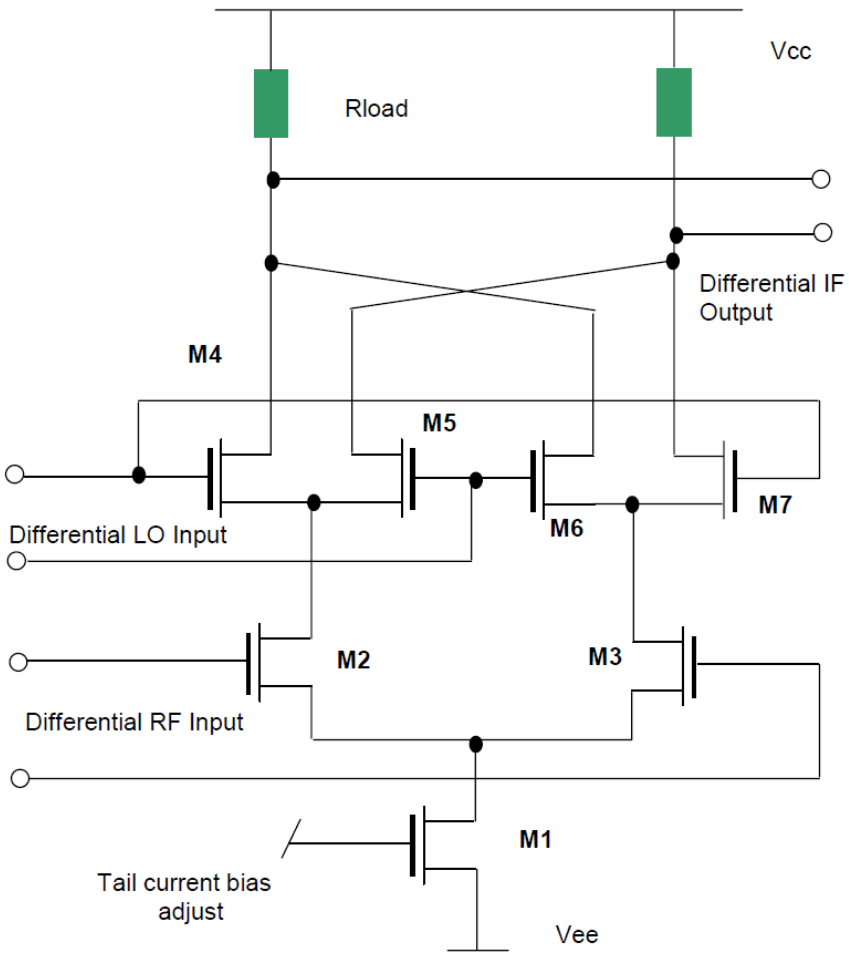

Fig. 6.3 - Basic Double balanced Down Conversion Gilbert Cell Mixer.

The up conversion mixer presented here is an improved version which offers high linearity, low noise and moderate image rejection. The mixer schematic can be split into three parts standard gilbert cell, tank circuit and current steering resistors. The three parts have three important functions which is necessary to reach certain target parameters. The Fig. 6.4 shows the schematic of the modified up conversion mixer.

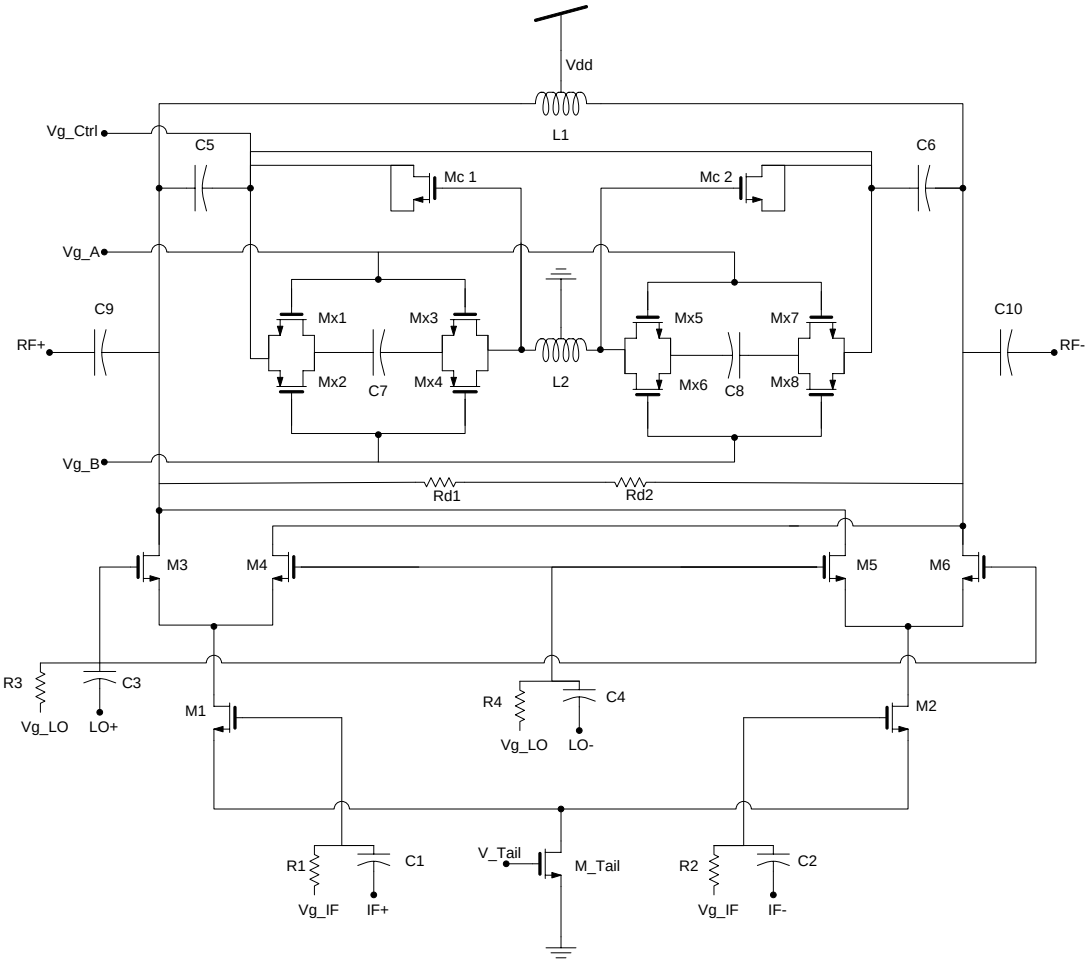

Fig. 6.4 - Modified Upconversion Mixer

The transconductance stage consists of M1 and M2. These devices are sized appropriately to obtain a conversion loss of 7 dB. The transconductance stage must be sized for linearity, gain and noise performance. A MOS driver largely eliminates linearity limitations from the input stage, therefore sizing can be done just considering the noise and gain only. This process has been addressed in the literature for MOS devices at those frequencies [45]. In brief, the optimum sizing of the device is made for both power match and noise match considerations, while constraining the power consumption of the device. This method was originally devised for LNA, but it can be applied to Mixer and further linearization of the MOS stage is obviated by the characteristics of the subsequent stag.

These methods yield an approximate method for determining the optimum device width,

$$W_{opt} = \frac{3}{2}\frac{1}{\omega L C_{ox} R_S Q_{SP}} \tag{6.15}$$

Where Qsp is the parameter relating the ratio of the MOSFET noise parameters γ and δ. Typical values of Qsp are between 3.5 and 5.5 and depend largely on the drain-source voltage and hot carrier effects. Assuming a value of 4.5, an optimal device size of W = 72 um and L = 0.28 um was chosen. A device with width of 60 um was used to ensure their linearity headroom available. Such a choice wasn't available for reducing the noise performance. Hence in order to reduce the overall mixer noise, a concept of current steering was adopted. The resistors Rd1 and Rd2 are the current steering resistors. The transconductance stage requires substantial dc current flow to establish the necessary g_m, but the same current when it flows through the LO stage contributes to high noise figure because of drain current noise. In addition to that the value of the resistor was chosen to ensure maximum voltage headroom is available across the transconductance stage. The tank circuit for this mixer is designed to have a band pass response. The tank circuit contains a mos capacitor whose gate voltage is varied to vary the effective capacitance. This effectively covers the output band from 2.8 to 3.6 GHz. The differential inductor is used in tank circuit of the up conversion mixer. This serves multiple purposes like being an element of a resonating circuit as well as effectively coupling the Vdd and Gnd connections to the circuit. This specific inductor has higher Q factor, layout symmetry and compact area, which is essential for miniaturized solution in commercial wireless applications. They are also superior compared to single ended counterparts due to their enhanced noise performance. A differential inductor structure consists of two single ended inductors. It is interesting to note that although the structure is differential; the excitation is single ended when applied to the structure. AC currents at the input and output ports flow in the opposite directions and, hence, some physical separation is

needed between the two single ended structures to limit the mutual inductance. Fig. 6.5 illustrates a fully symmetric differential inductor structure with differential excitation. This structure can be developed from our earlier understanding of microstripline segmentation of a spiral structure. This is accomplished by joining groups of coupled microstrips from one side of the axis of symmetry to the other using a number of cross-over and cross-under connections. Initially proposed by Rabjohn [43], this structure uses both electrical and geometrical symmetry, and uses the same area as two separate single-ended inductors. The common node of the structure can be utilized as a common mode biasing point for interfacing with circuits and significant advantage in terms of space reduction as compared to two single-ended asymmetric inductor structures. The two differential ports are at the same side of the inductor structure, thus aiding integration and layout compaction while designing with active circuits.

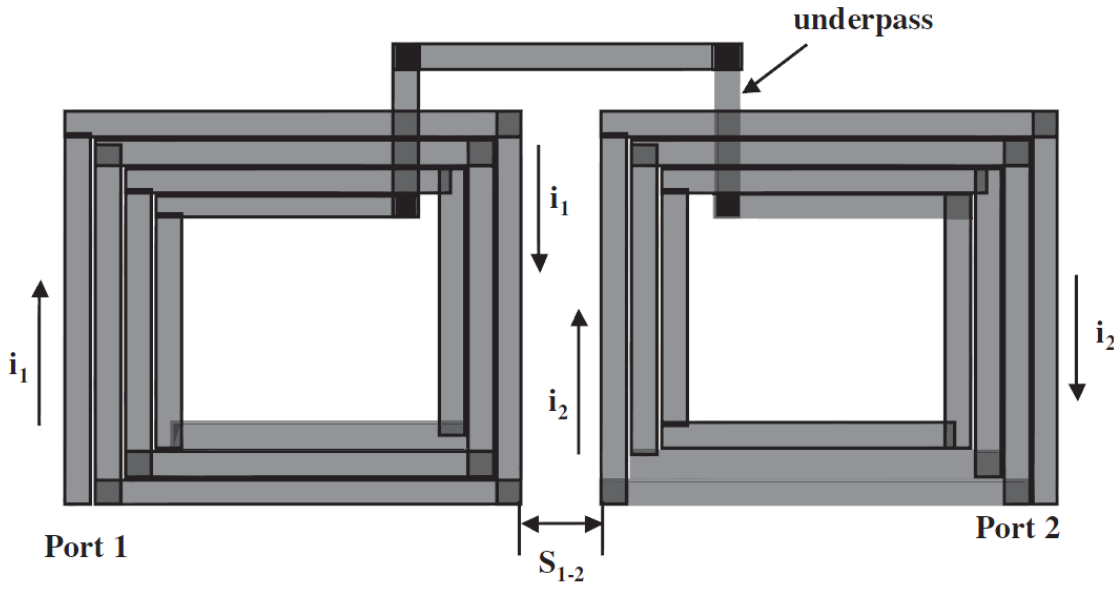

Fig 6.5 – Two single ended inductors connected in differential fashion

The differential inductor structure achieves higher *Q* than its single-ended counterpart. Two different lumped-element network models are shown in Fig.6.5 to illustrate the improvements in the case of differential excitation. *Z*L denotes the

impedance corresponding to the inductance and series resistance (L and r). ZP denotes an equivalent shunt-parasitic R–C network that provides the same impedance as substrate-parasitic

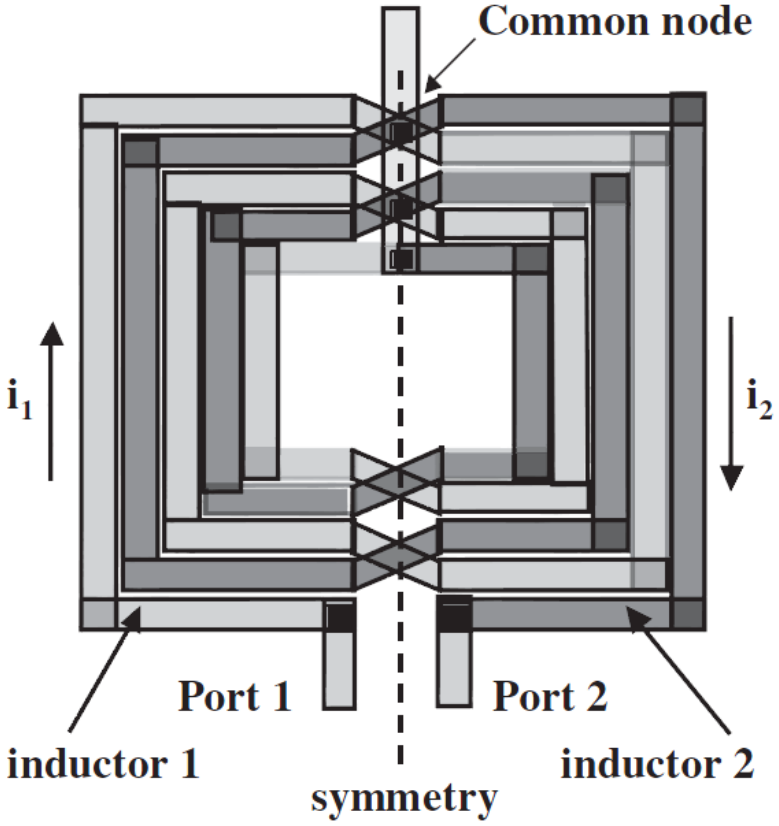

Fig 6.6 – Symmetric differential inductor with two ports

elements Cox, Csi, and Rsi at a given frequency. For a single-ended excitation, the input signal is applied across the inductor as a one-port structure, and the input impedance Zse is denoted by the parallel combination of the branch impedances (ZL and ZP). For differential excitation, signal is applied between the two ports, and the differential input impedance is represented by a parallel combination of ZL and 2ZP. Higher equivalent shunt impedance is obtained in case of differential excitation, and Zd approaches to ZL over a wider range of frequency than Zse. At lower frequencies, the input impedance in either shunt or the differential connections is almost the same, but at higher frequencies,

the substrate parasitic (*C*P and *R*P) contribute to the impedance expressions. In the case of differential excitation, the impedance presented by these parasitics is higher compared to the single-ended counterpart at a given frequency. Thus, the real part of the input impedance is reduced and the reactive part is increased, leading to an improvement in *Q*

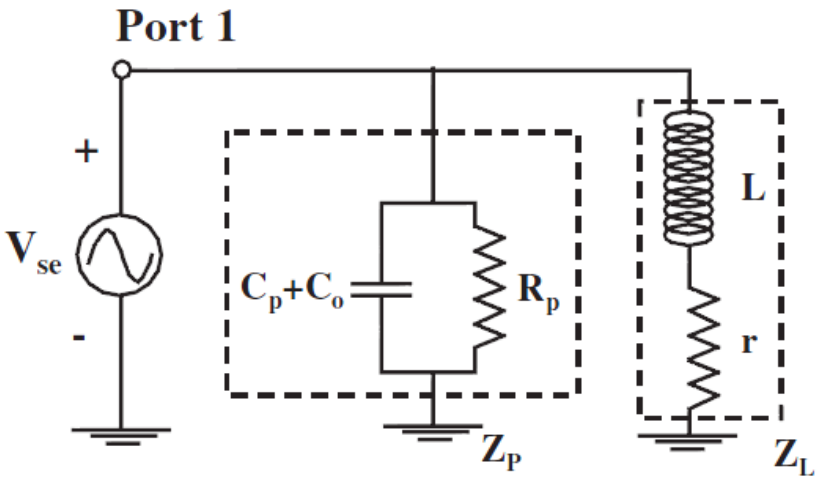

Fig 6.7 – Q illustration with single ended excitation

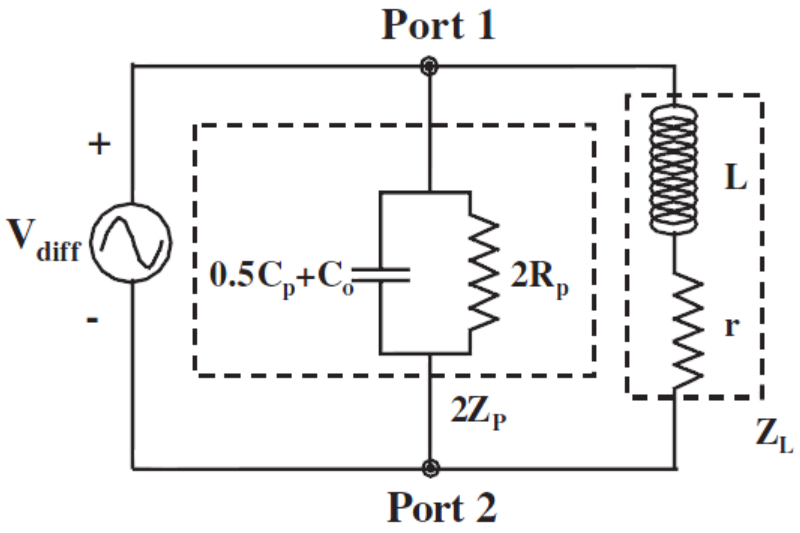

Fig 6.8 – Q illustration with differential excitation

value. The SRF also increases due to the effective reduction of parasitic capacitance from *C*P + *C*o to *C*P/2 + *C*o. The ratio of differential *Q* to single-ended *Q* is given by

$$\frac{Q_d}{Q_{sc}} = \frac{2R_p \parallel R_L}{R_p \parallel R_L} \tag{6.16}$$

$$R_L = r(1+Q^2) \tag{6.17}$$

$$Q_L = \frac{\omega L}{r} \tag{6.18}$$

At low frequency ranges, *R*P _ *R*L, leading to *Q*d _ *Q*L. *Q*L dominates in both the cases, and the *Q* factor increases with an increase in frequency. At higher frequencies, *R*L increases while *R*P decreases, leading to an effective increase in *Q* factor in case of differentially excited structures. From Eqn. 6.18, it is seen that the *Q* factor improvement in the case of differentially driven structures is about twice that of the single-ended structures. This improvement can also be observed in the case of other passive structures such as couplers, hybrids, and transformers.

Linearity

An active mixer topology is comprised of three stages, a reasonable approach is to consider each stage stage separately and determine the compression/modulation performance of each stage, and by combinig the non-linear contributions of each stage the overall linearity metric of the Mixer can be determined. An intuitive estimate of the sources of linearity will reveal that all non-linearity in the signal path is determined primarily by the input stage device.

Assuming a static non-linearity and expanding a Taylor series, estimates of input 1dB compression power and 3rd order intermodulation intercept power can be given as:

$$A_{-1dB} = \sqrt{0.145\frac{\alpha_1}{\alpha_3}} \tag{6.19}$$

$$IM3_A = \frac{3}{4}\frac{\alpha_3}{\alpha_1}V_{peak}^2 \tag{6.20}$$

Having ignored the non-linearity from the other sections of the circuit these calculated values can be used as an upper bound on the linearity performance of the mixer. This approach can be complicated by the presence of frequency dependent degeneration in many input stages. Large signal effects such as 1dB compression are often not simply the result of third order non-linearity. For this reason our initial approach will focus on the third-order intermodulation effects.

Far from completely estimating the lineariy of an RF stage, the approaches reviewed here are for single common source device. Additional elements in the circuit like impedance matching and parasitic must be taken into account when signal amplitude is to be determined at this node. If the real part of the input impedance is matched to the source impedance, the Input P1dB and IIP3 is given by Eqn 6.19 and 6.20.

MOSFET's operating in saturation region follow the square law relationship. But there is a need to augment the square law relationship with short channel effects like velocity saturation. It can be caused due to strong lateral field or mobility degradation due to strong normal field. Carriers in the short channel MOSFET experience very strong horizontal fields even under a moderate drain-source bias level. Under these conditions, the drift velocity of mobile carriers in the inverted channel approaches a limit. This effect is increasingly important in RF design due to interest in very short channel devices for high-speed performance. Writing velocity saturation in terms of mobility and accounting for changes in mobility, yielding

$$i_{DS} = \frac{W}{L}\frac{\mu_{eff} C_{ox}}{2L}\frac{V_{od}^2}{(V_{od}/E_{crit}L)+1} \tag{6.21}$$

The $i_{DS} - V_{od}$ relationship more closely resembles a linear function of input voltage as V_{od} becomes large relative to $E_{crit}L$ with the assumption that carrier mobility is constant.

Another interpretation notes that as gate length decreases, the drain current function becomes increasingly linear in V_{GS}. By accounting for mobility changes in the channel, we can obtain a more complete model for the non-linear behavior of the field effect device at low frequencies.

However carrier mobility doesn't remain constant under all conditions. The surface of the semiconductor under the gate has a strong vertical field as well as other terminals in the device cause surface scattering of carriers as they transit the channel region. An accurate model of the mobility variation models the electric field due to these vertical fields in and below the inversion layer which when combines with velocity saturation effect can be given as

$$i_{DS,vel-sat}(V_{od}) = \frac{W}{L}\frac{\mu C_{ox}}{2}\frac{V_{od}^2}{(1+\theta V_{od})(1+\frac{V_{od}}{E_{crit}})} \tag{6.22}$$

There parameter theta is the channel mobility degradation constant. Transconductance can be obtained from the Eqn. 6.23.

$$g_m = \frac{\delta I_{ds}}{\delta V_{gs}} = \frac{2I_{ds}}{V_{od}} - \frac{I_{ds}(2\frac{\theta V_{od}}{E_{crit}L} + \frac{1}{E_{crit}L} + \theta)}{(1+\theta V_{od})(1+\frac{V_{od}}{E_{crit}L})} \tag{6.23}$$

The first term can be thought of as the transconductance under long-channel conditions. However the transconductance is not a simple square-root function of the drain current. It is proportional to the drain current and this causes the transconductance to decrease as θ gets larger or L gets smaller. Clearly as shrinking device geometries push the operation into new regimes, MOSFET current and voltage characteristics become increasingly linear.

Taylor series expansion of i_{DS}, when computed around a suitable bias point, it is a simple matter to then compute input linearity metrics. For a MOS driver, lacking any degeneration the expansion of i_{DS} around an arbitrary bias points to obtain the first, second and third order coefficients α_1, α_2 and α_3. These are not included here due to complexity. Both the output compression and third-order intermodulation characteristics are proportional to α_3/α_1. For strong inversion and saturation conditions this term is given as

$$\frac{\alpha_3}{\alpha_1} \simeq -\frac{3}{8}\frac{E_{crit}L}{V_{od}}\frac{(E_{crit}L - V_{od}^2\theta)(4V_{od}\theta + \theta E_{crit}L + 1)}{(V_{od} + 2E_{crit}L)(V_{od} + E_{crit}L)^2(V_{od}\theta + 1)^2} \tag{6.24}$$

Two special cases are worth discussing to gather insight into the Eqn. 6.25. First, for the devices with thick gate oxide, theta approaches zero. In this case

$$\frac{\alpha_3}{\alpha_1} \simeq -\frac{3}{8}\frac{E_{crit}^2L^2}{V_{od}(V_{od} + 2E_{crit}L)(V_{od} + E_{crit}L)^2} \tag{6.25}$$

Where it is clear, that increasing the gate-drive improves linearity. Second, long channel devices exhibit little velocity saturation behavior and consequently when $E_{crit}L >> V_{od}$ where

$$\frac{\alpha_3}{\alpha_1} \simeq -\frac{3}{8}\frac{\theta}{V_{od}\theta + 1} \tag{6.26}$$

In the second case, the third order intermodulation will approach zero when θ approaches zero. This makes sense because it corresponds to the case for ideal MOSFETs, where the drain current is a function of square of V_{od} only. Although significant second-order distortion may result, no third order distortion can occur as the drain current versus gate source voltage characteristic is perfectly quadratic. However in practice all devices will experience mobility degradation and short channel effects leading to significant third order distortion. θ in thin oxide devices decreases, leaving both the second and third order effects reduces substantially. Most importantly, the

intermodulation decreases linearly with the gate control voltage ($V_{gs} - V_{T_0}$), implying that greater current bias, or smaller device width, would improve linearity. To obtain the linearity performance, harmonic balance simulations were performed by applying two closely spaced input tones. From the spectral content, third order intermodulation performance has been estimated.

Noise

Calculating noise in nonlinear circuit is a non-trivial problem. Noise sources are usually assumed to be stationary in linear circuits, but they should be evaluated in a circuit which changes periodically with time to simulate the effect of noise on a mixer. The resulting noise process is termed as cyclostationary. The special case of non-stationary noise is encountered in many applications from A/D converters, switched capacitor filters and RF mixers.

The mixer is an inherently periodic and time-varying network, where the dominant noise sources are switched to and fro by local oscillator. Due to the non-linear three port nature of Gilbert cell mixer, noise calculations require a non-linear summation of noise from the RF and LO ports to compute the noise power at the IF. Unlike linear circuits like LNA, where small signal techniques can be applied, a systematic means of computing the noise for frequency conversion mixer is necessary. Recent work has highlighted a simulation assisted method for these calculations without resorting to harmonic balance techniques.

The first step towards calculating the output noise under deterministic but time varying conditions, separate the operation of the circuit into time phases during which the different noise sources dominate. Combining the noise contributions in each of these

phases is done by computing the contribution of these sources to the total power spectral density of the output noise at IF frequency. Throughout these calculations, it's assumed that the output is always differential. Noise mixing in a single balanced design has multiple sources. The most relevant mechanisms for noise contribution are

a) When the switching devices are fully in the switched state, noise in the signal path, including the input stage noise, appears at the output as differential noise. The amount of time spent in the fully switched state is determined by the magnitude of the LO voltage waveform and in current commutating mixers, increases as a fraction of the total time as the LO amplitude is increased.
b) When the switching stage is in the process of changing switching states, noise form the input stage appears as common mode in the output currents contributing nothing to differential output current. The switch devices, on the other hand, are sharing the DC current and are contributing differential noise to the output. The duration of the period is similarly determined by the amplitude of the LO and decreases with stronger LO drive in the current commutating mixers.
c) Also noise in the LO signal can be significant during the switch phase. This can contribute to the output in a similar fashion to the noise from the switch devices.
d) The output I to V stage contributes differential noise at all times. Often this stage is implemented with a resistive load in which case it contributes thermal noise. More desirable is to implement this stage with a balun network, as is done by many receivers. Both on and off chip baluns can be designed. Ideally, these loads are comprised of an inductive and capacitive component only making them noiseless.

Starting from the Fig. 6.3, the systematic noise contributions arise when the circuit is in a fully switched state leading to noise contributions from both driver and switching stage. Differential output noise from the OFF device is assumed to be zero as there is no current. All the noise is contributed by the input driver and the cascaded device. Both of

these noise contributors are mixed to the output much like the input signal is mixed by the switch pair. That is, the noise in the bias current, I_{RF} along with the small signal current i_{rf} are mixed with LO frequency in this structure. Furthermore the cascaded device being turned on and off by the LO signal, noise is also turned on and off. Due to these mixing processes, noise present at image and harmonic images must be analyzed and mixed to the IF.

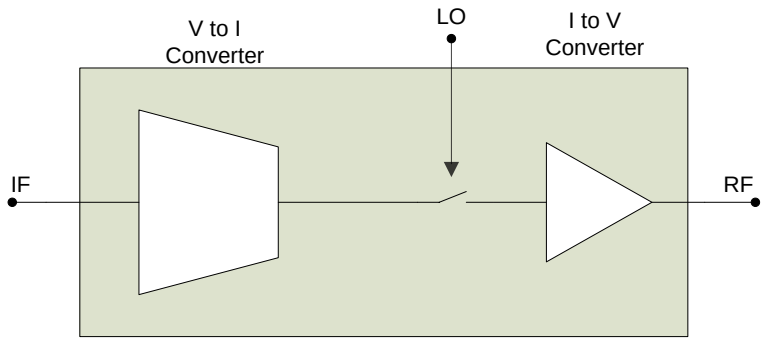

Fig. 6.9 - Block diagram of current commutating mixer illustrating all of its functional blocks. Small signal blocks include input and output amplifiers, whereas the non-linear section is represented by the simple ON-OFF switch. A more realistic model of the switch is needed to fully comprehend the LO dependent noise contributions from this stage. For a differential version replace the input and output lines with two each.

Computing noise from the phase is a simple matter of computing differential output noise current at the image and harmonic frequencies. By computing the gain due to the switching pair at each of these frequencies and then scaling the noise by these gain values, the noise at the IF frequency can be summed. In a well designed cascode structure, the upper device is well degenerated by the high output impedance of the lower device. In this switched state, however the driver device is degenerated by both the on and off devices. Calculating noise of the upper device now is a frequency dependent affair. If the frequency dependent degeneration is present in the driver, noise from the

input device may also be frequency dependent. Furthermore noise from the driver is shaped as is passed through the cascaded device.

Noise sources in the MOS driver stage can be summarized as follows. Only the gate current noise i_g^2 is frequency dependent,

$$i_g^2 = 4kT\delta\frac{\omega^2 C_{gs}^2}{5g_{do}}B \tag{6.27}$$

$$i_g^2 = 4kT\gamma g_{do}B \tag{6.28}$$

$$i_g^2 = 4kTr_gB \tag{6.29}$$

The parameter δ can take the value 4/3, in the long channel, to ~ 4 in short channel, while γ varies from 2/3, in long channel to ~ 2 in short channel. To produce a low noise device, layout of the gate polysilicon must be done carefully to avoid additional gate resistance r_g. Proper layout can all but eliminate this thermal noise term. Assuming source impedance of R_S, and no degeneration or noise correlation, the input referred voltage for a single common source device is

$$V_{nz,MOS}^2 = 4kT(R_S + r_g + \frac{\gamma}{g_{do}} + \frac{\omega^2 C_{gs}}{g_m}\delta R_S)B \tag{6.30}$$

Where g_{do} is the drain source conductance of the device when $V_{DS} = 0$. In long channel devices $g_{do} = g_m$, however in short channel devices, this is not the case and these must be computed separately.

The switching stage devices contribute shot noise and it appears the output from both ON and OFF devices in the process of switching states. Conceptually this is due to the differential ground which is established at the source of both devices in the forward

active region. As a consequence, the well degenerated conditions under the fully switched state no longer hold. The differential noise from these devices when

$$i_{out,nz}^2 = 2qI_{RF}B = kTg_mB \tag{6.31}$$

Eqn. 6.31 is valid only under the condition that the devices have appreciable small signal gain at the frequency of the LO, and can be applied to MOS or bipolar switching pairs. Since the noise source is linearly dependent on the current dissipation in the switches, one way to decrease the effect of this noise is to bias the switching pair with less current while maintaining the bias level in the driver pair of devices. To achieve this current steering resistor was used in the Gilbert cell mixer to reduce the overall noise figure.

Local oscillator signal offers both stationary and non-stationary sources of noise. The devices in switching stage are degenerated by the large drain-source impedance of the driver stage. When the device is not strongly switched, and the degenerating impedance is larger, noise from the base circuit will not be amplified. However during the switching event it will behave as a differential amplifier, providing gain for noise from the LO port.

Clearly, this noise contribution mechanism is similar to that of the switching devices shaped by the transconductance of the switching pair. When $v_{lo} = 0$, the differential noise current contributed by a series of LO source resistance, R_{LO}, to the output current of a differential pair is

$$i_{out,nz,LO}^2 = 4kTR_{LO}g_mB \tag{6.32}$$

In practical circuits this noise resistance doesn't just come from devices in the LO oscillator, but also from the thermal noise contributed by source resistance, as well as base or gate resistance in the switch pair devices. It is critical to note that the double balanced design doesn't have any noise contribution from source. Since the local

oscillator signal is cancelled at the outputs, it is clear that the noise from the LO port will also be cancelled. Device mismatch or uneven duty cycle in the LO signal; however will cause this assumption to be incorrect as LO signal will be present in RF port. Stating the differential noise contributions to $i_{out,nz}$ we can compute the overall noise figure for the mixer.

$$F_{mixer} = \frac{i_{out,nz,MIX} + i_{out,nz,SWITCH} + i_{out,nz,LO}}{G_{M_C}^2 4kTR_s} \tag{6.33}$$

Stronger switching and lowering the contributions from $i_{out,nz.SWITCH}$ and $i_{out,nz,LO}$ will maximizes the gain and minimizing noise figure. Local oscillator drive level can be made reasonably large by providing an LO buffer prior to driving these switches. In an all MOS mixer, the upper device must also be designed with the noise and gain considerations in mind. While the gate-resistance can be made very small, minimizing the contribution from this noise source, the drive voltage must be sufficiently large to switch the more linear MOS devices fully. For a MOS differential pair, the linear range is limited to

$$V_{ID} \le \sqrt{\frac{4I_{RF}}{\mu C_{ox} W/L}} = \sqrt{2}(V_{GS} - V_{TH}) \tag{6.34}$$

With an enormous device size, i.e W=240 um, L=0.28 um, and a bias current of 1mA this can be as small as 80 mV – still significantly larger than the switching range required in a MOS pair. This consideration can be mitigated by adding well designed LO buffers before applying LO signal to switching stage of the Gilbert cell mixer.

Performance Summary

The summary of the mixer performance is listed in the Table 6.1. The noise performance of the mixer was improved by adding current steering resistors, which reduced noise figure by 2 dB. The LO leakage to output port of mixer cannot be observed when the fully differential LO is perfectly in phase. Assuming a phase shift of 5 deg between the LO+ and LO- signals, the LO leakage at the output was estimated.

Table 6.1 – Performance Characteristics of the Mixer @ Input power = -15 dBm

Input	350 MHz	NA
LO	3.65 GHz	± 0.3 GHz
Output	3.3 GHz	± 0.3 GHz
Conversion Loss	9 dB	NA
OP1dB	0 dBm	NA
IP1dB	10 dBm	NA
IMD3	72 dBc	NA
NF	17 dB	NA
Image Rejection	10.02 dB	NA
1dB Bandwidth	315 MHz	± 10 MHz
3dB Bandwidth	615 MHz	± 10 MHz
Switch ON	3.0 -> 3.3 GHz	NA
Switch OFF	3.2 -> 3.6 GHz	NA

The mixer is designed to have a bandwidth of about 600 MHz. To cover the entire frequency band the tank circuit was tuned to cover the entire range with the help of a band switching network. When the switch is OFF it covers from 3 to 3.33 GHz and when it is ON it covers the band from 3.2 to 3.6 GHz.

Table 6.2 – Frequency Characteristics of the Mixer

Control Voltage	Switch State	Center Frequency	Image Frequency	Image Rejection
V		GHz	GHz	dBc
0.4	OFF	3	3.7	17.56
0.8	OFF	3.1	3.8	15.86
1.2	OFF	3.2	3.9	15.58
1.6	OFF	3.23	3.93	14.44
2	OFF	3.3	4	13.61
2.4	OFF	3.33	4.03	12.59
0.4	ON	3.2	3.9	15.81
0.8	ON	3.3	4	14.13
1.2	ON	3.4	4.1	13.84
1.6	ON	3.5	4.2	13.49
2	ON	3.55	4.25	12.61
2.4	ON	3.6	4.3	11.91

CHAPTER 7

3.5 GHZ TRANSMITTER DESIGN

The transmitter lineup here contains four components namely input buffer, upconversion mixer, filter and output buffer. The input buffer is designed to set the tone for high linearity and intermodulation performance for the lineup. The mixer discussed in Chapter 6 is used here. The filter is an active circuit where the number of stages is chosen to obtain a balance between image rejection and intermodulation performance. The output buffer is used to convert a differential to a single ended output.

Overall System

The transmitter lineup called as S Band transmitter was designed with certain specifications in mind. The 3.5 GHz transmitter acts as a feeder to a 6-40 GHz multiband transmitter, hence the crucial parameters like Linearity, Intermodulation performance and Noise Figure occupies primary importance. Secondary level emphasis is laid on LO leakage, Image rejection and 140 MHz IF leakage to the output. The system accepts a 350 MHz signal as input and generates a 3.5 GHz signal as output. In order to facilitate the conversion process, a 3.85 GHz local oscillator signal is used for the up conversion mixer. The receiver used in conjuction with this transmitter has an IF output of 140 MHz, which has a good chance of leaking into the transmitter and adding an unwanted frequency component in the output spectrum of the transmitter. The overall system is depicted in the Fig. 7.1. The highlighted region is the topic which is being discussed here in addition to which the constraints set by overall system design.

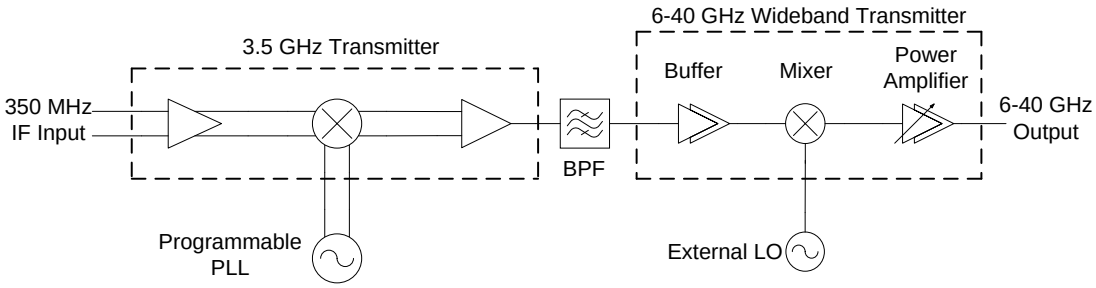

Fig 7.1 – 6-40 GHz Wideband Transmitter Lineup

Table 7.1 – CMOS Upconverter Summary

Parameter	Value	Notes
IF Input	[-30;0]dBm @ 350 MHz	100 Ohms Diff. Input
S Band Output	[-30;+5]dBm @ 3.5 GHz	50 Ohms Single Ended
Output P1dB	+ 5 dBm	-
Nominal Output Power @ 10 dB Backoff	- 5 dBm	-
S Band Upconverter Total Gain	[-5;+35] dB	-
LO Leakage at Output	< - 50 dBm	-
		-

Operating Conditions	Value	Notes
Min Temperature	-40 deg C	-
Max Temperature	+ 85 deg C	-
Bias	+ 5 dBm	-
Power Dissipation	- 5 dBm	-
Input Voltage ripple	50 mV pp	-

S Band Tx Output	Value	Notes
Output Impedance	50 Ohms	Single Ended
Return Loss	18 dB	-
RF Center Min	3.15 GHz	-
RF Center Max	3.51 GHz	-
Bandwidth	600 MHz	-
Output Power Min	-27 dBm	-
Output Power Max	+5 dBm	-
S Band – Total Gain	[-15;+35] dB	-
Linearity, Output power <= - 4 dBm	> 54 dBc	-
Linearity, Output power <= 0 dBm	> 47 dBc	-
Linearity, Output power > 0 dBm	> 39 dBc	-
Output Noise floor	< - 120 dBm/Hz	-

Input Buffer

The input buffer is a cascode differential amplifier. It consists of two pairs of differential pair which is switched for Low Gain and High Gain mode. The cascode device has two separate biasing inputs which is used to effective switch them between High gain and Low gain mode. To ensure gain control, a negative feedback loop was added to the differential pair which allows gain control in both high gain and low gain modes. The differential inductor and capacitors make the standard tank circuit which is tuned to a frequency of 350 MHz. The additional capacitor bank is for switching to another band thereby covering the entire input bandwidth.

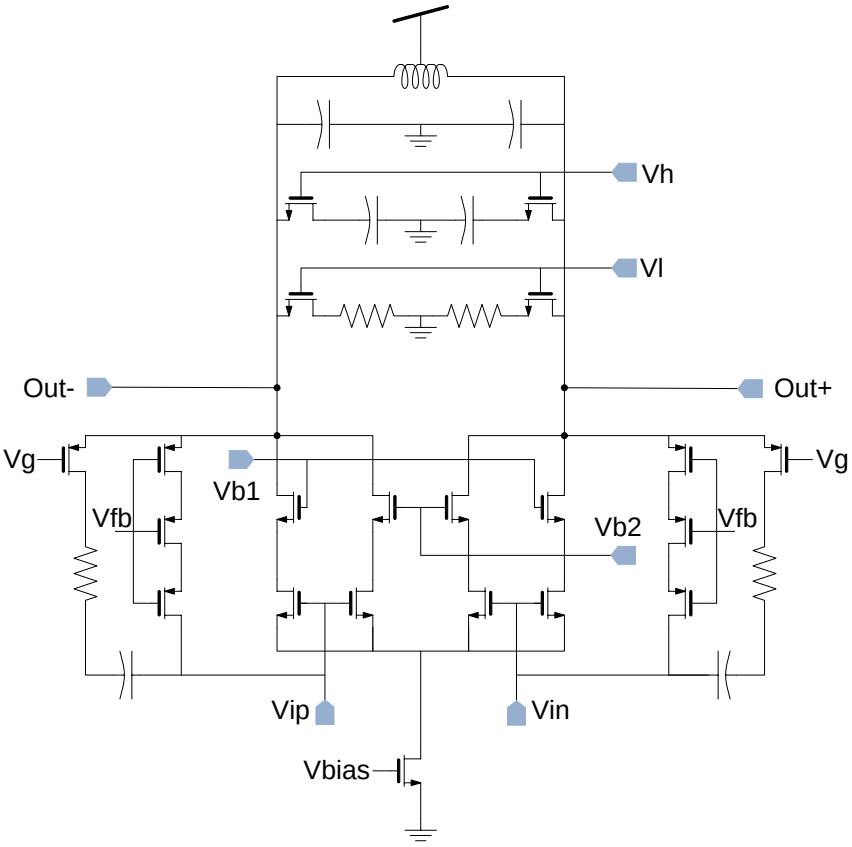

Fig 7.2 – Schematic of Input Buffer

Table 7.3 – Performance Summary of Input buffer

Parameters	Value
Input Power	-28 dBm
Gain	14 dB
Center Frequency	350 MHz
Bandwidth	180 MHz
Noise Figure	2.5 dB
Intermodulation IMD3	66 dBc
Output P1 dB	12 dBm

RF Filter

The RF Filter is an active filter where the gain is obtained cascode differential pair. The tank circuit is designed to obtain an image rejection of 8 dBc. This is a single cell and multiple stages of the same cell are used. The trade off in using multiple stages is reduction in linearity and intermodulation performance but gain in terms of imaga rejection and LO leakage reduction. The performance summary is given in Table 7.3

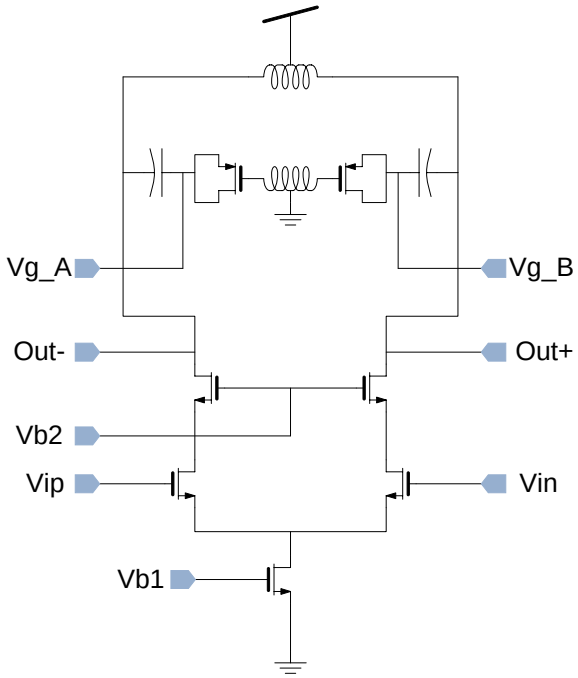

Fig 7.3 – Schematic of RF Filter

Table 7.3 – Performance Summary of RF Filter

Parameters	Value
Input Power	-23 dBm
Gain	6 to14 dB
Center Frequency	3.25 GHz
Bandwidth	612 MHz
Intermodulation IMD3	61 dBc
Output P1 dB	12 dBm

Output Buffer

The output buffer consists of a simple differential pair with current mirror load. This effective converts differential signal into a single ended signal. In order to select the 3.5 GHz signal, a tuning circuit in the form of R, L and MOS capacitor is employed. This is further amplifier with a common source amplifier to meet the output power requirements. In designing the buffer, a trade off is made between intermodulation performance and noise figure to obtain optimal performance.

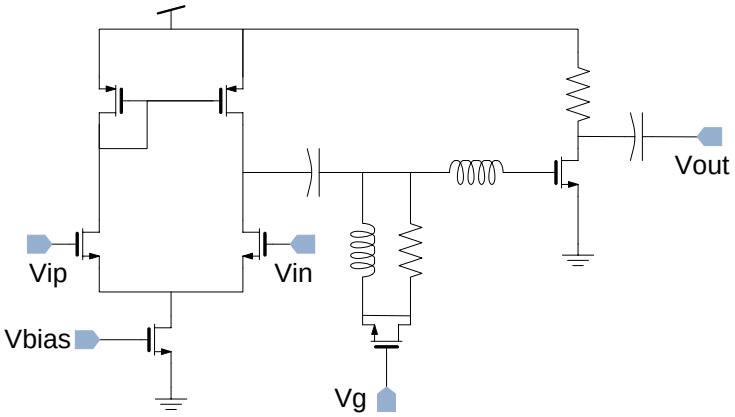

Fig 7.4 – Schematic of Output Buffer

Table 7.4 – Performance Summary of Output Buffer

Parameters	Value
Input Power	-17 to -9 dBm
Gain	-1/2 dB
IMD3	65 dBc
Output P1dB	7 dBm
Center Frequency	3.5 GHz

Performance Summary

The various components of this system when put together didn't meet the specifications. The rough target was to achieve OP1dB of 5 dBm, NF < 10 dB and IMD3

> 56 dBc. In order to comply with specs every component was fine tuned. To optimize the fine tuning process, the system was checked initially for linearity, noise figure and image rejection. To obtain a first estimate a 2 stage RF filter was used to obtain the results which are summarized in Table 7.5. From the Table 7.5 we can clearly state that the system doesn't meet the intermodulation specification and output gain compression point.

Table 7.5 – System simulation results with a 2-Stage Filter in the lineup

Parameters	Input Buffer	Mixer	RF Filter	Output Buffer	Overall Results
Gain (dB)	13.03	-6.64	6.26	1.91	14.56
OP1dB (dBm)	8.15	1.73	2.69	3.73	3.73
IP1dB (dBm)	-3.88	-3.68	-8.98	-9.86	-9.86
IMD3 (dBc)	69	57	53	51	51
LO Leakage (dBm)	NA	-104.8	-92.5	-89.9	-89.9
Image Freq. (dBm)	NA	-22.73	-39.99	-38.9	-38.9
Noise Figure (dB)	NA	NA	NA	NA	8.57

Table 7.6 – System simulation results with a 4-Stage Filter in the lineup

Parameters	Input Buffer	Mixer	RF Filter	Output Buffer	Overall Results
Gain (dB)	13.03	-6.73	5.44	1.89	13.63
OP1dB (dBm)	8.14	0.93	0.92	1.86	1.86
IP1dB (dBm)	-3.88	-4.38	-9.84	-10.79	-10.79
IMD3 (dBc)	69	57	51	50	50
LO Leakage (dBm)	NA	-113	-93	-91	-91
Image Freq. (dBm)	NA	-23.24	-48.92	-47.71	-47.71
Noise Figure	NA	NA	NA	NA	8.34

To obtain further insight into the system behavior the number of stages of filter was increased to 4, 5 and 7 stages. Their corresponding performance summary is given in Table 7.6, 7.7 and 7.8 respectively. From the summary it can be observed that the intermodulation performance and noise figure becomes worse with increasing the number of filter stages. To counter the effect of this the optimal number of filter stages was chosen to be 4 stages.

Table 7.7 – System simulation results with a 5-Stage Filter in the lineup

Parameters	Input Buffer	Mixer	RF Filter	Output Buffer	Overall Results
Gain (dB)	13.03	-7.05	7.02	1.89	14.89
OP1dB (dBm)	8.15	-0.98	-1.03	2.94	2.94
IP1dB (dBm)	-3.88	-4.99	-12.39	-10.11	-10.11
IMD3 (dBc)	69	62	46	46.4	46.4
LO Leakage (dBm)	NA	-101.9	-79.77	-77.85	-77.85
Image Freq. (dBm)	NA	-21.21	-63.12	-62.08	-62.08
Noise Figure (dB)	NA	NA	NA	NA	10.88

Table 7.8 – System simulation results with a 7-Stage Filter in the lineup

Parameters	Input Buffer	Mixer	RF Filter	Output Buffer	Overall Results
Gain (dB)	13.02	-6.91	7.15	1.896	15.17
OP1dB (dBm)	8.15	-0.99	1.73	4.18	4.18
IP1dB (dBm)	-3.88	-4.83	-10.07	-8.23	-8.23
IMD3 (dBc)	68.9	62.1	47.4	46.5	46.5
LO Leakage (dBm)	NA	-99.32	-79.65	-76.77	-76.77

Image Freq. (dBm)	NA	-21.14	-88.14	-96.58	-96.58
Noise Figure	NA	NA	NA	NA	12.58

The input buffer was re-designed to improve the noise performance, since it's the first element in the lineup and forms a major component of the overall noise figure. The mixer was optimized for improving linearity and noise figure. In order to achieve high input compression point for the mixer, the conversion loss was increased to 9 dB, thereby improving IP1dB by 2 dBm. The performance summary of the lineup when the mixer was optimized for noise figure and linearity is summarized in the Table 7.9 & 7.10.

Table 7.9 – System simulation results with Mixer optimized for Noise Figure.

Gilbert Cell Mixer Optimized for NF					
Case I					
LO = 3.95 GHz	IF 350 MHz	RF 3.6 GHz	Vg_Ctrl 2.2 V	Vg_Ctrl 1.6 V	CF 3.6 GHz
	Input Buffer	Mixer	Filter	Output Buffer	Overall
Power (dBm)	-14.33	-21.32	-16.31	-12.37	-
Image Rejection (dBc)		7.57	25.95	29.48	29.48
Gain (dB)	12.67	-6.99	5.01	3.94	14.63
NF (dB)	-	-	-	-	7.46
IMD3 (dBc)	69	61	57	54	54
OP1dB (dBm)	-	-	-	-	+4.55
IP1dB (dBm)	-	-	-	-	-9.07
Case II					
LO = 3.85 GHz	IF	RF	Vg_Ctrl	Vg_Ctrl	CF

	350 MHz	3.5 GHz	1.4	1.2	3.5 GHz
	Input Buffer	Mixer	Filter	Output Buffer	Overall
Power (dBm)	-14.33	-21.31	-16.35	-12.52	-
Image Rejection (dBc)	-	7.81	25.76	29.42	29.42
Gain (dB)	12.67	-6.98	4.96	3.83	14.48
NF (dB)	-	-	-	-	7.82
IMD3 (dBc)	69	61	56	54	54
OP1dB (dBm)	-	-	-	-	4.45
IP1dB (dBm)	-	-	-	-	-9.03
Case III					
LO = 3.55 GHz	IF = 350 MHz	RF = 3.2 GHz	Vg_Ctrl = 0.4	Vg_Ctrl = 0.4	CF = 3.2 GHz
	Input Buffer	Mixer	Filter	Output Buffer	Overall
Power (dBm)	-14.33	-22	-17.61	-14.02	-
Image Rejection (dBc)	-	7.75	26.08	30.38	30.38
Gain (dB)	12.67	-7.67	4.39	3.59	12.98
NF (dB)	-	-	-	-	8.16
IMD3 (dBc)	69	61	55	53	53
OP1dB (dBm)	-	-	-	-	3.47
IP1dB (dBm)	-	-	-	-	-8.49

Table 7.10 – System simulation results with Mixer optimized for Noise Figure.

Gilbert Cell Mixer Optimized for Linearity					
Case I					
LO = 3.85 GHz	IF = 350 MHz	RF = 3.5 GHz	Vg_Ctrl = 2.2 V	Vg_Ctrl = 1.2 V	CF = 3.5 GHz
	Input Buffer	Mixer	Filter	Output Buffer	Overall
Power (dBm)	-14.34	-21.11	-16.16	-12.32	-
Image Rejection (dBc)	-	6.55	24.55	28.21	28.21
Gain (dB)	12.66	-6.77	4.95	3.84	14.68
NF (dB)	-	-	-	-	8.37
IMD3 (dBc)	69	61	56	54	54
OP1dB (dBm)	-	-	-	-	4.51
IP1dB (dBm)	-	-	-	-	-9.15
Case II					
LO = 3.8 GHz	IF = 350 MHz	RF = 3.45 GHz	Vg_Ctrl = 1.4 V	Vg_Ctrl = 1 V	CF = 3.45 GHz
	Input Buffer	Mixer	Filter	Output Buffer	Overall
Power (dBm)	-14.33	-21.26	-16.36	-12.54	-
Image Rejection (dBc)	-	7.22	25.48	29.27	29.27
Gain (dB)	12.67	-6.93	4.9	3.82	14.46

NF (dB)	-	-	-	-	8.63
IMD3 (dBc)	69	61	56	53	53
OP1dB (dBm)	-	-	-	-	+4.34 dBm
IP1dB (dBm)	-	-	-	-	-9.16 dBm
Case III					
LO = 3.6 GHz	IF = 350 MHz	RF = 3.25 GHz	Vg_Ctrl = 0.4 V	Vg_Ctrl = 0.4 V	CF = 3.25 GHz
	Input Buffer	Mixer	Filter	Output Buffer	Overall
Power (dBm)	-14.33	-21.79	-17.37	-13.75	-
Image Rejection (dBc)	-	8.76	27.39	32	32
Gain (dB)	12.67	-7.46	4.42	3.62	13.25
NF (dB)	-	-	-	-	8.98
IMD3 (dBc)	69	61	54	52	52
OP1dB (dBm)	-	-	-	-	+3.16
IP1dB (dBm)	-	-	-	-	-9.01

After optimization of components for intermodulation performance the overall system performance is given by the Table 7.11. This design finally meets the target specifications with a low noise figure and high intermodulation performance. The overall gain was sacrificed a little bit, but the bandwidth and tuning range was kept intact.

Table 7.11 – Summary of overall system performance for 3.5 GHz Transmitter

	Input Buffer	Mixer	Filter	Output Buffer	Overall	Units
Power	-14.34	-22.92	-18.67	-17.12	-17.12	dBm
Image Rejection	NA	4.53	23.58	27.41	27.41	dBc
Gain	12.67	-8.58	4.25	1.55	9.89	dB
NF	NA	NA	NA	NA	8.26	dB
IMD3	67.75	64.58	61.72	61.39	61.39	dBc
OP1dB	NA	NA	NA	NA	2.99	dBm
IP1dB	NA	NA	NA	NA	-5.8	dBm
LO Leakage	NA	-101.3	-99.13	-94.89	-94.89	dBm
Upconv 140 MHz to 3.71 G	NA	-86.72	-88.48	-92.36	-92.36	dBm
Upconv 140 MHz to 3.99 G	NA	-87.69	-92.69	-99.31	-99.31	dBm

CHAPTER 8

CONCLUSION

The design of high frequency systems on silicon has left a lot of parameters to be controlled or compensated on chip. The system on chip solutions is subjected to ambient temperature variations, process corner variation and external power supply fluctuation.

With the advances in technology from 0.35 um CMOS heading towards 45 nm CMOS, all the process is tailored for digital circuit design. This has left the bipolar and field transistor theory unusable for sub-micron CMOS technologies. This complicated the process of circuit design where the mathematical relations can only show us the base chord to start the design. Temperature and process corner variations are the most evident ones which the designer needs to handle in design process, but there are certain issues which by nature doesn't lend themselves to be analyzed. For example the startup circuit design for bandgap reference is a condition where in no current flows in the temperature controlled elements.

The design of high frequency mixers in 90 nm CMOS lends its own challenges towards design iteration. The performance is tuned to obtain a trade-off between noise figure and linearity. Post layout simulation combined with parasitic extraction gives us a close estimate of the results. The design of a feedback control loop with precise data converters opens avenues for more external parameters to be controlled and compensates for their variation internally. Temperature is the aspect that was handled in this thesis, while the future course of action is on process corner detector, which implements a

similar feedback loop to the control the output of the bias core based on the process which is prevalent in the particular area of the chip.

APPENDIX A

VERILOG CODE FOR SUCCESSIVE APPROXIMATION LOGIC

```
//////////////////////////////////////////////////////////////////////////////////
* Company: Georgia Electronic Design Center
* Group: Multi Gigabit Wireless Research group
* Team: RF Transmitter
* Project: SAR ADC for Temperature Sensor / RSSI / CCA applications
* this is a 6b SAR ADC built for the Temperature Sensor application, modified to suit
* RSSI & CCA applications as well.
* Expected Clock Frequency = 27 MHz
* One conversion should take 8 clock cycles = 1 SOC + 6 data conversion + 1 EOC
//////////////////////////////////////////////////////////////////////////////////
//////////////////////////////////////////////////////////////////////////////////
* Functional description:
* V1:
* this is a 6b SAR ADC built for the Temperature Sensor application.
* The clock is running at 27MHz.
* One conversion should take 10 clock cycles = 1 SOC + 6 data conversion + 1 EOC + 2

//////////////////////////////////////////////////////////////////////////////////
* Parameters:
* Clock Cycle              Operation
* ----------          ------------------------
```

```
*       1           SOC, Start of Conversion
*     2 - 7           Data Conversion
*       8           EOC, End of Conversion
 ********************************************************************************
* Synthesis reports:
*    + Design Compiler targeting 90nm
*    - Minimum period: 5ns (Target Maximum Frequency: 200MHz)
*    - Area:
********************************************************************************
* Revisions:
*    + Revision 1.0 (26/06/2009)
*    - Initial check-in
********************************************************************************
include "sar_adc_logic_6b_v1.h"
module sar_adc_logic_6b_v2(
    input clock,
    input reset_n,
    input cmp_decision,
    output reg soc,
    output reg eoc,
    output reg [5:0] result,
    output [5:0] vref_mask);

 // To store the result values while the conversion step is ON
reg [5:0] idr_result;
 // The actual register with a '1' being shifted
 reg [5:0] sar;
```

```
 // This gets OR'ed with idr_result and gets applied to vref_mask
// To count which cycle we are currently in (when in convert_state)
 reg [2:0] count;
// To count the number of wait cycles
 reg    [1:0] wait_cnt;
 // Indicates which state we are in, at any given time
 reg [2:0] state;
/* Definitions of local parameters used */
/* Parameter definitions */
 parameter reset_state = 0, sample_state = 1, convert_state = 2, eoc_state = 3, wait_state
= 4;
/* Main Code for Successive Approximation calculations */
 always @(posedge clock or negedge reset_n) begin
        if(!reset_n) begin
           result   <=  6'b0;
           idr_result   <=  6'b0;
           soc  <=  1'b0;
           eoc  <=  1'b0;
           sar   <=  6'b0;
           state  <=  3'b0;
           wait_cnt  <=  2'b0;
           count  <=  3'b0;
        end
        else begin
           case (state)
              reset_state : state  <=    sample_state;
              sample_state : begin
```

```
   soc  <=    1'b1;           // T/H is now in the Track mode
   sar   <=    6'b0;          // Set the sar register to all 0's, before SOC
   idr_result  <=    6'b0; // Reset the intermediate result register
   eoc   <=  1'b0;           // EOC is set to zero, if there are no wait cycles
   state  <=  convert_state;
   count  <=  3'b0;
   wait_cnt    <=    2'b0
   end

 convert_state : begin
 soc <= 1'b0; // We have completed sampling the input. T/H is now in Hold mode

 if (count == 3'b000)
 sar  <= 6'b100000; // MSB=1, we are preparing for the 1'st comparison
 else
 sar <=  sar >> 1; // Right shift the 'sar' contents by 1
count  <=  count + 1'b1; // Increment the counter by 1

if (cmp_decision)
idr_result    <=    idr_result    | sar;    // OR the previous result with the current

 if (count == 3'b101)
 state  <=  eoc_state; // We are currently in the 6th cycle of conversion
end

 eoc_state: begin
 eoc  <=  1'b1; // Indicate that we are now in End of Conversion state
```

```
            result   <=    idr_result + cmp_decision;
            // The last comparator decision is available only now
            sar  <=  6'b0; // Set the sar register to all 0's, after conversion completes
            idr_result    <=    6'b0;
            state  <=  sample_state;
              end

              wait_state       :    begin
              state <= sample_state; // Go back to sample state if you come here by mistake
              end

       default: state  <=  sample_state;
       endcase
     end
end
 // vref_mask gets applied to SAR ADC Vref/DAC switches
assign vref_mask = sar | idr_result;
endmodule
```

The above verilog code was synthesized using Synopsys Design Compiler. The synthesized output is exported to Cadence Virtuoso environment, where the digital logic and accompanying layout was used in design of Successive Approximation Data converters.

APPENDIX B

MATLAB CODE FOR INL/DNL COMPUTATION

```
% M-File to compute INL / DNL for SAR ADC.
% Apply slow ramp input to the ADC input with a slope of n samples/CODE
load DNL_Output;
time = DNL_Output(:,1);   %  copy first column into time
amp = DNL_Ouptut(:,2);    %  and second column into amp
length = size(amp)
J = 101;     % number of average count/bin
for n=1:8
   CODE(n) = 0;
end

for j=length(2):length(1)
   if amp(j) == 0
      CODE(1) = CODE(1) + 1;
   end
   if amp(j) == 125
      CODE(2) = CODE(2) + 1;
   end
   if amp(j) == 250
      CODE(3) = CODE(3) + 1;
   end
```

```
    if amp(j) == 375
      CODE(4) = CODE(4) + 1;
    end
    if amp(j) == 500
      CODE(5) = CODE(5) + 1;
    end
    if amp(j) == 625
      CODE(6) = CODE(6) + 1;
    end
    if amp(j) == 750
      CODE(7) = CODE(7) + 1;
    end
    if amp(j) == 875
      CODE(8) = CODE(8) + 1;
    end
end
% Normalize the Histogram
for n=1:8
    CODE(n) = (CODE(n)-J)/J;
end
plot(CODE,'o','MarkerEdgeColor','k','MarkerFaceColor','g')
title('DNL [100samples/code]');  %  add title
xlabel('Code','Color','b');    %  add axis labels and plot title
ylabel('DNL [LSB]','Color','b');   %  add axis labels and plot title
```

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