

# Complete system test-bench

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April 26, 2016

## 1 System overview

The overall structure of the system is seen in Figure 1.

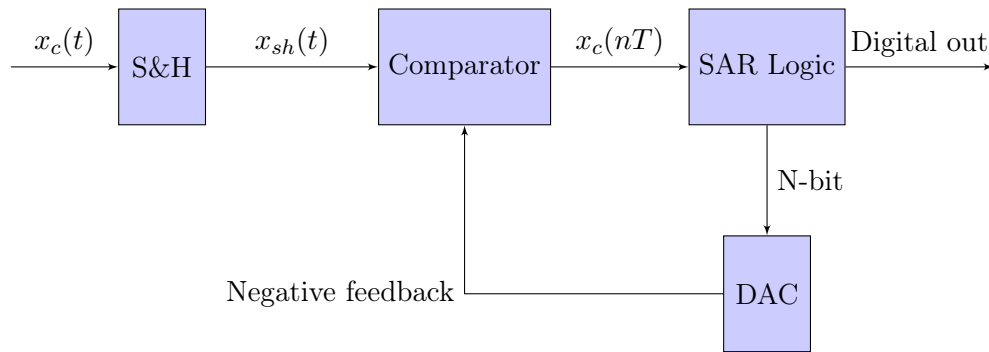


Figure 1: Block diagram

## 2 Schematic

We have not completed our research in circuits to use in this project. We have created schematics for some simple circuits but we expect that some (or all) of the circuits is going to change. See test-benches in the next section.

### Schematic: SAR\_system

The SAR\_system is the complete schematic for the whole system. It consists of a sample and hold block, a comparator block, the SAR logic and the digital-to-analog converter block. Figure 2 shows the schematic that has been created.



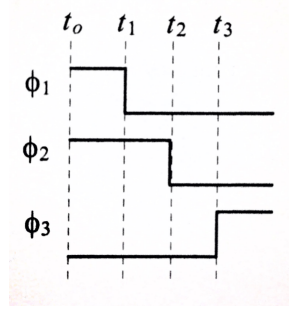


Figure 3: Single-ended S/H operation [1]

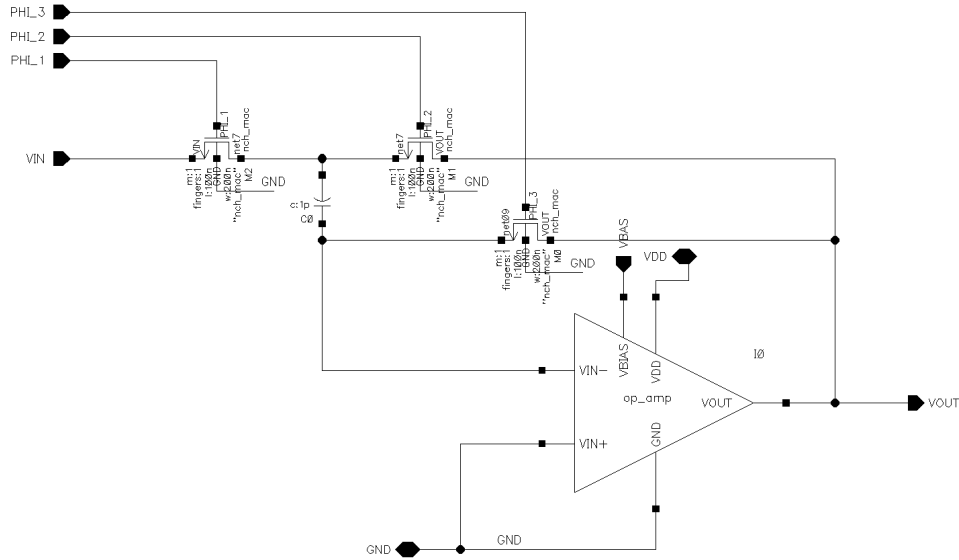


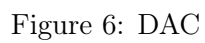
Figure 4: Sample and hold

## Schematic: SAR\_logic

We have not completed the schematics for the SAR logic. The chematic for the SAR is therefor not invluded in this document.

## Schematic: dac

This DAC circuit is based on the R-2R ladder from the book Analog Integrated Circuit Design by Carusone, Johns and Martin [2]. This design commonly used in many applications, and is therefor the main reason for why we have chosen to make this design. The DAC schematic can be seen



in Figure 6.

## Schematic: op\_amp

The op-amp circuit is based on a design from CMOSedu.com (R. Jacob Baker), and is a commonly used differential pair op-amp. We have tried some different designs, but we have not succeeded in any of the other designs. This is not the final version, since it is not fully tested. The dimensions for the NMOS and PMOS transistors are based on a former thesis that R. Jacob Baker has referred to in his web-page. For the NMOS and the PMOS, we have used the relation  $10/2$  and  $22/2$  respectively [3]. The final design can be seen in Figure ??

To test the op-amp, we have made a simple test-bench that can be seen in section **Schematic: SIM\_op\_amp**.

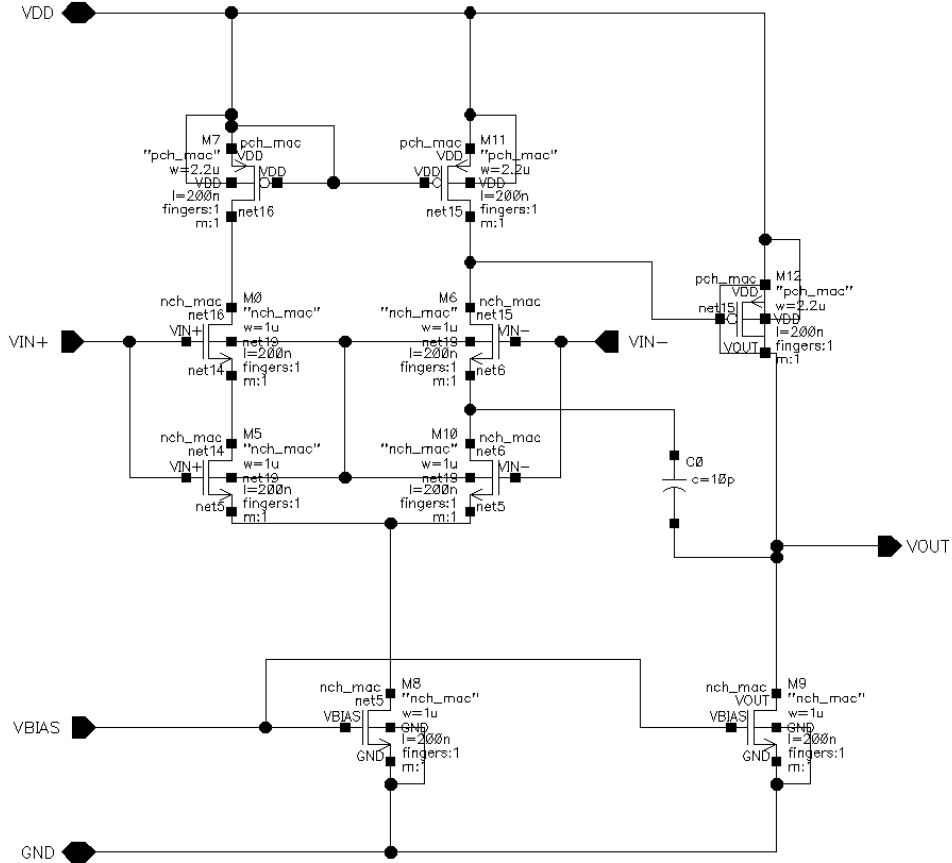


Figure 7: Opamp

### 3 Test bench

In this section a short overview of the different test-benches for our components is presented.

#### Schematic: SIM\_system

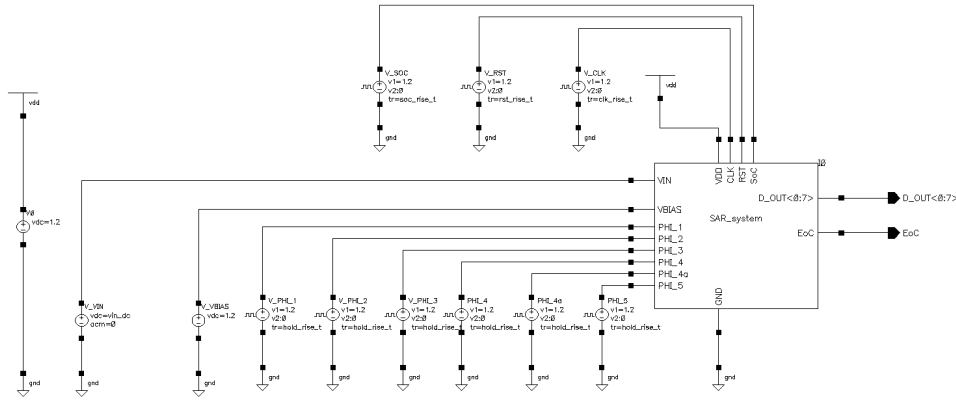


Figure 8: Test bench for SAR-ADC circuit

This is a complete system test bench. Here all the different components come together to form the full SAR-ADC architecture.

Testing on a system level is necessary to ensure that the circuit performs according to the interface the circuit provides to the outside world.

This test scenario is quite hard to set up since many signals have to be timed to each other. The verification of the circuit is also challenging since many signals have to be considered. In order to manage this test we need to generate a test procedure with the specified stimuli and check the results to a expected pattern. See Figure 8.

#### Schematic: SIM\_sample\_hold

To test the sample and hold we need to generate 3 clocks (see timing diagram in figure 3). The output is ideally expected to match the input value and

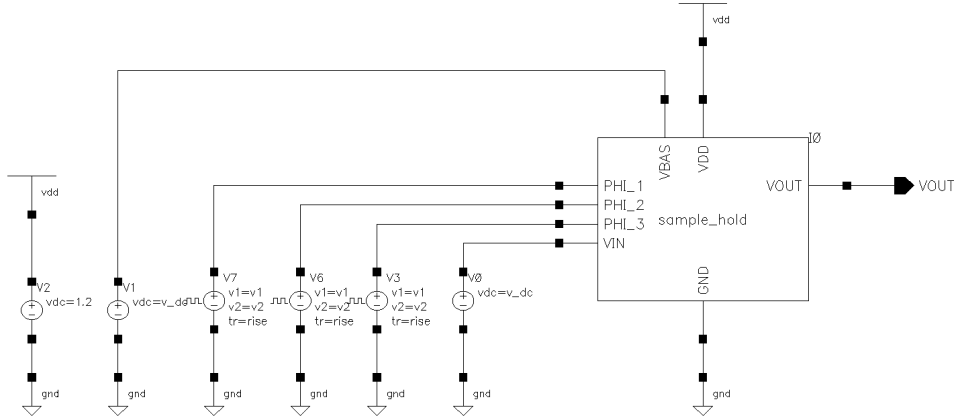


Figure 9: Test bench for sample and hold circuit

hold it in the phi\_3 phase. See Figure 9.

### Schematic: SIM\_comparator

In the test bench for the comparator we need 3 clocks for the timing. When sweeping the input (let's say VIN-) we expect that at some point (dependent on VIN+,) that the comparator will change state. See Figure 10.

### Schematic: SIM\_SAR\_logic

Some of the circuit in the SAR-logic is given but some extra circuitry is needed. In this test bench we want to test that the acquisition state is started when the SoC signal is pulsed. And that we receive a EoC after N-bits clock pulses. We also need to test the reset functionality. The main function of generating the digital output is easy to test since the input signal decides the value of the current bit. See Figure 11.

### Schematic: SIM\_dac

The test-bench for the DAC consists of N-bits pulse generators so that we can apply a binary pattern. VOUT should be proportional to the binary value. See figure 12.

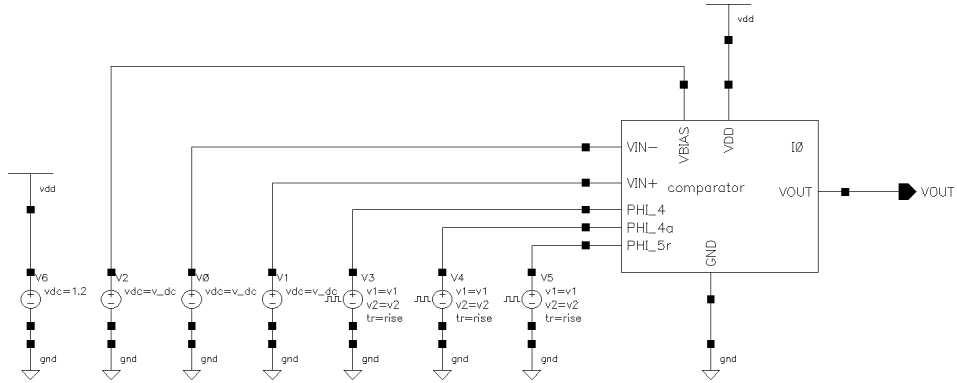


Figure 10: Test bench for comparator circuit

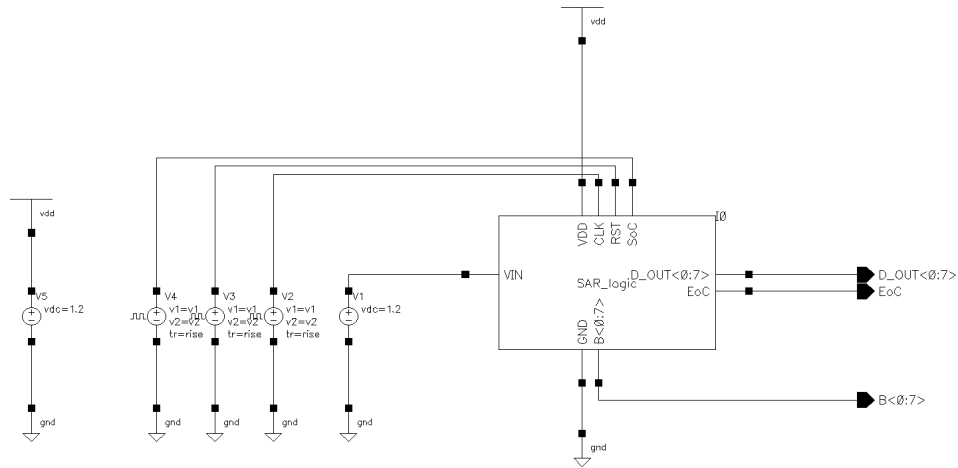


Figure 11: Test bench for SAR-logic circuit

## Schematic: SIM\_op\_amp

In our test bench for the op-amp we have an open circuit amplifier that expect is going to saturate to either (almost) GND or VDD, if our gain is high



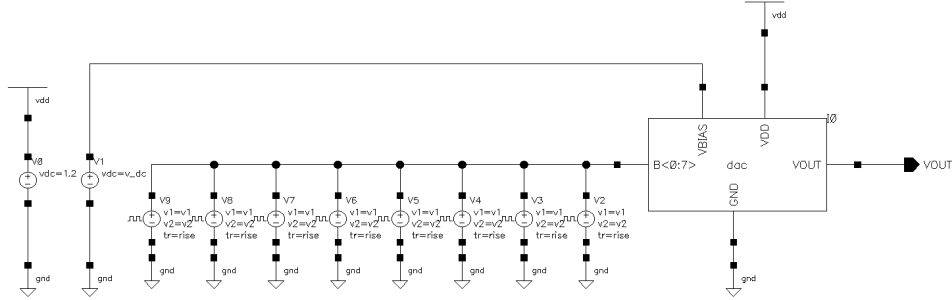


Figure 12: Test bench for DAC circuit

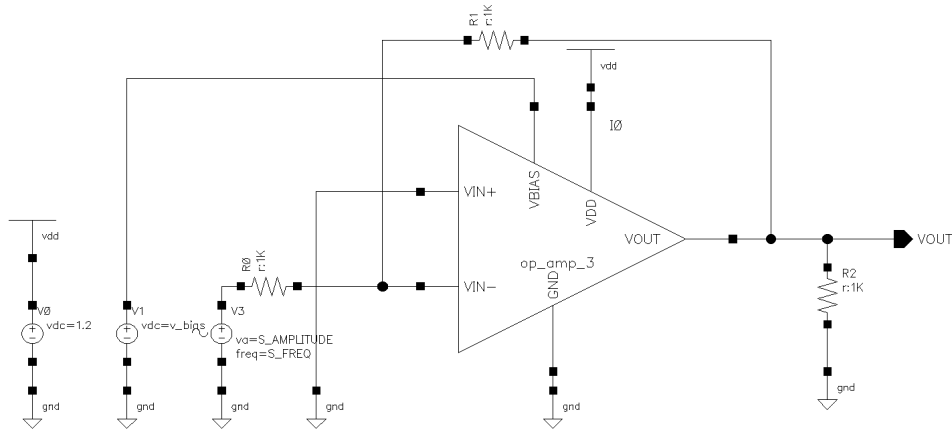


Figure 13: Test bench for op-amp circuit

enough. This simulation is a test to check for response and not performance. This simple test gives little information about the performance of the op-amp. To get a better test of the performance of the circuit we need more

tests where we test other configurations of the op-amp. See Figure 13 and 14.

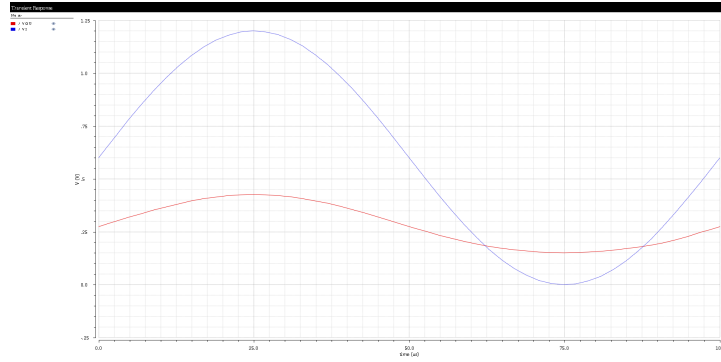


Figure 14: AC response from op-amp circuit used as a non-inverting amplifier

## References

- [1] R. Jacob Baker. *CMOS Mixed-Signal Circuit Design*. IEEE Press, John Wiley, and Sons, 2009.
- [2] Carusone et al. *Analog Integrated Circuit Design, 2nd. edition*. John Wiley and Sons, 2013.
- [3] Vishal Saxena. "INDIRECT FEEDBACK COMPENSATION TECHNIQUES FOR MULTI-STAGE OPERATIONAL AMPLIFIERS". Boise State University, "2007".