An 8-Bit 100-MHz CMOS Linear Interpolation DAC

Yijun Zhou and Jiren Yuan

***Abstract*—An 8-bit 100-MHz CMOS linear interpolation digital-to-analog converter (DAC) is presented. It applies a time-interleaved structure on an 8-bit binary-weighted DAC, using 16 evenly skewed clocks generated by a voltage-controlled delay line to realize the linear interpolation function. The linear interpolation increases the attenuation of the DAC's image components. The requirement for the analog reconstruction filter is, therefore, greatly relaxed. The DAC aims for the single-chip integration of a wireless transmitter.**

The chip was fabricated in a 3.3-V 0.35-μm double-poly triple-metal CMOS process. The core size of the chip is 0.67 mm $\times$ 0.67 mm, and the total power consumption is 54.5 mW with 3.3-V power supplies. The attenuation (in decibels) of image components is doubled compared with a conventional DAC.

***Index Terms*—CMOS integrated circuits, digital-to-analog converter (DAC), filter, interpolation.**

I. Introduction

THE pressure to reduce the cost and size of various electronic products has impacted the system-on-chip design. In such a system, there is a strong demand for a high-speed and high-resolution digital-to-analog converter (DAC), which enables digital and analog blocks to be integrated on a single chip in CMOS technology.

A conventional DAC can be seen as a zero-order-hold converter whose frequency response is a sinc function. A high-performance analog reconstruction filter is normally needed to remove the image components. The implementation of such an analog reconstruction filter is expensive and difficult in a CMOS process. A system which uses the DAC's sinc response to attenuate the image components has been reported [1]. However, the sinc function was not enough to attenuate the images of a wide-band signal. Therefore, it is necessary to look for new DAC structures to relax the requirement of the analog reconstruction filter or even to remove it. In this brief, a binary-weighted linear interpolation DAC using a time-interleaved structure is introduced. The frequency response of the presented linear interpolation DAC is approximately the square of the sinc function. Compared with a zero-order-hold DAC, the presented DAC can provide a higher attenuation of the image signals, especially when the image components are near to the clock frequency. This DAC aims for the single-chip integration of a wireless transmitter [2].

Manuscript received May 7, 2002; revised May 15, 2003.

Y. Zhou is with the Institute for Infocomm Research (I^2R), A*Star, Singapore 117674, Singapore.

J. Yuan is with the Competence Center for Circuit Design, Department of Electroscience, Lund University, SE 221 00 Lund, Sweden.

Digital Object Identifier 10.1109/JSSC.2003.817593

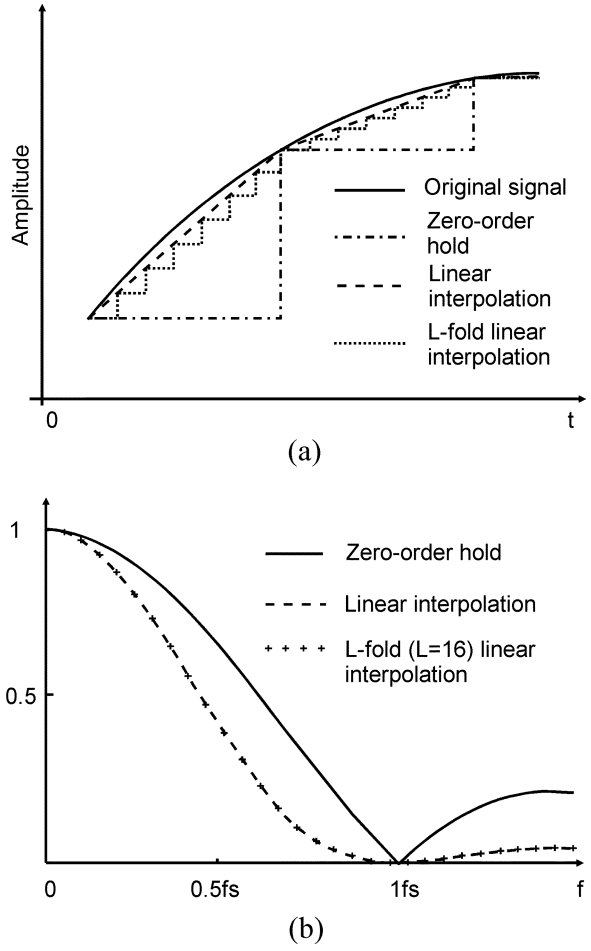

Fig. 1. Zero-order-hold, linear interpolation, and L-fold linear interpolation DAC's responses, in (a) the time domain and (b) the frequency domain.

II. Linear Interpolation DAC

The most widely used DAC is of the zero-order-hold type, having the output shown in Fig. 1(a), which constantly holds the value of one sample until the next sample. It generates a staircase approximation to the original signal. The spectrum of the zero-order-hold output, shown in Fig. 1(b), is a sinc function. In practice, this type of DAC is often followed by a low-pass filter to attenuate the image components. Especially for a wide-band signal, the requirement on the reconstruction filter is strict. If the zero-order hold is replaced by the linear interpolation, shown in Fig. 1(a) as well, the attenuation of the DAC's image components can be improved since the frequency response of the latter, which is illustrated with the dashed line in Fig. 1(b), is the square of the sinc function [3]. The requirement of the reconstruction filter can, therefore, be relaxed. However, from a

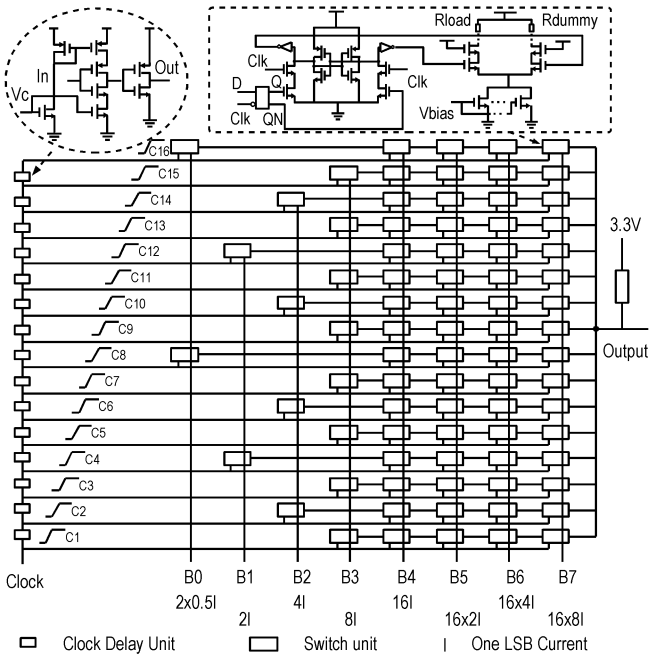

Fig. 2. An 8-bit linear interpolation DAC.

practical viewpoint, the realization of such a linear interpolation is complex and difficult. Instead, an L-fold linear interpolation, shown in Fig. 1(a), is employed in this brief to approximate the linear interpolation and to achieve the frequency response close to the square of the sinc function [4].

Fig. 2 shows the basic design of the proposed linear interpolation DAC which has a binary-weighted current steering structure. Current steering DACs are widely used in the high-speed and high-resolution design because they are intrinsically fast and easy to integrate in a CMOS technology. The binary-weighted structure is simple and does not require complex decoding logic. Based on this structure, the linear interpolation function was developed. In this design, the input clock period is skewed into 16 subclocks C1, C2, ..., C16 at equal intervals by a voltage-controlled delay line. The binary-weighted current source of each bit is divided into L identical subcurrent source units. The L subcurrent source units are sequentially triggered by the subclocks, and in such a way the L-fold linear interpolation is realized. This linear interpolation DAC combines the functions of linear interpolation finite impulse response (FIR) filter and the DAC together. Traditionally, this function has been realized by using separate DSP and DAC chips or integrating them together, but more power consumption and chip area are required. In such case, the clock frequency has to be L times higher.

In this design, the number of subcurrent source units L is different in each bit. It uses 2, 2, 4, 8, 16, 16, 16, and 16 subcurrent source units for B0 (LSB), B1, B2, B3, B4, B5, B6, and B7 (MSB), respectively. The maximum value of L is 16. Of course, if the binary-weighted current source is divided into 16 subcurrent source units in B0, B1, B2, and B3 also, the best performance can be achieved. However, this solution needs more chip area and power consumption. If the number of the subcurrent source units and their trigger times for each bit are properly selected, the approximate linear interpolation can still be achieved. The number of the subcurrent source units and their trigger times of each bit for minimum glitch energy are specified in Fig. 2. In this design, the tradeoff between the number of subcurrent source units for each bit and the resulting chip area and power consumption was carefully considered, and the trigger times of subcurrent source units has been chosen to achieve the best performance.

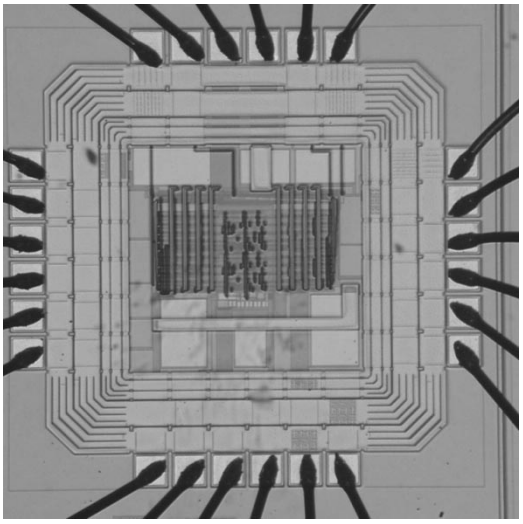

Fig. 3. Chip micrograph.

III. Circuit Implementation

In this design, the voltage-controlled delay line generates 16 rising edges at equal intervals in one clock period to trigger the subcurrent source units. It consists of 15 current-starved voltage-controlled delay units. All the current-starved voltage-controlled delay units produce equal delays. One of the current-starved voltage-controlled delay units is shown in Fig. 2, which employs the current-starved inverter structure. V_c is used to adjust the delay of the current-starved unit by controlling the current of the inverter. With the adjustment of V_c, the voltage-controlled delay line can work at different input clock frequencies.

The subcurrent source unit shown in Fig. 2 includes switches and unit current source cells. The number of unit current source cells depends on the weight of the bit. For B7, there are eight unit current source cells in each subcurrent source unit, i.e., 8I if 1 LSB is represented as 1I, and the total number of unit current source cells is 128, i.e., 128I (8I $\times$ 16). To satisfy the binary-weighted rule, each subcurrent source unit in B7 (MSB), B6, B5, B4, B3, B2, and B1 consists of 8, 4, 2, 1, 1, 1, and 1 unit current source cells, respectively, and for B0 (LSB), it consists of a half unit current source cell. This arrangement aims for improving the matching among the current sources of each bit. In addition, in the layout, the first 128 unit current source cells are grouped into B7, and the next 64 cells into B6, etc. The two half-sized unit current source cells are grouped into B0. The total 254 unit current source cells and two half-unit current source cells form a 16 $\times$ 16 matrix structure. In order to reduce the coupling from the clock signal to the output through the parasitic capacitance of the switch transistors, cascaded transistors are used. The current source is switched to either the output load

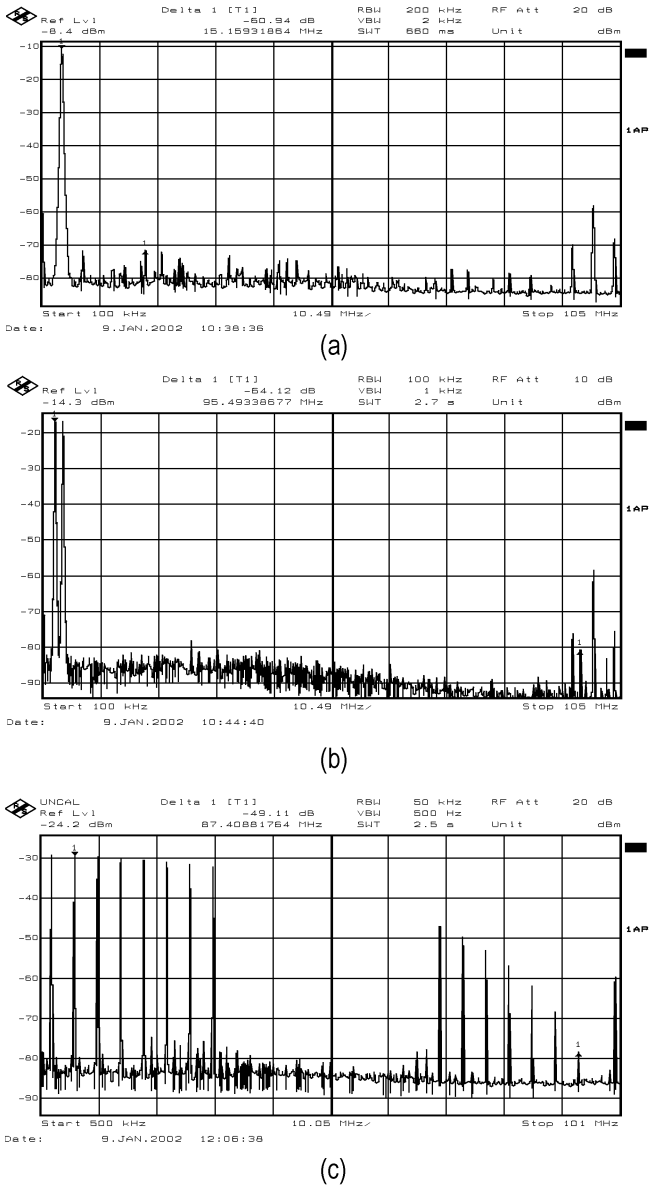

Fig. 4. Measured performance at $F_{\rm clk} = 100$ MHz. (a) $F_{\rm sig} = 3.79$ MHz. (b) $F_{\rm sig1} = 2.37$ MHz, $F_{\rm sig2} = 3.79$ MHz. (c) Multitone output.

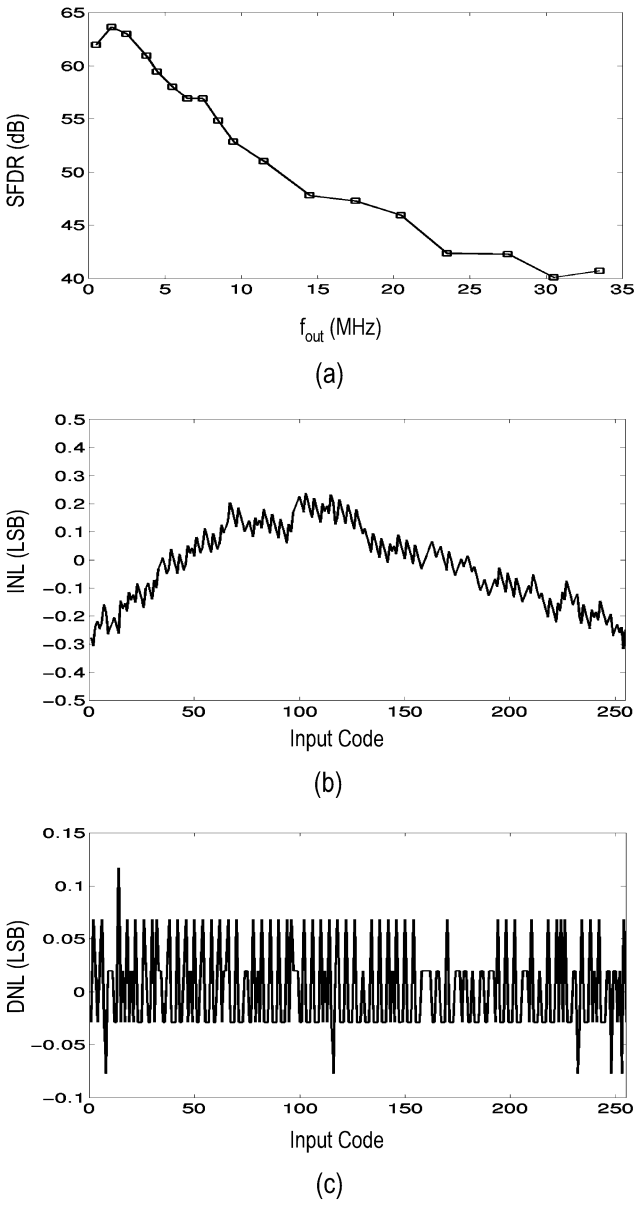

Fig. 5. (a) Measured SFDR as a function of the output signal frequency. (b) INL characteristics. (c) DNL characteristics.

or the dummy load, controlled by the logic value of each bit, which comes from the driving stage. Changing $V_{\rm bias}$ can adjust the output current of each unit current source cell.

There is a driving stage for each subcurrent source unit. As shown in Fig. 2 [5], [6], each driving stage is a rising-edge triggered flip-flop, formed by a D latch and a clocked set/reset (SR) flip-flop. In order to speed up the settling and minimize the voltage fluctuation at the drain of the current sources, differential current switches are designed not to be turned off simultaneously. In the design, the dimensions of the transistors for the SR flip-flop are properly selected to generate the overlapped driver signals.

As mentioned above, in order to minimize the overall mismatch, the unit current source cells are put close to each other to form the matrix. The matrix occupies the center of the die, in which the unit current source cells are distributed properly to locate the centroid of the current sources at the center of the matrix to decrease the gradient effect of the process. Dummy current source cells are laid around the matrix. The voltage-controlled delay line is laid on the top part of the chip, which is directly above the output port connection; it is the main reason why high clock leakage has been measured. The driver stages are put in the left and right sides. To reduce the noise coupling, separated power supplies and grounds for the current source and for the digital part are used. Guard rings are used between the current source and the digital part to prevent the noise coupling via the substrate.

IV. Measurement Results

The DAC based on Fig. 2 has been fabricated in a 0.35-μm double-poly triple-metal CMOS process. Fig. 3 shows the chip micrograph. The core size of the chip is 0.67 mm $\times$ 0.67 mm. The digital and analog voltage supplies are each 3.3 V. The full-scale output is 264 mV, and the total power consumption is

TABLE I
MULTITONE PERFORMANCE SUMMARY

Frequencies (MHz)	Measured Attenuation of image components (dB)	Calculated from $\frac{(\mathrm{sinc}(f/f_{clk}))^2}{(\mathrm{sinc}(f_{image}/f_{clk}))^2}$ (dB)	SFDR (dB)
2.37	64.12	64.59	42.5
6.37	49.11	46.69	
10.37	38.61	37.46	
14.37	31.85	31.01	
18.37	26.49	25.91	
22.37	22.06	21.61	
26.37	18.29	17.84	
30.37	14.84	14.41	

TABLE II
PERFORMANCE SUMMARY

Resolution	8 Bit
Update Rate	100 Mhz
INL	±0.32 LSB
DNL	±0.12 LSB
Power @ 3.3 V Supply	54.5 mW
Core Size of the Chip	0.67mm x 0.67mm
SFDR (2.49 MHz@Fclk = 100 Mhz)	62.13 dB
The attenuation of image components	See Table I

54.5 mW. A measured sine-wave spectrum for $F_{\mathrm{clk}} = 100$ MHz and $F_{\mathrm{sig}} = 3.79$ MHz is shown in Fig. 4(a), in which the spurious free dynamic range (SFDR) is 60.94 dB and the attenuation of the image signal is 59.66 dB. Fig. 4(b) shows the result of two tones measurement. The two signals are 2.37 and 3.79 MHz. The SFDR is 61.69 dB, and the image attenuation of the 2.37-MHz signal is 64.12 dB. Fig. 4(c) is the measured multitone spectral plot. Fig. 5(a) presents the measured SFDR as a function of the output signal frequency. A summary of the multitone measurement, which compares the image signal with the original signal, is given in Table I. From the measurement results, the DAC doubles the attenuation (in decibels) of the image signal with respect to the zero-order-hold DAC, and the results show a good agreement with the square of the sinc function. Fig. 5(b) and (c) shows the measured integral nonlinearity (INL) and differential nonlinearity (DNL) versus input code, respectively. The INL errors lie between -0.32 and 0.24 LSB, and the DNL errors lie between -0.08 and 0.12 LSB.

Table II summarizes the measured performance of the 8-bit 100-MHz linear interpolation DAC.

V. CONCLUSION

An 8-bit 100-MHz CMOS current steering linear interpolation DAC has been presented. The DAC has been implemented in a 3.3-V 0.35-μm double-poly triple-metal digital CMOS process. The key feature of the DAC is the use of linear interpolation technique to double the attenuation (in decibels) of the image components. The measured attenuation of the image components presents a good agreement with the theoretical prediction. The traditional analog reconstruction filter can, therefore, be simplified or even eliminated. With this feature, the DAC is more suitable for the full integration of a wireless transmitter.

REFERENCES

[1] A. Rofougaran, G. Chang, J. J. Rael, J. Y.-C. Chang, M. Rofougaran, P. J. Chang, M. Djafari, M.-K. Ku, E. W. Roth, A. A. Abidi, and H. Samueli, "A single-chip 900-MHz spread-spectrum wireless transceiver in 1-μm CMOS—Part I: Architecture and transmitter design," *IEEE J. Solid-State Circuits*, vol. 33, pp. 515–534, Apr. 1998.

[2] Y. Zhou and J. Yuan, "A 10-bit wide-band CMOS direct digital RF amplitude modulator," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1182–1188, July 2003.

[3] K. A. Essenwanger, "Slewer fractional-order-hold: the ideal DAC response for direct digital synthesizers," in *Proc. Frequency Control Symp.*, 1998, pp. 379–389.

[4] S. J. Orfanidis, *Introduction to Signal Processing*. Englewood Cliffs, NJ: Prentice-Hall, 1996.

[5] J. Bastos, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 12-bit intrinsic accuracy high-speed CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1959–1969, Dec. 1998.

[6] D. Mercer and L. Singer, "12-b 125-MSPS CMOS D/A designed for spectral performance," in *Proc. Int. Symp. Low Power Electronics and Design*, 1996, pp. 243–246.