Complete system testbech

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1 Report contents

This report contains a brief explanation of the different part in our project.

2 Structure

The overall structure of the system is seen in Figure 1.

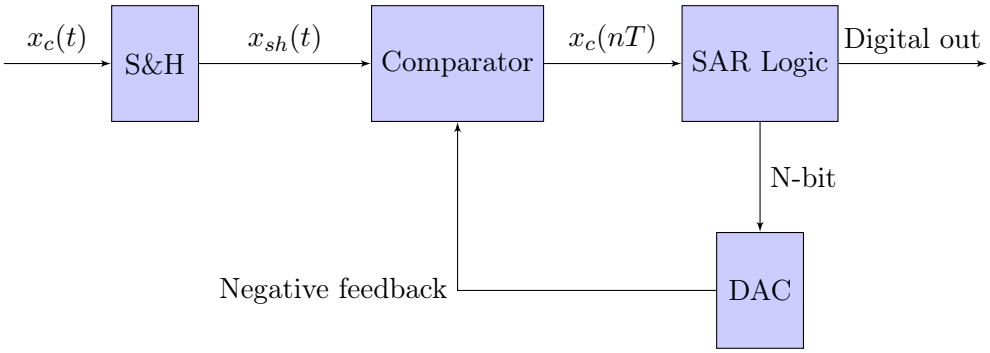

Figure 1: Block diagram

3 Schematic

We have not completed our resarch in circuits to use in this project. We have created schematics for some simple circuitis but we expect that some (or all) of the circuits is going to change.

Schematic: SAR_system

The SAR_system is the complete schematic for the whole system. It consists of a sample and hold block, a comarator block, the SAR logic and the

digital-to-analog converter block. Figure 2 shows the schematic that has been created.

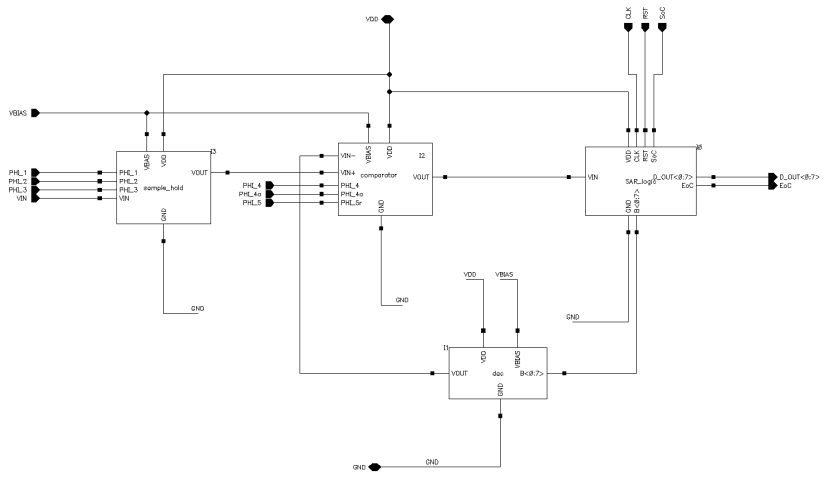

Figure 2: SAR_system

Schematic: sample_hold

The sample and hold (S/H) is based on a circuit provided by R. Jacob Baker in the book CMOS Mixed-Signal Circut Design **[CMOS-baker]**. The implementation is a single-ended S/H implementation. When ϕ_1 and ϕ_2 is high, ϕ_3 is low, and the bottom plate of the hold capacitor is charged by the input signal, while the top plate is held to ground by the feedback around the op amp. When the ϕ_2 is turned off, its charge will be injected into the low impedance input, VIN, since the impedance looking into the left of the ϕ_2 switch is large.

This implementation has not yet beed tested, and may therefor be changed during the project.

Schematic: comparator

The design of the comparator is based on a design in the book Analog Integrated Circuit Design by Carusone, Johns and Martin **[Analog-integrated]**.

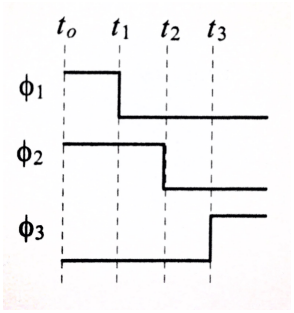

Figure 3: Single-ended S/H opartion [**CMOS-baker**]

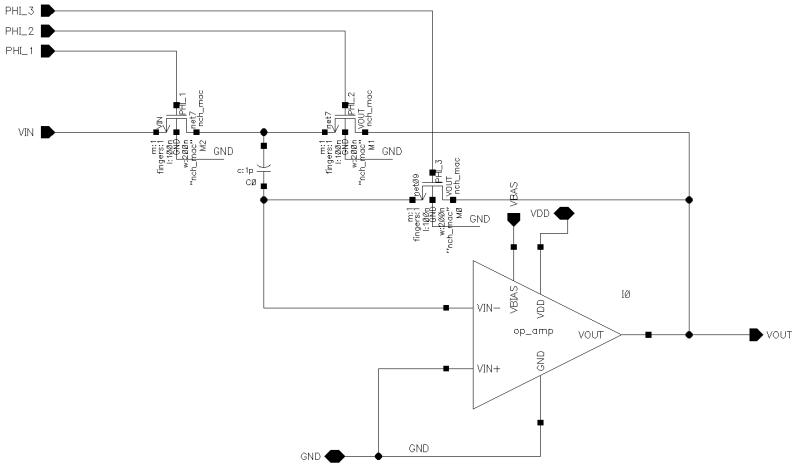

Figure 4: Sample and hold

Schematic: SAR_logic

We have not completed the schematics for the SAR logic.

Schematic: dac

This DAC circuit is based on the R-2R ladder from the book Analog Integrated Circuit Design by Carusone, Johns and Martin [**Analog-integrated**]. This design commonly used in many applicaions, and is therefor the main reason for why we have choosen to make this design.

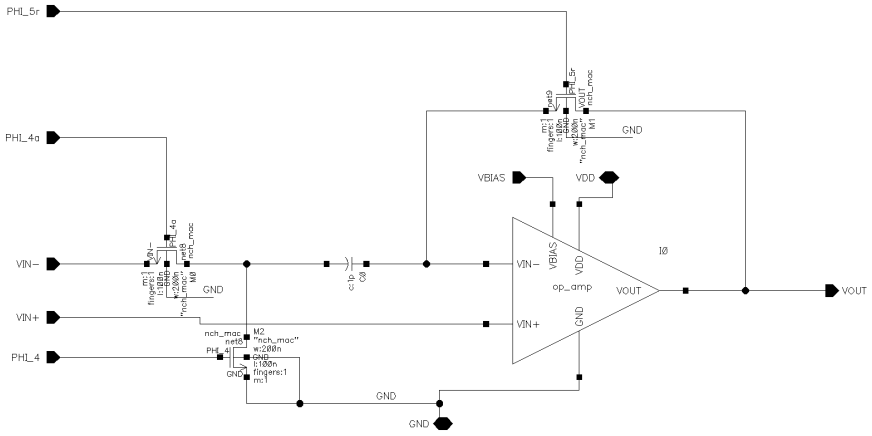

Figure 5: Comparator

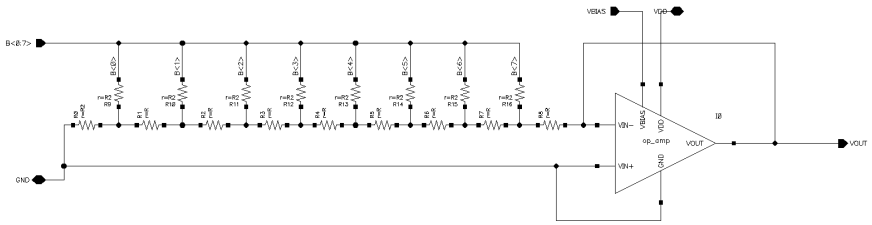

Figure 6: DAC

Schematic: op_amp

The op-amp circuit is based on a design from CMOSedu.com (R. Jacob Baker), and is a commonly used differential pair op-amp. We have tried some different designs, but we have not succeded in any of the other designs. This is not the final version, since it is not fully tested. The dimentrions for the NMOS and PMOS transistors are based on a former thesis that R. Jacob Baker has reffered to in his webpage. For the NMOS and the PMOS, we have used the relation 10/2 and 22/2 respectivly. The final design can

be seen in Figure 7

To test the opamp, we have made a simple testbech that can be seen in section **Schematic: SIM_op_amp**.

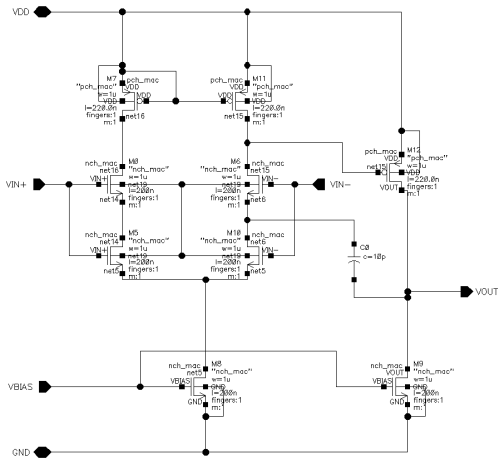

Figure 7: Opamp

4 Test bench

In this section a short overview of the different test-beches for our components is presented.

Schematic: SIM_system

This is a complete system test bench. Here all the different components come together to form the full SAR-ADC architechture. Testing on a system level is nessesary to enshure that the circuit performes according to the interface the circuit provides to the outside world. This test senario is quite hard to set up since many signals have to be timed to each other. The verification of the circuit is also challanging since many signals has to be considerd. In order to manage this test we need to generate a test procedure with the spesified stimuli and check the results to a expected pattern.

Schematic: SIM_sample_hold

To test the sample and hold we need to generate 3 clocks (see timing diagram in figure 3). The output is ideely expected to match the input value and hold

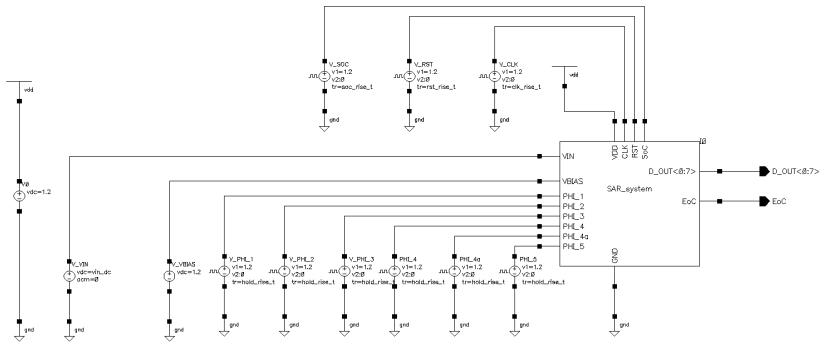

Figure 8: Test bench for SAR-ADC circuit

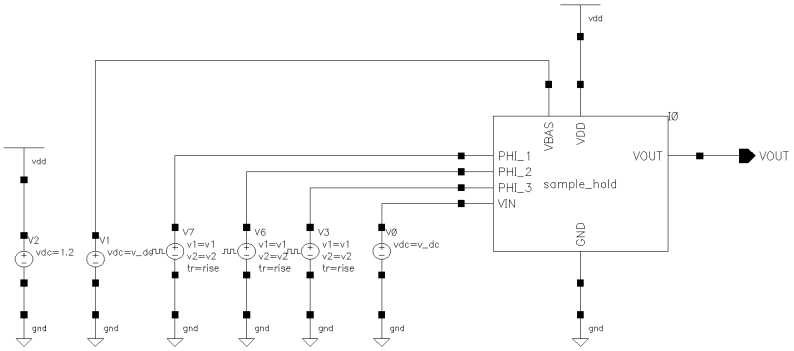

Figure 9: Test bench for sample and hold circuit

it in the phi_3 phase.

Schematic: SIM_comparator

In the test bench for the comparator we need 3 clocks for the timing. When sweeping the input (let's say v-) we expect that at some point (, dependent on v+,) that the comparator will change state.

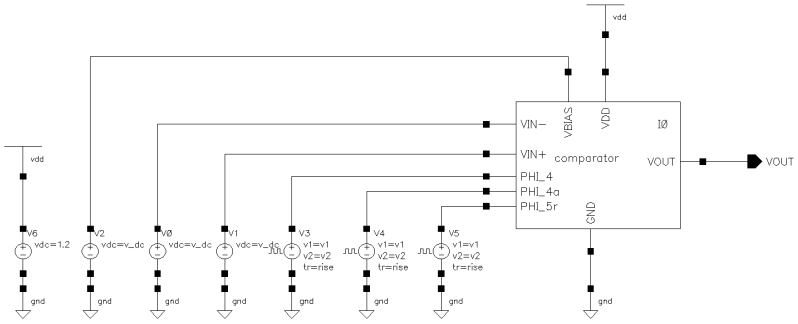

Figure 10: Test bench for comparator circuit

Schematic: SIM_SAR_logic

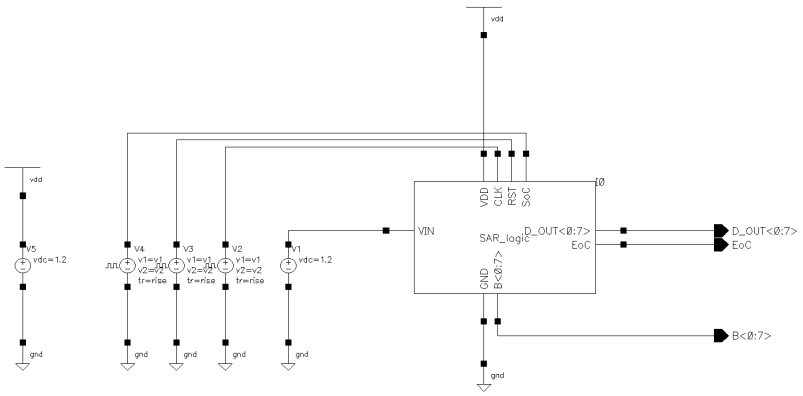

Figure 11: Test bench for SAR-logic circuit

Some of the circuit in the SAR-logic is given but some extra circuitry is needed. In this test bench we want to test that the acquisition state is started when the SoC signal is pulsed. And that we recive a EoC after N-bits clock pulses. We also need to test the reset functionality. The main function of generating the digital output is easy to test since the input signal decideds the value of the current bit.

Schematic: SIM_dac

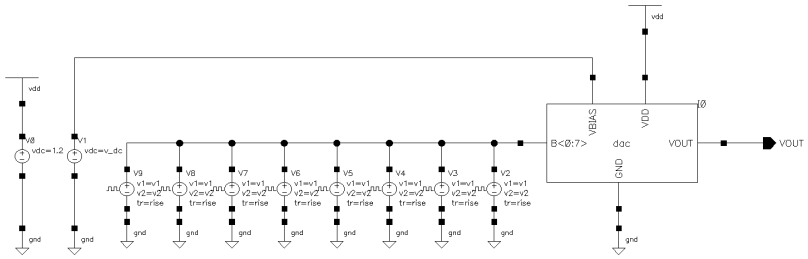

Figure 12: Test bench for DAC circuit

The testbench for the DAC consists of N-bits pulse generators so that we can apply a binary pattern. VOUT should be proportonal to the binary value.

Schematic: SIM_op_amp

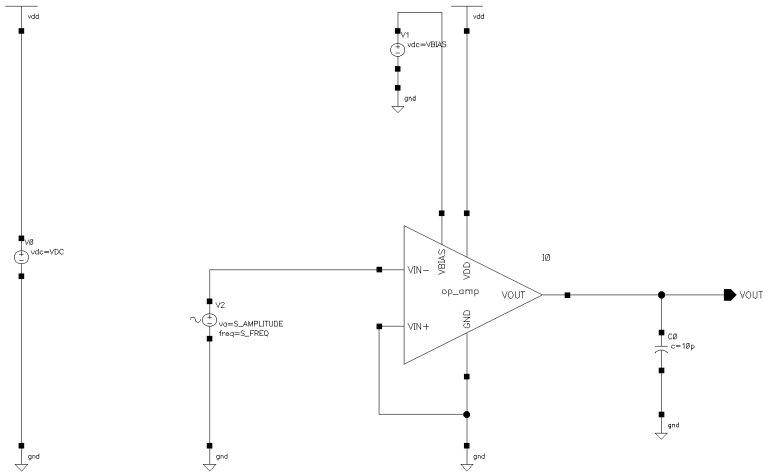

Figure 13: Test bench for op-amp circuit

In our test bench for the opamp we have an open circuit amplifier that expect is going to saturate to either (almost) GND or VDD, if our gain is high enugh. This simulation is a test to check for response and not performence. This simple test gives litle information about the performence of the opamp. To get a better test of the performence of the circuit we need more tests where we test other configurations of the opamp.