A 1.2V rail-to-rail 100MHz amplifier.

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Abstract - This paper presents a compact 3 stage, 1.2V CMOS opamp with rail-to-rail inputs and output, and a 100MHz unity gain frequency and over 80dB of low frequency gain. The design is implemented on a 0.25μ CMOS process and consumes area of 0.01mm^2. The opamp contains a sub threshold-gm rail-to-rail input stage, and is compensated using Miller pole splitting technique, resulting in a unity gain frequency >100MHz and a phase margin >65° while driving a 2pF load capacitor. The compact design provides power consumption of <2mW.

I. Introduction

The design of low–cost mixed mode VLSI system requires compact, power-efficient library of cells. Digital library cells fully benefit from the continuing down-scaling of CMOS processes as well as from the ongoing reduction of supply voltage. In contrast to digital cells, analog library cells often cannot be designed with minimum length components for reasons of gain, offset, etc. Furthermore, a low voltage supply does not necessarily decrease the dissipation of the cell because it often leads to more complex designs, resulting in additional quiescent currents [3]. To obtain compact, low-voltage, power-efficient analog cells, simple library cells with good performance need to be developed.

II. Theory of Operation

In order to achieve large low frequency gain using large voltage supplies, devices can be cascoded to produce large circuit node impedances, resulting in ample low frequency gain. As voltage supplies decrease, available headroom decreases, forcing the cascoded topology to be replaced with cascaded gain stages. As each additional high impedance node adds a low frequency pole, sufficient phase margin at unity gain frequencies becomes a challenging design constraint. For this design despite the limited supply voltage all of the required gain is achieved in 2 gain stages plus an inverting stage. Miller pole splitting was then used to stabilize the design.

A. Placement of second (non-dominant) pole.

Many of the standard texts [5] do an effective job explaining why the dominant pole reduces in frequency due to the Miller capacitor. However explanations for the increase in frequency of the second pole are often buried in complex non-intuitive mathematics, resulting in a poor understanding of the position of the second pole, and the troublesome right half plane zero. For multi stage design, the second Miller stage may be comprised of multiple stages, with multiple poles and zeros; this can make the positioning of the non-dominant pole difficult. This paper will present a simple explanation of the position of the second pole, resulting in a more user friendly method of how to place the second pole at a specified frequency. First, the open loop gain for an amplifier with a Miller capacitor is (equation 1)

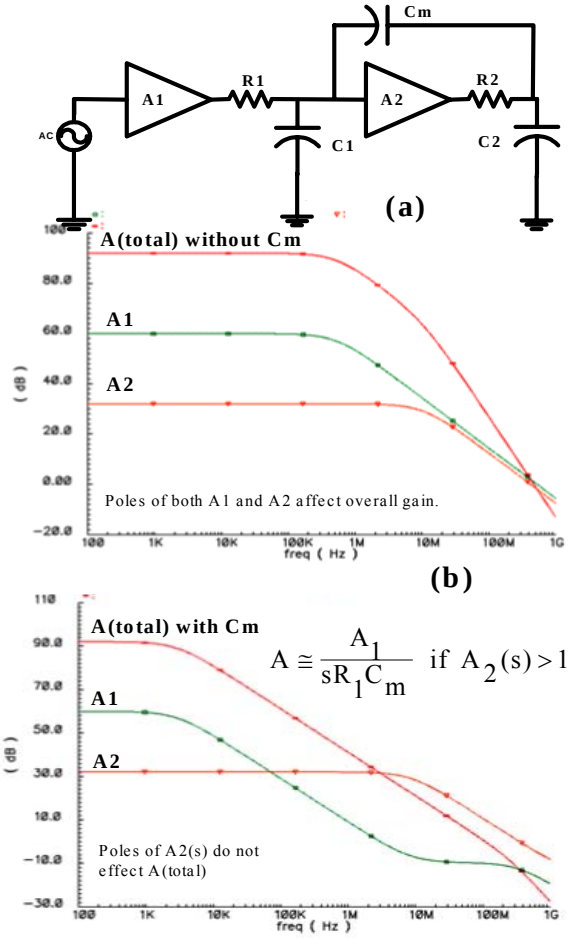

Figure 1: Simulating poles and zeroes using ideal components. (a) A two stage operational amplifier. (b) Stage A_2 amplifier with Miller capacitor. Note that the pole in the second stage does not cause a pole in the over all gain as it causes zero in A_1.

$$A(s) = A_1(s) \cdot A_2(s) \cong \frac{A_1}{1 + sR_1(C_1 + C_m(A_2(s)+1))} \cdot A_2(s) \quad (1)$$

The dominant pole occurs at $\omega_{p1} \cong 1/R_1C_mA_2(s)$ as the effective capacitance seen at the output to the first stage is the Miller capacitor multiplied by a factor of $A_2(s)$. Provided that $A_2(S)>>1$ and $sR_1C_m(A_2(s)+1)>1$ then equation (1) simplifies to

$$A(s) = \frac{A_1}{sR_1C_mA_2(s)} \cdot A_2(s) \cong \frac{A_1}{sR_1C_m} \quad if \ A_2(s) > 1. \quad (2)$$

After the dominant pole (note: as $A_2(S)>>1$ and $S*R_1C_m*1(A_2(S)+1)>1$ then $A_2(S)$ appears in both the dominator and the numerator of equation (1), and hence cancels). The key observation is the overall gain of the system

remains A_1/S, as long as $A_2(s)>1$, as $A_2(s)$ appears in both the numerator and denominator of equation 1. Hence the pole at the second stage output does not cause a pole in the overall system (Figure 1(b)). Additionally, if $A_2(s)>1$ until well above cross over of the amplifier, than the gain of the second stage will not effect the cross over of the system. i.e. An increase in A_2 will cause an increase in both the DC gain of the amplifier, and the effective value of Miller capacitor, and hence the cross over frequency will not be affected. It is only when the second stage crosses its unity gain frequency that the condition $A_2(S)>1$ becomes invalid, and if $A_2(S)<1$ equation 1 reduces to

$$A(s) \cong \frac{A_1}{R_1(C_1+C_m)S} A_2(s) \;\; if \;\; A_2(s)<1 \qquad (3)$$

and hence both the poles of the first stage and the second stage are present in the over all transfer function $A_2(s)=1$ corresponds to the position of the second pole.

Therefore a design strategy of making the unity gain frequency of the second stage to be equal to the allowed position of the second pole can be followed. This design method is particularly effective in multi stage design, where the second stage A_2 (the Miller stage) may be comprised of multiple stages, and hence many poles and zeroes may be present in the second stage. As long as the unity gain of the Miller stage is placed well above the overall crossover cross-over frequency, then equation (2) remains valid, and stable operation can be achieved.

A useful alternative analysis, which will produce the same results, is when a Miller capacitor C_m is wrapped around an inverting amplifier A_m, the effective capacitance seen at the input side is $C_m(1+A_m)$ and the capacitance at the output stage is $C_m(1+1/A_m)$ [5]. When considering the capacitance at the output node it is usual to ignore the $1/A_m$ term (as A_m is assumed to be big), and approximate the total capacitance as C_m. However, after the unity gain frequency of the Miller gain stage the gain of the stage is less than 1 and hence the $1/A_m$ term becomes the dominant term. As the Miller gain can be approximated as A_m/s (assuming it has only one pole) the capacitance seen at the output is $C_m(1+s/A_m)\sim C_mS/A_m$, which will produce a second pole in the transfer function at the position of the unity gain of the second stage.

B. Feed forward zero.

With any capacitor which is connected from output to input of an amplification stage, there is an alternative path for the signal from input to output of the stage, and which means there is potentially a zero in the system transfer function. If the gain stage is an inverting stage (such as a miller amplifier) then the zero will be in the right half plane which will cause degeneration of the phase margin. When the Miller gain stage is made up of a single stage, the position of the zero can be approximated as $s_z = +g_m/(C_{Miller}+C_{load})$ [6] where the g_m is the transconductance of the miller stage. The zero is typically close to the cross over frequency of the Miller stage, as it represents the frequency at which the gain path from input to output is greater through the capacitor than through the gain stage. As discussed already, the second stage will have a unity gain frequency well above the unity gain of the overall system, resulting in the zero being placed above the cross over frequency. However the effects on phase of the zero can span a decade in frequency, hence to reduce the effects of the zero a series resistor will be added in order to change the position of the zero to $w_z = +1/(1/g_m - Rc)\cdot(C_{Miller}+C_{load})$. [6]

C. Practical Design targets and implications.

The target cross over frequency for the overall system is 100MHz. As discussed the Miller amplification stage will require a cross over frequency well above this number. As will be seen in section III, increasing the cross over of the final stage (which will be driving a 2pF capacitor), will require a significant amount of quiescent current. A cross over of 400MHz will be targeted for the cross over of the Miller stage, which is well above the unity gain of the system.

As discussed earlier, the gain of the Miller stage does not affect the cross over frequency of the system. However if the gain of the Miller stage is very large then the effective value of the Miller capacitance seen at the output to the first stage may be large enough to slew the first stage. For this reason, it the gain of the miller stage will be designed to have a gain of around 30dB, which is large enough to place the dominant node at the output of the first stage without slewing it.

An additional benefit of the wide band Miller gain is realized when considering the required output swing of the first stage. If the output of the amplifier is required to swing from rail-to-rail, then the required swing at the output of the first stage is equal to the output swing divided by the gain of the second stage. As the second stage will be designed to have a gain of at least 30dB (31 numeric) over the entire frequency range of the amplifier, then the maximum required voltage swing at the output of the first stage will be $V_{DD}/31 \cong 40mV$ (@1.2V). As the first stage only has to support a small voltage swing at its output, the output stage of the first stage can be easily cascoded, which results in large DC gain, and hence the low frequency design specs can be meet with only 2 gain stages (plus an additional buffer stage).

III. Design Implementation

A. Input stage.

The purpose of the input stage is to provide differential amplification of the input signal, from rail-to-rail. To achieve this, a folded cascode input stage will be used.

When the input common mode is close to ground the P devices act as the input stage, and when the input common mode is close to V_{DD} the N stage act as the input stage. As discussed in [1] a standard difficulty faced with low supply input stages is that in the center of the common mode swing, it is difficult to have either input pair turned on, as both pairs require a V_{TH} and $2V_{Dsat}$ of headroom. As the nominal V_{TH} for devices on this process is 0.55/0.6V for N/P devices respectively, this means that it will be impossible to achieve rail-to-rail operation with input devices operating in their standard saturation region and a 1.2V supply. Of the various techniques used to solve this problem, operating the input devices 50mV into the sub-threshold region was chosen, and hence effectively reducing the required headroom, as the V_{GS}'s of the input devices no longer need to be greater than V_{TH}. Additionally the current mirrors for each set of stages were designed to have a

very low V_{Dsat} of 50mV. The down side of this is that the output impedance of the current mirror will be low, and the mirroring ratio may be inaccurate. Both sets of input devices were operated with 20μA tail currents. The g_m for devices acting in their sub-threshold is $g_m=I_D/(\zeta V_T)$ resulting in a transconductance of 140μ. As discussed earlier, the output of the first stage needs to support a voltage swing of only 40mV, resulting in ample headroom for cascoding. The result is that the output impedance of the first stage is large, resulting in large low frequency gain.

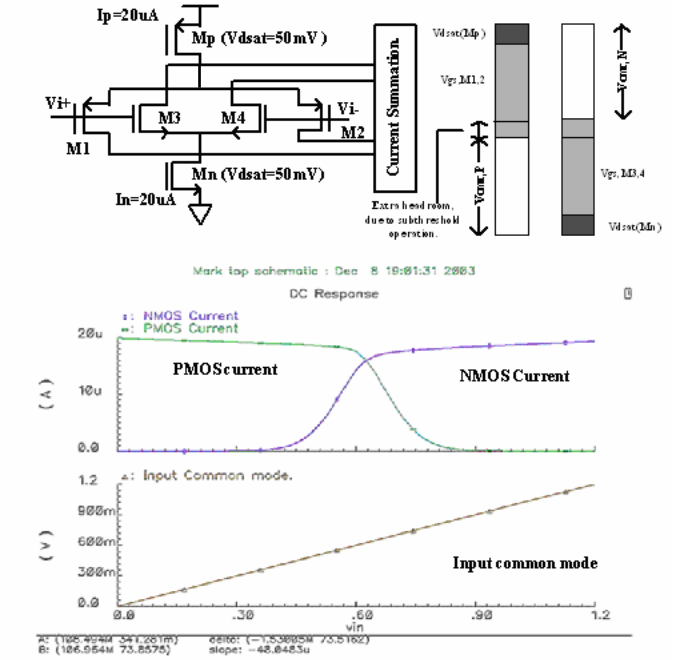

Figure 2: (a) Description of how to fit PMOS pair and NMOS pair into low voltage headroom. (b) shows that over the entire common mode range there is always current in either the NMOS pair or PMOS pair

B. *Buffering stage.*

As discussed already, because of the limited output swing of the first stage, high gain can be achieved with the first stage, making the overall gain spec relatively easy to achieve with just two stages. The Miller capacitor that will be used requires an inverting stage across it and, as will be seen the, the output stage will be non-inverting, meaning an additional stage needs to be added to invert the signal. This stage will require a wide bandwidth, as it is part of the Miller amplifier, which needs to have a unity gain frequency well above the cross over of the overall amplifier. Additionally it is required to have a low gain, as it will contribute to A_2, which will already have more than enough gain to meet the spec of 30dB. For this reason a common source PMOS input with a diode connected NMOS load was chosen. The PMOS input will set the output common mode of the first stage to be roughly a V_{TH} below supply. As the PMOS V_{TH} is roughly equal 0.6V, when the supply voltage is at its lowest of 1.2V the common mode output of the first stage will be around V_{DD}-V_{TH}(P)≅0.6. Hence the DC output of the first stage will be approximately $V_{DD}/2$ when V_{DD} is at its lowest, which gives optimum headroom for the cascade stages of the first stage amplifier. The diode connected NMOS load, will provided a low impedance load, hence the second stage will provide a predictable low gain, which will be set to the ratio of the 2 g_ms.

C. *Output stage.*

The output stage needs to drive a 2pF capacitor, with a bandwidth of 400MHz, and low frequency gain limited to around 30dB. Our first effort of an output stage was a common source amplifier. However, consider the following analysis. The maximum output current will be $I_{Max}=C_{Load}\times dV/dt$. For a required output swing of 1V at a 100MHz, this corresponds to $V_{out}=1\times\sin\omega t$, $dV_{out}/dt=w\times\cos\omega t$, which has a maximum value of ω. Therefore $I_{Max}=C_{Load}\times w$ (with 1V output swing) $=2pF\times 2\pi\times 100MHz=1.25mA$. Hence the maximum current that this stage will be required to provide is 1.25mA. This means if the output is a common source amplifier, a standing current of at least 1.25mA will be required in order to avoid slewing. Instead, a low voltage class AB amplifier will be used, such as described in [4]. A class AB amplifier can output positive and negative currents much greater than its quiescent current, breaking the relationship between slew limit and quiescent current.

In this implementation, it is also required that the output stage will have a unity gain frequency well above the system cross over frequency. In order to achieve a cross over of 400MHz for the output stage, $G_m/C=2\pi\times 400MHz$ is needed, and $G_m=2\pi\times 400MHz\times 2pF=3.7mS$ (where G_m refers to net transconductance of the output stage). It was also decided to set the Vdsat of the output transistors to 200mV.

$$G_m=(g_{mn}+g_{mp})\cong 2g_{m_{n,p}}=4\times\frac{I_D}{V_{GS}-V_{TH}}=4\times\frac{I_D}{200mV}=3.7mS$$

$$I_D=0.25\times G_m\times(V_{GS}-V_{TH})=0.25\times 3.7mS\times 200mV=185\mu A$$

In simulation it was found that current needed to be tweaked up to 320μA in order to achieve the required value of the overall G_m of the output stage.

The equation $V_{Dsat}=\sqrt{2I_D/(\mu_n C_{OX}(W/L))}$ was used to work out the appropriate sizes for the N and P devices. As discussed in Section I, if there is too much low frequency gain in the Miller stage then this may have slewing implications for the first stage. For this reason, minimum length devices were used for the output transistors.

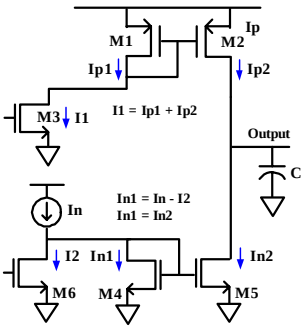

Figure 3: Class AB output stage

The principle of operation is as follows; Transistors M3 and M6 are the same size with the same gate connection, hence they have the same current. When the gate voltage of M3 increases, I1 increases, which will cause an increase in the output PMOS current, which will cause the output voltage to rise. Additionally, the same increase in input voltage will cause current I2 to increase. As In is fixed, the current in

M4 and hence the output NMOS current will decrease. This will also cause the output to rise. The inverse happens when the input goes down and output goes down.

The output can source or sink current much greater the value of quiescent current, resulting in better power performance for the same slew rate than a common source amplifier. (A common source amplifier can only provide current greater than the quiescent current in one direction.) This is important as 2pF capacitor is being driven. However this circuit does have a slew limit in the negative direction. The maximum current that the transistor M5 can sink is equal to In*(width of M5/width of M4). This can easily be set to be much larger than 1.25mA. (The number we've calculated already)

D. Biasing stages.

As can be seen in the schematic and the layout, around half of the design is taken up with the biasing circuit. The purpose of the biasing circuit is to provide the cascode and bias voltages for the various amplifier legs, all generated from a single 10μA ideal current source. The cascode voltages can be generated by sinking/sourcing a 10μA reference current into a diode connected NMOS/PMOS device. The W/L of this device will be smaller than all the other devices, and hence has bigger V_{Dsat} ($V_{Dsat} \propto \sqrt{1/(W/L)}$).

Capacitors were also added in order to reduce the high frequency signals that were coupled on to the bias lines. It was found in the transient simulations, that without the capacitors, the bias lines are very noisy, resulting in noisy current being mirrored around the design.

IV. Results and Measurements

A. AC response.

In Figure 5(a), one method of measuring the AC performance is presented. In this configuration, the amplifier is open loop, and the AC small signal is applied at the input. The input DC offset needs to be tweaked in simulation to try to approximate a reasonable DC operating point. This method is cumbersome as it requires tweaking and the circuit will almost certainly have AC characteristics measured at the incorrect DC operating point.

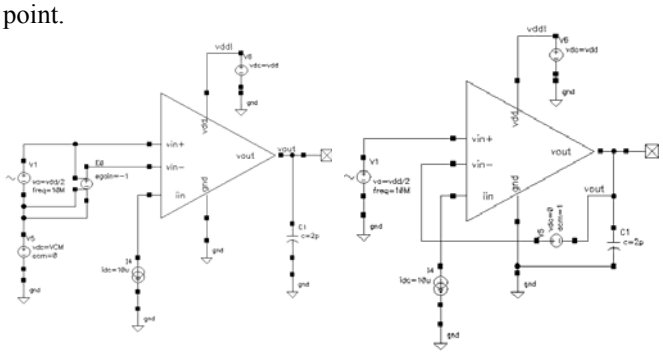

Figure 5: AC response testing circuit (a) one method (b) improved method

In Figure 5(b), a far superior method is presented. The AC source (DC value = 0) is placed in the feedback loop. When the simulator calculates the DC operating point, the AC source looks like a short circuit, and the simulator will calculate the correct DC operating point for unity gain configuration. The

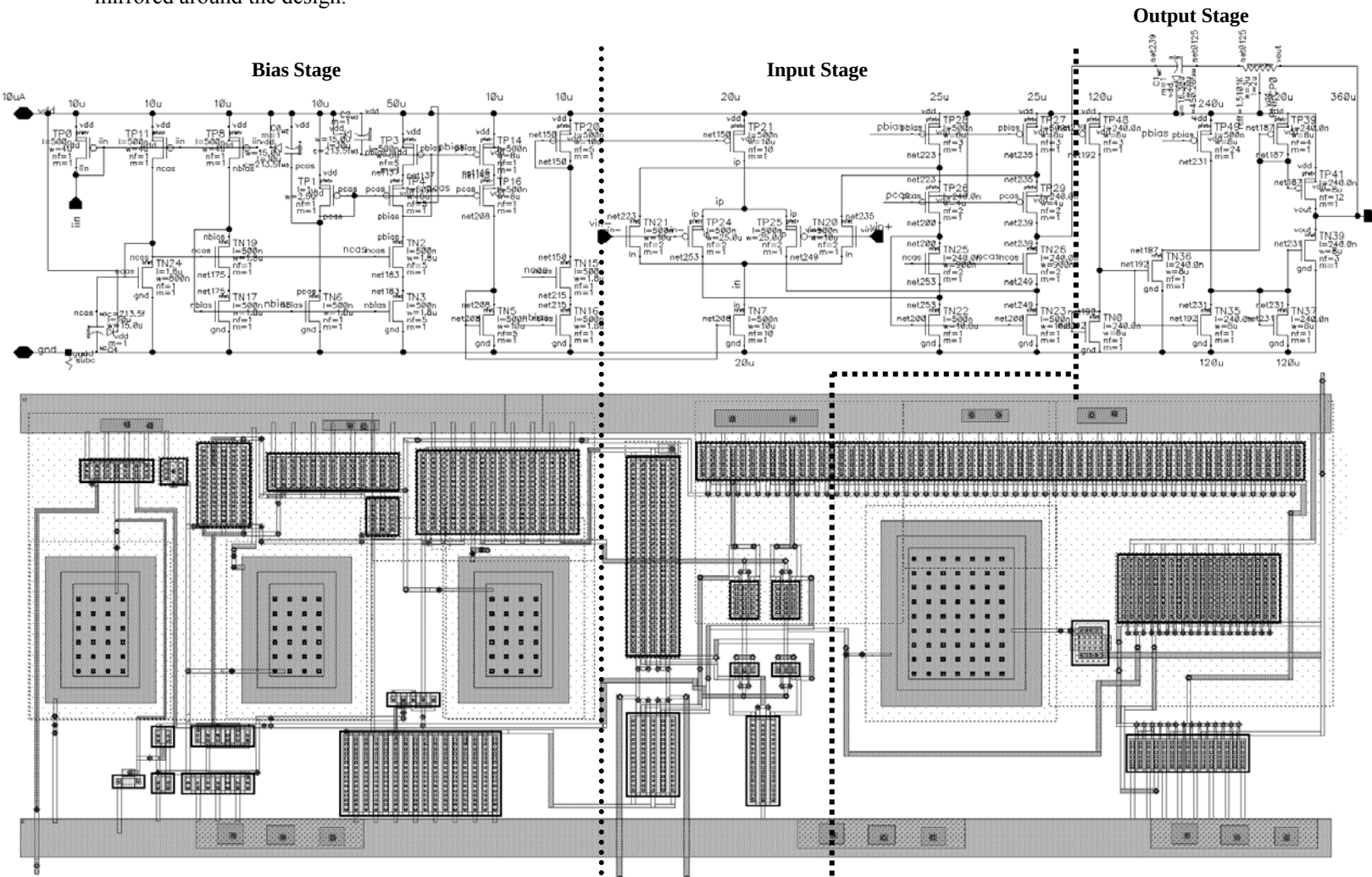

Figure 4: (a) top, schematic of the opamp (b) bottom, layout of the opamp

AC gain can be found as the AC signal at the output over the AC signal at the negative input.

In figure 6, a Bode and phase plot for 1.2V 27°C is shown. As can be seen, the open loop gain is above 85dB, and a phase margin is 72.9°. Also plotted is closed loop gain (unity gain configuration) which is 0dB, and which exhibits some peaking at the crossover frequency. The phases' of the two plots are a 180° apart. This is because the open loop gain is from the negative input to the output and the closed loop gain is from the positive input to the output.

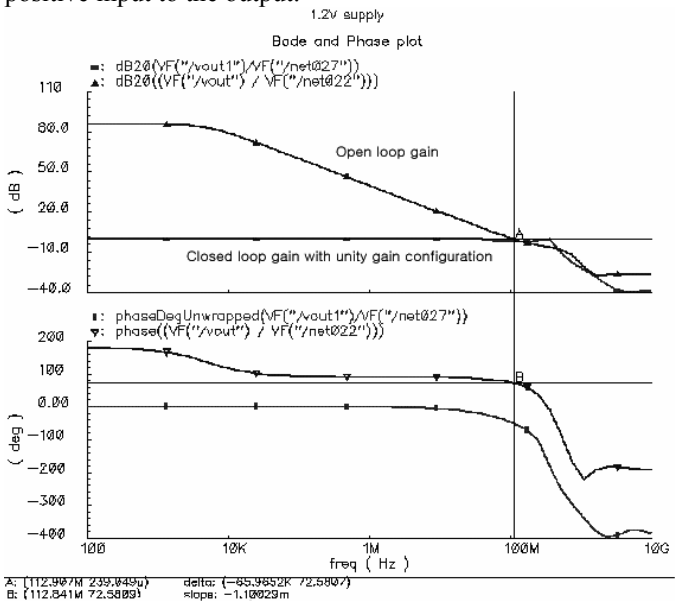

Figure 6: Bode and phase plot of OPAMP at 1.2V power supply

B. *Transient response.*

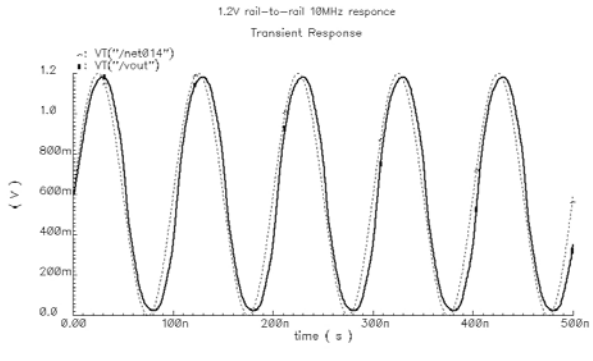

Figure 7(a): Input and output signals for transient analysis

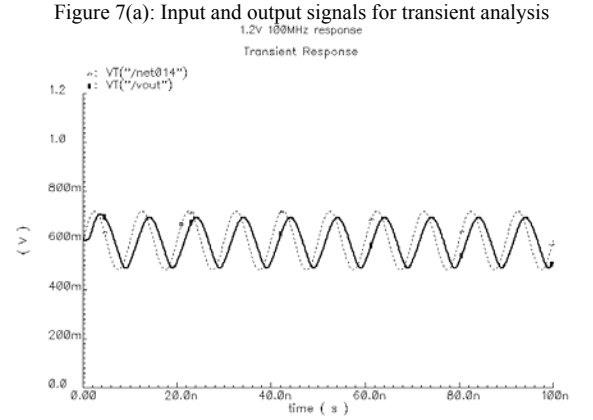

Figure 7(b): Output tracks input even for 100MHz signal due to peaking near crossover

A transient simulation of the amplifier in unity gain configuration with the swing at the input rail-to-rail is the most insightful simulation presented (Figure 7(a)), because it exercises the amplifier over the entire common mode range and shows the amplifier is not slewing and is exhibiting reasonable linear behavior. The excellent transient performance of this amplifier is due to the output class AB stage. When an amplifier with similar gain and phase performance, but which has a common source output stage, is tested in the similar manner the slewing in one direction fully distorts the output. This demonstrates the need for a class AB output.

In general, an amplifier will not be used close to its unity gain frequency because in order for negative feedback to effectively linearize the transfer function, the open loop gain needs to be very large. In figure 7(a), the amplifier is exercised at 10MHz, which is a decade below its unity gain frequency, and hence has a gain of 10. When the overall transfer function is analyzed, a 10% error is expected, which can be seen in the simulated result.

$H(s)=A(s)/(1+A(s))$ @10MHz, $A(s)\cong 10$, $H(10Mhz)\cong 10/11\cong 0.909$

C. *Step response.*

In Figure 8(a), a step from ground to V_{DD} is applied at the input with unity feedback configuration. As was measured, the amplifier's slew rate is 52V/μs. In general, a step response contains frequency components well outside the range of the amplifier. In Figure 8(b), some ringing is observed, because when the amplifier slews, the output stage is tilted over completely to one side, and the amplifier is no longer effectively in a feedback loop. When the amplifier stops slewing, all the signal nodes inside the amplifier will no longer be at their nominal quiescent DC operating points and will take a little time to recover.

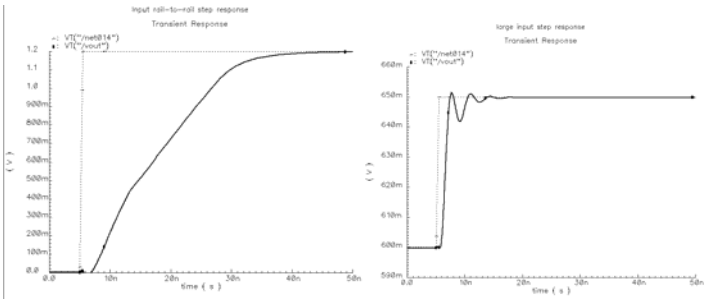

Figure 8(a): step response of unity gain feedback configuration with rail-to-rail step input (b) step response of unity gain feedback configuration with 50mV step input

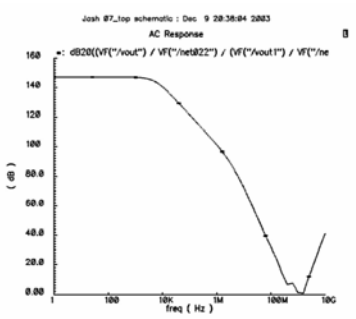

Figure 9: common mode rejection ratio

D. *Common Mode Rejection Ratio.*

In order to simulate common mode rejection, the amplifier is placed in unity gain feedback with an ideal buffer in series with an AC source of 1V in the feedback path. Additionally, a 1V AC source is placed on the

positive input. When the simulator calculates DC operating point, the buffer in the feedback path has no effect, hence the correct DC operating value for unity gain feedback will be calculated. When the simulator sweeps the frequency, there will be a 1V AC source on both the positive and negative inputs and hence the AC signal at the output will be the common mode gain. The previously calculated gain (Figure 9) can be divided by this gain to give the CMRR. The common mode rejection ratio was found to be 146dB at low frequency, and reduces to 0dB at 1GHz.

E. Power Supply Rejection Ratio.

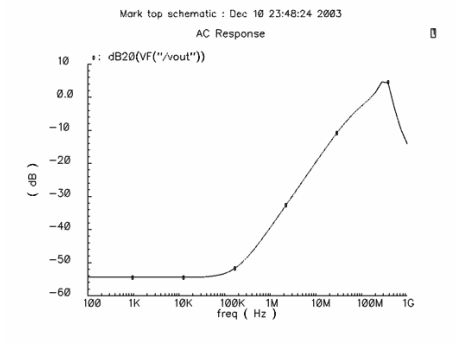

Figure 10: power supply rejection ratio

PSRR was measured by placing a 1V AC signal on the power supply where the amplifier is in unity gain feedback configuration. PSRR is equal to the ratio of the AC signal at the output node to the AC signal on V_{DD}. At low frequencies a result of -54.5dB was measured. At low frequency, the gain of the amplifier will act to force the output voltage to be equal to the positive input voltages (which will have an AC value of 0); hence a low PSRR is expected. At high frequency, the gain of the amplifier reduces; hence the amplifier can no longer effectively force the output and input voltages to be equal, and a PSRR of 0dB is measured at 160MHz.

F. Table of results.

	Supply	Gain	Unity Gain (MHz)	Phase Margin	Power (mW)
Target	1.2V	85dB+	100.0	65.0°	<2mW
Our Design Result	1.2V 27°C	85.6dB	108.5	70.4°	1.224
	1.2V 85°C	85.5dB	105.7	63.5°	1.234
	1.5V 27°C	90.1dB	132.7	69.0°	1.645
	1.5V 85°C	89.7dB	118.1	64.2°	1.650
	1.14V 27°C	85.7dB	113.6	72.9°	1.139
	1.14V 85°C	83.2dB	98.7	64.2°	1.152
	1.575V 27°C	90.5dB	137.6	69.0°	1.754
	1.575V 85°C	90.1dB	120.8	63.6°	1.757

All measurements were taken with input common mode of $V_{DD}/2$ and the amplifier tied in unity gain configuration. At high temperatures, the phase margin was slightly less than 65°.

G. Table of comparison.

parameter	Presented Amplifier	[7]	[8]	Unit
Supply voltage	1.2	1.5	1	V
Gain	85	65	>100	dB
Unity gain frequency	100	0.3	1.8	MHz
Power consumption	1.2	0.23	0.41	mW
PSRR	54.5	75	107.46	dB

As can be seen in the table, this amplifier performs well in comparison with results from some published papers.

V. Conclusions

A multi stage compact operational amplifier with rail-to-rail input and output ranges has been presented. The opamp contains a rail-to-rail input stage that operates in the sub-threshold region, with a class AB output. The class AB output enables non-slewing transient behavior even at high frequency. The amplifier operates with ultra low supply of 1.2V with a miller compensation providing stability. Its unity gain frequency is 100MHz, even in the presence of a 2pF load capacitor. The amplifier's large 85dB of low frequency gain demonstrates that more than 2 gain stages is not required for high gain even in the presence of low voltage supply. The amplifier consumes area of 0.01mm^2, and nominal power consumption of 1.2mW.

VI. References

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VII. Appendix

Our simulation file is stored in the following folder.
/afs/engin.umich.edu/class/f03/eecs413/group2/
Our key Cadence schematic Library/Cell is in Josh/08_layout_all.