Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)

1. Introduction

Data converters are one of the fundamental building blocks in integrated circuit design. Their purpose is to interface the analog and digital domains. Data converters can be realized in many different ways and may be found in a wide variety of applications. One often used ADC topology is the SAR ADC, shown in Figure 1. This topology uses a Digital-to-Analog converter (DAC), Sample-and-Hold circuit, Comparator and some digital circuits to convert an analog signal into a digital form of representation.

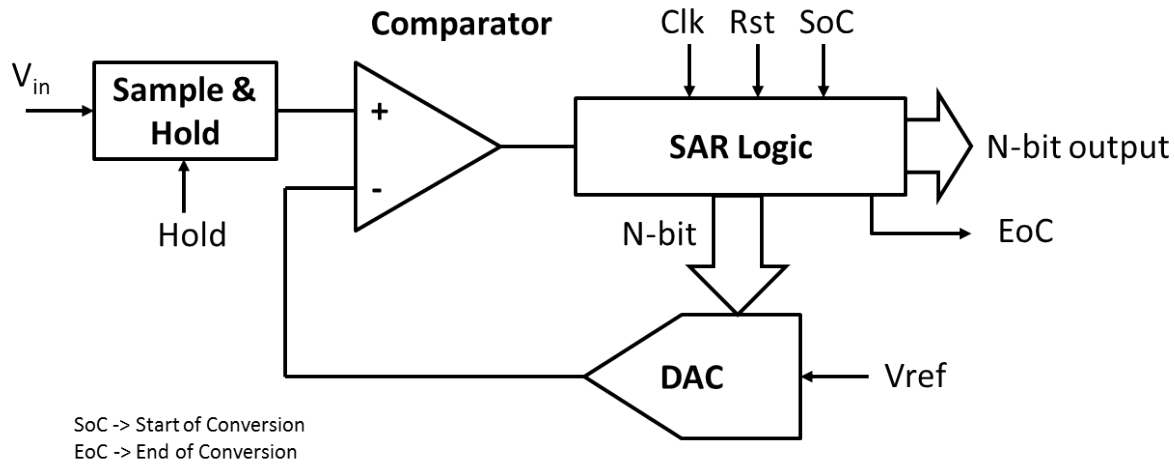

Figure 1: SAR ADC

2. Project requirements

The main purpose of this project is to design and simulate a SAR ADC, which meets the specifications outlined in section 3. Other than these specifications, the students have the freedom to choose the methods used to implement the system. The students can work in groups of two as the workload in this project is intended for two students. The group members must read this document completely and carefully assess the task. The work must be distributed almost equally among the members of the group and the same must be mentioned in the final report. PhD students have a slightly different requirements, which are explicitly mentioned.

2.1. Practical tasks

1. A full schematic for the system and its sub-modules must be drawn. Separate symbol for all sub-modules must be made. The top-level representation should include these sub-modules in a well-organized hierarchical design.
2. For all modules qualified through schematics simulations, a full physical layout should be made. The sub-modules must be combined into a well-organized layout of the entire system. It is important to identify and focus the effort on the most critical sub-modules that are most likely to limit the overall system performance.

3. When combining both analog and digital electronics on a single small CMOS die, the different challenges and potential noise sources must be identified. Based on the assessment of the potential risks, the necessary mitigations must be implemented. The strategies used should be explained in the final report.
4. Design Rule Checking (DRC) and Layout Versus Schematic (LVS) for sub-modules and the total system must be completed. These checks have to be free of errors. The reports should be enclosed in the final report.
5. When the layout is ready for sub-modules and system, back annotation of all parasitic components into the schematic must be performed. The full schematic including back annotated parasitic elements must be simulated and the results compared to the simulation without parasitic elements. Comment and explain the results in the final report.

3. Specifications

3.1. SAR ADC

1. Input sampling rate: 1 M samples/s
2. Output resolution: 8 bits (12 bits for PhD students) parallel
3. Supply voltage: V_{DD} = 1.2 V, V_{SS} = 0 V
4. No missing codes
5. Monotonic

3.2. DAC

1. Sampling rate: 8 M samples/s
2. Resolution: 8 bits (12 bits for PhD students)
3. Supply voltage: V_{DD} = 1.2 V, V_{SS} = 0 V
4. DNL < ±0.5 LSB
5. INL < ±0.5 LSB
6. $V_{out(p\_p)} \geq 0.6$ V
7. C_{load} = 50 fF

3.3. Comparator

1. Delay ≤ 0.5 clock cycle
2. Supply voltage: V_{DD} = 1.2 V, V_{SS} = 0 V
3. Offset < 0.5 LSB
4. Gain > $V_{DD}/(V_{ref}/2^n)$
5. C_{load} = 50 fF

4. Assignments

4.1. Task 1: Design a test bench for the DAC and SAR ADC

Make a suitable test bench for the DAC. Write a small report of about 2 pages and include the following:

(a) Typical SAR ADC architecture description with a block diagram and waveforms

(b) Compare SAR ADC architecture with at least three other ADC architectures (using just a tabular column. No textual explanation is required).

4.2. Task 2: DAC design

Study different types of DAC and implement a DAC of your choice. Explain the reason for selecting a particular type in your report.

There are several important specifications that are required for choosing a DAC. Identify these specifications and include those values observed in your DAC simulations in your final report.

4.3. Task 3: Implementation of a Sample & Hold, Comparator and SAR logic

Implement a Sample & Hold circuit based on the ADC specifications mentioned in section 3. Similarly, implement a comparator based on the specifications mentioned in section 3. Use the ideal component available for SAR logic.

4.4. Task 4: Implementation of DAC into SAR ADC

Implement your DAC design into the SAR ADC topology. Design all the required input and output signal lines on the chip, so that your device can be interfaced with the external circuit to build a useful circuit.

Assign a ramp up signal to the ADC input and verify that you get a corresponding digital values at the ADC output. Include these observations in the report.

Identify various specifications that you think are relevant to the ADC. Run the simulations and include the results in the report.

Test your circuit with different types of input signals.

5. Report requirements

The report should be written using LATEX, Word or a similar word processor and must document all the different phases of the project. Plots of schematics, layout and simulated results for sub-modules and total system must be included in additions to LVS reports. You must also explain and justify the different choices made for matching, dimensioning/ implementation of active/passive devices and noise mitigating techniques. The organization of the project and the distribution of responsibility within the group must also be included. In addition the location of all design files should be listed. Please remember that the report must be considered a stand-alone document that should give the reader a complete view of what you have done. This is important to make sure that the entire picture is included in the final assessment and grading of the project.

6. Assessment

This project counts 40% towards the final grade.

7. Milestones and deadline

To ensure a good progress during the project period and that all groups completes the project within the deadline certain milestones must be met. The students are responsible to meet the deadlines and to get the necessary approval. The milestones are:

11.03.2016 - A short description of one to two pages on how you understand this assignment and how you plan to solve it. Also, include the test input and predicted waveforms at different points and the output of the ADC.

25.03.2016 - The complete system test bench should be completed.

29.04.2016 - Design and simulations of the entire circuit should be finalized for both schematic and layout. The system performance should be demonstrated with simulations and approved by the lab teacher.

The project should be completed and the final report submitted before Monday, **09.05.2016, 5 pm**.

8. Resources

Application notes, White papers & Data sheets

(a) www.maximintegrated.com

(b) www.ti.com

(c) www.analog.com

Books

(a) Analysis and Design of Analog Integrated Circuits, 5th Edition by Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer

(b) Design of Analog CMOS Integrated Circuits by Behzad Razavi

(c) CMOS Analog Circuit Design, 3rd Edition by Phillip E. Allen, Douglas R. Holberg

(d) Data Converters by Franco Maloberti

Good Luck :)