INF4420 - Project description

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Introduction

In this project we are going to design a Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC). The project is a part of the cource INF-4420 at the University of Oslo, department of Informatics.

The purpose of data converting is to interface the analog to the digital diomain, which is essential in almost every circuit.

The SAR-ADC is buildt up by several modules, including sample-and-hold (S&H), comparator and digital to analog converter. It is our task to design each of these modules, except the digital logic (the module is given by the cource instructor) for the system. The project covers all aspects of designing and implementing the SAR-ADC system, going from schematics to a circuit implemented in CMOS technology. There are given some minimum requirements that we must meet. The different modules of the system is to be simulated in Virtuoso by Cadence (schematics) and later simulated in layout. The parasitics is also going to be included in the simulation in Virtuoso.

Since we are creating layout we must also make the circuit comply with the schematics by running Layout-vs-Schematics (LVS), Design-rule-check (DRC) and antenna tests. There are several other considerations in order to make a good layout. The task is therefore to identify theese challenges and find solutions to mitigate the situation. There are also several noise sources in the system whitch must be handled.

The system consists of sevral parts, mainly:

- Sample & hold

- Comparator
- Digital to Analog Converter
- Digital SAR logic

The task is given in such a way that we are free to choose the implementation of the different modules as long as it meet the requirements. We must therefore research circuits that can perform these tasks and meet the specifications.

Project plan

The assignment is divided into subtasks where the different parts of the design, is to be designed.

The order is:

- Design testbench
- DAC design
- Implementation of S&H, Comparator and SAR logic
- Implementation of DAC into SAR-ADC

We assume that we are supposed to create and simulate schematics (etc.) and create layout for each task consecutively (as opposed to first creating all the schematics and then all layout).

The final deadline is: 09.05.2016, 5pm.

Execution

Task1: Design testbench

The purpose of this task is to create a simulation enviroment for testing our solution. This setup should encourage testdriven development so we can spot implementation flaws early. In this testbench we want to identify correctnes and performance (and limitations and stability).

To create a suitable test enviroment we are going to create multiple (*simple*) test benches to test the different modules. We are also going to create

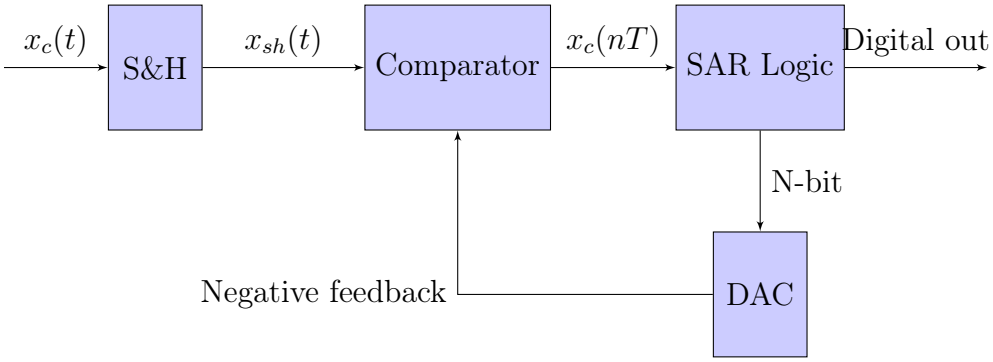

Figure 1: Block diagram

a high-level testbench to simulate the complete system. The overall block diagram is shown in Figure 1. For a test input of 0.5V we expect a behavior as depicted in the waveform-drawing in Figure 2.

The SAR ADC architecture is compared with three other architectures, as seen in Table 1.

	SAR	Flash	Sigma-Delta	Integrating
Conversion speed	Low-medium	Fast	Low	Depending on resolution and clock
Sampling rate	Nyquist	Nyquist	Oversampling	Nyquist
Area	Low	High	Medium	Low

Table 1: Comparation of different ADCs

Task2: DAC design

In this task, we will study different DAC designs and make a schematic in Cadence. When designing DACs, there are several importaint specifications that needs to be considered. It is our task to identify different specifications to fit with our requirements.

Task3: S&H, Comparator, SAR logic

There are many different approces to create S&H, comparator and SAR logic. Also here we need to investigate different designes.

Task4: Implementation of DAC into SAR-ADC

In this task the DAC is to be integrated into the SAR system.

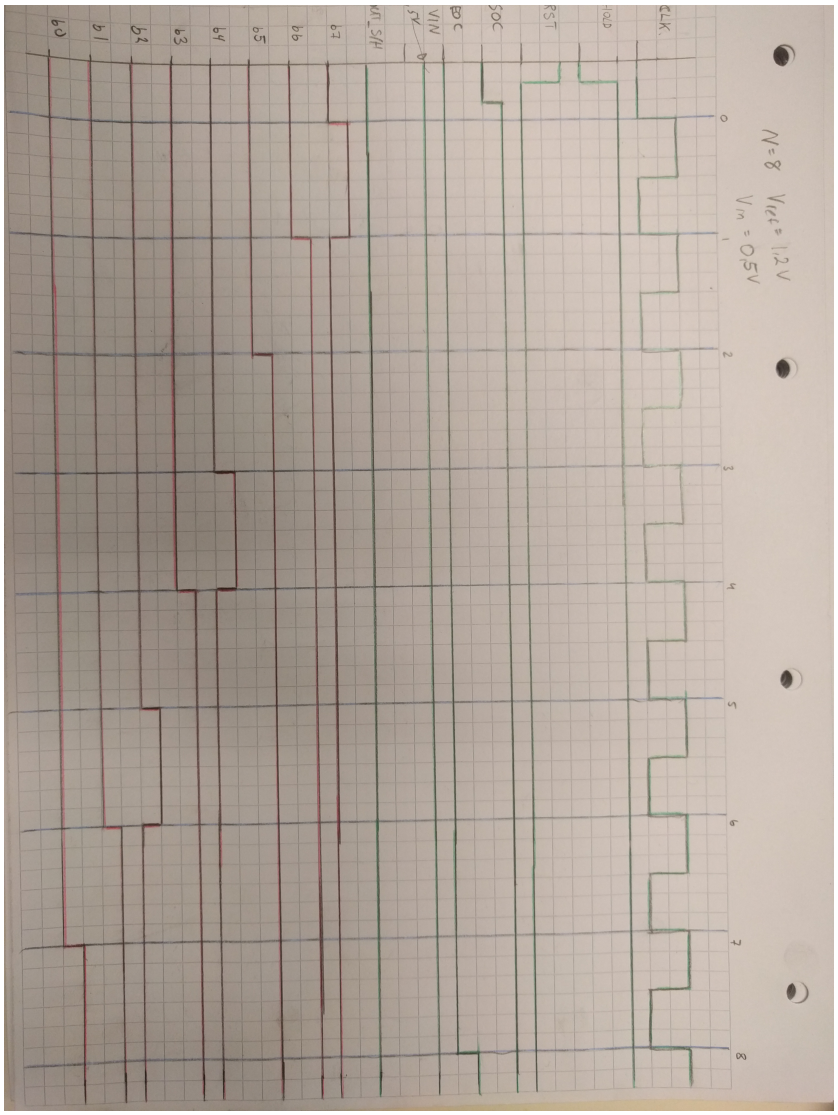

Figure 2: Timing diagram