UiO : Institutt for informatikk
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Successive Approximation Register (SAR) Analog to Digital Converter (ADC)

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Content

- Introduction
- Requirements
- Solution
- Conclusion

Introduction
SAR ADC

- Sample-and-Hold
- Comparator
- Digital-to-Analog Converter
- SAR Logic

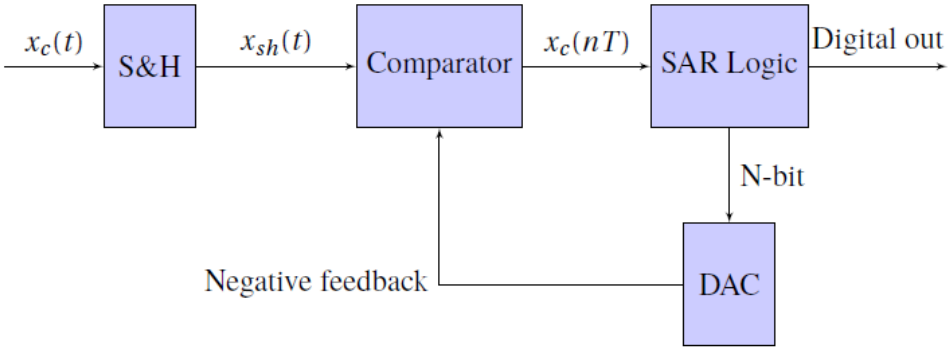

Figure 1.1: Block diagram

Introduction
SAR ADC

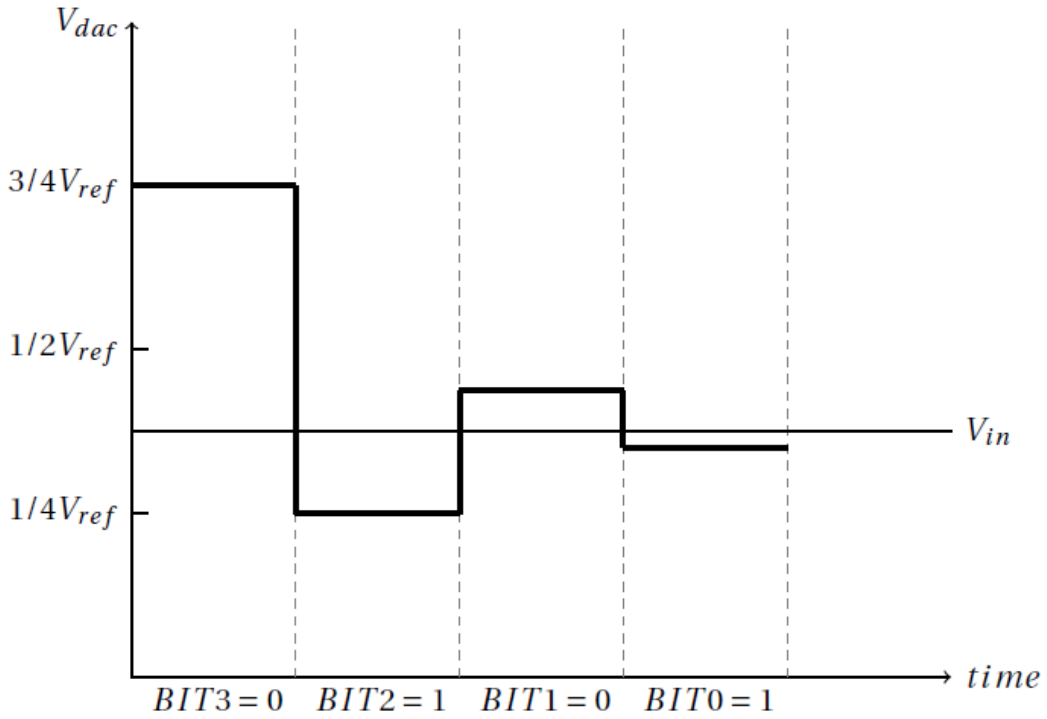

Figure 1.2: Example of 4-bit SAR ADC conversion

Introduction
Sample-and-Hold

- Snatches a value of a analog signal and holds it constant
- Φ1:on
  →C charges to Vin
- Φ1:off
  → Vout = Vin

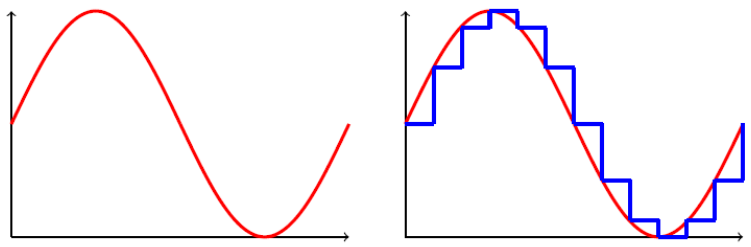

Figure 1.3: Input signal and sampled signal

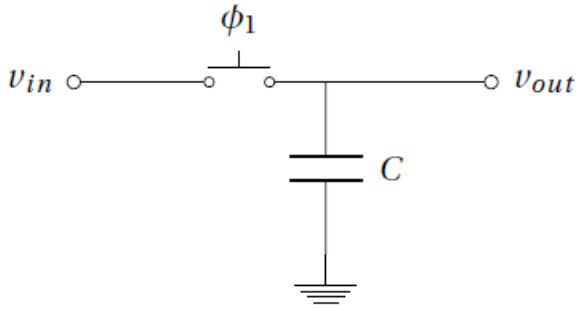

Figure 1.4: Sample and Hold

Introduction
Comparator

- Compares two input signals
- Outputs logic high or low

Introduction

Digital-to-Analog Converter

- R-2R ladder

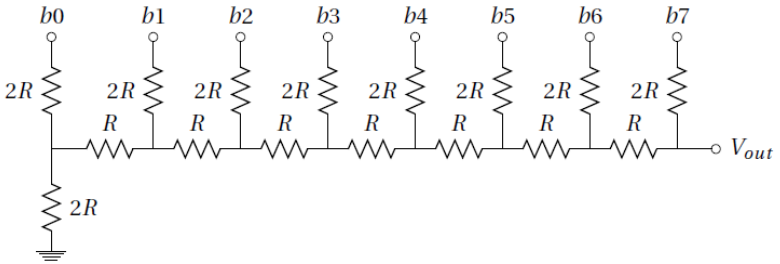

Figure 1.5: Example of 8-bit R-2R ladder

$$V_{LSB} = V_{ref} \cdot \frac{1}{2^N}$$

$$BinVal = \sum_{i=0}^{N-1} 2^i \cdot b_i$$

$$V_{out} = V_{LSB} \cdot BinVal$$

$$V_{Max} = V_{ref} \cdot \frac{2^N - 1}{2^N}$$

d7	d6	d5	d4	d3	d2	d1	d0	Voltage	Bit
0	0	0	0	0	0	0	1	4,687 mV	d0
0	0	0	0	0	0	1	0	9,375 mV	d1
0	0	0	0	0	1	0	0	18,75 mV	d2
0	0	0	0	1	0	0	0	37,50 mV	d3
0	0	0	1	0	0	0	0	75,00 mV	d4
0	0	1	0	0	0	0	0	150,0 mV	d5
0	1	0	0	0	0	0	0	300,0 mV	d6
1	0	0	0	0	0	0	0	600,0 mV	d7
1	1	1	1	1	1	1	1	1,195 mV	all

Table 3.2: Output voltage DAC

Introduction
SAR Logic

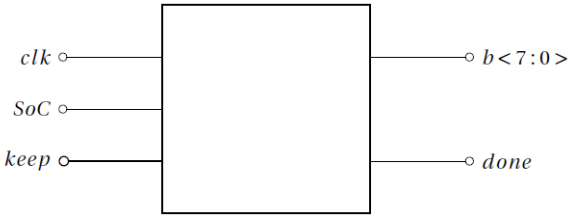

Figure 1.7: SAR logic block

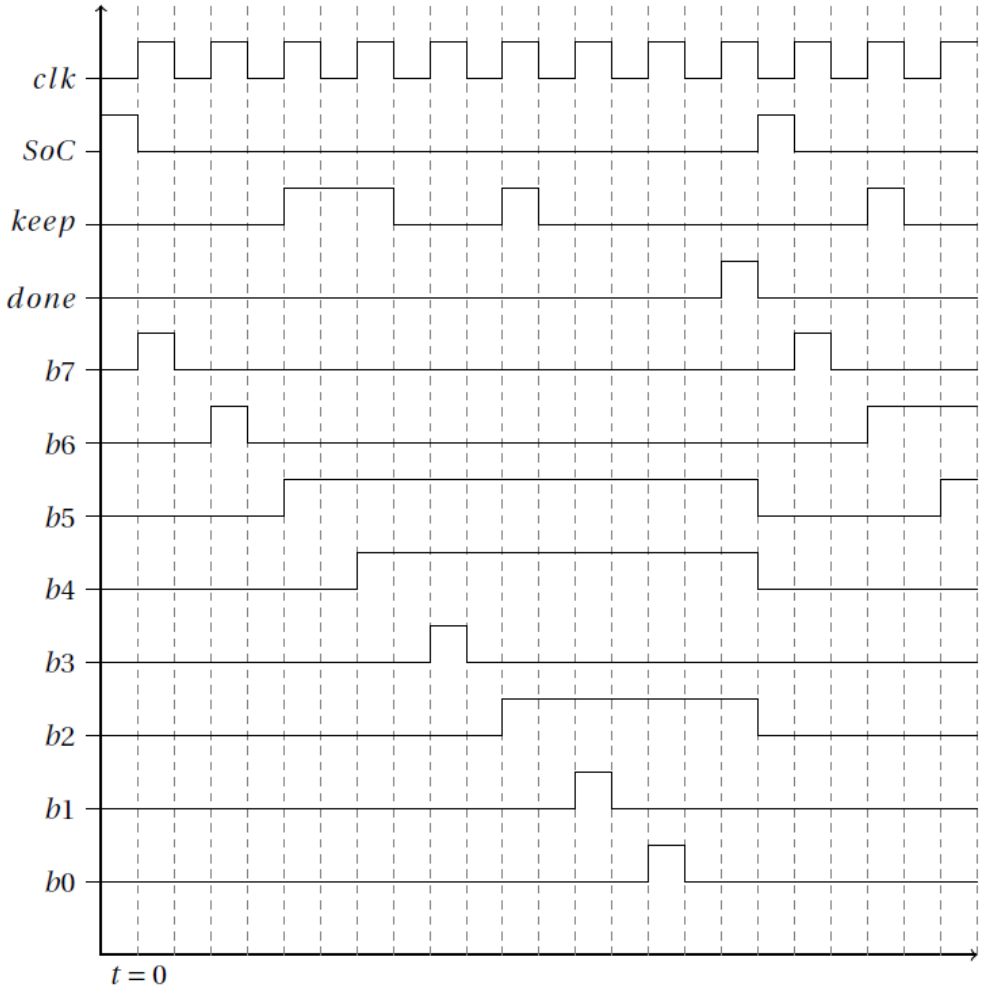

Figure 1.8: Typical timing diagram for the SAR logic block

Requirements

SAR ADC

- Input sampling rate: 1 M samples/s
- Output resolution: 8 bits
- Supply voltage: $VDD = 1.2V$, and $VSS = 0V$
- No missing codes

Requirements
DAC

- Sampling rate: 8 M samples/s
- Resolution: 8 bits
- Supply voltage: $VDD = 1.2V$, and $VSS = 0V$
- DNL < ± 0.5 LSB
- INL < ± 0.5 LSB
- *VOUT* (*P-P*) >= 0.6*V*
- *Cload* = 50 *fF*

Requirements
Comparator

- Delay <= 0.5 clock cycle
- Supply Voltage: *VDD* = 1.2*V* and *VSS* = 0*V*
- Offset < 0.5 LSB
- Gain > *VDD*/*Vref* /2*n*
- *Cload* = 50 *fF*

Results

- Sample-and-Hold
- Comparator
- Digital-to-Analog Converter
- SAR logic
- SR Latch
- Output buffers

Results

Sample-and-Hold Implementation and Layout

- Transmission gate
- Inverter

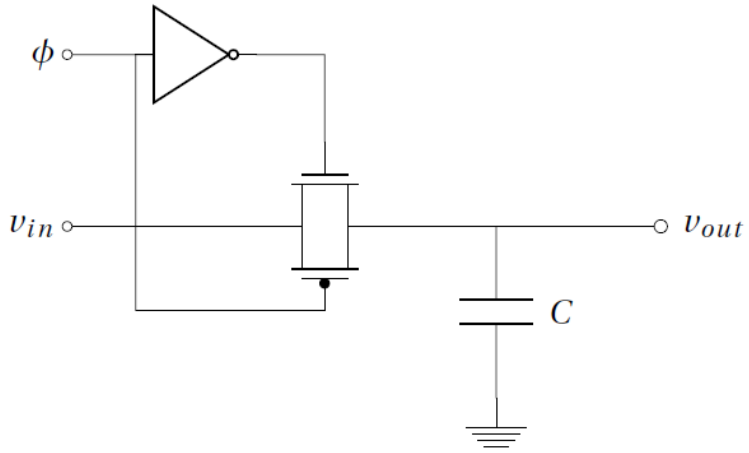

Figure 3.1: Sample and Hold design

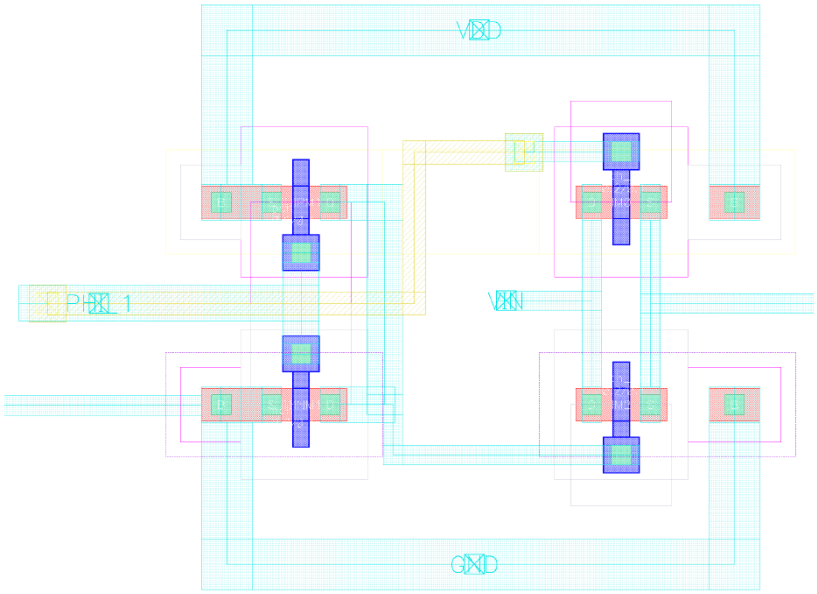

Figure 3.3: Layout for Sample and hold without capacitor

Results
Sample-and-Hold Implementation and Layout

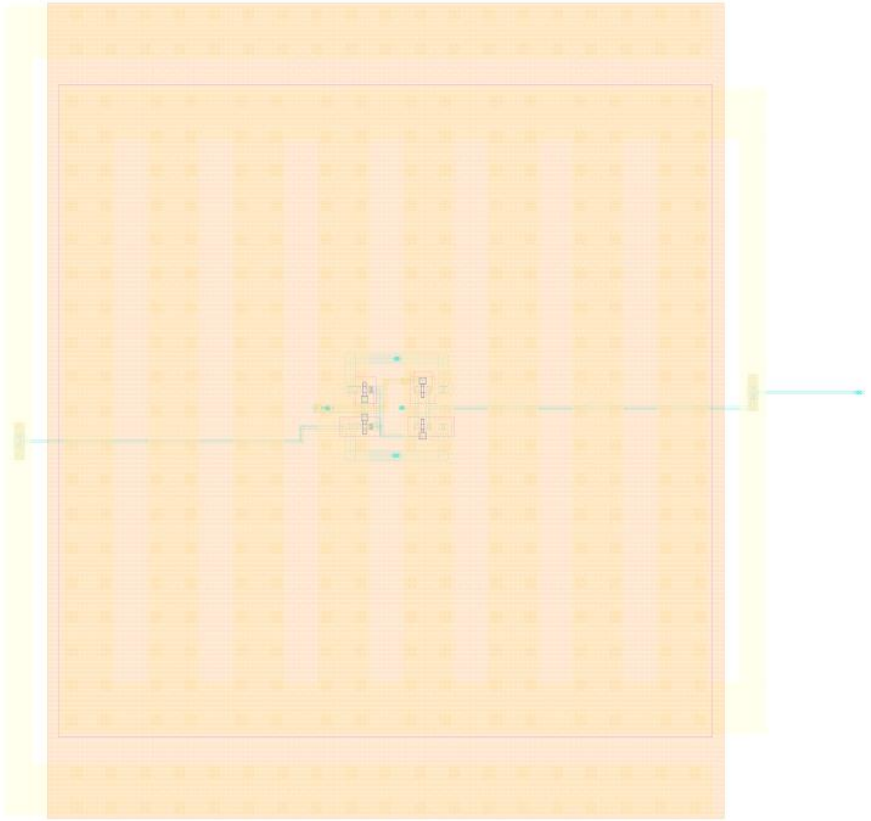

Figure 3.4: Layout for Sample and hold

Results
Sample-and-Hold Simulation

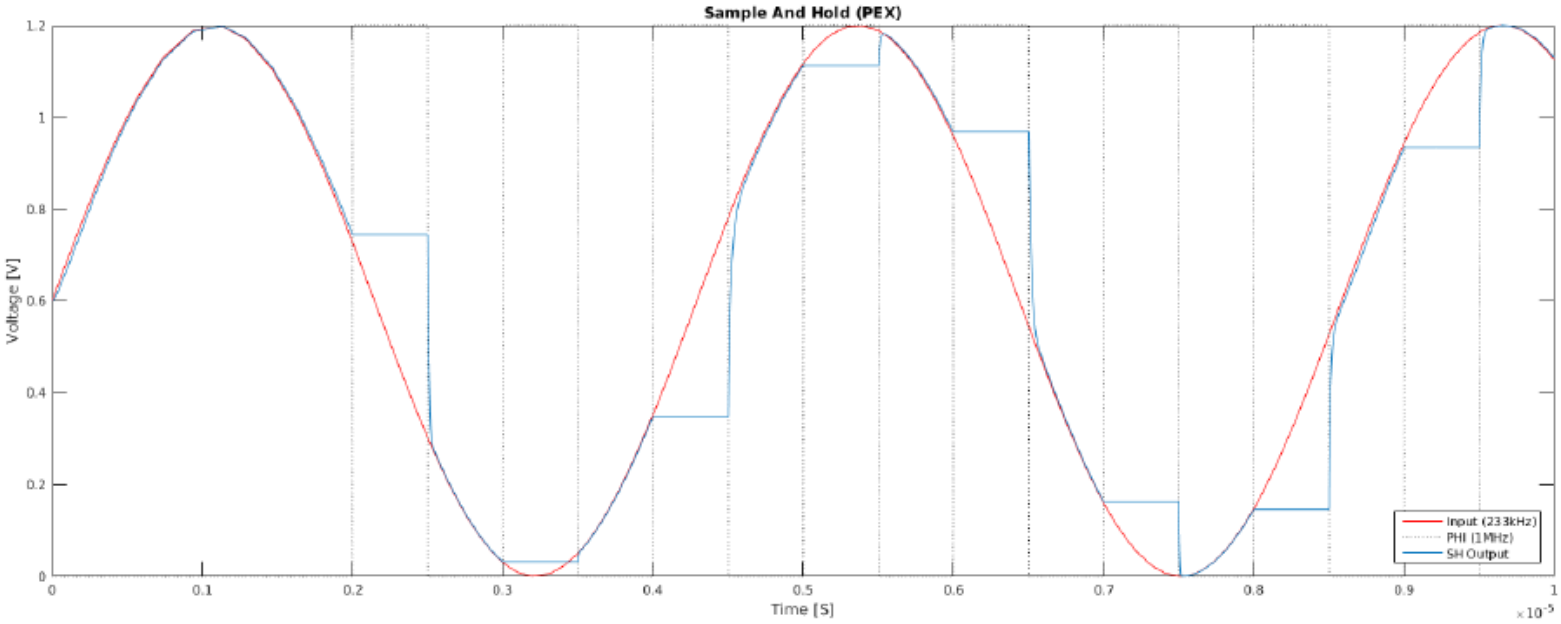

Figure 3.2: Sample and Hold simulation output

Results

Comparator Implementation and Layout

- Rail-to-rail input
- Large transistors

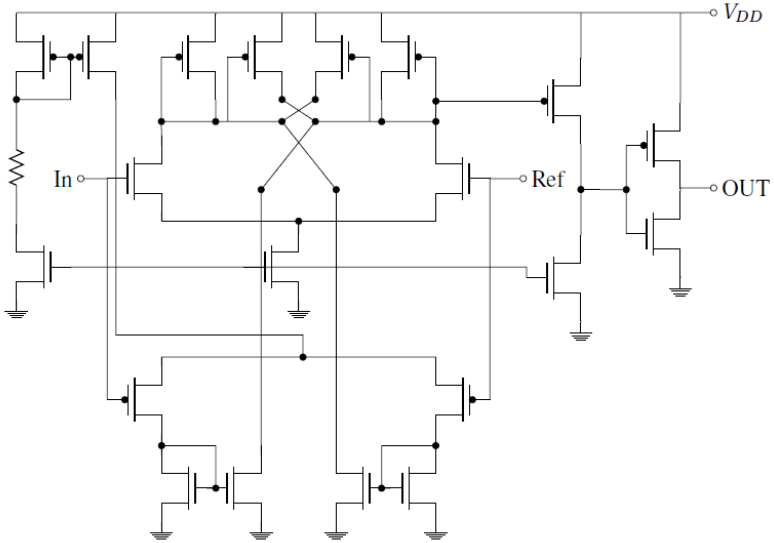

Figure 3.5: Comparator design

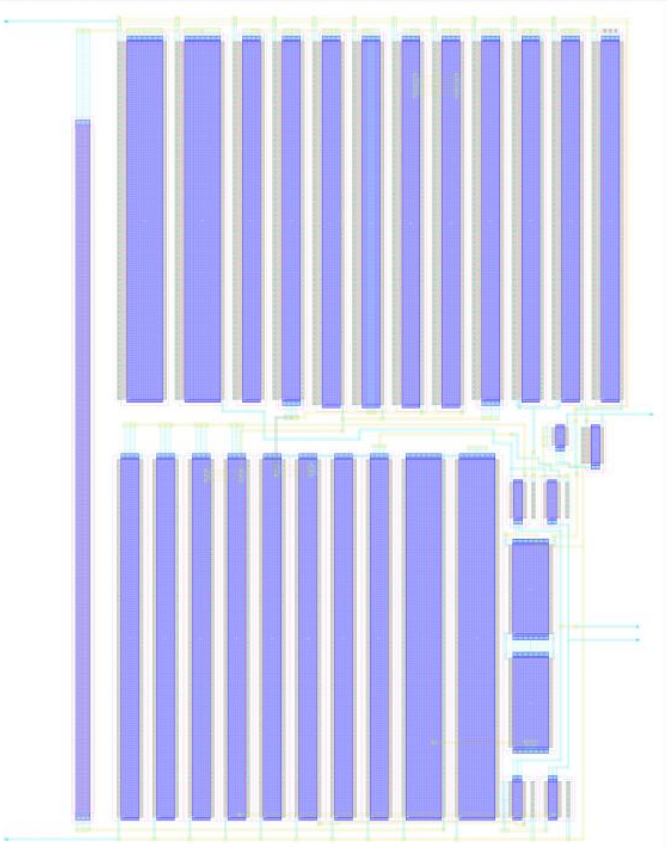

Figure 3.8: Layout for the Comparator

Results
Comparator Simulation

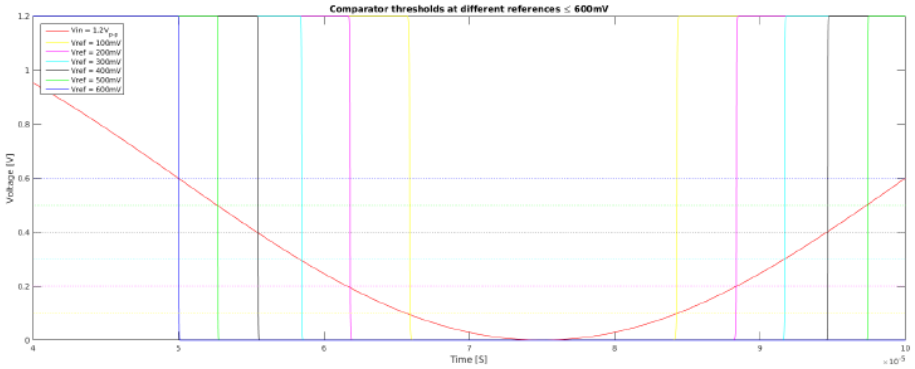

Figure 3.6: Comparator simulation output, $V_{ref} \leq 600mV$

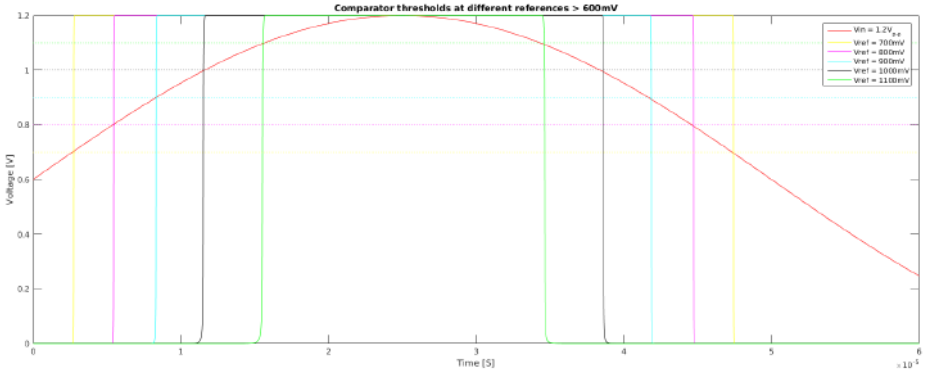

Figure 3.7: Sample and Hold simulation output, $V_{ref} > 600mV$

Results

Requirement fulfillment

- Achieved
  - Delay
  - Offset
  - Gain

Results

Digital-to-Analog Converter Implementation and Layout

- R-2R
- Buffers convert from 1V to 1.2V
- Each resistance divided in four
- R = 320 kOhm

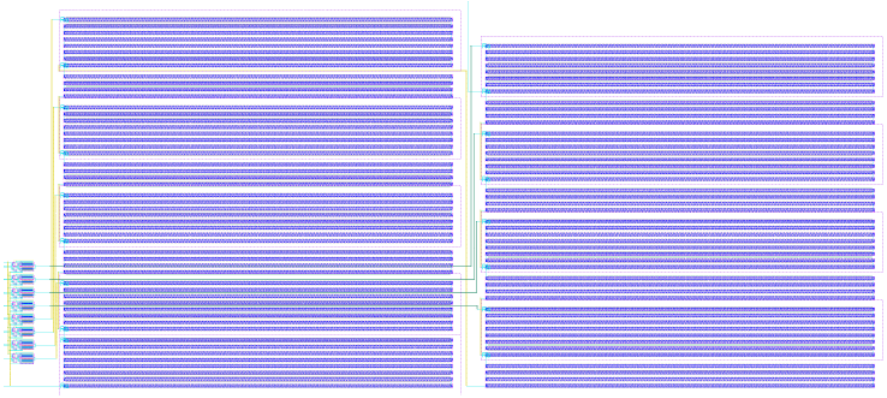

Figure 3.16: Layout for DAC

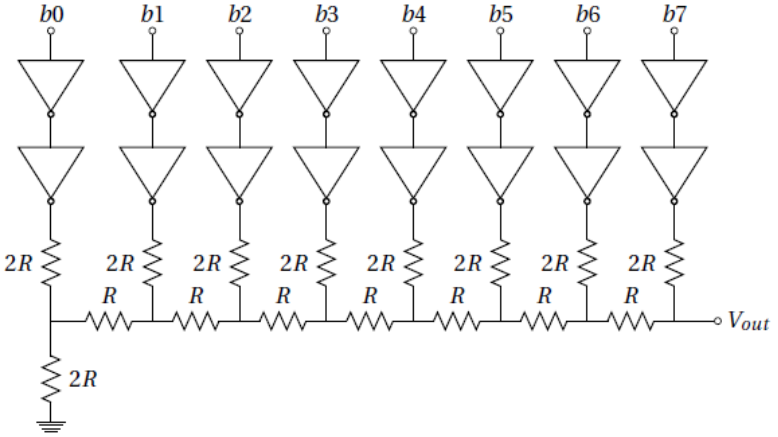

Figure 3.12: Implemented 8-bit R-2R ladder

Results
Digital-to-Analog Converter Simulation

R = 10K
2R = 20K

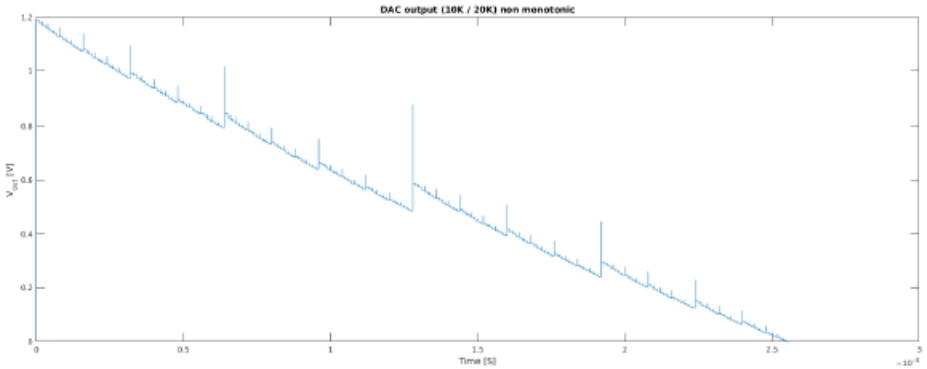

Figure 3.13: Simulation using 10k (20k)Ω

R = 100K
2R = 200K

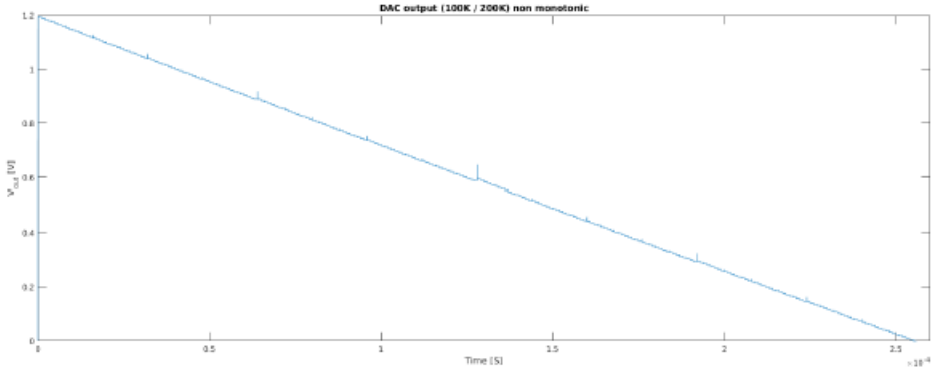

Figure 3.14: Simulation using 100k (200k)Ω

Results
Digital-to-Analog Converter Simulation

R = 320K
2R = 640K

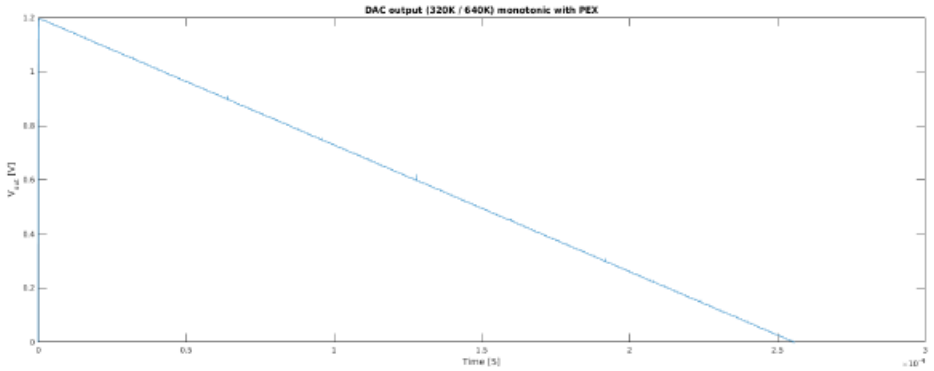

Figure 3.15: Simulation using 320k (640k)Ω

Results
Requirement fulfillment

- Achieved
  - Sampling rate of 8 M samples/s (10 M ok)
  - INL and DNL (software calculations)
  - Monotonic
  - Output voltage

Results
SAR logic

- Not simulated on its own
- Verified with the complete system

Results

SR Latch

- Needed to include SR Latch for control of sample-and-hold

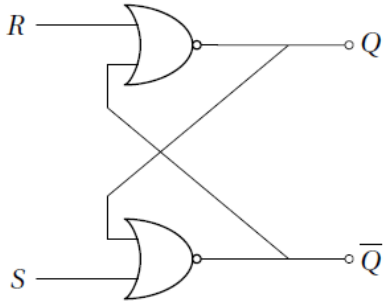

Figure 3.18: SR latch

S	R	Q	$\overline{Q}$
0	0	NC	NC
0	1	0	1
1	0	1	0
1	1	0	1

Table 3.3: SR latch function table

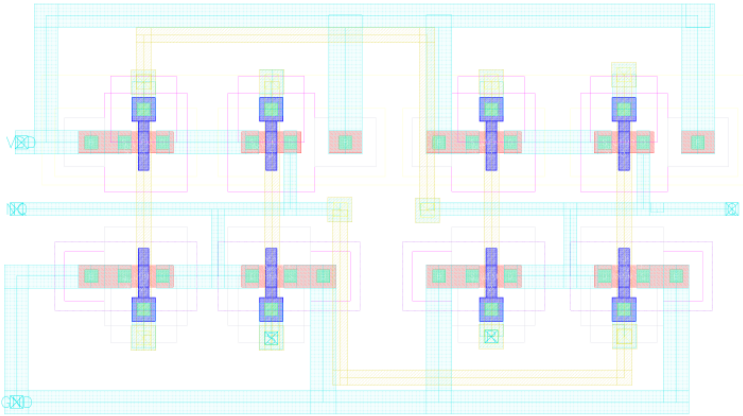

Figure 3.19: Layout for the SR Latch

Results

Output buffers

- High impedance for the DAC
- Not simulated

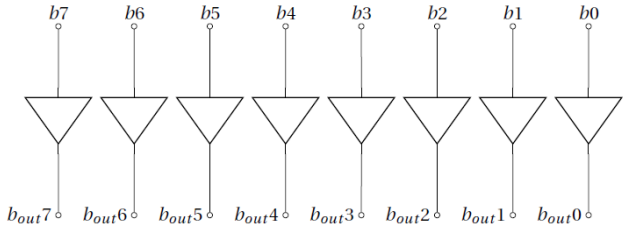

Figure 3.20: Output buffers

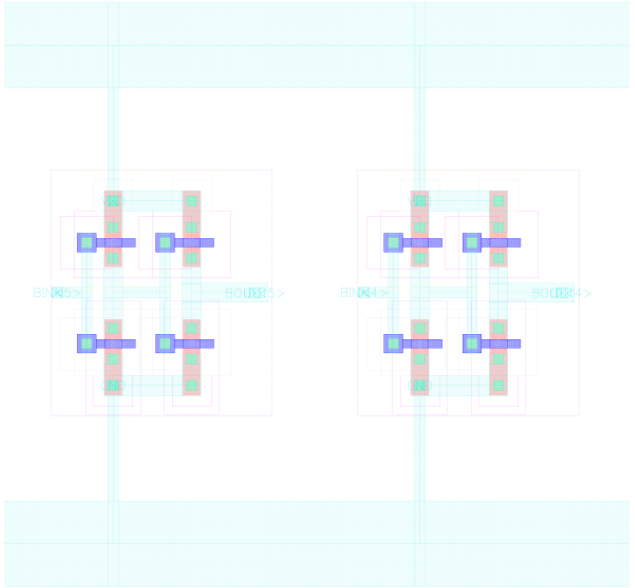

Figure 3.21: Layout for the Output buffers

Results
SAR System Implementation and Layout

- The total area consumed:
  - 220μm x 140μm

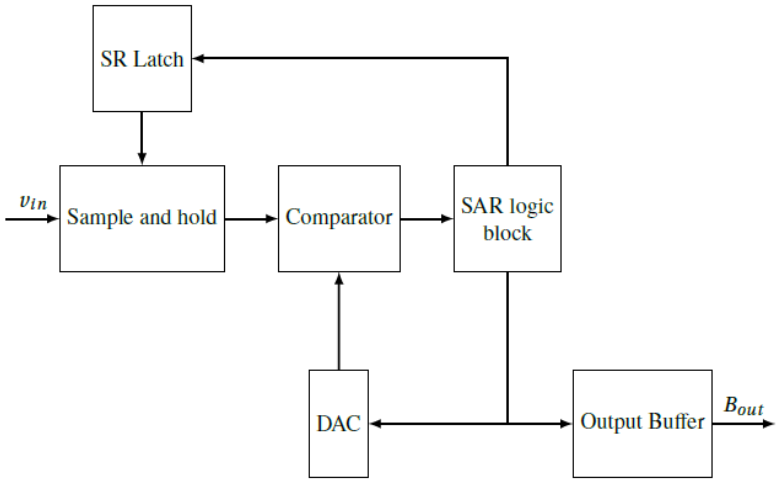

Figure 3.22: Block diagram representing the complete system

Results
SAR System Implementation and Layout

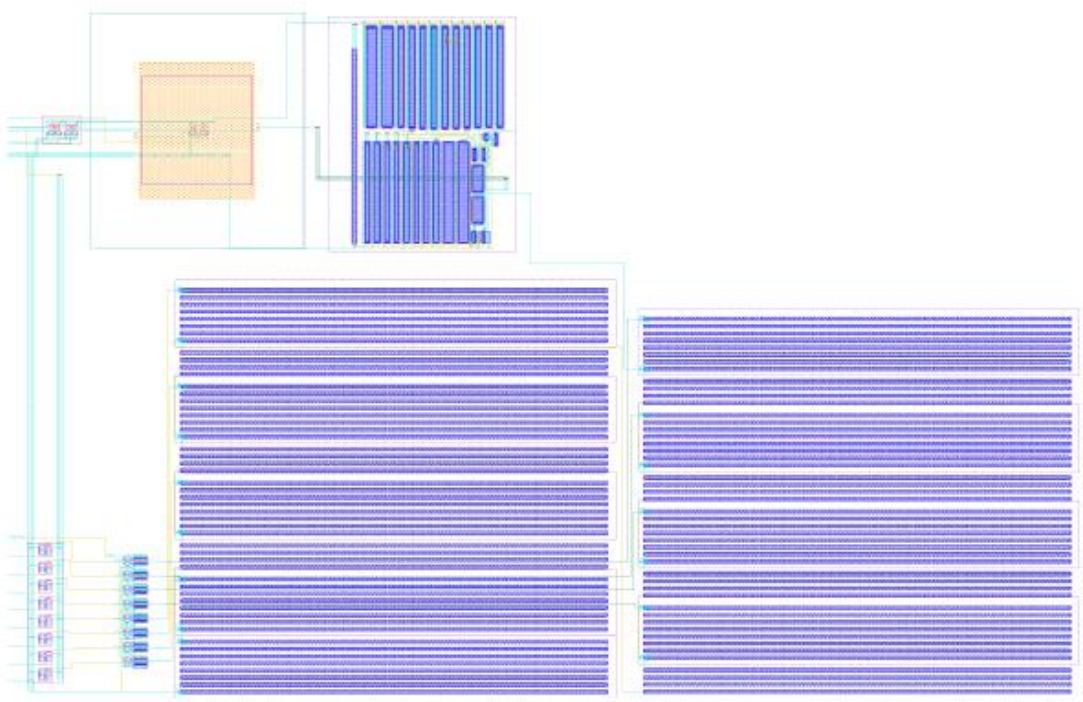

Figure 3.24: Implementation of the SAR system in layout

Results
SAR System Simulation

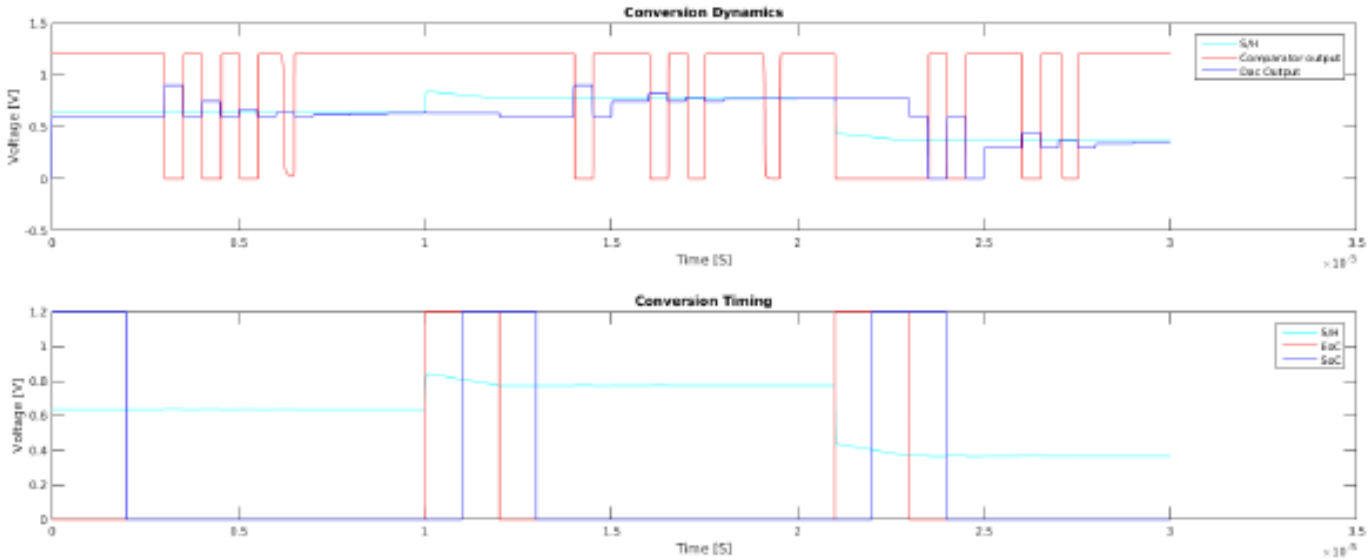

Figure 3.26: SAR system performance dynamics

Results
Requirement fulfillment

- Achieved
  - Input sampling rate of 1 M samples/s
  - Output resolution: 8 bits
- Not Verified
  - No missing codes

Conclusion

- Improvements
  - DAC design
  - SR latch
  - Layout
- Almost all requirements fulfilled