Complete system test-bench

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1   System overview

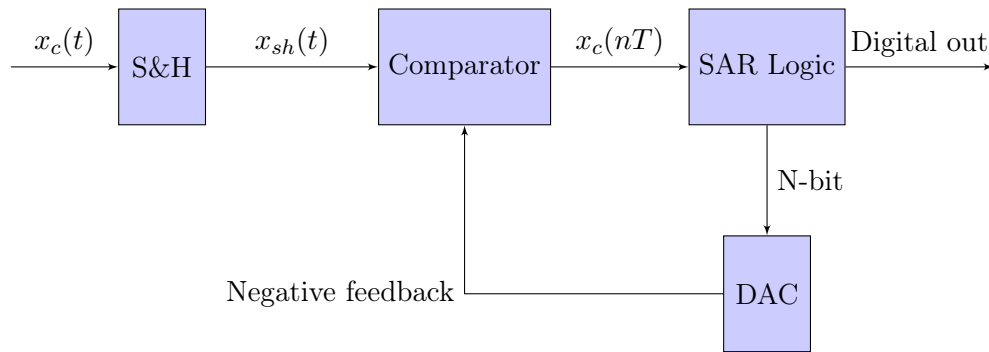The overall structure of the system is seen in Figure 1.

Figure 1: Block diagram

2   Schematic

We have not completed our research in circuits to use in this project. We have created schematics for some simple circuits but we expect that some (or all) of the circuits is going to change. See test-benches in the next section.

Schematic: SAR_system

The SAR_system is the complete schematic for the whole system. It consists of a sample and hold block, a comparator block, the SAR logic and the digital-to-analog converter block. Figure 2 shows the schematic that has been created.
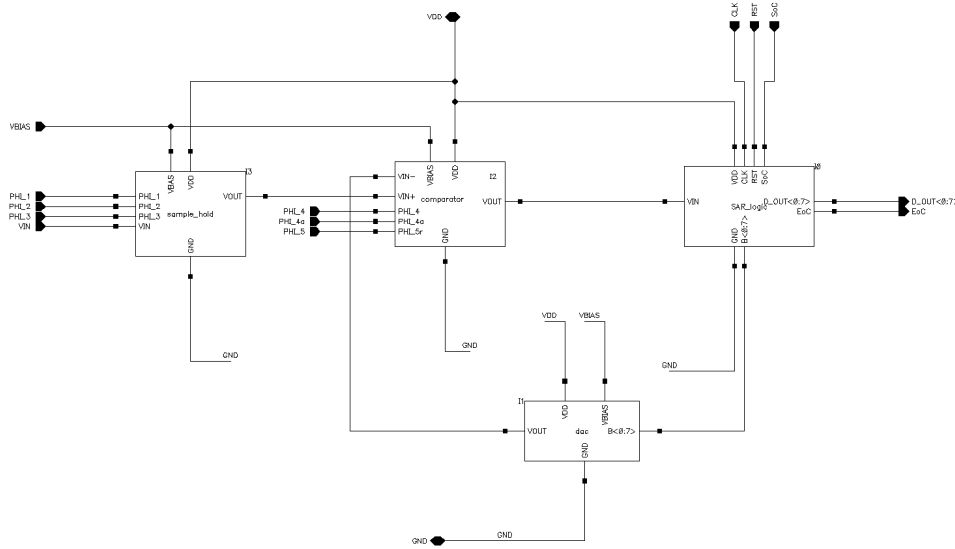
Figure 2: SAR_system

Schematic: sample_hold

The sample and hold (S/H) is based on a circuit provided by R. Jacob Baker in the book CMOS Mixed-Signal Circuit Design [1]. The implementation is a single-ended S/H implementation. When ϕ_1 and ϕ_2 is high, ϕ_3 is low, and the bottom plate of the hold capacitor is charged by the input signal, while the top plate is held to ground by the feedback around the op amp. When the ϕ_2 is turned off, its charge will be injected into the low impedance input, VIN, since the impedance looking into the left of the ϕ_2 switch is large.

This implementation has not yet been tested, and may therefor be changed during the project.

Schematic: comparator

The design of the comparator is based on a design in the book Analog Integrated Circuit Design by Carusone, Johns and Martin [2].

Schematic: SAR_logic

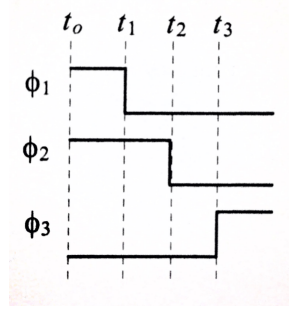We have not completed the schematics for the SAR logic.
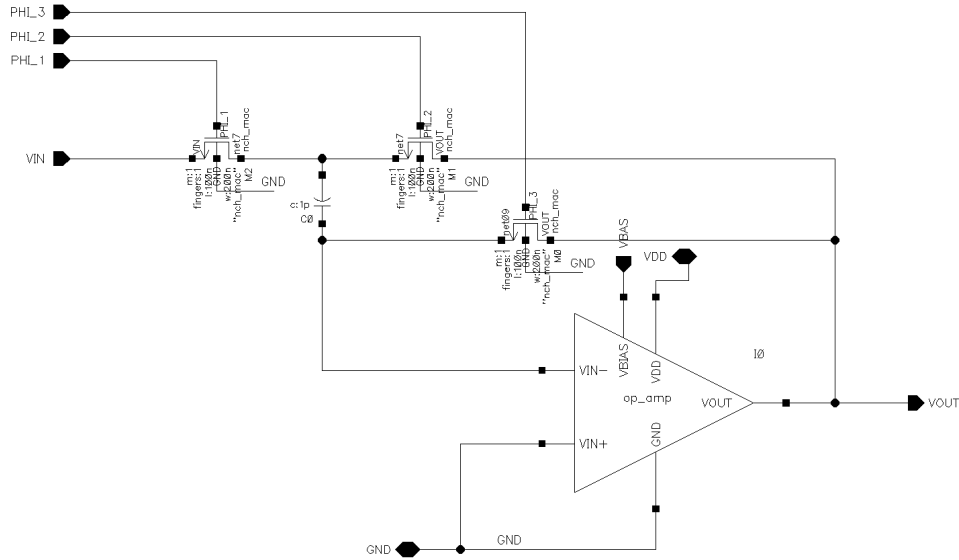
Figure 3: Single-ended S/H operation [1]

Figure 4: Sample and hold

Schematic: dac

This DAC circuit is based on the R-2R ladder from the book Analog Integrated Circuit Design by Carusone, Johns and Martin [2]. This design commonly used in many applications, and is therefor the main reason for why we have chosen to make this design.

Schematic: op_amp

The op-amp circuit is based on a design from CMOSedu.com (R. Jacob Baker), and is a commonly used differential pair op-amp. We have tried
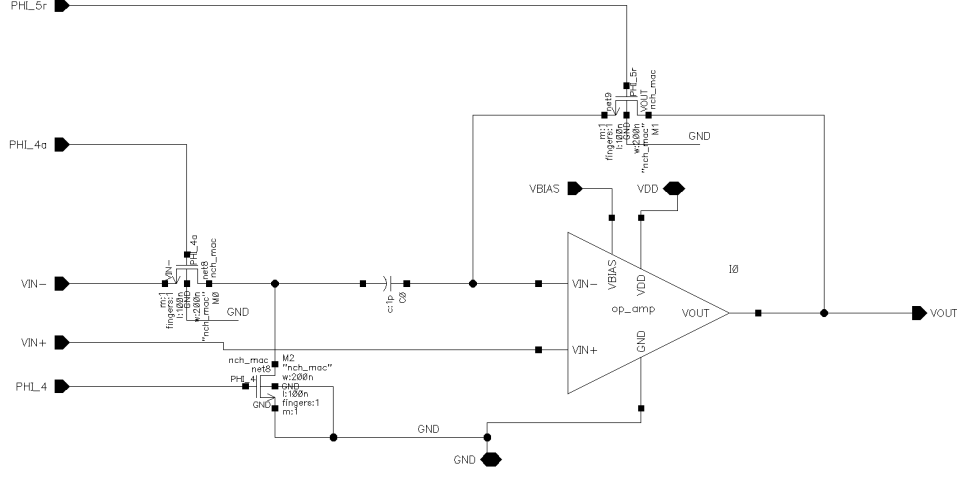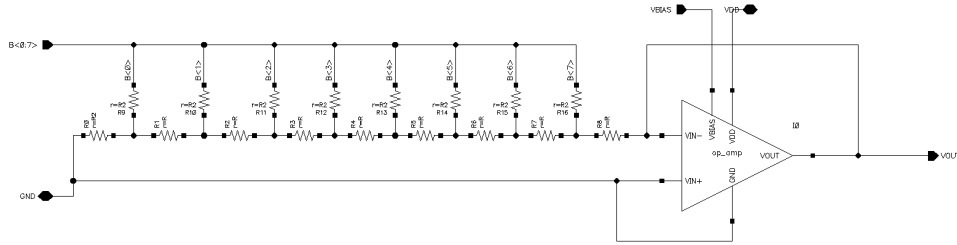
Figure 5: Comparator

Figure 6: DAC

some different designs, but we have not succeeded in any of the other designs. This is not the final version, since it is not fully tested. The dimensions for the NMOS and PMOS transistors are based on a former thesis that R. Jacob Baker has referred to in his web-page. For the NMOS and the PMOS, we have used the relation 10/2 and 22/2 respectively. The final design can be seen in Figure 7

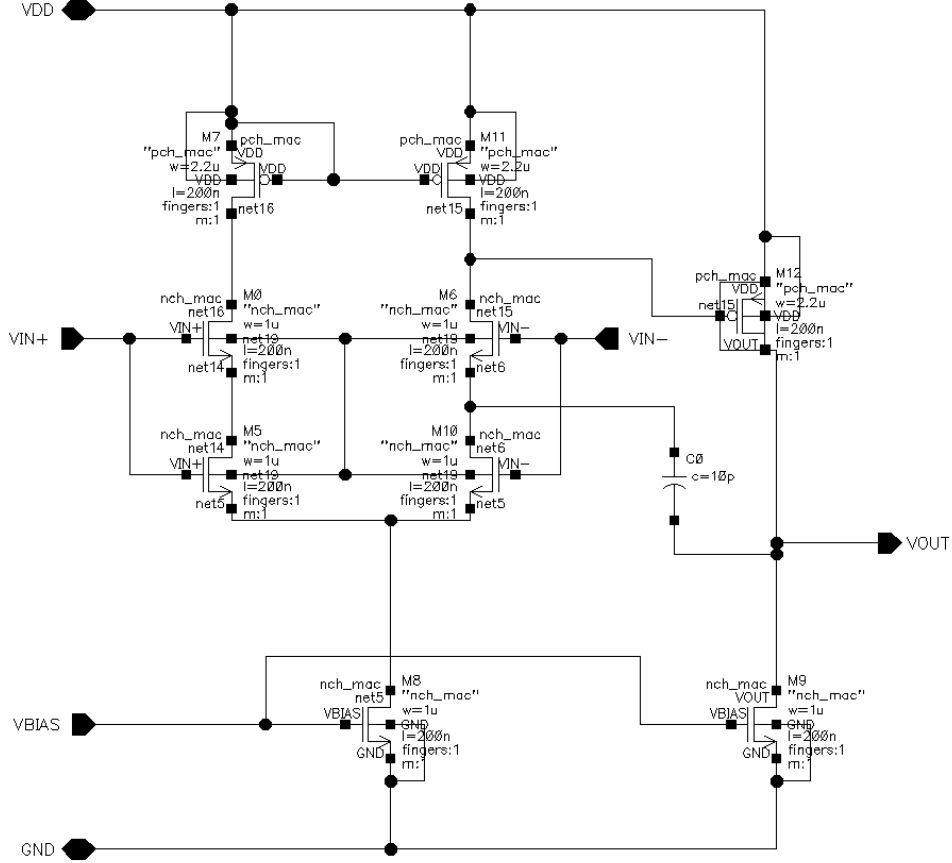To test the op-amp, we have made a simple test-bench that can be seen in section **Schematic: SIM_op_amp**.

Figure 7: Opamp

3   Test bench

In this section a short overview of the different test-benches for our components is presented.

Schematic: SIM_system

This is a complete system test bench. Here all the different components come together to form the full SAR-ADC architecture.
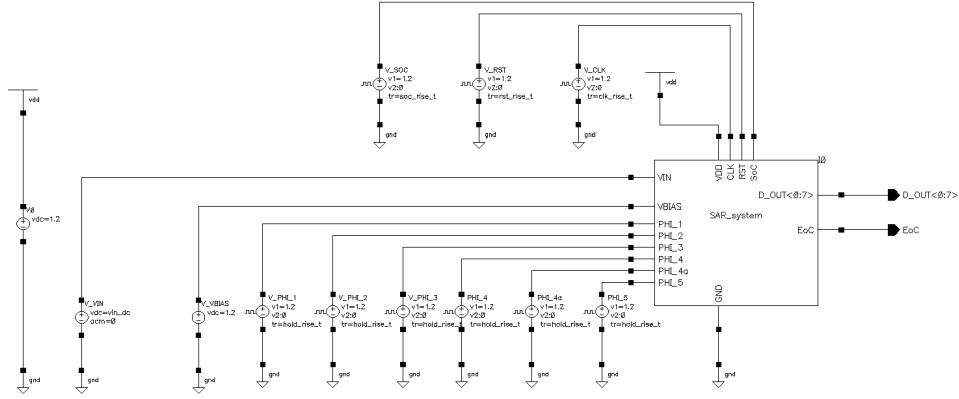
Figure 8: Test bench for SAR-ADC circuit

Testing on a system level is necessary to ensure that the circuit performs according to the interface the circuit provides to the outside world.

This test scenario is quite hard to set up since many signals have to be timed to each other. The verification of the circuit is also challenging since many signals has to be considered. In order to manage this test we need to generate a test procedure with the specified stimuli and check the results to a expected pattern. See figure 8.

Schematic: SIM_sample_hold

To test the sample and hold we need to generate 3 clocks (see timing diagram in figure 3). The output is ideally expected to match the input value and hold it in the phi_3 phase. See figure 9.

Schematic: SIM_comparator

In the test bench for the comparator we need 3 clocks for the timing. When sweeping the input (let's say v-) we expect that at some point (, dependent on v+,) that the comparator will change state. See figure 10.
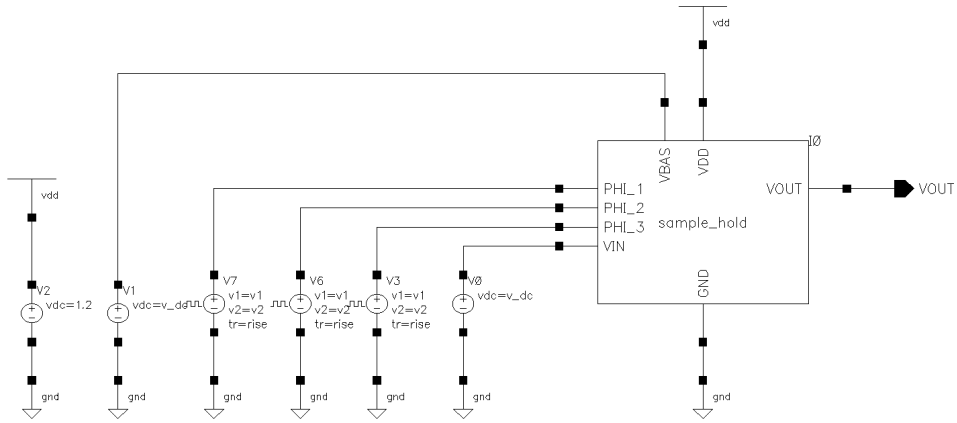
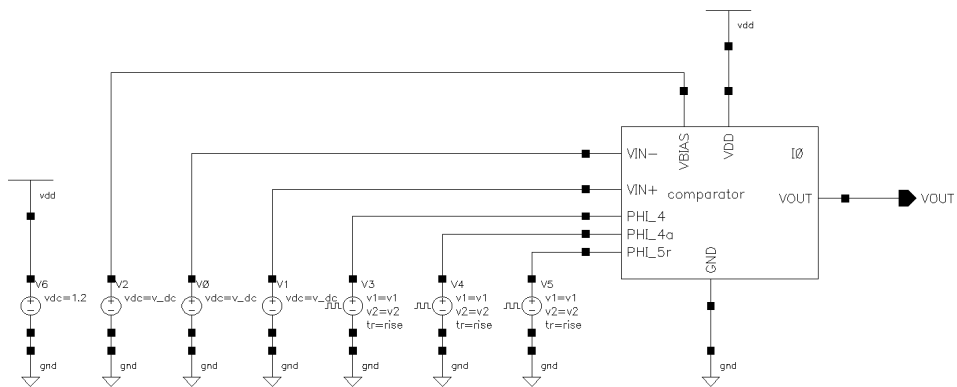Figure 9: Test bench for sample and hold circuit

Figure 10: Test bench for comparator circuit

Schematic: SIM_SAR_logic

Some of the circuit in the SAR-logic is given but some extra circuitry is needed. In this test bench we want to test that the acquisition state is
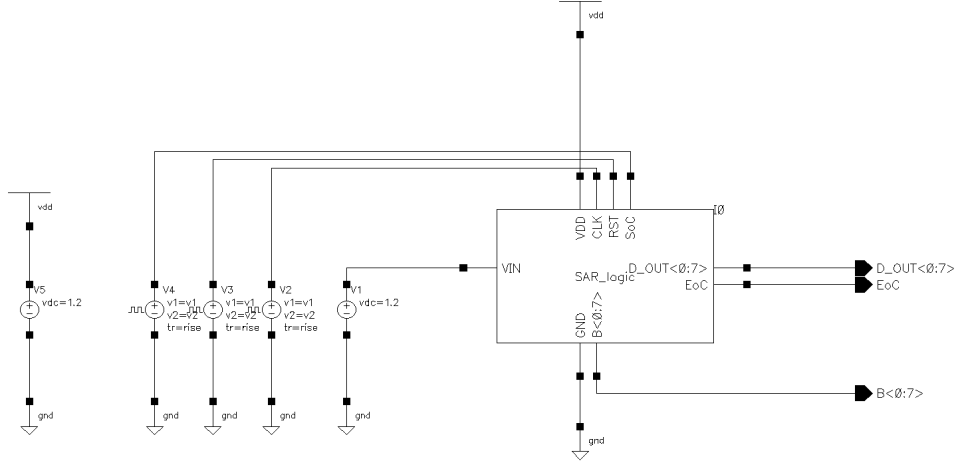
Figure 11: Test bench for SAR-logic circuit

started when the SoC signal is pulsed. And that we receive a EoC after N-bits clock pulses. We also need to test the reset functionality. The main function of generating the digital output is easy to test since the input signal decides the value of the current bit. See figure 11.

Schematic: SIM_dac

The test-bench for the DAC consists of N-bits pulse generators so that we can apply a binary pattern. VOUT should be proportional to the binary value. See figure 12.

Schematic: SIM_op_amp

In our test bench for the op-amp we have an open circuit amplifier that expect is going to saturate to either (almost) GND or VDD, if our gain is high enough. This simulation is a test to check for response and not performance. This simple test gives little information about the performance of the op-amp. To get a better test of the performance of the circuit we need more tests where we test other configurations of the op-amp. See figure 13 and 14.
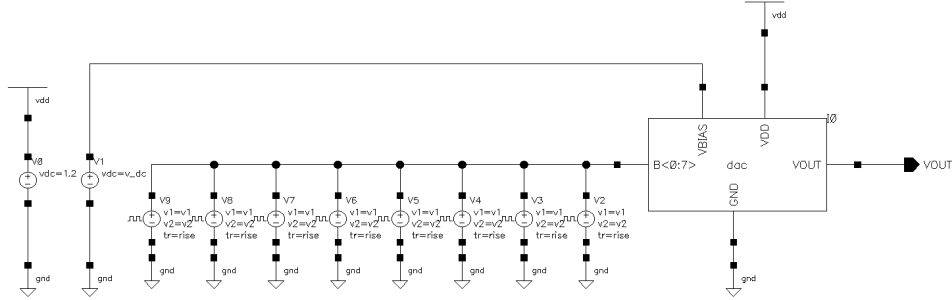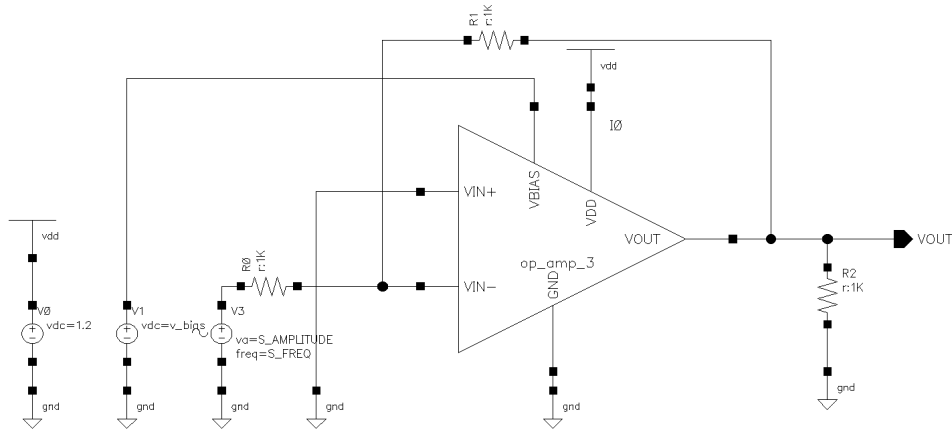
Figure 12: Test bench for DAC circuit

Figure 13: Test bench for op-amp circuit

References

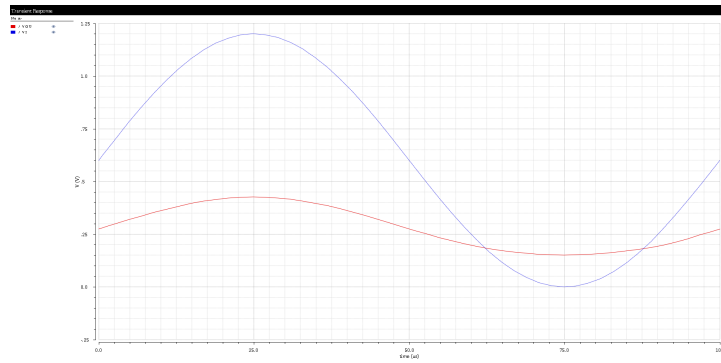[1]   R. Jacob Baker. *CMOS Mixed-Signal Circuit Design*. IEEE Press, John Wiley, and Sons, 2009.

Figure 14: AC response from op-amp circuit used as a non-inverting amplifier

[2] Carusone et al. *Analog Integrated Circuit Design, 2nd. edition.* John Wiley and Sons, 2013.