Brief Papers

1.2-V CMOS Op-Amp with a Dynamically Biased Output Stage

G. Giustolisi, G. Palmisano, G. Palumbo, and T. Segreto

***Abstract*—A very low-voltage operational amplifier in a standard CMOS process with a 0.75-V threshold voltage is presented. It uses a novel dynamically biased output stage based on the switched-capacitor approach. Thanks to this, drive performance is greatly improved and accurate current control is also achieved.**

The amplifier is capable of working with a power supply as low as 1.2 V while providing a −74-dB total harmonic distortion with a 700-mV peak-to-peak output voltage into a 500-Ω and 20-pF output load. The open-loop gain and the gain-bandwidth product are higher than 90 dB and 2.2 MHz, respectively.

***Index Terms*—CMOS analog integrated circuits, MOSFET amplifiers, operational amplifiers.**

I. Introduction

DURING recent years, the literature has paid more and more attention to integrated circuits working at very low-voltage power supplies (i.e., 1.5 V or less). This is mainly due to the wide use of portable equipment, requiring low-consumption IC's to increase battery life.

Cutting down power consumption usually means reducing both the power-supply voltage and current. However, given the dependence of transistor noise on the quiescent current, the latter cannot be achieved in some high-performance analog building blocks. Therefore, the only way to reduce power consumption in many cases is to reduce the supply voltage.

Today, typical supply voltages for analog circuits are around 2.5–3 V, but future trends suggest supply voltages of 1.5 V or even less. With such low values, traditional CMOS circuit solutions can be adopted only if a low threshold process is available. Otherwise, new circuit solutions capable of working with a reduced power supply have to be designed [1]–[6].

A fundamental building block in analog processing is the power operational amplifier (op-amp). Unlike the transconductance amplifier, it includes an output stage capable of driving off-chip, low load resistances. Obviously, the output stage must respect the specifications required of drive capability, linearity, and output swing.

Another critical aspect in low-voltage design is the common-mode input swing, which depends on the input stage. Indeed, while the output bias voltage $V_{\rm BOUT}$ is preferably set to half the power supply to provide maximum output swing, the input terminals must be set to a common-mode input voltage $V_{\rm CM}$, which may be higher or lower than $V_{\rm BOUT}$, depending on whether the source-coupled pair uses NMOS or PMOS transistors. This drawback can be overcome by adopting the switched-capacitor (SC) approach, which is very suitable for low-voltage analog signal processing.

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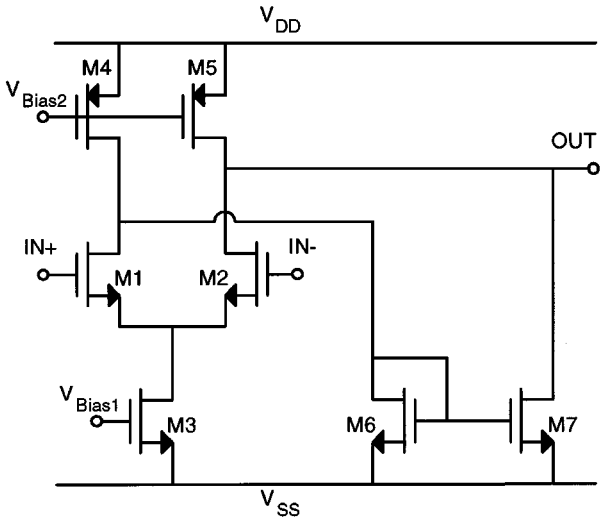

Fig. 1. Schematic of the input stage.

In this paper, a new operational amplifier that works with a 1.2-V power supply is presented. It adopts a folded mirror load in the input stage, which saves input swing, and includes a dynamically biased class-AB output stage providing both a rail-to-rail output swing and a high output current.

The operational amplifier has been implemented in a standard 1.2-μm CMOS process with threshold voltages of around 0.75 V. It dissipates less than 150 μW.

II. Circuit Description

A. The Input Stage

The input stage is shown in Fig. 1. It is made up of the source-coupled pair M1–M2 and the folded mirror M6–M7. Transistors M3–M5 bias current sources [6].

The common-mode input voltage $V_{\rm CM}$ must satisfy the following conditions:

$$V_{\rm CM} \geq V_{\rm DSsat3} + V_{\rm DSsat1.2} + V_{\rm Tn} \tag{1}$$

and

$$V_{\rm CM} \leq 2V_{\rm Tn} + V_{\rm DSsat6}. \tag{2}$$

In effect, for a 1.2-V power supply, the upper bound of $V_{\rm CM}$ is the power supply itself. Therefore, we can achieve an upper

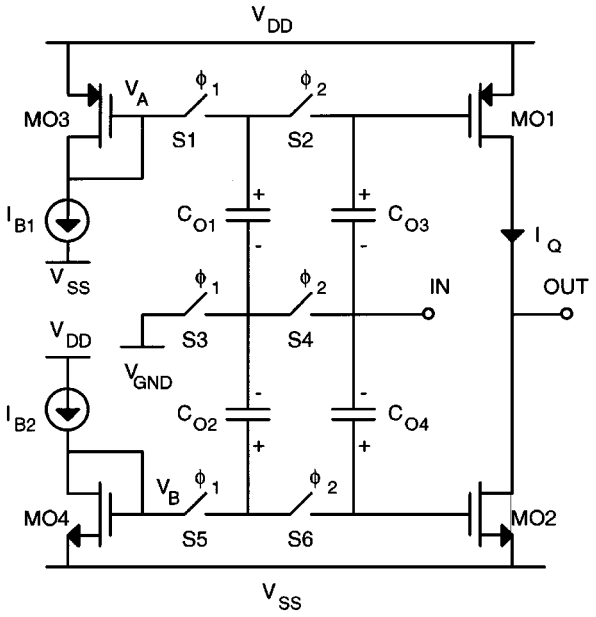

Fig. 2. Schematic of the output stage.

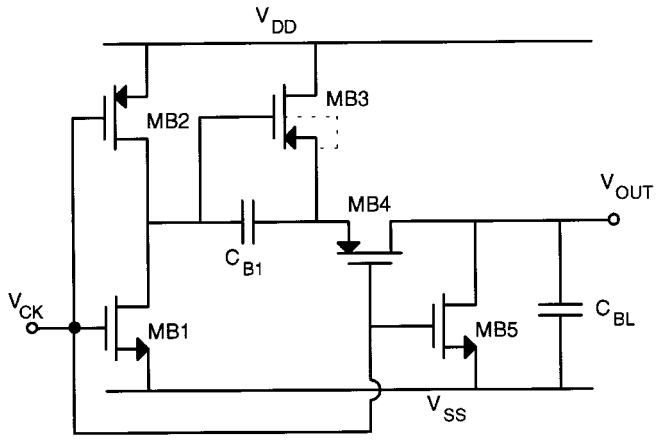

Fig. 3. Schematic of the clock booster.

bound that is higher than $V_{\rm DSsat}$ with respect to the traditional differential stage loaded with a p-type current mirror. By setting $V_{\rm CM}$ to 1 V and assuming values of $V_{\rm DSsat}$ lower than 0.1 V, a common-mode range (CMR) of around 400 mV is achieved.

B. The Output Stage

1) Circuit Behavior: The novel class-AB output stage is shown in Fig. 2. Common source transistors MO1 and MO2 provide a rail-to-rail output swing, diode-connected transistors MO3 and MO4 set the bias voltages for the control of the quiescent current I_Q in the output branch, and the SC network, composed of capacitors C_{O1}-C_{O4} ($C_{O1} = C_{O2}$ and $C_{O3} = C_{O4}$) and switches S1–S6, performs a dynamic biasing and feeds the input signal [7]. Switches S1–S6 are controlled by complementary clock phases ϕ_1 and ϕ_2.

Assuming standby conditions, capacitors C_{O1}, C_{O3} with switches S1–S4 and capacitors C_{O2}, C_{O4} with switches S3–S6 perform as two SC damped integrators. In steady-state conditions, the voltages across capacitors C_{O3} and C_{O4} are equal to the gate voltages of MO3 and MO4, V_A and V_B, respectively. Since the closed-loop amplifier sets the current in MO1 and MO2 as equal, the gate voltages of MO1 and MO2, and the input bias voltage, are forced to V_A, V_B, and $V_{\rm GND}$, respectively. Therefore, current I_Q is set by currents I_{B1} and I_{B2} and the aspect ratios of MO1, MO3 and MO2, MO4.

The input bias voltage, i.e., $V_{\rm GND}$, was set to half the supply voltage to achieve maximum input overdrive while capacitors C_{O3} and C_{O4} were set larger than the gate-source capacitances of MO1 and MO2 to avoid signal attenuation at the gate nodes of MO1 and MO2.

Note that the gate voltages of MO1 and MO2 are pulled beyond $V_{\rm SS}$ and $V_{\rm DD}$, respectively, due to the large input overdrive. The maximum swing on the gates of MO1 and MO2 is limited by the forward biasing of the switch bulk junctions.

2) The Clock Booster: Since the process threshold voltages are around 0.75 V and the power supply is as low as 1.2 V, switches S3 and S4, at least, need a gate voltage that is higher than the available power supply because their drain and source terminals are at half the supply voltage. Therefore, the clock booster in shown Fig. 3 was adopted [8]. Moreover, to simplify the clock phase generator, all the switches were implemented as NMOS pass-transistors.

The clock booster is made up of capacitor C_{B1} and transistors MB1-MB5, which have the bulk terminal short-circuited with the source terminal. Capacitor C_{B1} was set much larger than the load capacitor $C_{\rm BL}$.

The clock booster works as follows. Transistors MB1 and MB2 perform an inverter stage. When the clock $V_{\rm CK}$ is high, capacitor C_{B1} is precharged to $V_{\rm DD}$ through transistor MB3, which will be in the linear region. Moreover, transistor MB4 is open and load capacitor $C_{\rm BL}$ is discharged through transistor MB5. Next, when the clock goes down, the output of the inverter MB1–MB2 goes to $V_{\rm DD}$, transistors MB3 and MB5 open, and transistor MB4 closes. Since capacitor C_{B1} is much larger than $C_{\rm BL}$, the output voltage is boosted above the power supply. More exactly, the output voltage tries to reach about twice $V_{\rm DD}$, but during the last part of the transient, the bulk junctions of MB3 clamp the output voltage to around $V_{\rm DD} + 0.6$. This overdrive is sufficiently high to drive the switches of the output stage.

C. Complete Amplifier

The whole operational amplifier is shown in Fig. 4. It is made up of three main stages, which are the input and the output stage in Figs. 1 and 2, respectively, and the intermediate stage M8–M12. This last stage is composed of the folded-mirror inverter M8–M10 and the common source M11–M12. The inverter was included for frequency compensation purposes.

The circuit shows three low-frequency poles at the output of each gain stage. Then the nested Miller compensation was used to provide frequency stability [9]–[12]. The two capacitors C_{m1} and C_{m2} were connected between the output of the amplifier and the output of the inner stages in order to achieve a single low-frequency pole at the output of the input stage and to move the other two poles to frequencies higher than the gain-bandwidth product. Resistors R_{m1} and R_{m2} were included to transform the right half-plane zeros into high-frequency left half-plane zeros.

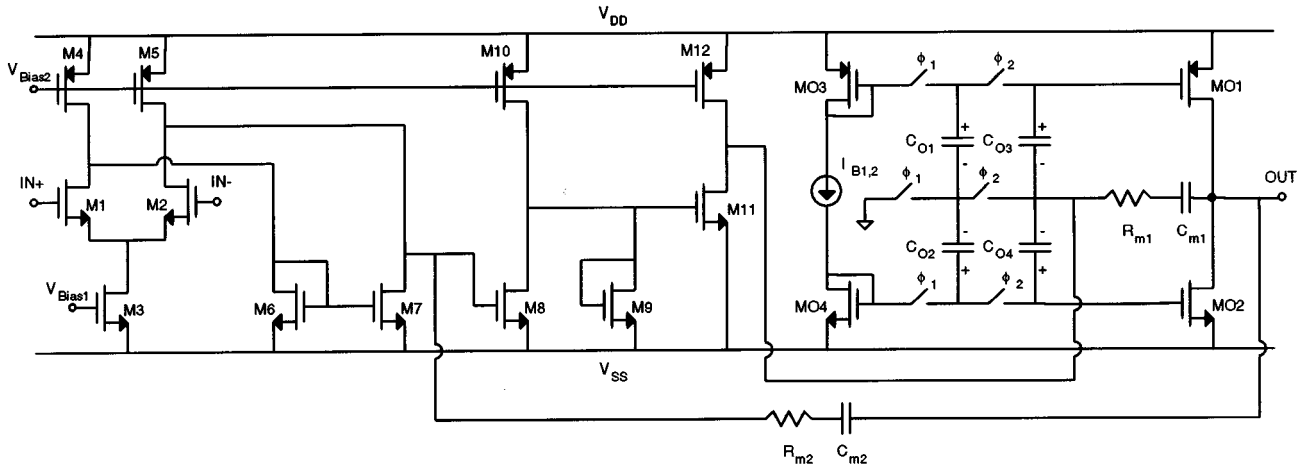

Fig. 4. Schematic of the operational amplifier.

TABLE I
PARAMETERS OF THE FREQUENCY RESPONSE

A_0	$-2 \cdot g_{m1,2} r_{o1} \cdot g_{m11} r_{o2} \cdot g_{mo1,2} R_L$
GBW	$\frac{g_{m1,2}}{2\pi C_{m2}}$
s_{p1}	$-\frac{1}{2 \cdot C_{m2} r_{o1} \cdot g_{m11} r_{o2} \cdot g_{mo1,2} R_L}$
s_{p2}	$-\frac{g_{m11}}{C_{m1}}$
s_{p3}	$-2\frac{g_{mo1,2}}{C_L}$
s_{z1}	$-\frac{1}{C_{m1}}\left(R_{m1}-\frac{1}{2g_{mo1,2}}\right)$
s_{z2}	$-\frac{1}{C_{m2}}\left(R_{m2}-\frac{1}{2g_{mo1,2}}\right)$

TABLE II
COMPONENT VALUES AND BIAS CURRENTS

Component	Value	Current
Main Amplifier		
M1, M2	60/2	5 μA
M3	120/4	10 μA
M4, M5	40/4	10 μA
M6, M7	30/4	5 μA
M8	30/2	12 μA
M9	6/1.4	3 μA
M10	30/2	15 μA
M11	90/4	15 μA
M12	60/4	15 μA
MO1	420/1.4	50 μA
MO2	140/1.4	50 μA
MO3	42/1.4	5 μA
MO4	14/1.4	5 μA
C_{O1}, C_{O2}	1 pF	
C_{O3}, C_{O4}	2.5 pF	
C_{m1}	13 pF	
R_{m1}	2.5 kΩ	
C_{m2}	7.7 pF	
R_{m2}	2.36 kΩ	
Clock Booster		
MB1, MB3, MB4, MB5	2/1.2	
MB2	5/1.2	
C_{B1}	3 pF	

The expressions of the gain, the gain-bandwidth product, and the main poles and zeros of the frequency response are summarized in Table I. Resistances r_{o1}, r_{o2}, and R_L are the output resistances of the input stage, the intermediate stage, and the load resistance, respectively.

III. EXPERIMENTAL RESULTS

The circuit was fabricated in a standard 1.2-μm CMOS process with threshold voltages around 0.75 V for both PMOS and NMOS transistors. The power supply was set to 1.2 V. Component values and bias currents are shown in Table II. With the clock frequency is set to 100 kHz, the power dissipation is equal to 150 μW and the power-supply current has a ripple less than 10%.

Step response measurements were carried out with the amplifier in a noninverting configuration and with a closed-loop gain of six (around 15 dB) by loading the output with 20 pF in parallel to 1 kΩ. Figs. 5 and 6 show the rising and the falling edge of the step response, respectively, for an input voltage of 100 mV. The settling time at 1% is 1.6 μs, and the slew rate is 0.54 V/μs.

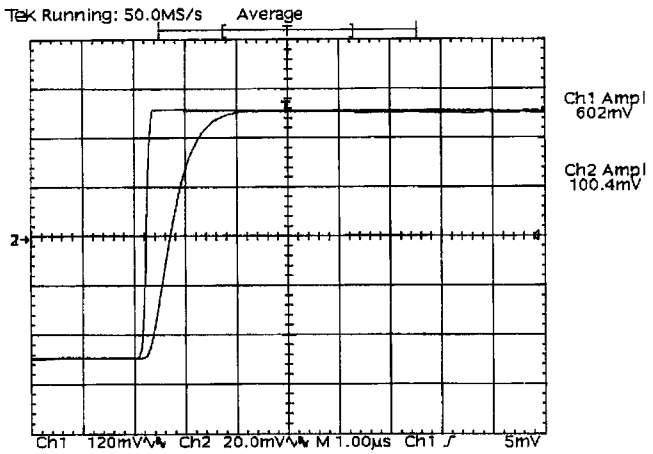

Fig. 5. Positive step response.

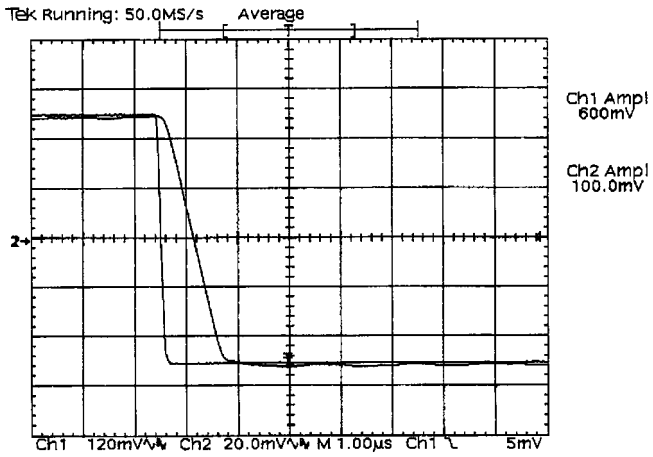

Fig. 6. Negative step response.

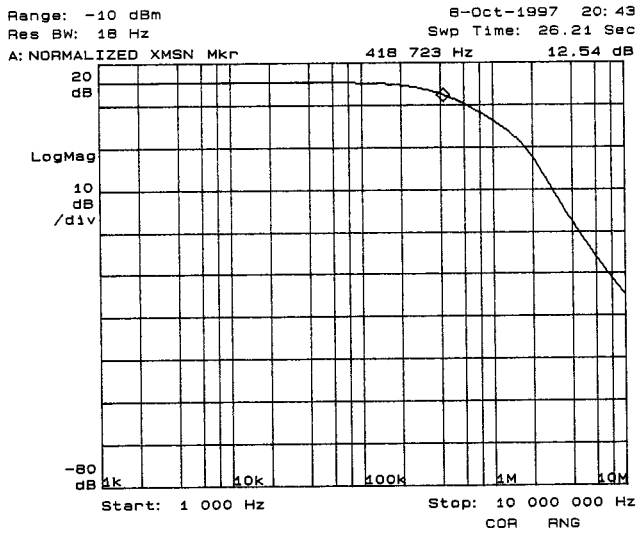

Fig. 7. Closed-loop frequency response.

For the same configuration, the closed-loop frequency response is shown in Fig. 7. Measurements with unity feedback of gain-bandwidth product and phase margin were also carried out,

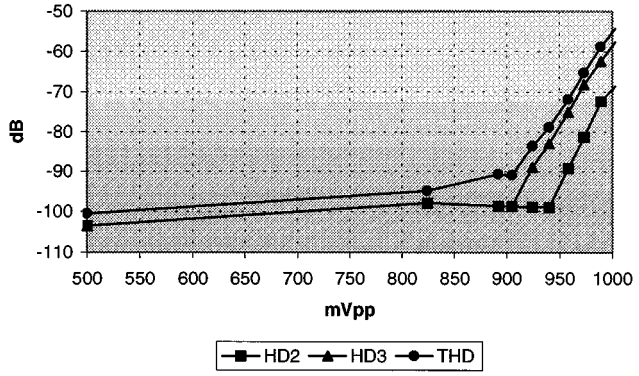

Fig. 8. HD2, HD3, and THD versus output voltage ($R_L = 1\ \mathrm{k}\Omega$).

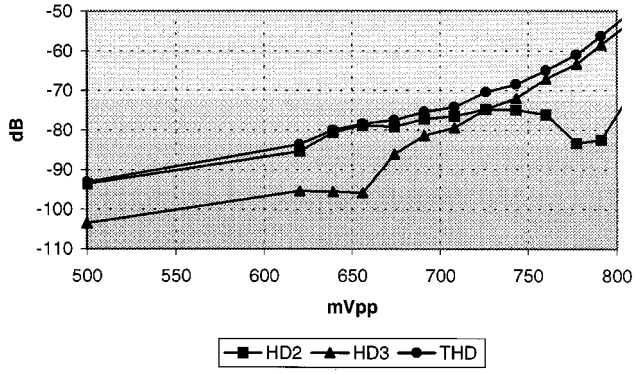

Fig. 9. HD2, HD3, and THD versus output voltage ($R_L = 500\ \Omega$).

TABLE III
MEASURED MAIN PERFORMANCE

Open Loop Gain (R_L=1 kΩ)	> 90 dB
GBW	2.2 MHz
Phase Margin (R_L=1 kΩ , C_L=20 pF)	56°
Settling Time (1%) (R_L=1 kΩ , C_L=20 pF)	1.6 µs
Slew Rate (R_L=1 kΩ , C_L=20 pF)	0.54 V/µs
THD @ 1 kHz (V_{out}=700 mV_{pp} , R_L=500 Ω)	-74 dB
Offset	9 mV
Power Dissipation	150 µW
Die Size	0.2 mm^2

resulting in 2.2 MHz and 56°, respectively. The output voltage ripple due to the switching activity is less than 1 mV.

The maximum efficiency of the output stage is close to 45% for a 1-V peak-to-peak output signal. It decreases linearly with the decreasing of the output voltage with a slope of $115 \cdot 10^{-3}$%/mV.

Total harmonic distortion (THD) measurements were carried out for two different resistive loads and with a 1-kHz input signal frequency. Then measures for the unity-gain configuration were extrapolated and plotted in Figs. 8 and 9 for a resistive load of 1 kΩ and 500 Ω, respectively. Despite the low aspect ratios of the

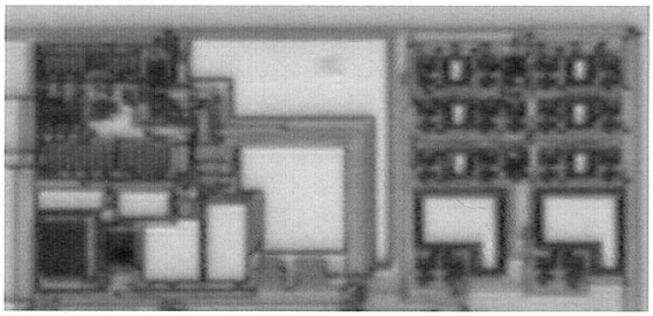

Fig. 10. Chip photo.

NMOS and PMOS output transistors (140/1.4 and 420/1.4) and the low quiescent output current (50 μA), very good linearity performance is achieved. Indeed, THD is around -70 dB for an output swing that is 80% and 60% of the power-supply value with a 1-kΩ and a 500-Ω load, respectively.

Main electrical parameters are summarized in Table III, and a die photo is shown in Fig. 10.

IV. Conclusion

A 1.2-V CMOS operational amplifier has been presented that is based on a novel class-AB output stage. The SC approach has been used to overcome the swing limitation coming from the low supply voltage in the output stage and to provide both high overdrive and accurate current. This has been achieved with a small increase in circuit complexity and in layout area.

The clock phases to drive the switches were derived by a clock booster. If the circuit is not used in more general SC signal processing, the master clock can easily be implemented with a simple oscillator since no accuracy or frequency stability is required.

The very good linearity performance achieved validates the proposed solution.

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