BOISE STATE UNIVERSITY

# Understanding Design and Operation of Successive Approximation Register (SAR) ADC

ECE 614 - Spring '08

April 28,2008

By Prashanth Busa

# Talk Outline

- Various ADC Architectures
- SAR ADC Introduction and Operation
- Charge Redistribution SAR ADC
- Different SAR ADC topologies
- Comparison with other ADCs
- Summary

# Various ADC Architectures

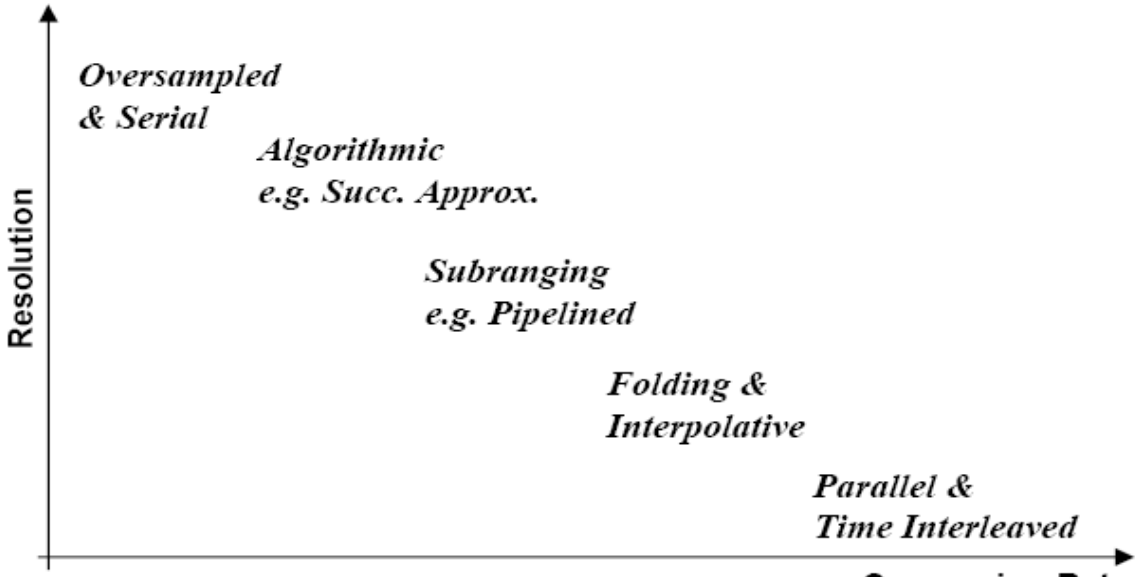


Figure from ref [2]

- Plot of Resolution vs Conversion rate.
- SAR ADCs are available from 8-18 bits resolution with sampling rates up to 5Msps.
- Higher accuracy, low power and used in medium speed/medium-high resolution applications.

# SAR ADC History

- 19" × 15" × 26"
- 150 lbs
- $8,500.00


Courtesy,
Analogic Corporation
8 Centennial Drive
Peabody, MA 01960

http://www.analogic.com

- First commercial converter, 1954 "DATRAC" 11-Bit, 50-kSPS SAR ADC Designed by Bernard M. Gordon at EPSCO.
- Today, the state of the art SAR ADC reported is 18 bit, 2Msps fully differential with a single power supply of 2.5v.

# Successive Approximation ADC

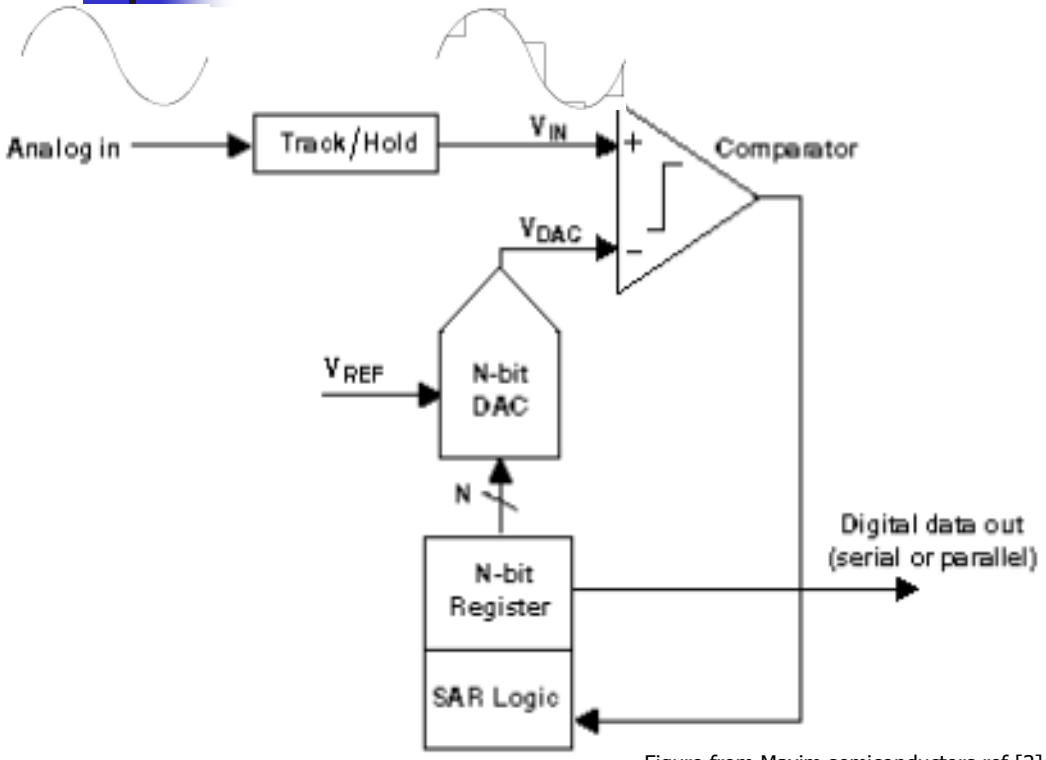
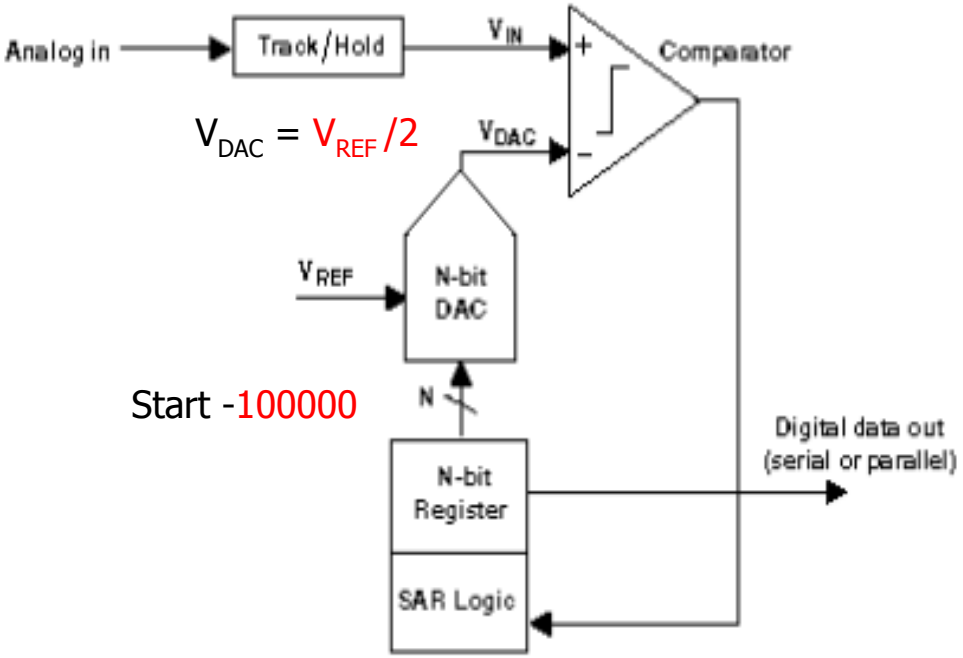



Figure from Maxim semiconductors ref [3]

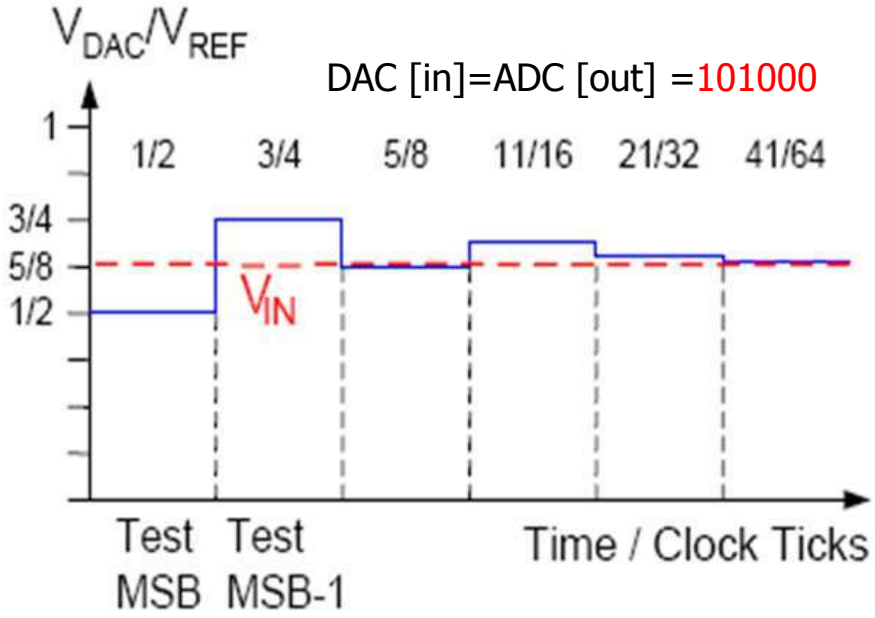
Simplified SAR ADC Architecture

- Implements Binary search algorithm
- Initially, DAC input set to midscale (MSB =1)
- $V_{IN} < V_{DAC}$ , MSB remains 1
- $V_{IN} > V_{DAC}$ , MSB set to 0
- Algorithm is repeated until LSB
- End of algorithm, DAC [input] = ADC [output]
- N cycles required for N-bit conversion

# SAR Operation




Simplified SAR ADC Architecture




A 6-bit SAR ADC Example, $V_{IN} = 5/8\ V_{REF}$

# SAR Timing diagram

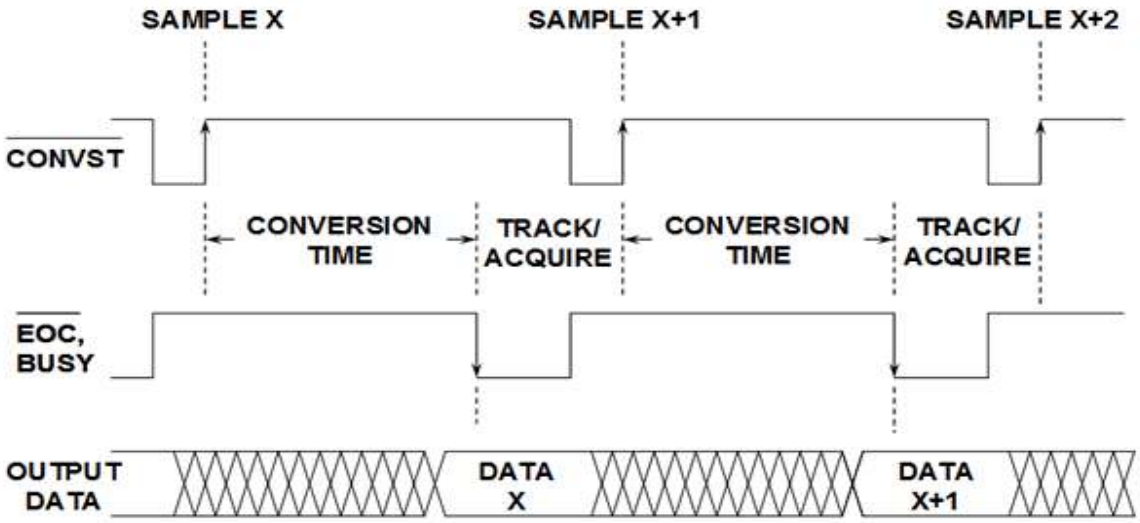
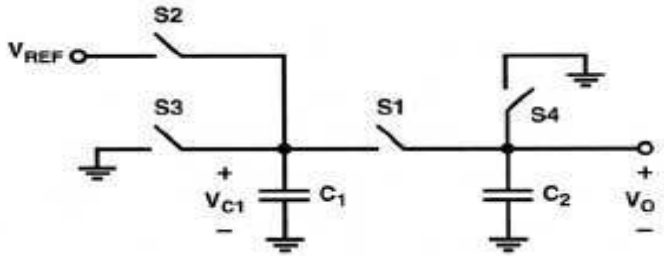



Figure from Analog Devices, ref[4]

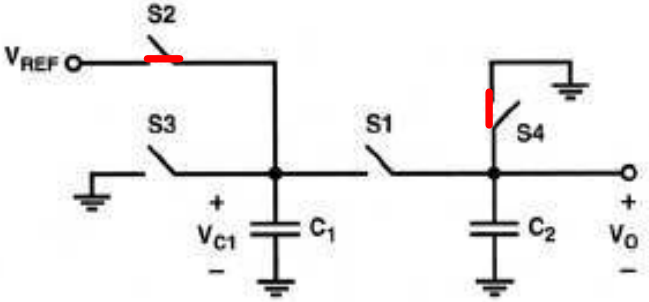
- The positive going edge of $\overline{\text{CONVST}}$ indicates the start of conversion, the input sample and hold is in the hold mode from this edge and various bits are determined using SAR algorithm.
- When $\overline{\text{CONVST}}$ goes low the busy signal goes high and the BUSY line goes low at the end of conversion process.

# A simple Charge Redistribution DAC

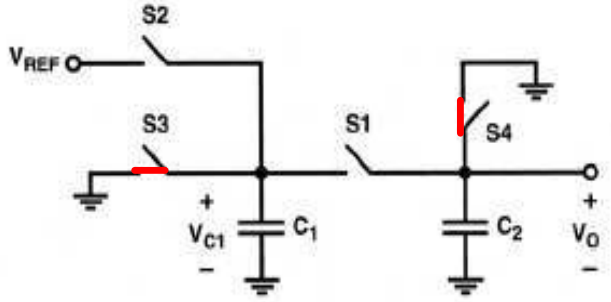
Assuming C1=C2



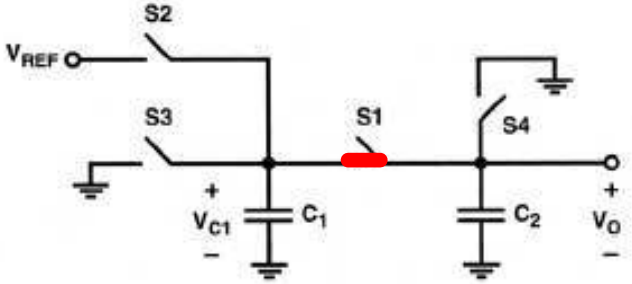

Charging C1 to Vref, C2 grounded




Discharging C1,C2 – S3 and S4 closed

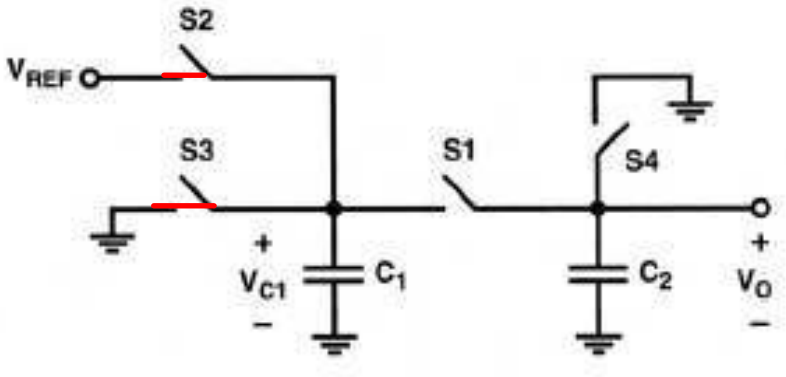


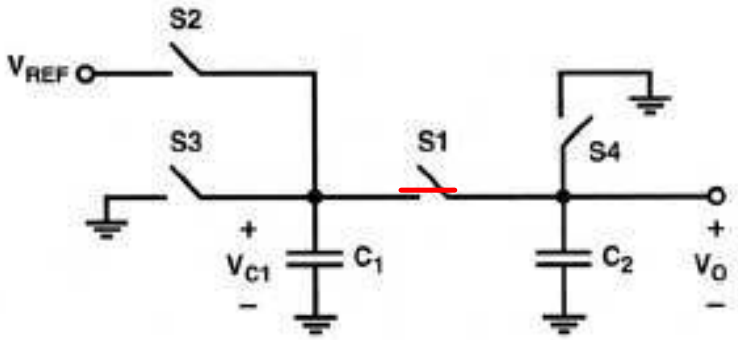

Charge sharing C1,C2 –> $V_0$ = Vref/2




Figures from ref[2]

# Simple Charge redistribution DAC cont'd




If bit =1, S2 is closed

=0, S3 is closed

Depending on input,

$V_0 = (V_{ref}/2 + V_{ref}/4)$ for S2 closed (b=1)

$= V_{ref}/4$ for S3 closed (b=0)

Figures from ref[2]

# Charge Redistribution SAR ADC

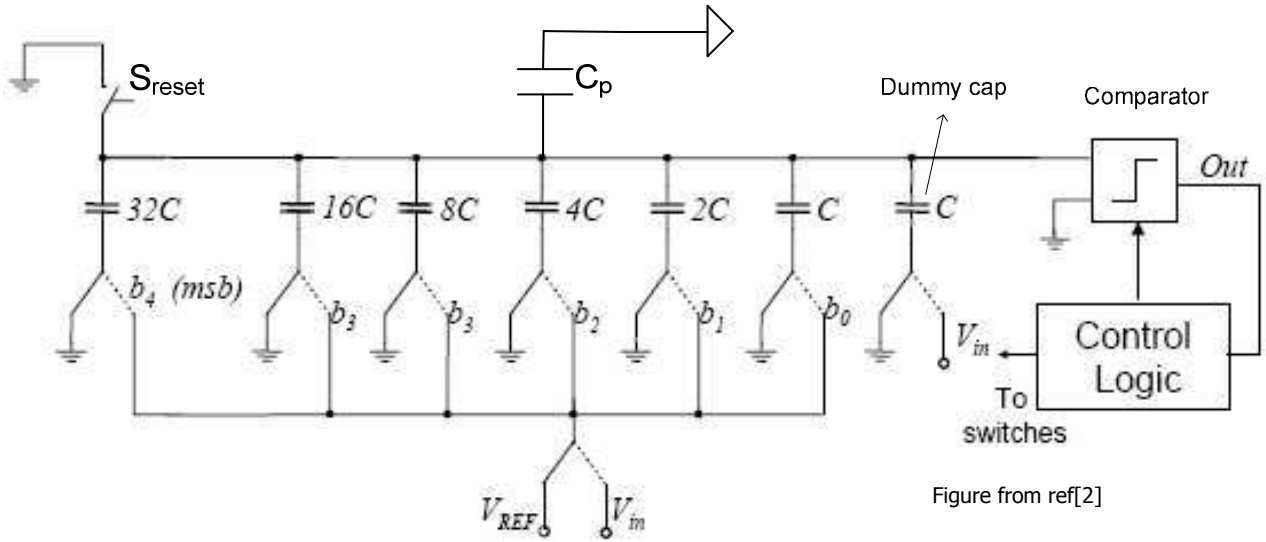
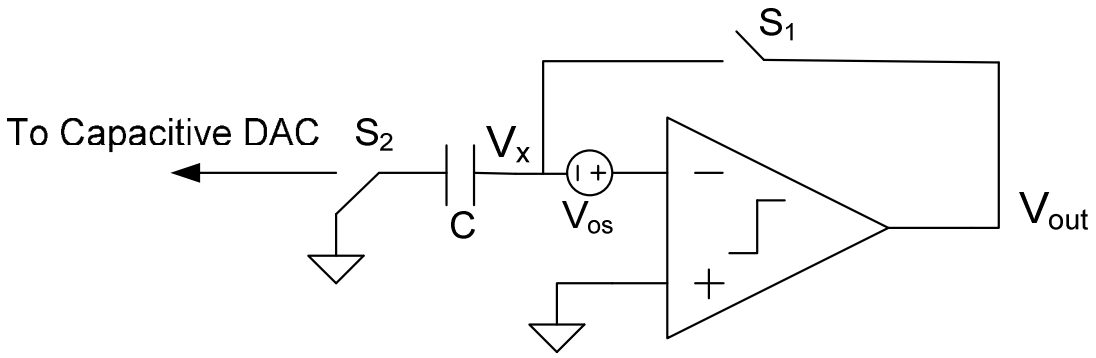



Figure from ref[2]

- Provides inherent T/H operation.
- Initially, $S_{reset}$ is grounded and all the capacitors connected to $V_{IN}$.
- MSB top plate is opened and MSB cap bottom plate connected to $V_{REF}$ resulting in $-V_{IN} + V_{REF}/2$ on the input of comparator.
- If $-V_{IN} + V_{REF}/2 > 0$ ,MSB =0 else MSB =1.
- Next cycle MSB-1 bit is connected to $V_{REF}$ ,algorithm is repeated until LSB.

# Charge Redistribution SAR ADC Cont'd..




Comparator Offset Cancellation

- Comparator offset needs to addressed.
- Switch S1 is closed, S2 is grounded, storing the offset voltage across the capacitor.
- Now, $V_x > V_{os}$ result in $V_{out}$ going high and $V_x < V_{os}$ results $V_{out}$ going low.
- Parasitic capacitance on the top plate is not a concern due to the presence of global negative feed back.

# INL and DNL Calculations

- Linearity of the ADC depends on the capacitor ratio (matching).
- Process should have good capacitors.
- INL is defined as,

  $$|INL|_{max} = 2^{N-1}(C+|\Delta C|_{max,INL})- 2^{N-1} C = 2^{N-1}|\Delta C|_{max,INL}$$

- For INL to be less than ½ LSB, maximum ΔC is

  $$|\Delta C|_{max,INL}= C/2^{N}$$

- DNL is defined as,

  $$|DNL|_{max} = (2^{N} – 1) |\Delta C|_{max,DNL.}$$

- For DNL to be less than ½ LSB, maximum ΔC is

  $$|\Delta C|_{max,DNL}= C/(2^{N+1}-2).$$

- MSB capacitor accuracy is more critical in determining the DNL!!

From ref[1]

# Charge Redistribution SAR Tradeoffs

Advantages:

- Low power dissipation.
- Inherent T/H operation.
- Offset cancellation is incorporated.
- Requirement of less analog circuitry.

Disadvantages:

- Need of good capacitive material.
- Large capacitors, making matching difficult.
- Not inherently monotonic.

# Other Charge Redistribution topologies

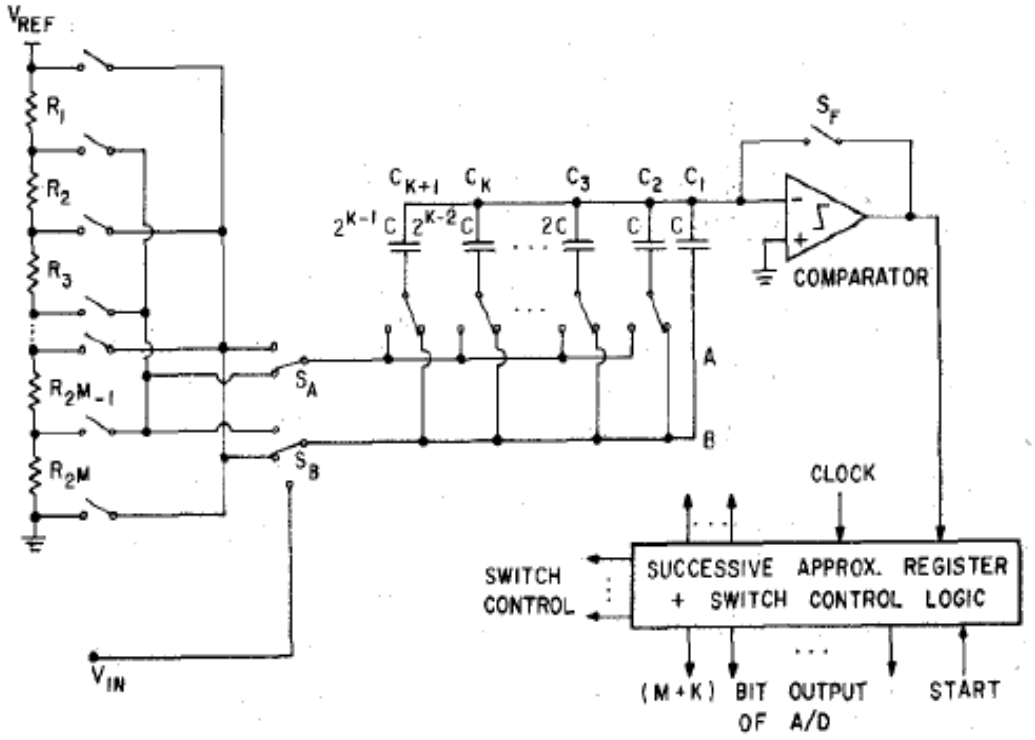



Figure from ref [5]

SAR hybrid ADC Architecture

- Resistor DAC for MSBs and Capacitors for LSBs.
- Operation starts by closing $S_F$ and charging top plate to $V_{IN}$ - $V_{OS}$. Next $S_F$ is opened and a search is performed in the resistive divider. Finally bottom plates of capacitors are switched from $S_A$ and $S_B$ to converge to $V_{OS}$.
- ADC is inherently monotonic and there will be no missing codes.

# SAR ADC Configurations

- A commonly used Figure of merit (FOM) for ADC's in terms of resolution, bandwidth and power dissipation is given by,

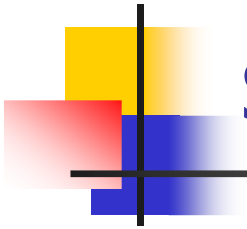
$$FOM = \frac{10^{(SNR[dB]-1.78[dB])} \text{x } (\frac{\text{Sampling rate}}{2})}{\text{power dissipation}}$$

From ref [6]

- Lower power dissipation gives higher FOM, hence techniques like Switched opamp, reset opamp circuits and boot-strapping techniques have been explored using Successive Approximation ADC's operating at lower VDDs.

# SAR vs other ADCs

- A pipelined ADC introduces latency, consumes more power and takes up more area for same resolution. Also requires calibration for more than 12 bits resolution like SAR.
- Flash ADC is much faster, less accurate and takes more silicon area due to the number of comparators $2^N$ for N bit resolution.
- Oversampled/Σ-Δ ADCs have low conversion rates, high precision, averaging noise and no requirement for trimming or calibration even up to 16 bits of resolution.
- Power dissipation of SAR ADCs vary with the sampling rate unlike Flash and Pipeline architectures. Hence find applications in PDAs.

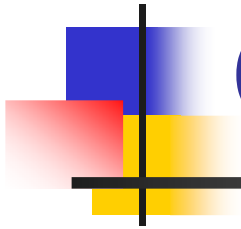


# SAR Summary

- Critical components are DAC and comparator.
- Settling time of DAC must be less than ½ LSB and determines the speed of conversion.
- Accuracy of the DAC is critical since an incorrect decision could result in ending up the value in wrong leg of binary tree.
- Comparator should resolve small differences between $V_{IN}$ and $V_{DAC}$.
- The clock frequency should be equal to the sampling frequency multiplied by the number of bits.
- SAR ADCs are efficient, easy to understand and ideally suited for modern CMOS processes.

# References


- [1] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation, Revised Second Edition*, Wiley-IEEE, 2008
- [2] http://webcast.berkeley.edu/EE 247
- [3] http://www.maxim-ic.com/appnotes.cfm/an_pk/1080
- [4] http://www.analog.com/
- [5] David A. Hodges, Bahram Fotouhi "High-Resoultion A/D conversion in MOS/LSI" *IEEE Journal of Solid-State Circuits*, vol. SC-14, no 6**,** December 1979
- [6] R. Thewes J. Sauerbrey, D. Schmitt-Landsiedel "A 0.5-V 1-uW Successive Approximation ADC " *IEEE Journal of Solid-State Circuits*, vol. 38,no 7,July 2003



# Questions ??

# Pipeline ADC

Bill Filipiak
ECE 614

# Overview

- Basic Operation
- Advantages/Disadvantages
- Ideal/Non-Ideal Switching Points
- INL/DNL
- S/H Design
- 1.5 Bits/Stage
- Summary

# Basic Operation

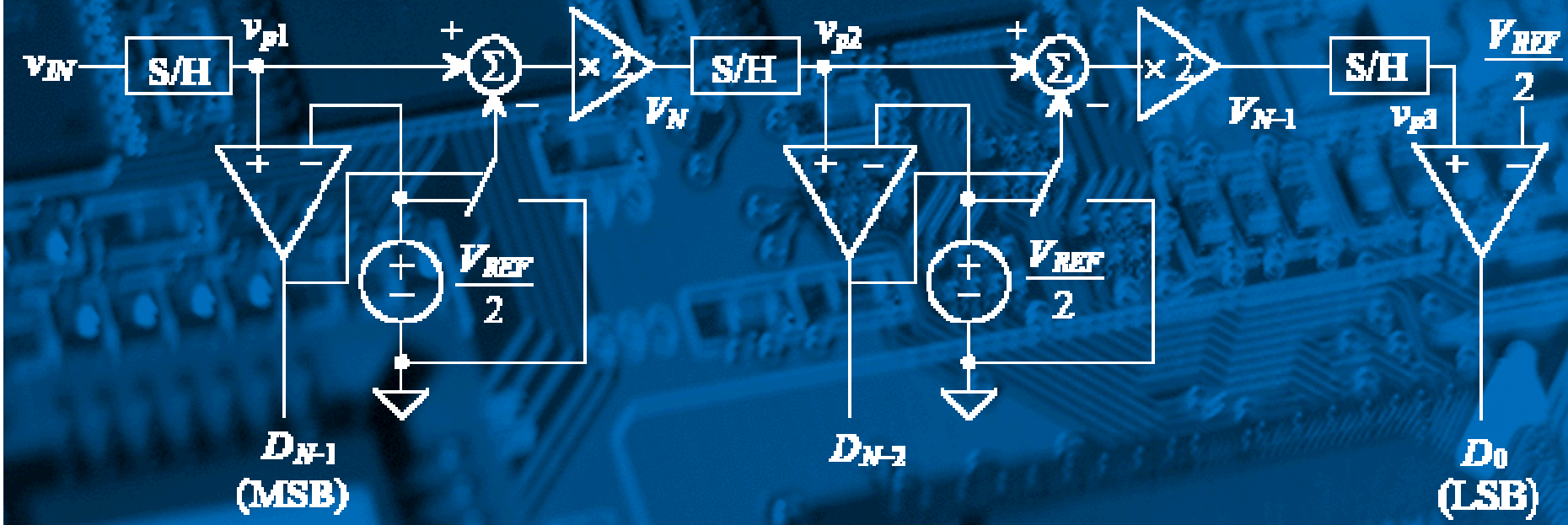
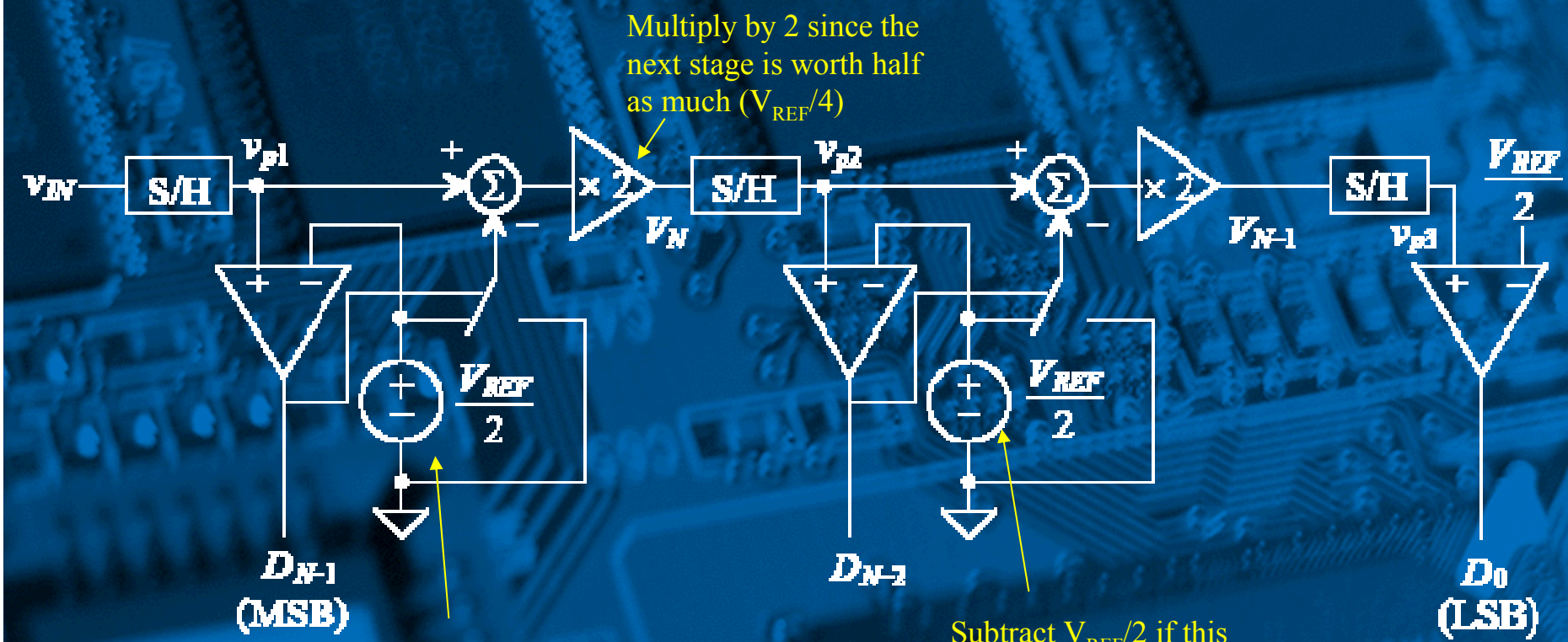



Figure 29.30

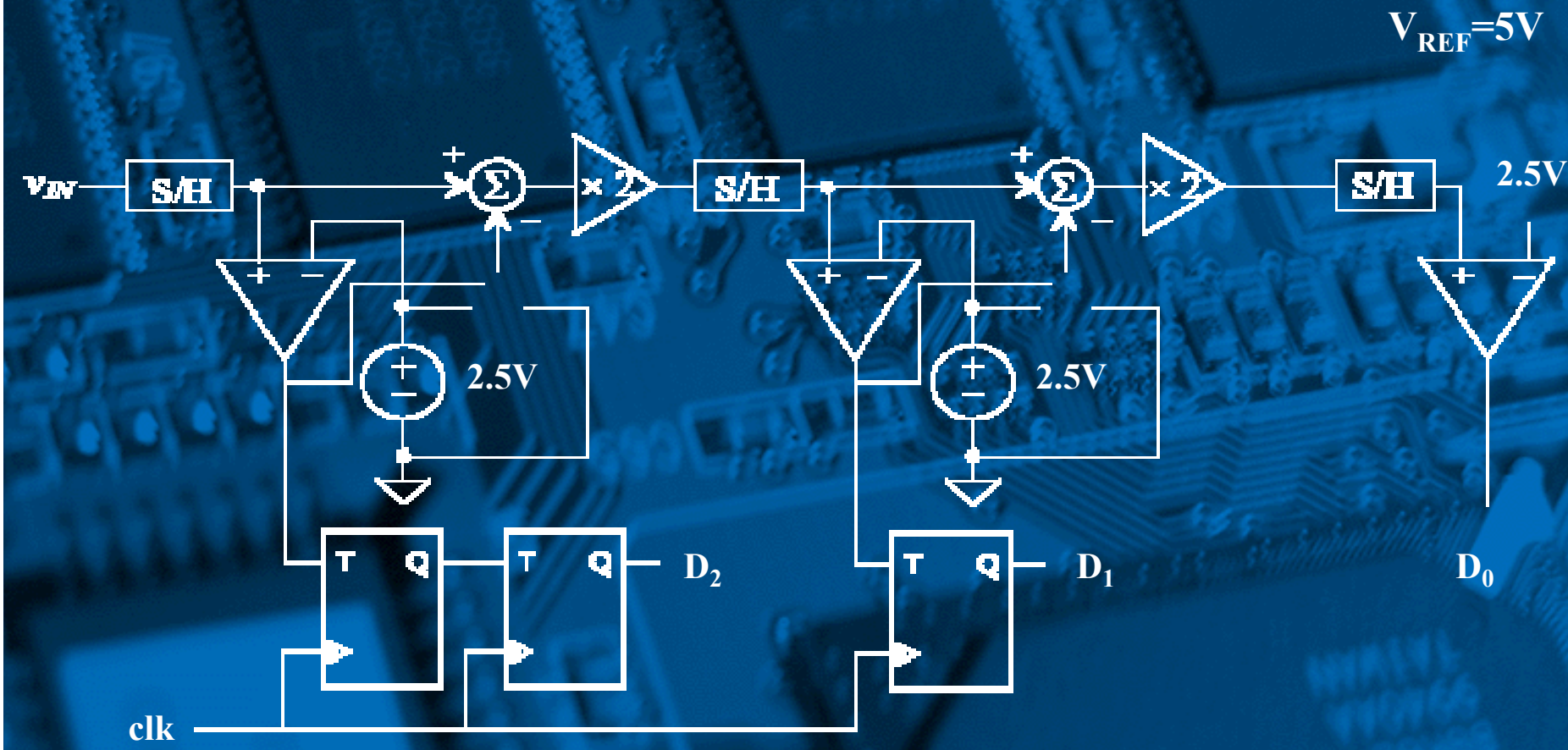
# Basic Operation




Digital Value (2.5V for a 1 and 0 V for a 0) + ½ of the analog output must always equal the input for each stage

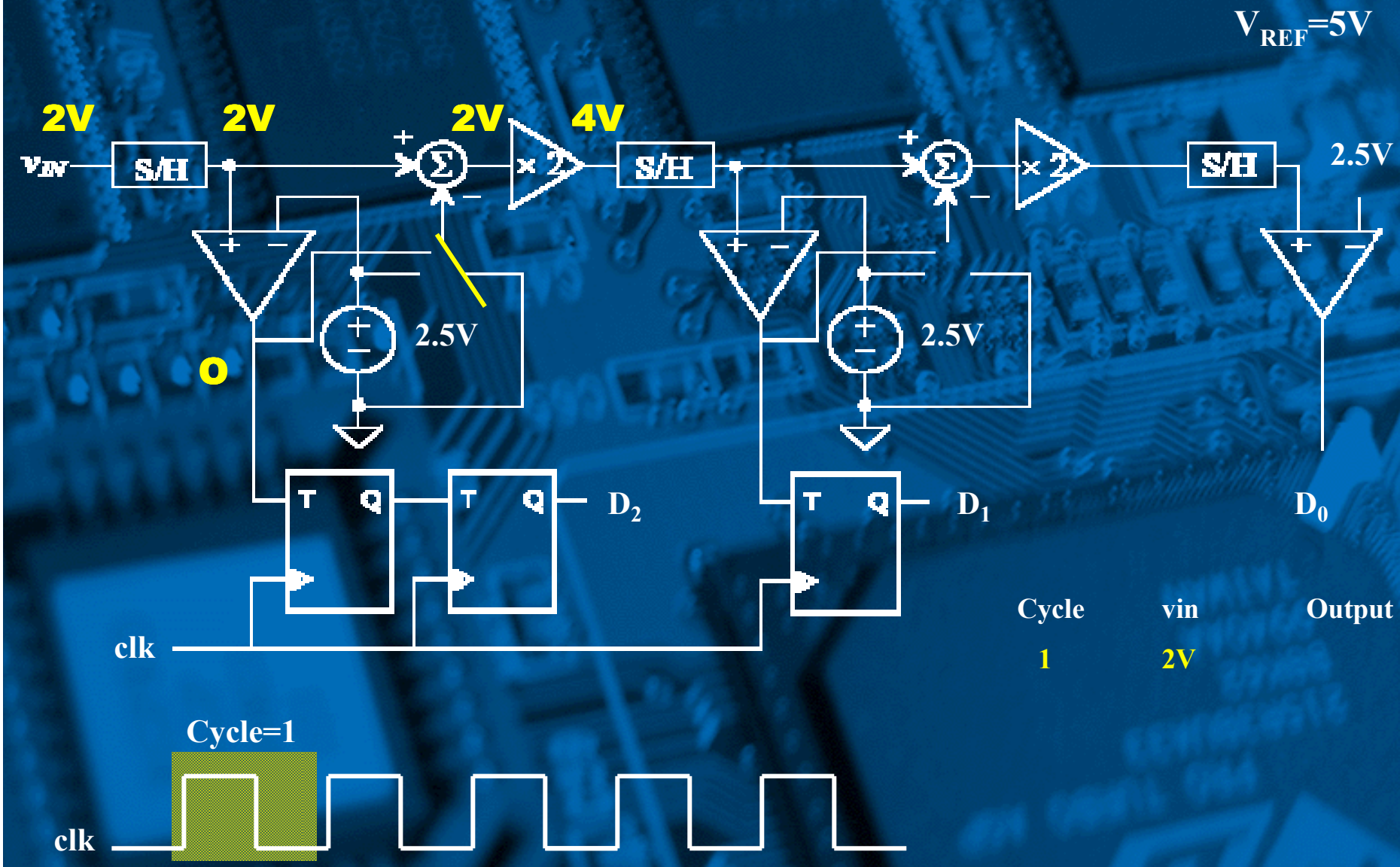
**Figure 29.30**

# Basic Operation

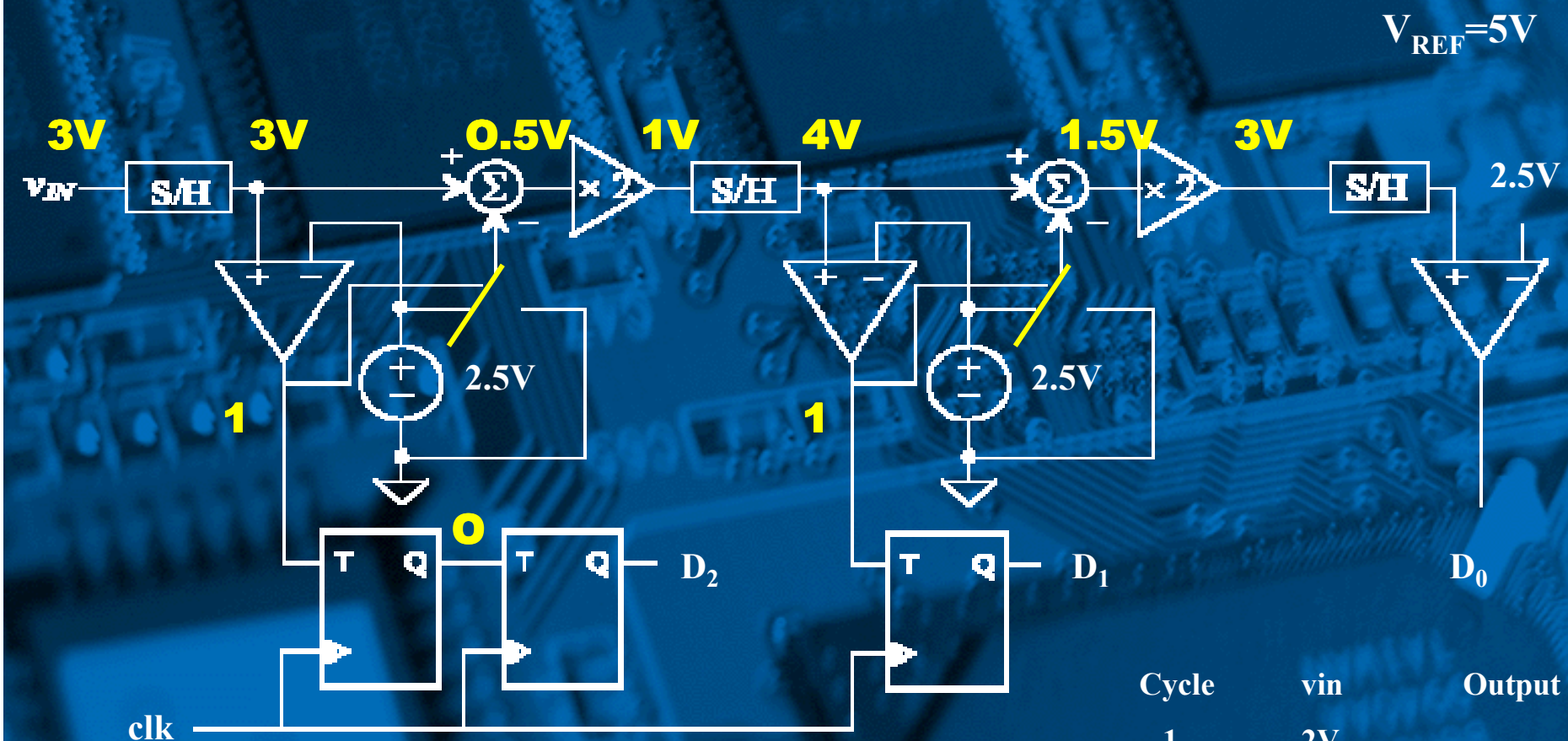



Adapted from Figure 29.30

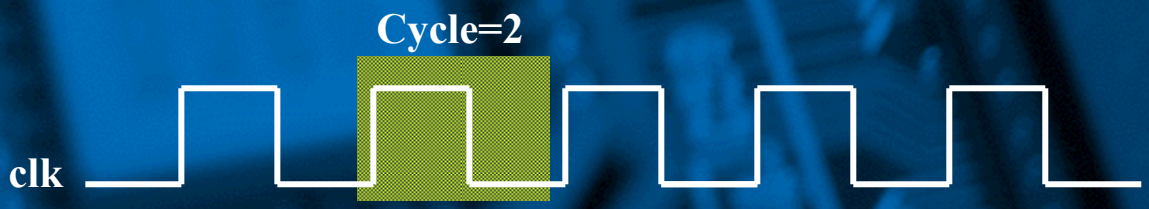
# Basic Operation



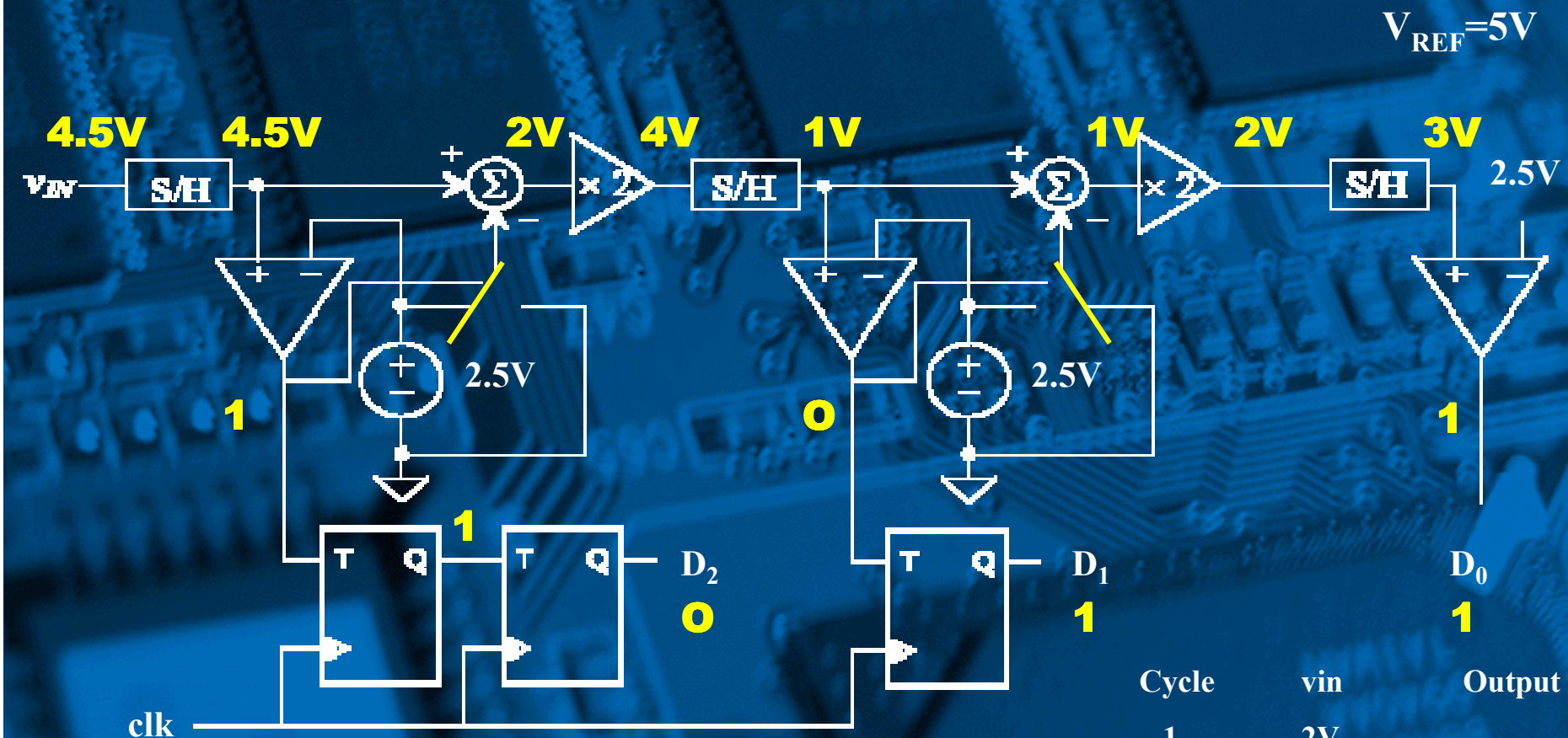
# Basic Operation



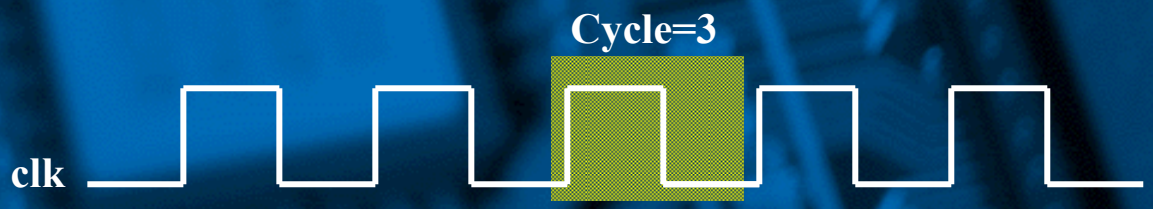

| Cycle | vin | Output |
|---|---|---|
| 1 | 2V | |
| 2 | 3V | |



# Basic Operation




| Cycle | vin | Output |
|---|---|---|
| 1 | 2V | |
| 2 | 3V | |
| 3 | 4.5V | 011 |



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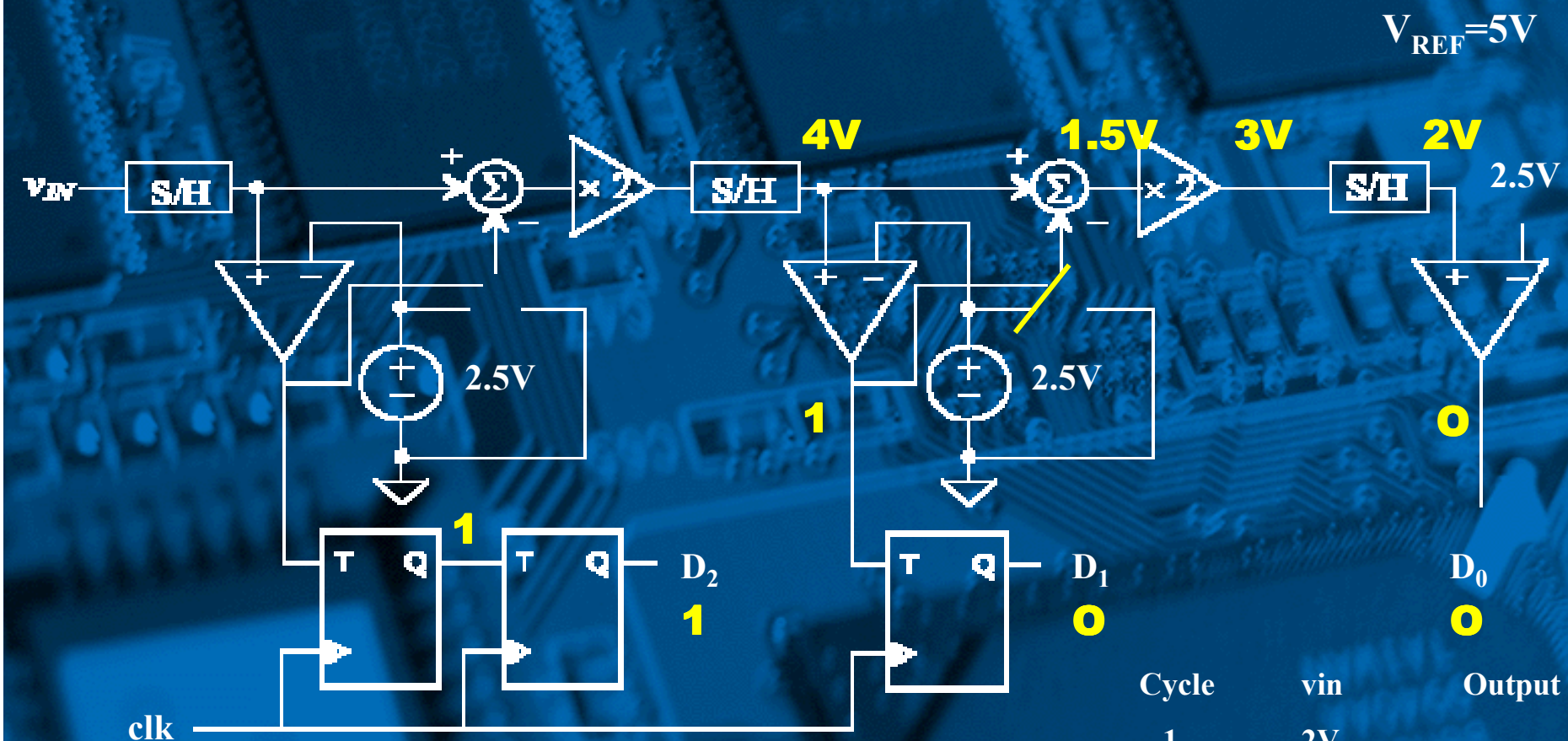
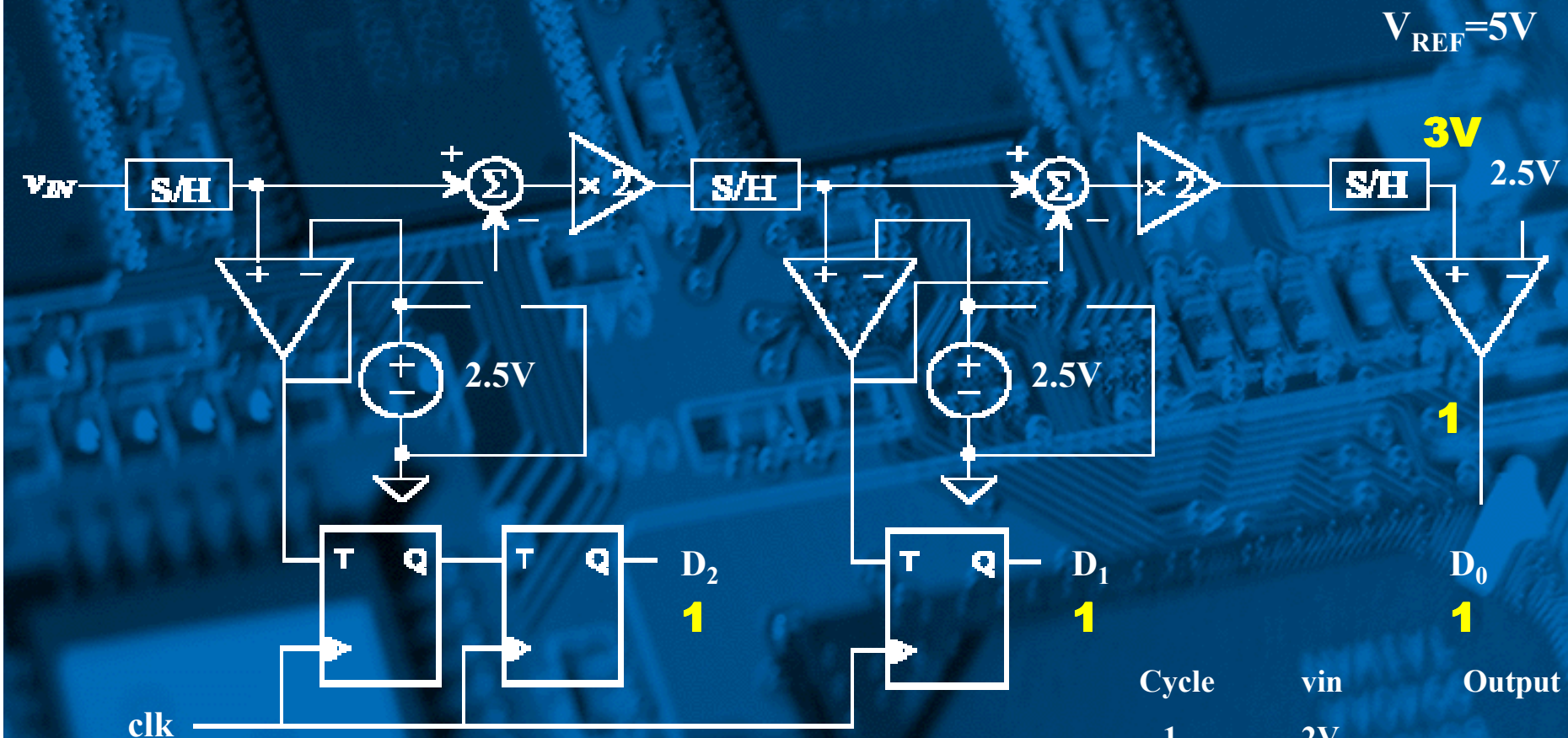



| Cycle | vin | Output |
|---|---|---|
| 1 | 2V | |
| 2 | 3V | |
| 3 | 4.5V | 011 |
| 4 | | 100 |

# Basic Operation




| Cycle | vin | Output |
|---|---|---|
| 1 | 2V | |
| 2 | 3V | |
| 3 | 4.5V | 011 |
| 4 | | 100 |
| 5 | | 111 |

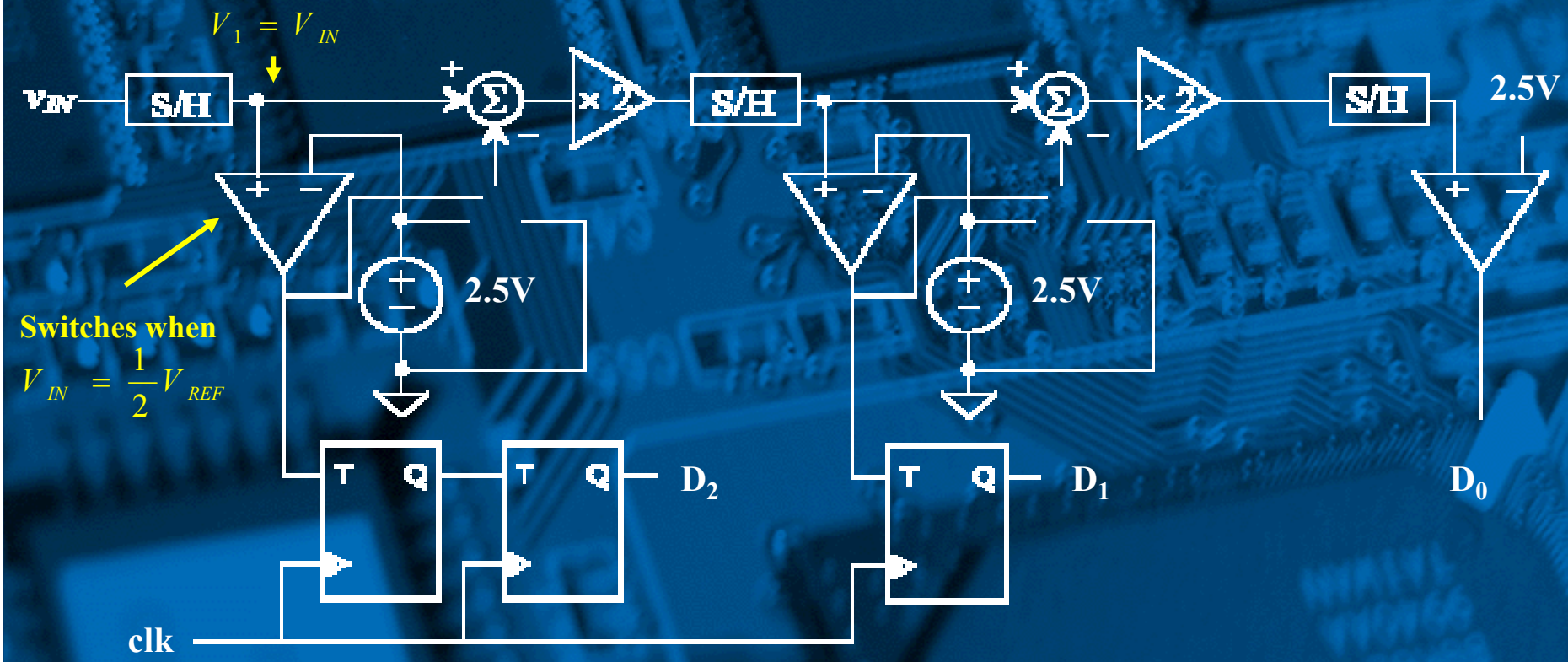
# Advantages

- Low number of comparators (N comparators)
  - Flash ADC requires $2^N$-1 comparators
  - Two-step ADC requires $2(2^{N/2}-1)$ comparators
- High throughput – One conversion is completed per clock cycle
  - Two-step ADC requires two clock cycles per conversion

# Disadvantages

- Latency of N clock cycles before the ADC outputs comparison data
- Errors propagate through system since each stage operates on the residue passed from previous stage
  - Accuracy of most significant stages becomes more important than downstream stages

# Ideal Switching Point



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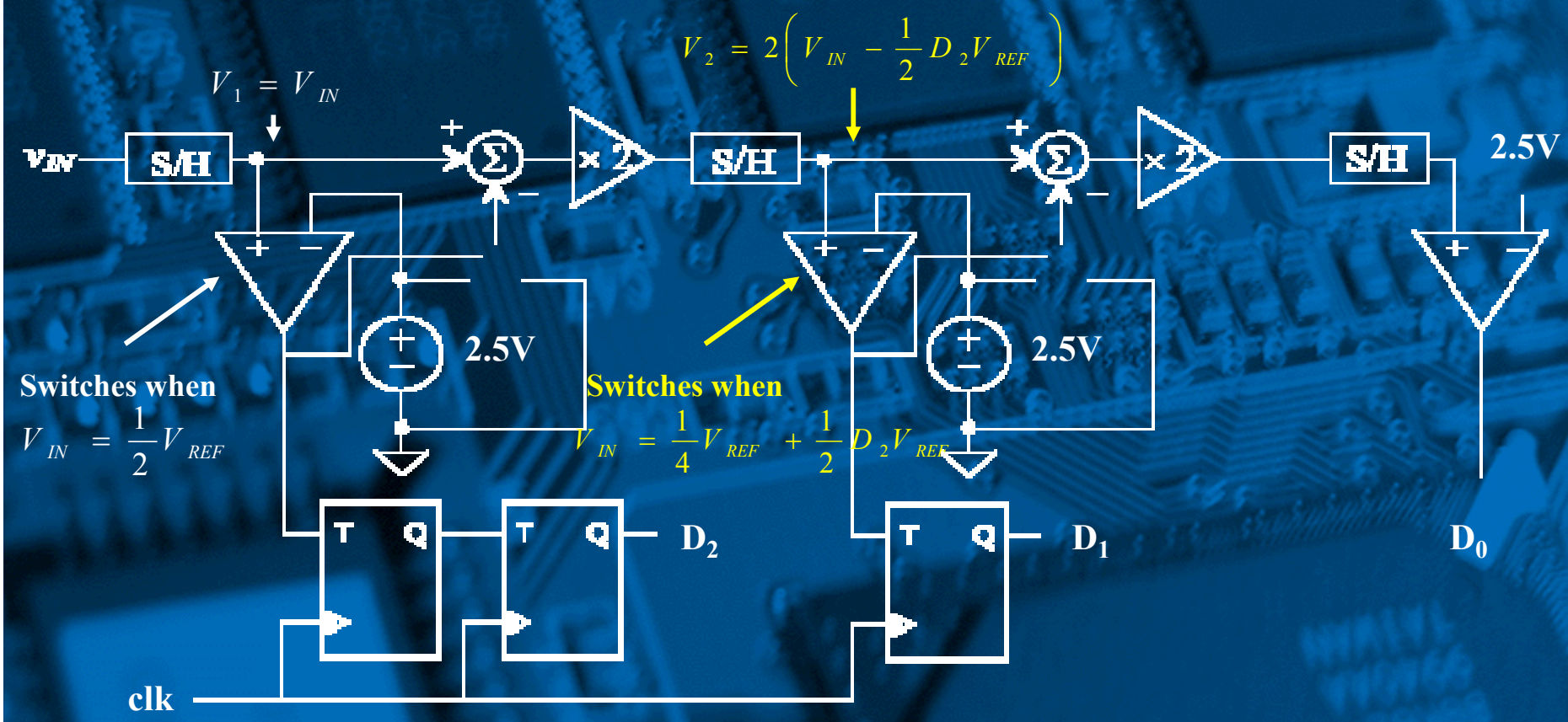
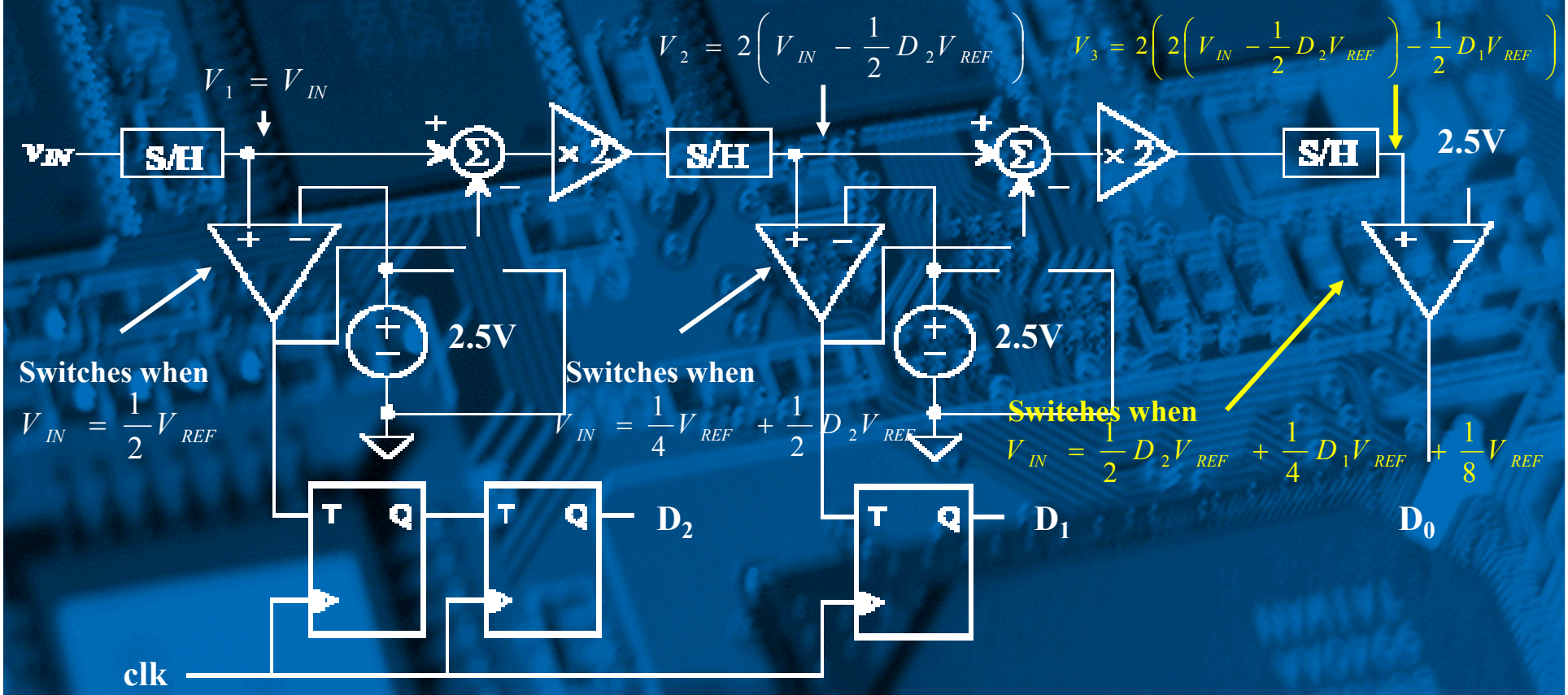


# Ideal Switching Point



# Ideal Switching Point

- 1st comparator switches when:

$$V_{IN} = \frac{1}{2} V_{REF}$$

- 2nd comparator switches when:

$$V_{IN} = \frac{1}{4} V_{REF} + \frac{1}{2} D_2 V_{REF}$$

- 3rd comparator switches when:

$$V_{IN} = \frac{1}{2} D_2 V_{REF} + \frac{1}{4} D_1 V_{REF} + \frac{1}{8} V_{REF}$$

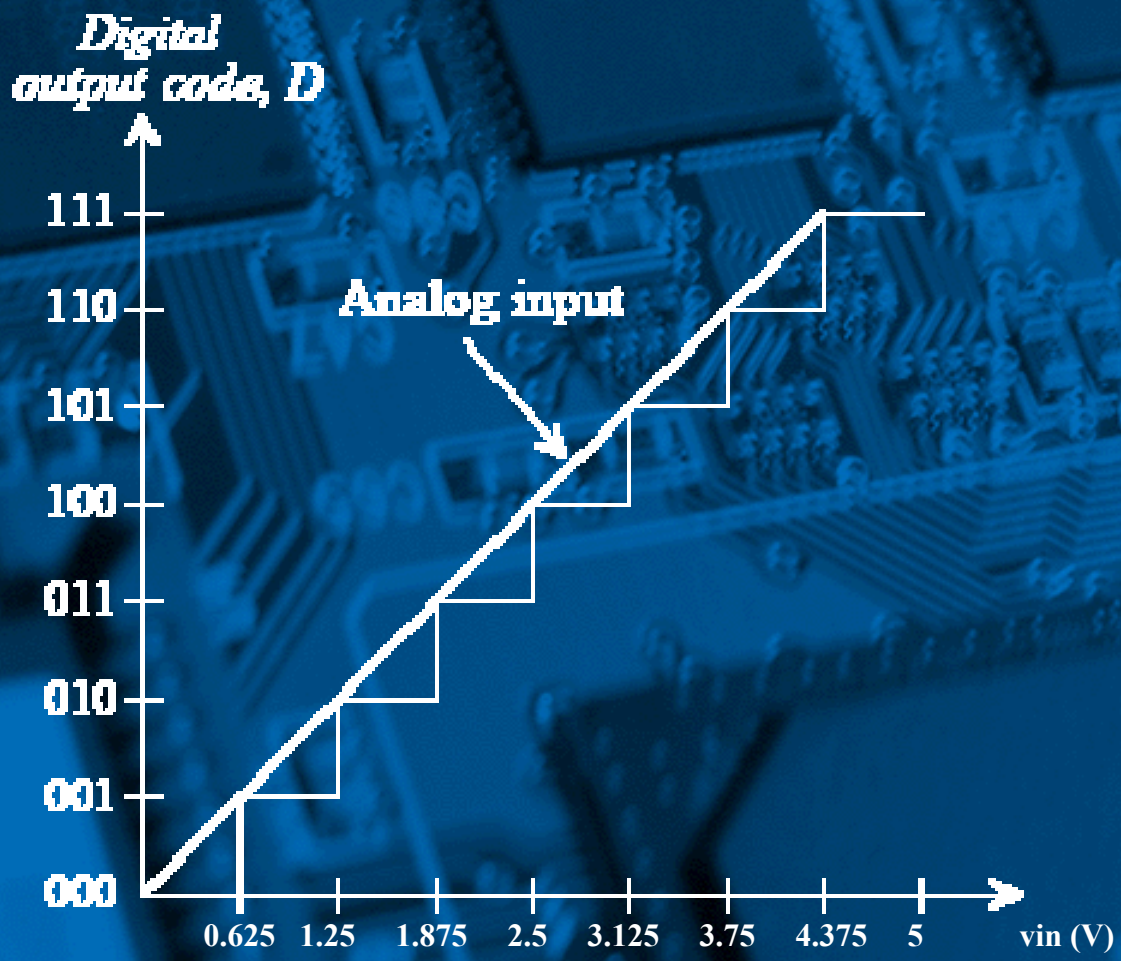
- Nth comparator switches when:

$$V_{IN} = \frac{1}{2} D_{N-1} V_{REF} + \frac{1}{4} D_{N-2} V_{REF} + \frac{1}{8} D_{N-3} V_{REF} + \cdots + \frac{1}{2^{N-1}} D_1 V_{REF} + \frac{1}{2^N} V_{REF}$$

# Quantization

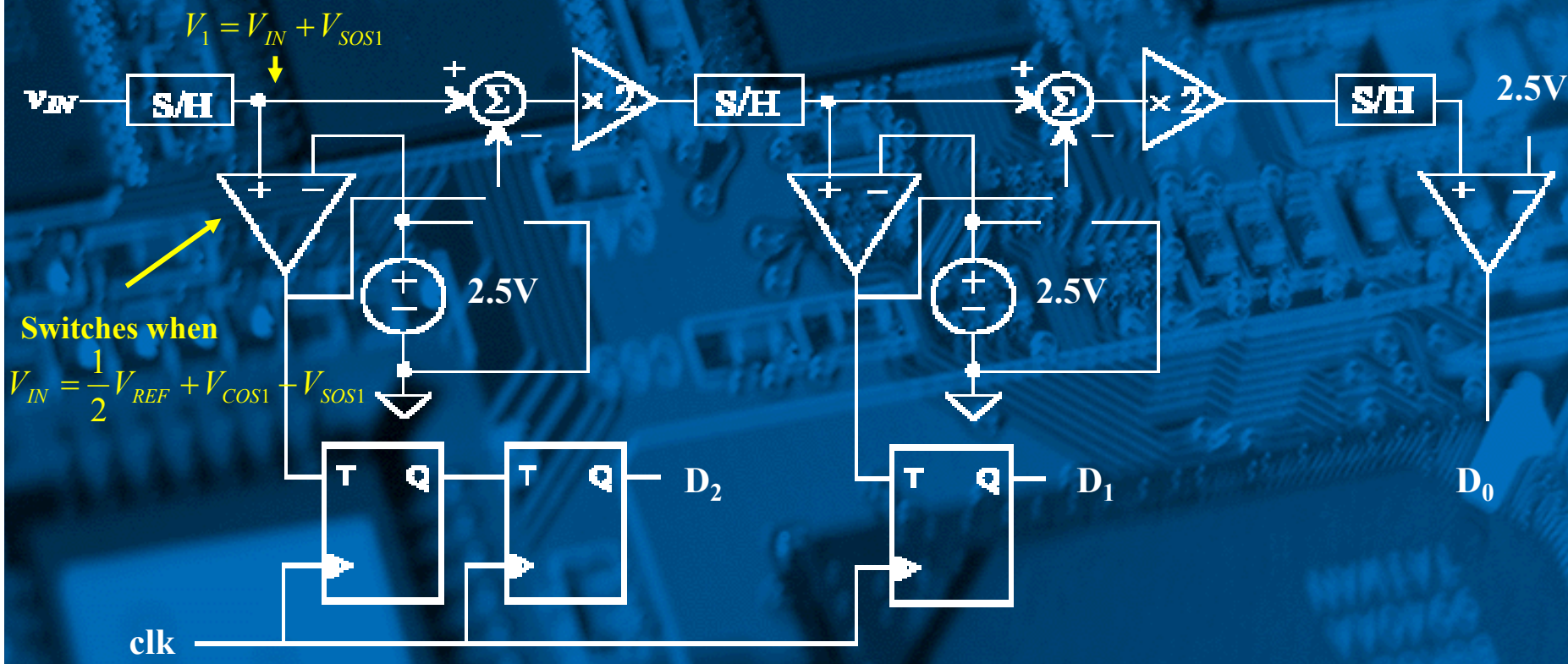
| Digital Output | Input Range | Input Voltage ($V_{REF}$=5V) |
|---|---|---|
| 000 | $0 \rightarrow \frac{1}{8}V_{REF}$ | 0→0.625V |
| 001 | $\frac{1}{8}V_{REF} \rightarrow \frac{1}{4}V_{REF}$ | 0.625V→1.25V |
| 010 | $\frac{1}{4}V_{REF} \rightarrow \frac{1}{4}V_{REF} + \frac{1}{8}V_{REF}$ | 1.25→1.875V |
| 011 | $\frac{1}{4}V_{REF} + \frac{1}{8}V_{REF} \rightarrow \frac{1}{2}V_{REF}$ | 1.875→2.5V |
| 100 | $\frac{1}{2}V_{REF} \rightarrow \frac{1}{2}V_{REF} + \frac{1}{8}V_{REF}$ | 2.5→3.125V |
| 101 | $\frac{1}{2}V_{REF} + \frac{1}{8}V_{REF} \rightarrow \frac{1}{2}V_{REF} + \frac{1}{4}V_{REF}$ | 3.125→3.75V |
| 110 | $\frac{1}{2}V_{REF} + \frac{1}{4}V_{REF} \rightarrow \frac{1}{2}V_{REF} + \frac{1}{4}V_{REF} \quad \frac{1}{8}V_{REF}$ | 3.75→4.375V |
| 111 | $\frac{1}{2}V_{REF} + \frac{1}{4}V_{REF} \quad \frac{1}{8}V_{REF} \rightarrow V_{REF}$ | 4.375→5V |

# Quantization




Adapted from Figure 28.19

# Non-Ideal Switching Point



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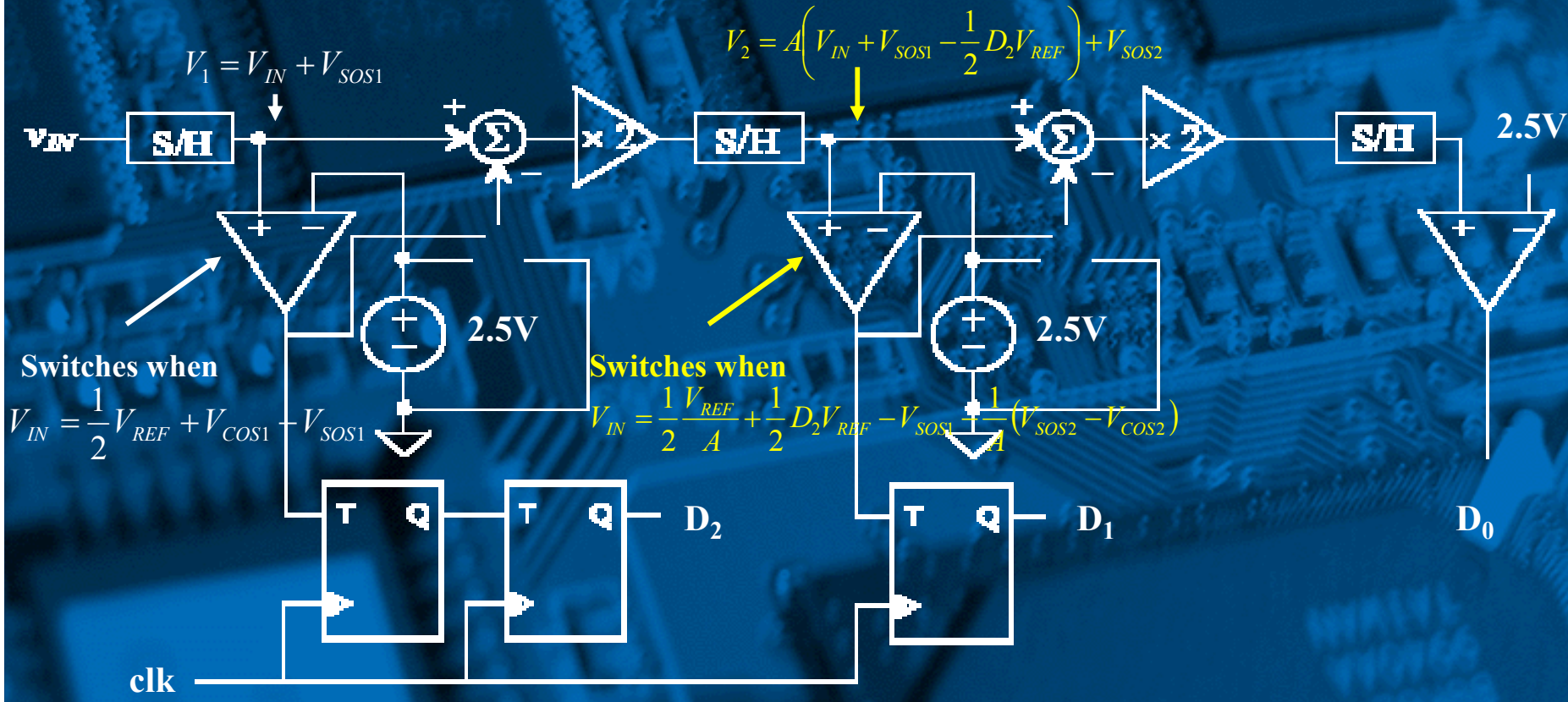
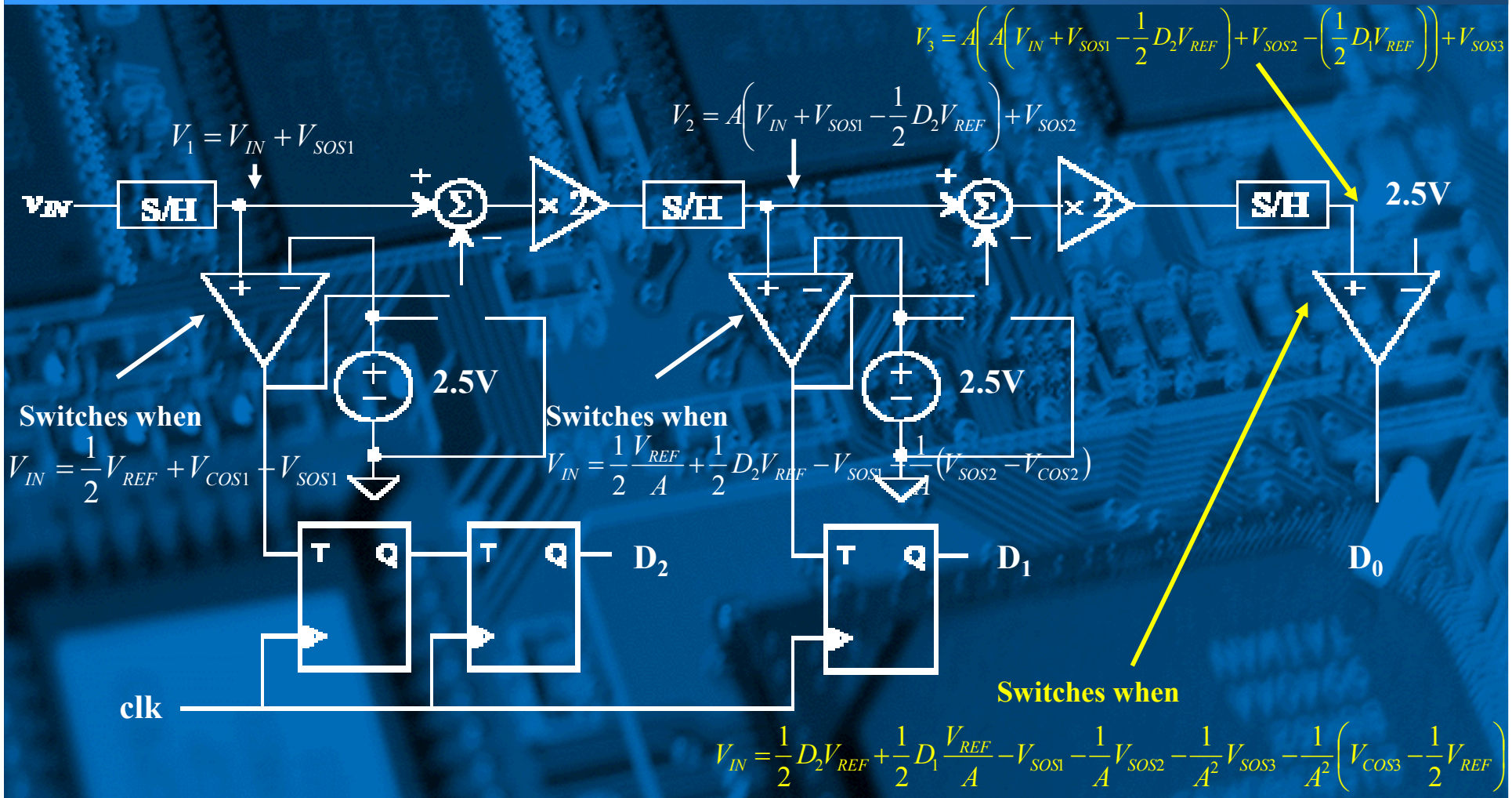


# Non-Ideal Switching Point



# Non-Ideal Switching Point

- 1st comparator switches when:

$$V_{IN} = \frac{1}{2}V_{REF} + V_{COS1} - V_{SOS1}$$

- 2nd comparator switches when:

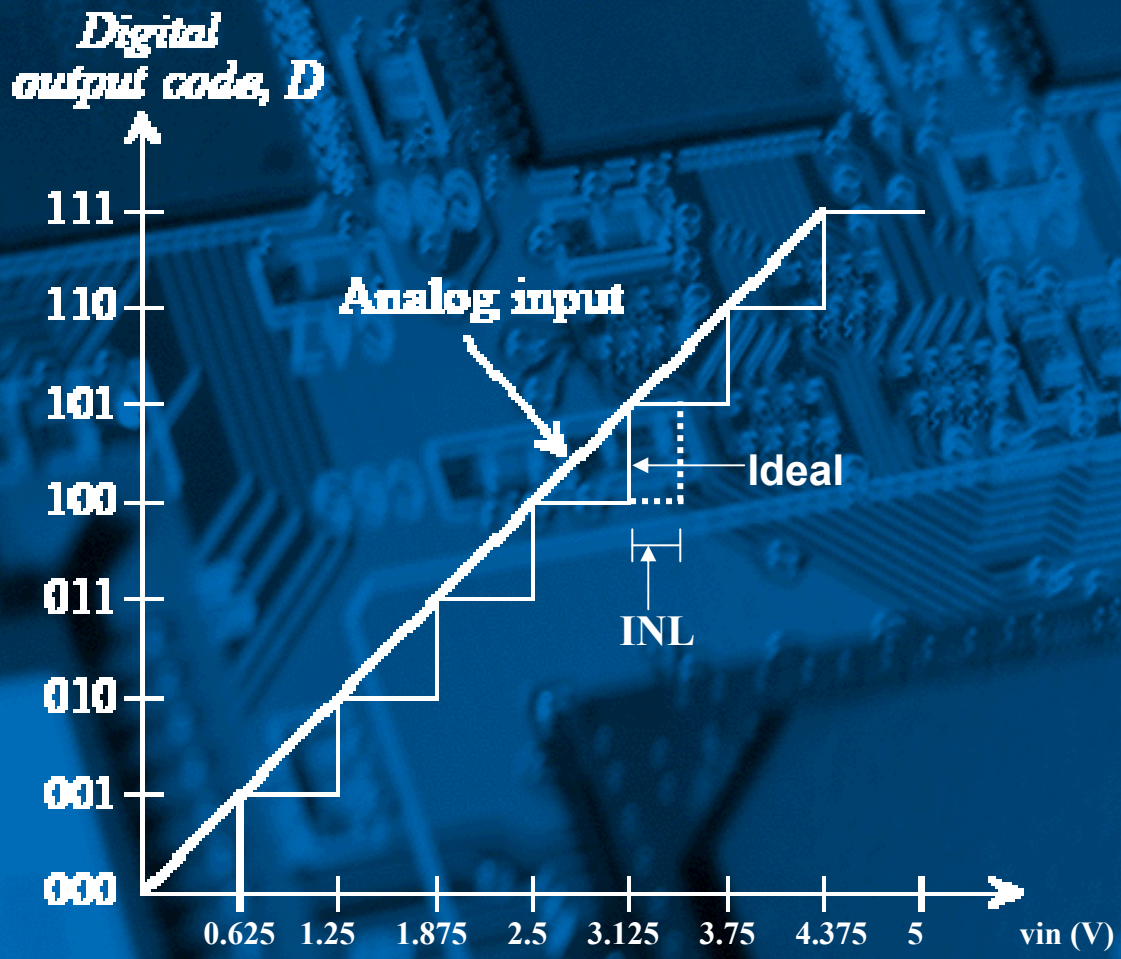
$$V_{IN} = \frac{1}{2}\frac{V_{REF}}{A} + \frac{1}{2}D_2 V_{REF} - V_{SOS1} - \frac{1}{A}\left(V_{SOS2} - V_{COS2}\right)$$

- 3rd comparator switches when:

$$V_{IN} = \frac{1}{2}D_2 V_{REF} + \frac{1}{2}D_1\frac{V_{REF}}{A} - V_{SOS1} - \frac{1}{A}V_{SOS2} - \frac{1}{A^2}V_{SOS3} - \frac{1}{A^2}\left(V_{COS3} - \frac{1}{2}V_{REF}\right)$$

- Error from first sample-and-hold propagates through and causes a larger error at the last stage of the converter
- This analysis only includes major sources of error (sample-and-hold and comparator)
- It also assumes that the gain of each amplifier is A, although in reality, each amplifier may have a different gain error

# INL




Adapted from Figure 28.23

# INL

- INL is calculated by subtracting the ideal switching point from the non-ideal switching point
- For the first stage:

  Ideal: $V_{IN} = \frac{1}{2} V_{REF}$

  Non-Ideal: $V_{IN} = \frac{1}{2} V_{REF} + V_{COS1} - V_{SOS1}$

  INL: $INL_1 = V_{COS1} - V_{SOS1}$
- For the second stage:

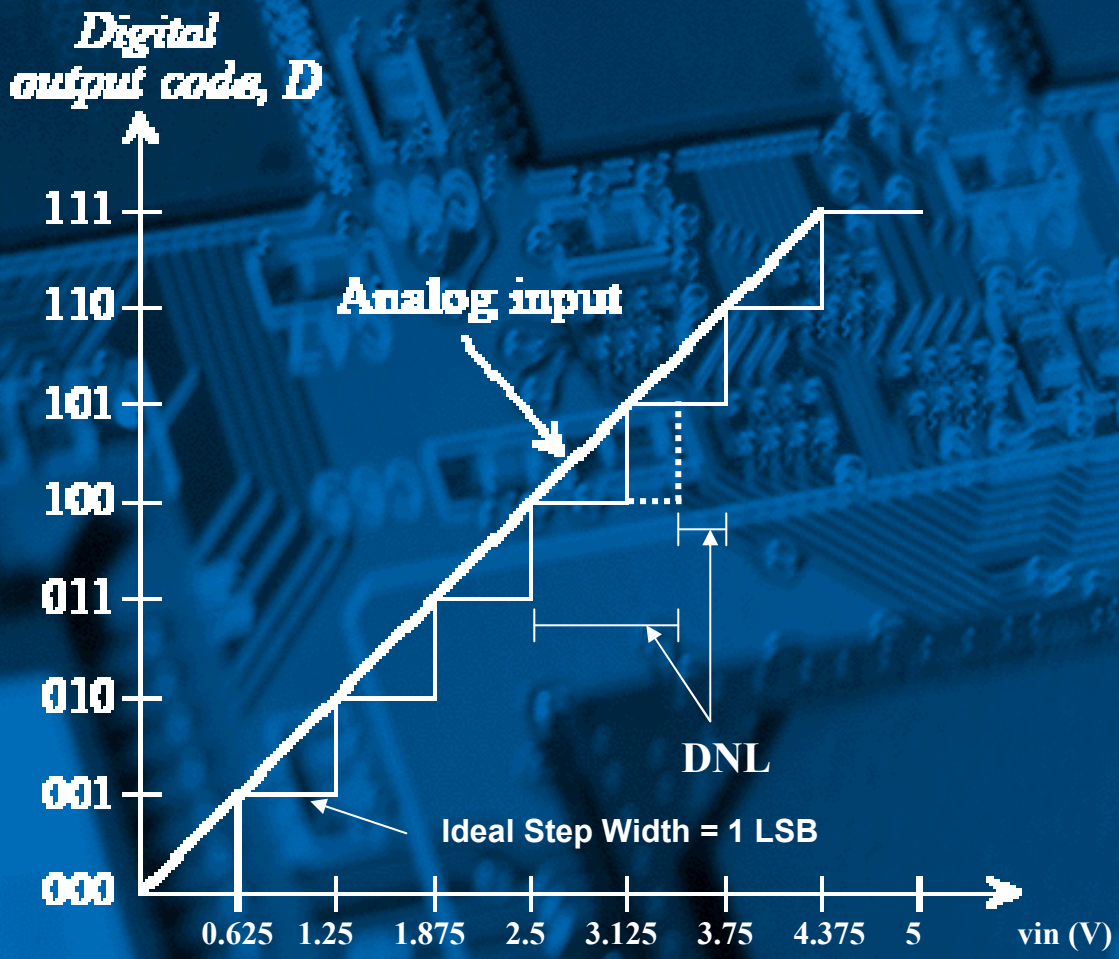
  INL: $INL_2 = \frac{V_{REF}}{2}\left(\frac{1}{A} - \frac{1}{2}\right) - V_{SOS1} - \frac{1}{A}\left(V_{SOS2} - V_{COS2}\right)$
- For the third stage:

  INL: $INL_3 = \frac{V_{REF}}{2}\left(\frac{1}{A} - \frac{1}{2}\right) - V_{SOS1} - \frac{1}{A} V_{SOS2} - \frac{1}{A^2} V_{SOS3} - \frac{1}{A^2} V_{COS3} + \frac{V_{REF}}{2}\left(\frac{1}{A^2} - \frac{1}{4}\right)$

# INL

- Worst case addition of offsets must be <1/2 LSB to be N-bit accurate
- Offsets of later stages are divided by a large gain so they are less important than the first stage
- Less accurate designs can be used for later stages to save power and area

# DNL




Adapted from Figure 28.23

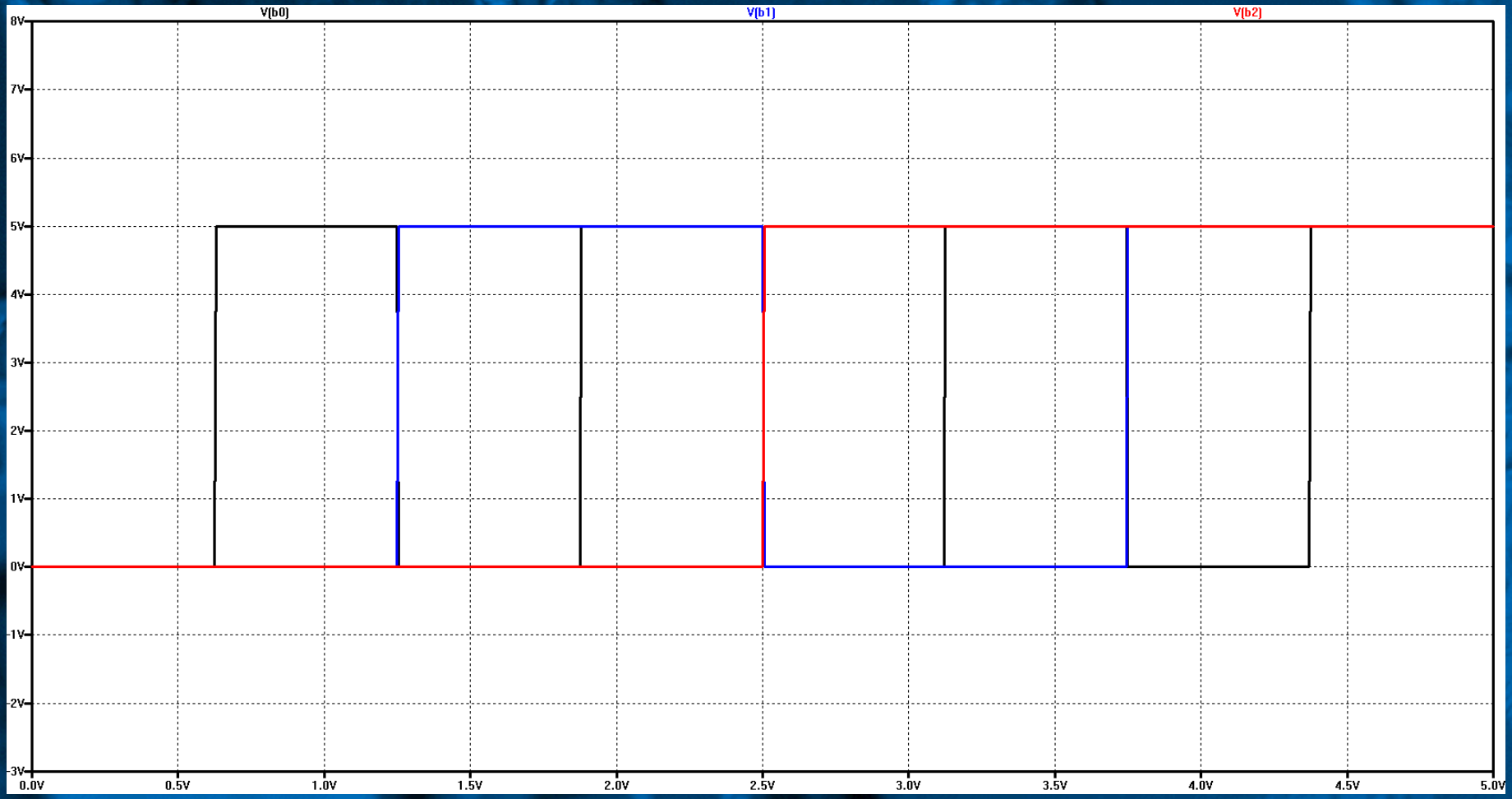
# DNL

- DNL is calculated by subtracting the ideal step width (1 LSB) from the actual step width
- $LSB = \frac{V_{REF}}{2^N} = \frac{V_{REF}}{8}$
- Worst case DNL tends to occur at the midpoint (switching from 011 to 100)
- $DNL_{MAX} = V_{IN,SW1} - V_{IN,SW3} - \frac{V_{REF}}{8}$ which is the point where the MSB switches minus the point where the LSB switches (to get 011) minus 1 LSB
- Knowing that the worst case output is 011 for $V_{IN,SW3}$:

$$DNL_{MAX} = \frac{1}{2}V_{REF} + V_{COS1} - \frac{1}{2}\frac{V_{REF}}{A} + \frac{1}{A}V_{SOS2} + \frac{1}{A^2}V_{SOS3} + \frac{1}{A^2}\left(V_{COS3} - \frac{1}{2}V_{REF}\right) - \frac{V_{REF}}{8}$$

- Notice that the comparator of the first stage and the sample-and-hold of the second stage have the largest impact on the worst case DNL
- $DNL_{MAX}$ must be less that ½ LSB to have N-bit resolution

# Simulation




**No Offset**

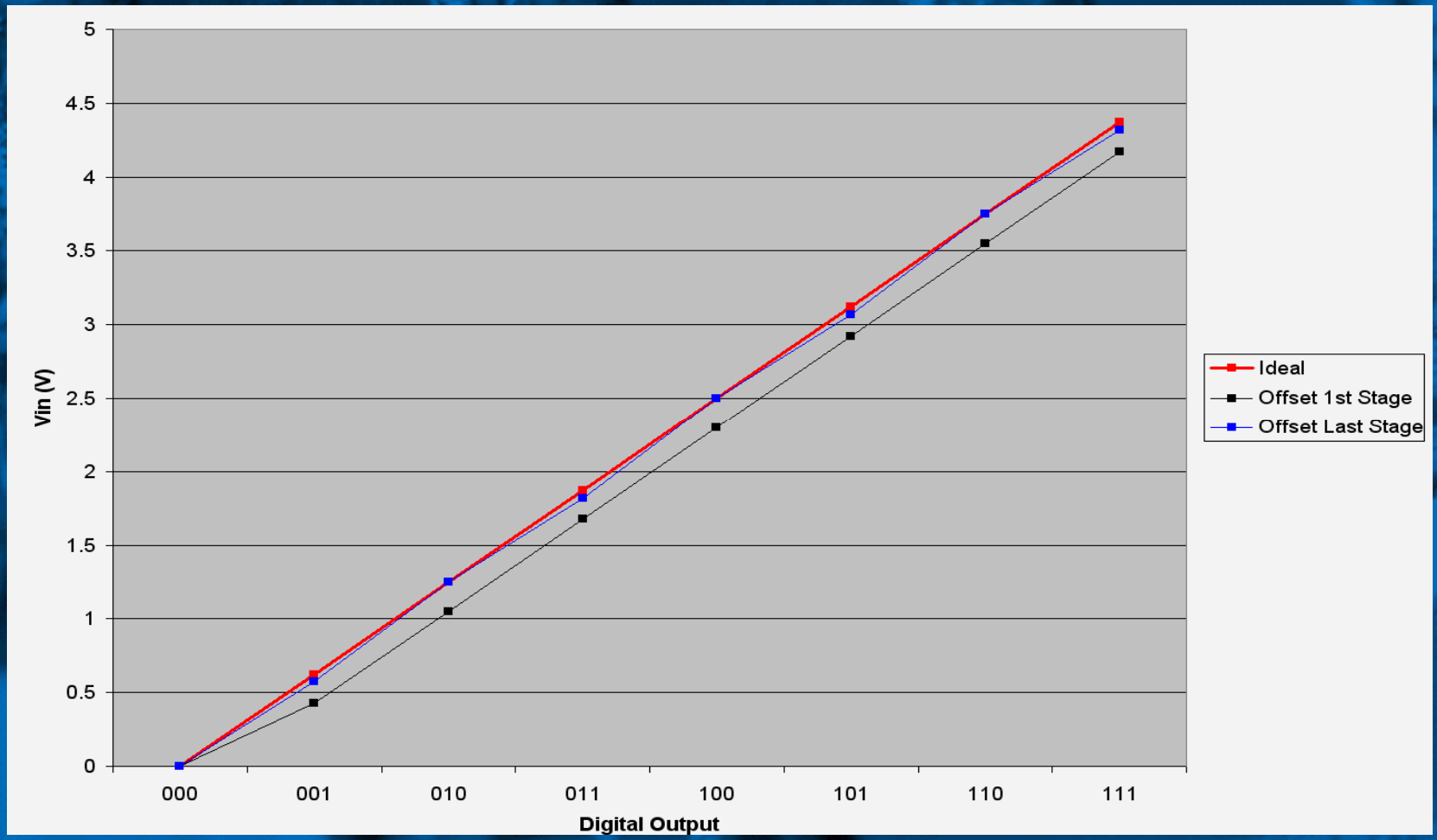
# Simulation


**200mV offset on first S/H**

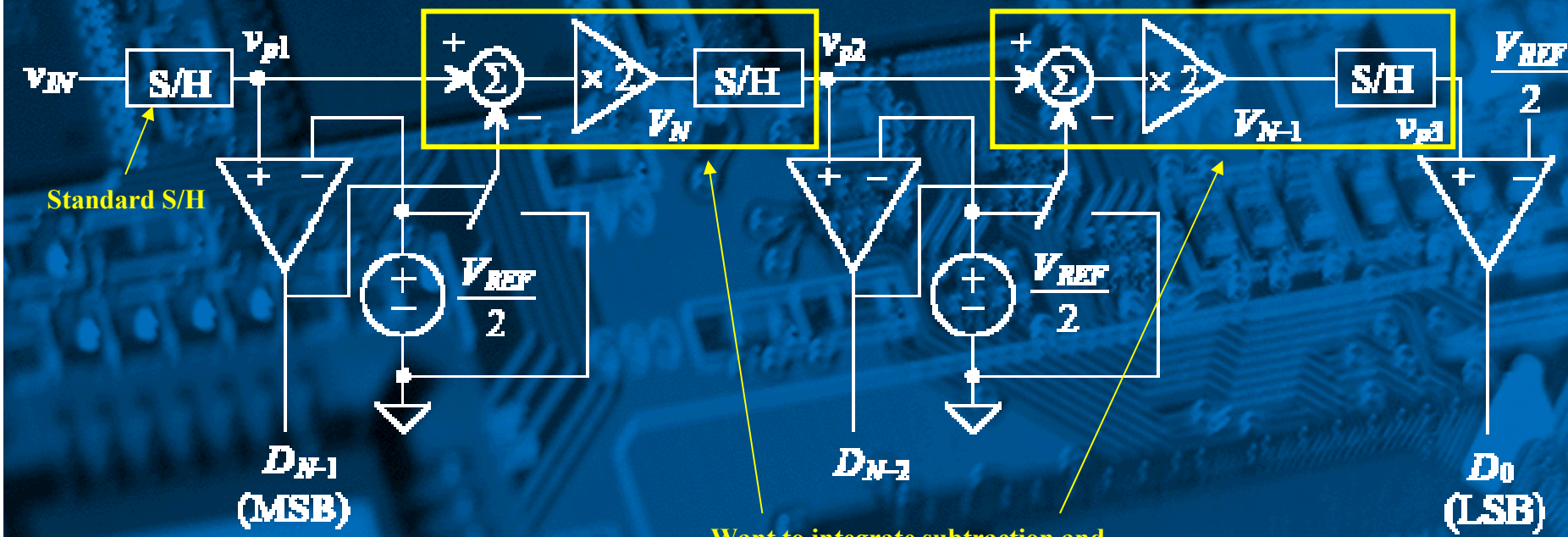
# Simulation


**200mV offset on last S/H**

# Simulation


5
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
Vin (V)
000
001
010
011
100
101
110
111
Digital Output
Ideal
Offset 1st Stage
Offset Last Stage

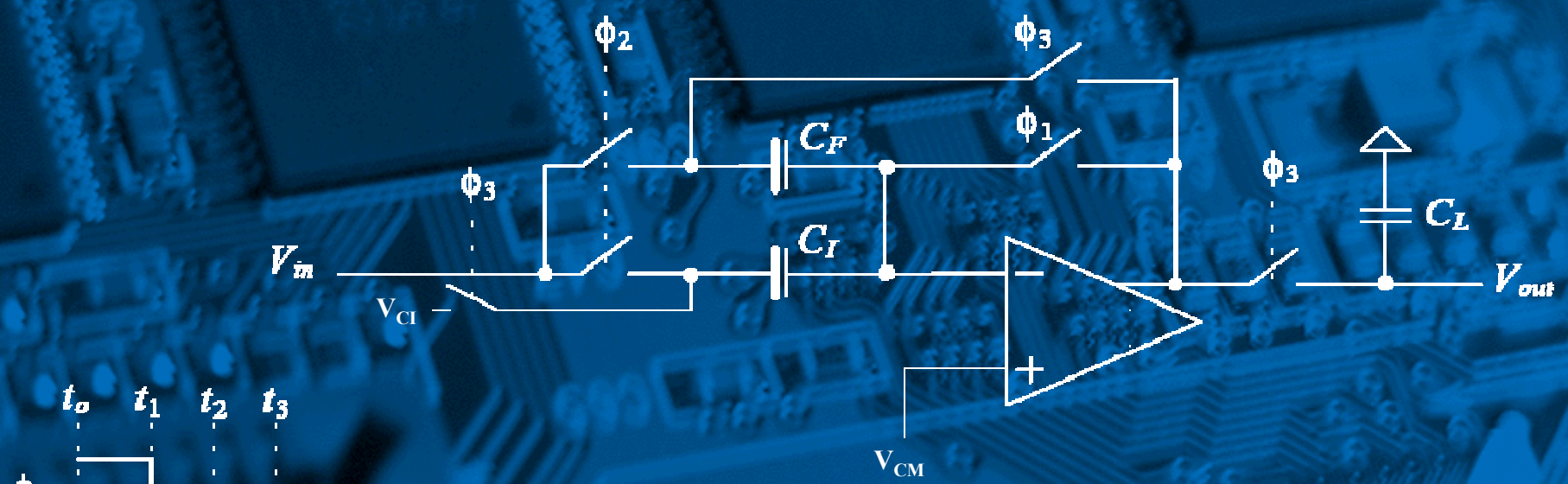
# S/H Design

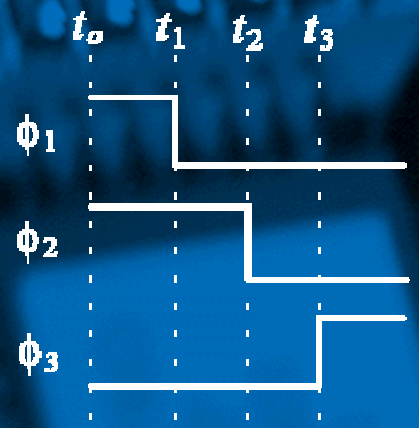



Note that input to S/H is not fully differential so we will use a single ended design

Figure 29.30

# S/H Design

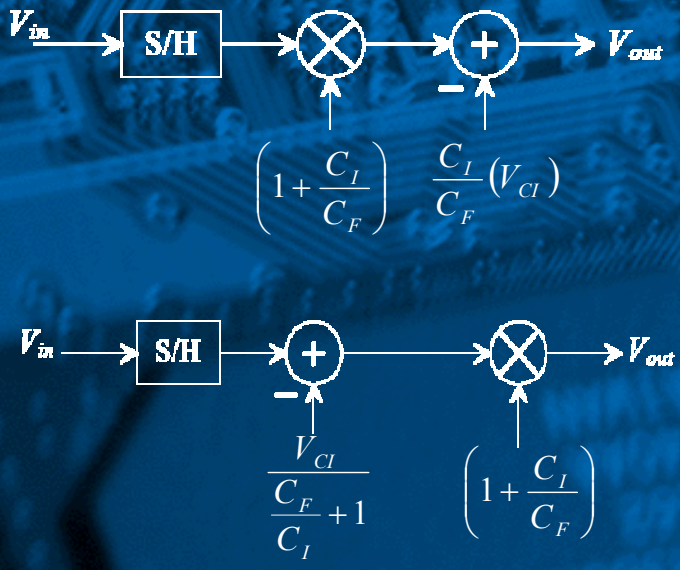



Adapted from Figure 34.30

# S/H Design

- $Q_{I,F}^{\phi 1} = C_{I,F}(V_{IN} - V_{CM} \pm V_{OS})$
- $Q_I^{\phi 3} = C_I(V_{CI} - V_{CM} \pm V_{OS})$
- $Q_F^{\phi 3} = C_F(V_{OUT} - V_{CM} \pm V_{OS})$
- $Q_I^{\phi 1} + Q_F^{\phi 1} = Q_I^{\phi 3} + Q_F^{\phi 3}$
- $V_{OUT} = \left(1 + \frac{C_I}{C_F}\right)V_{IN} - \frac{C_I}{C_F}V_{CI}$
- $V_{OUT} = \left(1 + \frac{C_I}{C_F}\right)\left(Vin - \frac{V_{CI}}{\frac{C_F}{C_I} + 1}\right)$



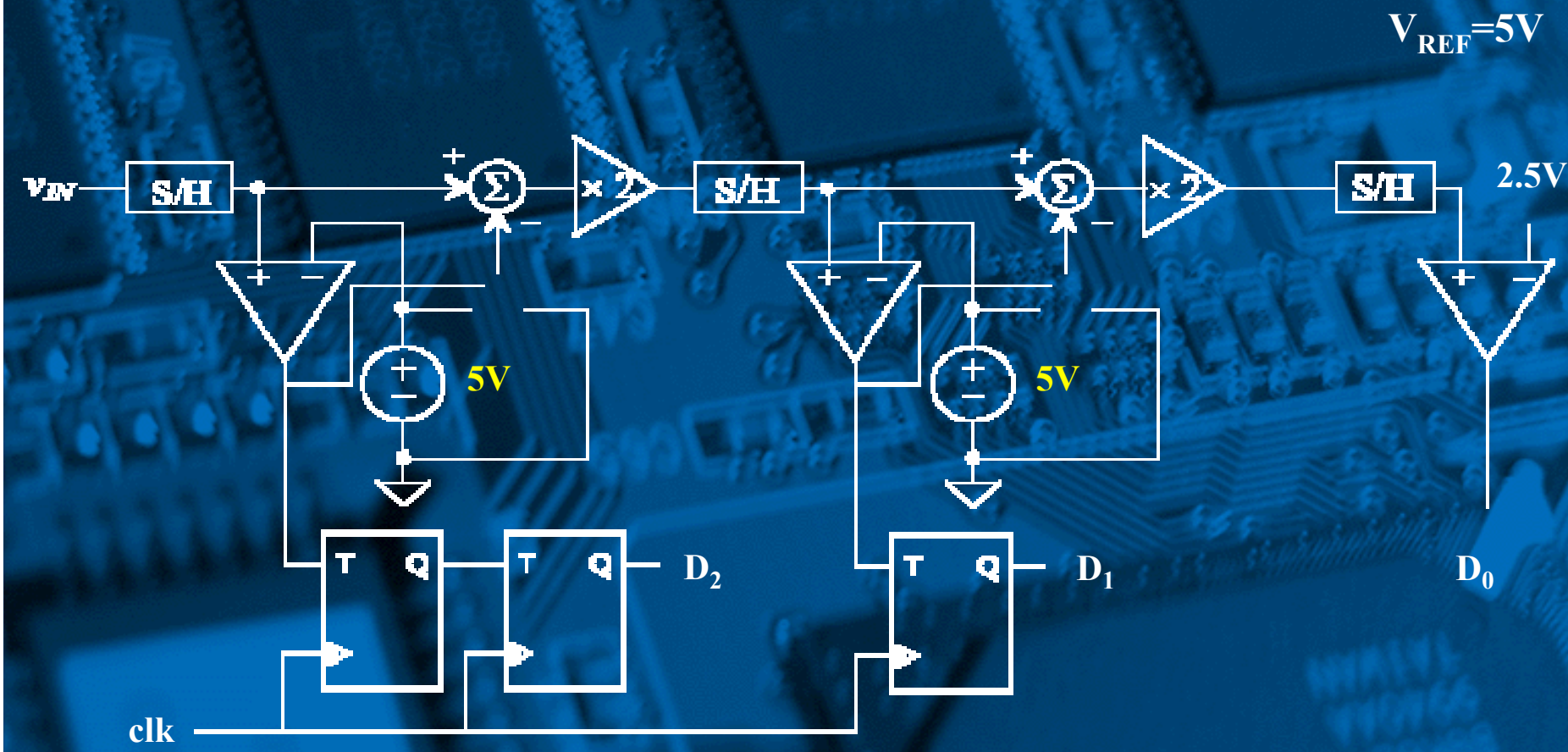
# S/H Design

- We want to multiply $V_{IN}$ by 2, so $C_I = C_F$
- The final output is:

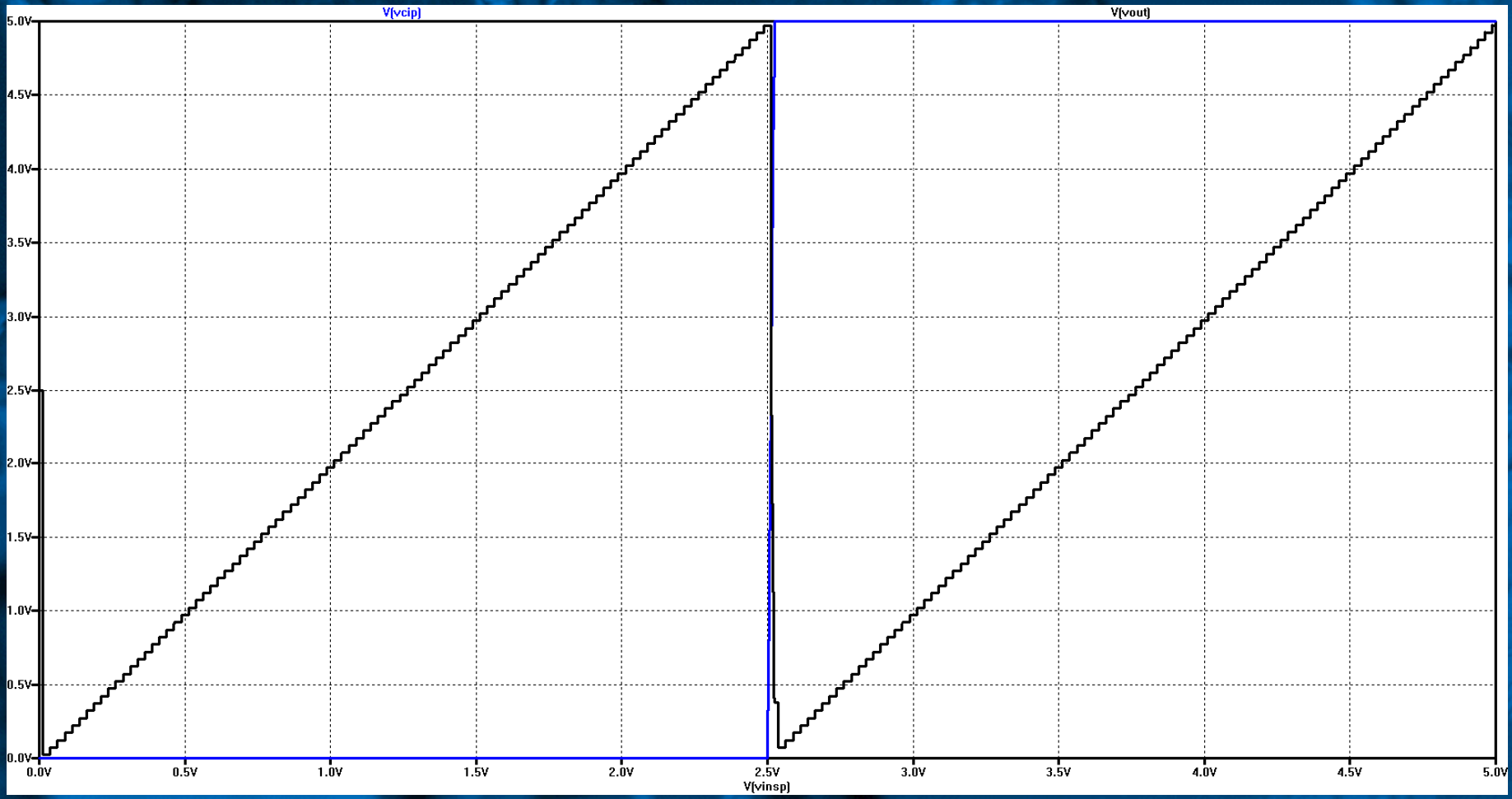
$$V_{OUT} = 2\left(V_{IN} - \frac{V_{CI}}{2}\right)$$

- We want to subtract $V_{REF}/2$ from the input, but this implementation will divide $V_{CI}$ by 2
- This means we need to supply $V_{REF}$ on $V_{CI}$ instead of $V_{REF}/2$ for this implementation to work
- $V_{CI}$ will be either $V_{REF}$ or GND, depending on the state of the switch
- Notice the op-amp offset is auto-zeroed out, but there is still offset from the switches

# S/H Design



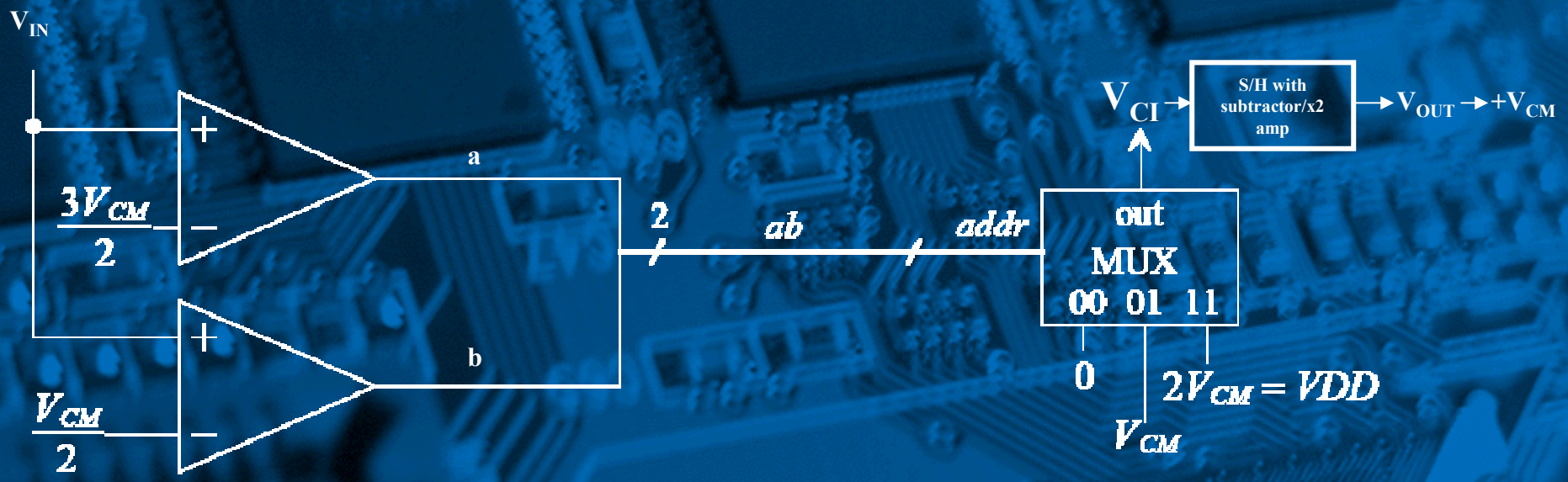
# Simulation


V(vcip)
V(vout)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
0.0V
0.5V
1.0V
1.5V
2.0V
2.5V
3.0V
3.5V
4.0V
4.5V
5.0V
V(vinsp)

# 1.5 Bits/Stage

- Traditional design uses a single comparator, which results in a single bit per stage and two levels (0 or a 1)
- Two bits per stage would result in four levels (00, 01, 10, 11)
- 1.5 bits per stage means that we use three levels which is based on a thermometer code (00, 01, 11)
- 1.5 bits per stage requires two comparators per stage instead of one as used in the basic design

# 1.5 Bits/Stage




$$V_{OUT} = 2\left(V_{IN} - \bar{a}\bar{b}0 - \bar{a}bV_{CM} - ab2V_{CM}\right) + V_{CM}$$

$$V_{OUT} = 2\left(V_{IN} + \bar{a}\bar{b}\frac{V_{CM}}{2} - \bar{a}b\frac{V_{CM}}{2} - ab\frac{3V_{CM}}{2}\right)$$

Difficult to add and subtract using single sided design

This does not account for the fact that the S/H will divide $V_{CM}$ by 2, so these would need to be compensated

Adapted from Figure 34.51

# 1.5 Bits/Stage

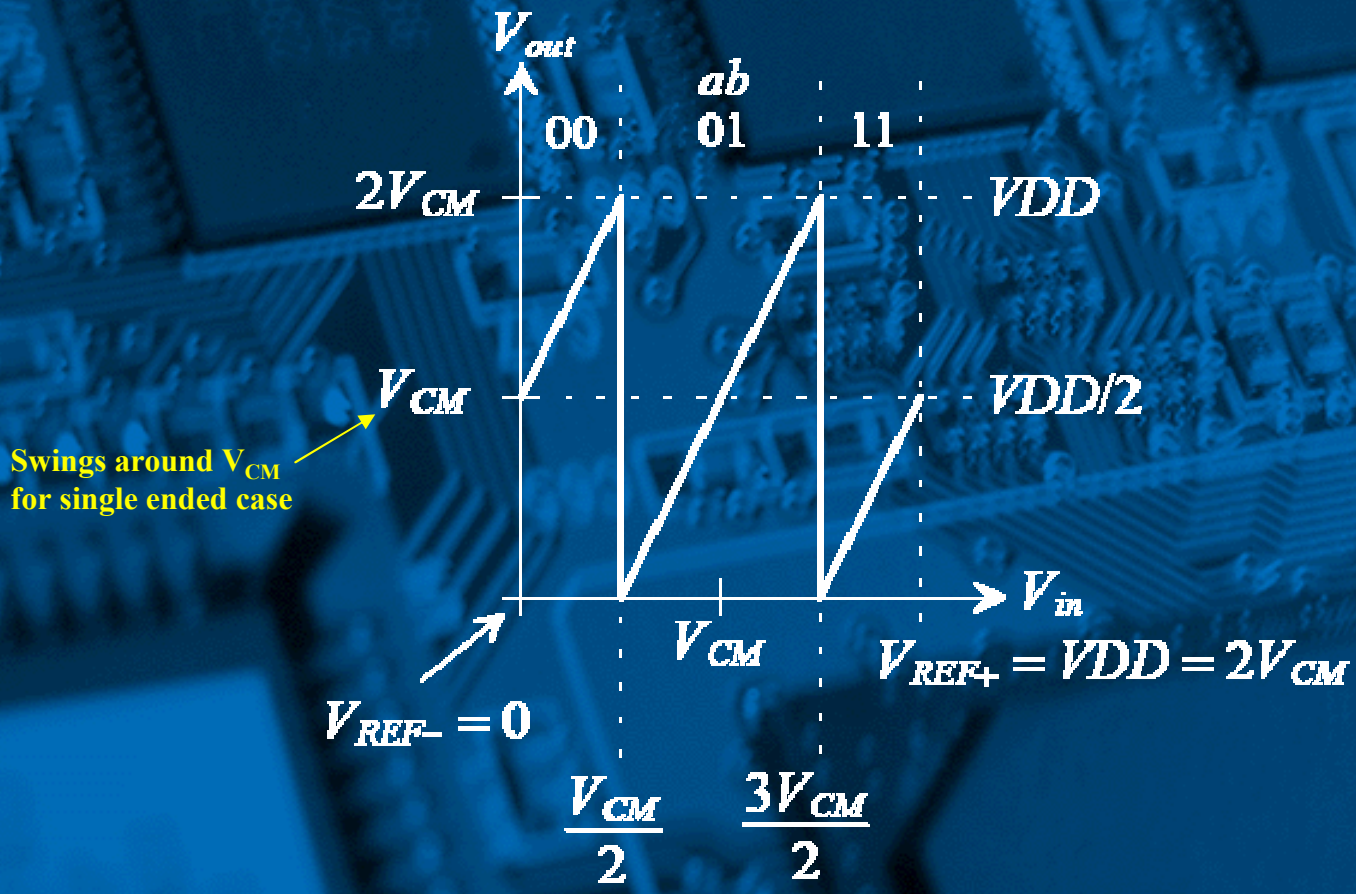
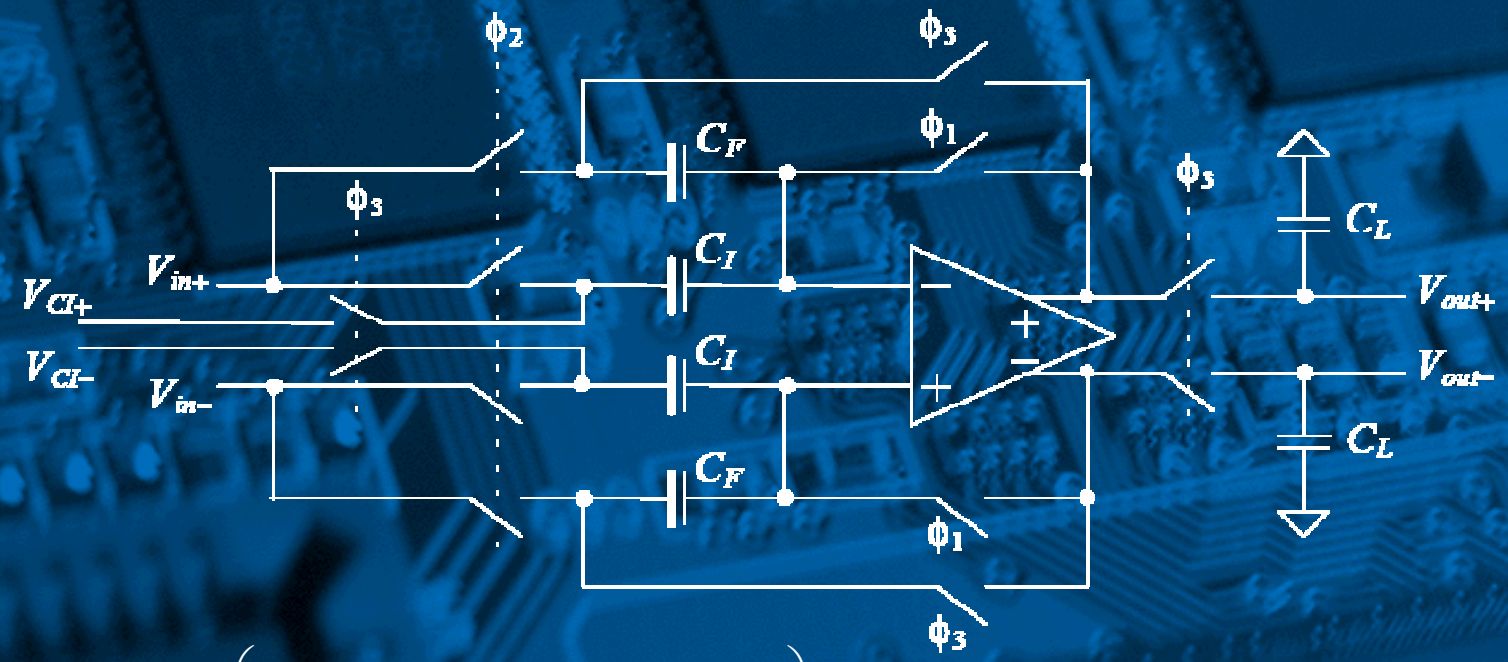



Figure 34.50

# 1.5 Bits/Stage

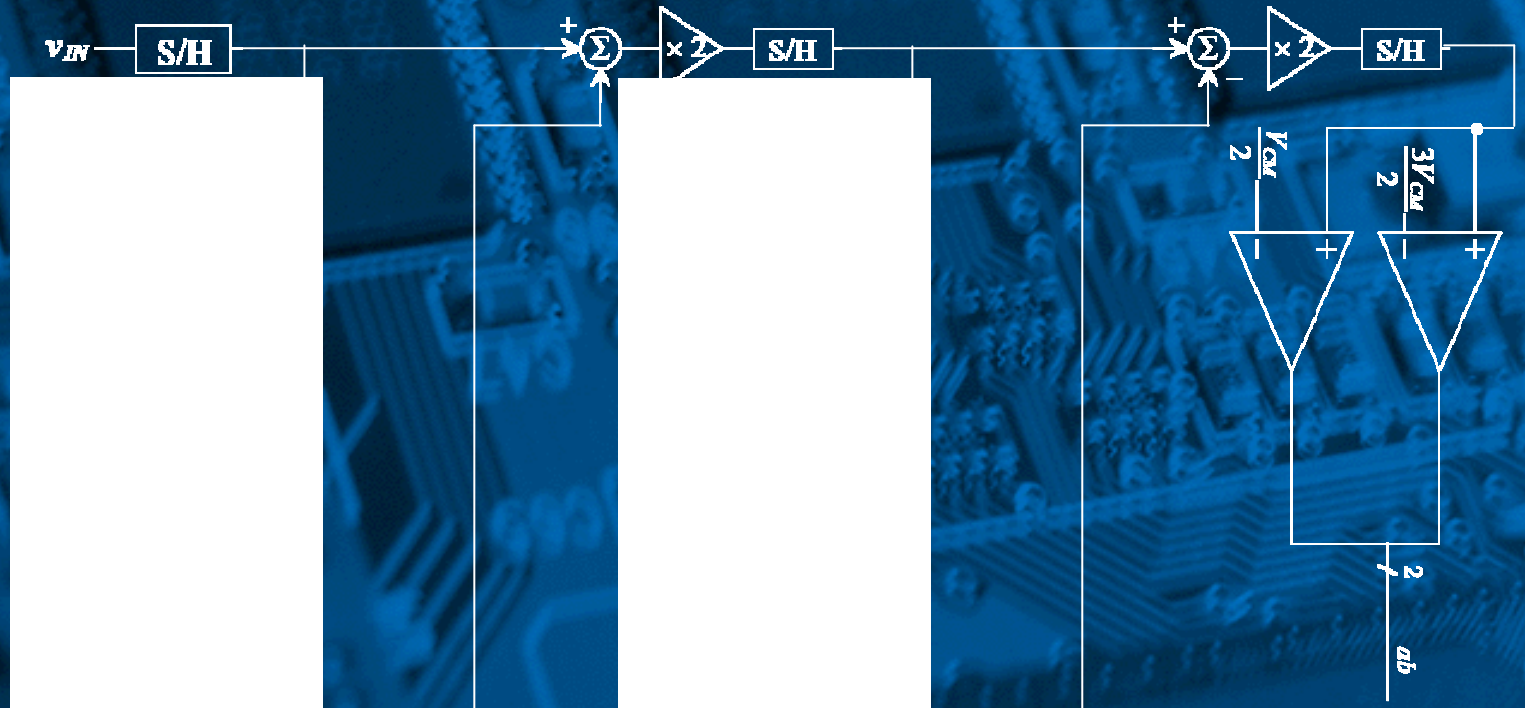



$$V_{OUT} = \left(1 + \frac{C_I}{C_F}\right)\left((V_{in+} - V_{in-}) - \frac{(V_{CI+} - V_{CI-})}{\frac{C_F}{C_I} + 1}\right)$$

$$V_{OUT} = 2\left((V_{IN+} - V_{IN-}) - \frac{(V_{CI+} - V_{CI-})}{2}\right)$$

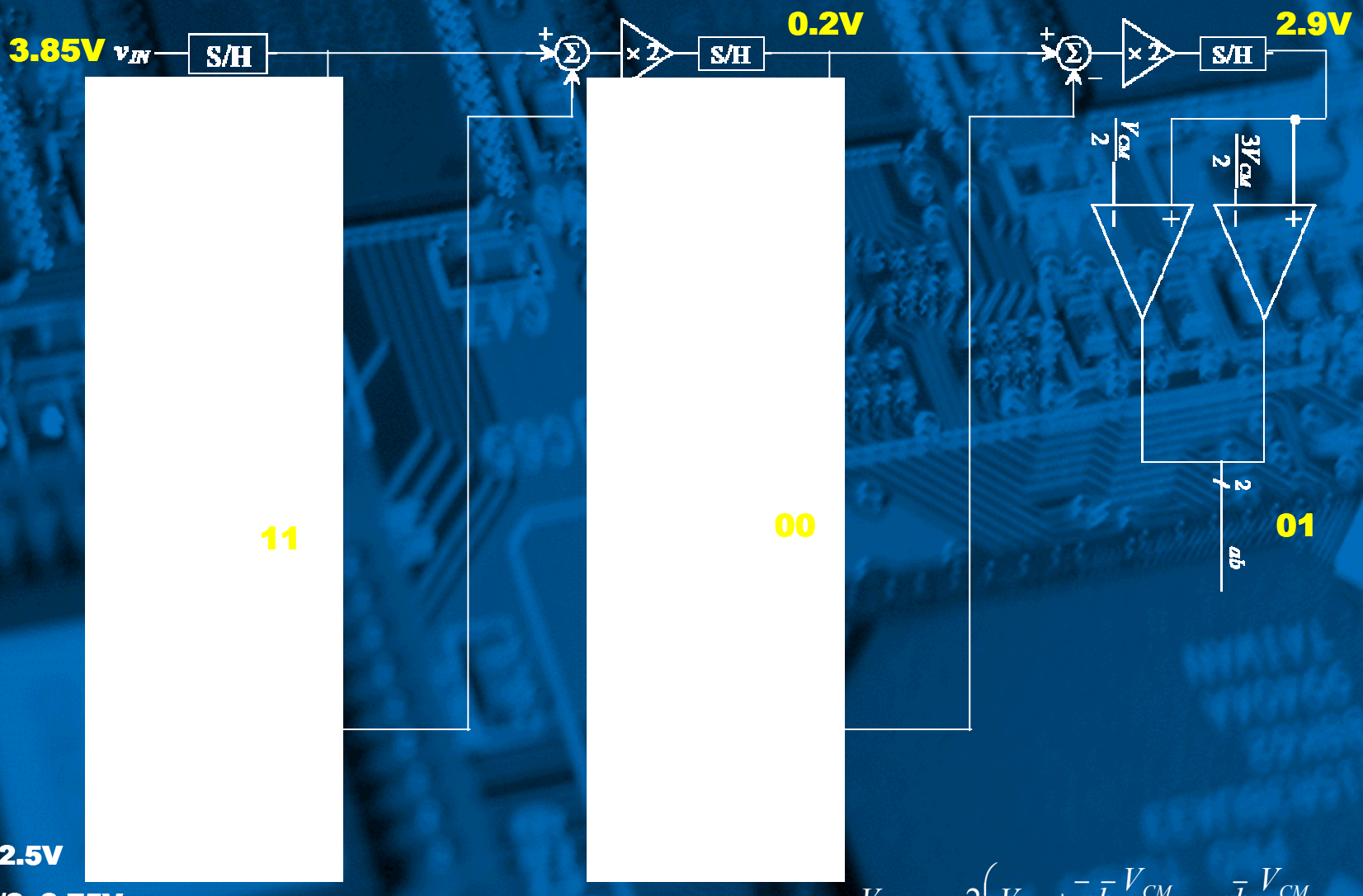
Figure 34.42

# 1.5 Bits/Stage




al Value + ½ of the analog output must always equal the input for each stage, just like the standard implementation

# 1.5 Bits/Stage



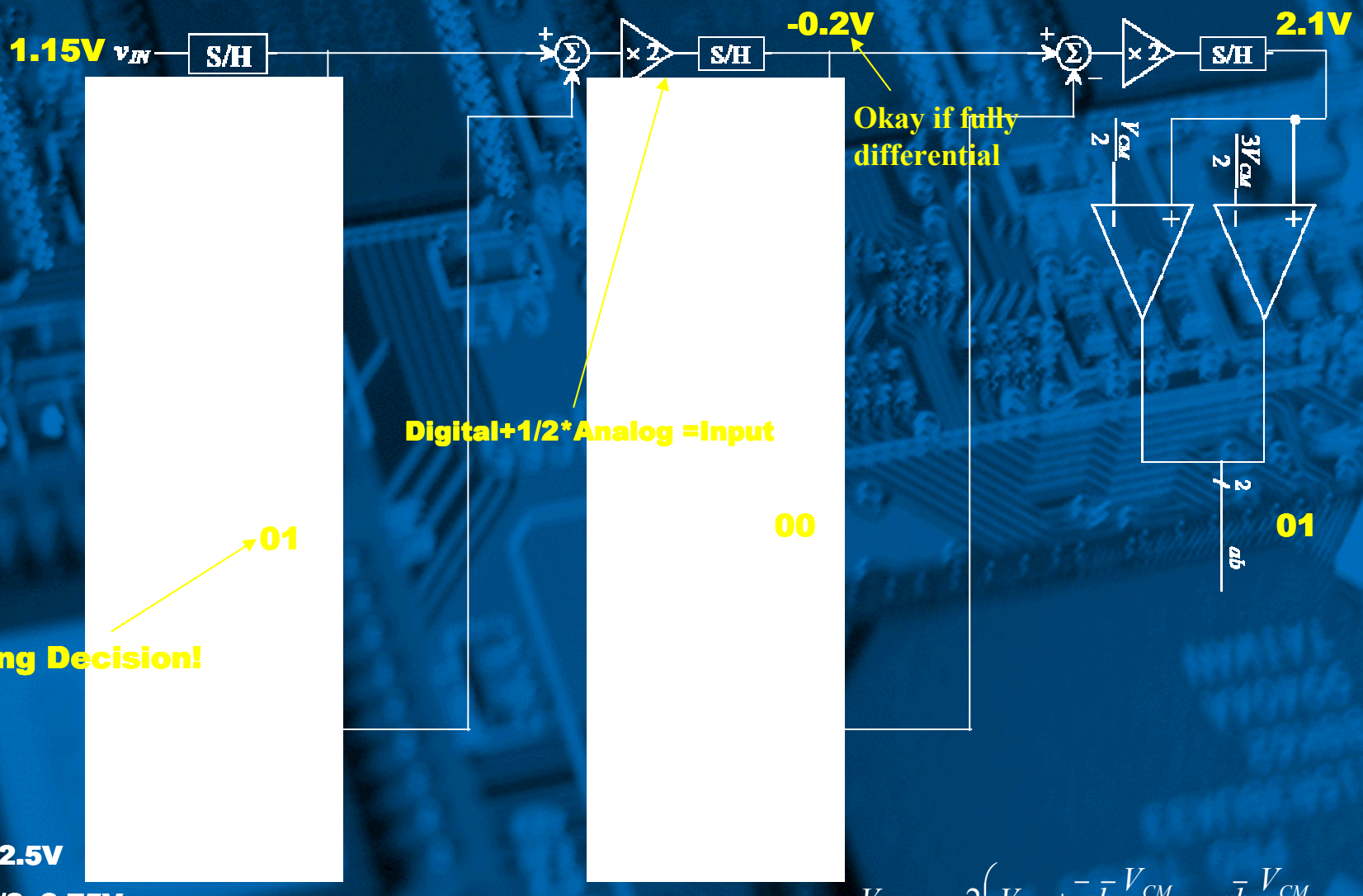

$V_{CM}$=2.5V

$3V_{CM}/2$=3.75V

$V_{CM}/2$=1.25V

$$V_{OUT} = 2\left(V_{IN} + \bar{a}\bar{b}\frac{V_{CM}}{2} - a\bar{b}\frac{V_{CM}}{2} - ab\frac{3V_{CM}}{2}\right)$$

# 1.5 Bits/Stage




$V_{CM}$=2.5V

$3V_{CM}/2$=3.75V

$V_{CM}/2$=1.25V

$$V_{OUT} = 2\left(V_{IN} + \bar{a}\bar{b}\frac{V_{CM}}{2} - a\bar{b}\frac{V_{CM}}{2} - ab\frac{3V_{CM}}{2}\right)$$

# 1.5 Bits/Stage

- **Advantage:**
  **Comparators can be “sloppy” and can make mistakes without ruining the entire conversion**
- **Disadvantage:**
  **Requires 2N comparators instead of N comparators**
  **Requires extra logic overhead to convert 2 bit output to single bit output**

# Summary

- Basic Operation
  - Pipeline with a S/H, comparator, subtractor, and x2 amplifier
  - Each stage operates on residue of previous stage
- Advantages/Disadvantages
  - N comparators, one computation per clock cycle
  - Latency of N clock cycles, errors propagate
- Ideal/Non-Ideal Switching Points
- INL/DNL
  - Accuracy of early stages more important than later stages
- S/H Design
  - Integrate subtractor and x2 amplifier in S/H
- 1.5 Bits/Stage
  - Increase accuracy at the cost of area

# References


- Baker, R.J., CMOS Circuit Design, Layout, and Simulation, Second Edition, Wiley-IEEE, 2008.
- Baker, R.J., CMOS Mixed-Signal Circuit Design, First Edition, Wiley-IEEE, 2002.

# Questions?