Complete system testbech

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1 Report contents

This report contains a brief explanation of the different part in our project.

2 Structure

The overall structure of the system is seen in Figure 1.

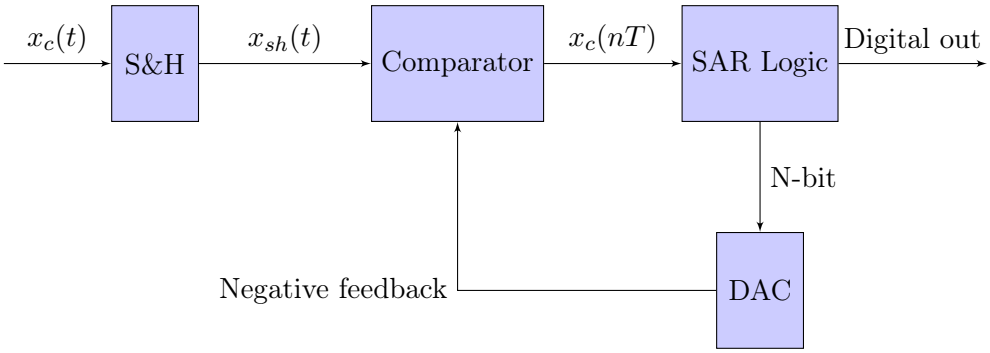

Figure 1: Block diagram

3 Schematic

Schematic: SAR_system

The SAR_system is the complete schematic for the whole system. It consists of a sample and hold block, a comarator block, the SAR logic and the digital-to-analog converter block. Figure 2 shows the schematic that has been created.

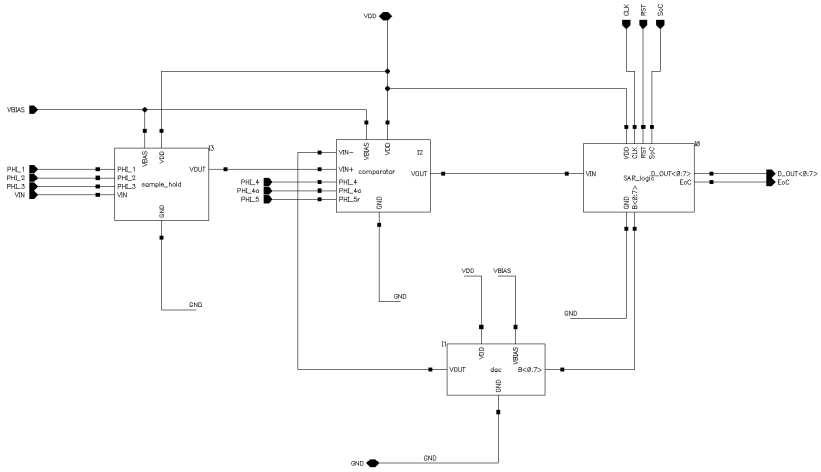

Figure 2: SAR_system

Schematic: sample_hold

The sample and hold (S/H) is based on a circuit provided by R. Jacob Baker in the book CMOS Mixed-Signal Circut Design [**CMOS-baker**]. The implementation is a single-ended S/H implementation. When ϕ_1 and ϕ_2 is high, ϕ_3 is low, and the bottom plate of the hold capacitor is charged by the input signal, while the top plate is held to ground by the feedback around the op amp. When the ϕ_2 is turned off, its charge will bee injected into the low impedance input, VIN, since the impedance looking into the left of the ϕ_2 switch is large.

This implementation has not yet beed tested, and may therefor be changed during the project.

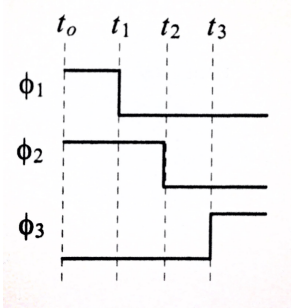

Figure 3: Single-ended S/H opartion [**CMOS-baker**]

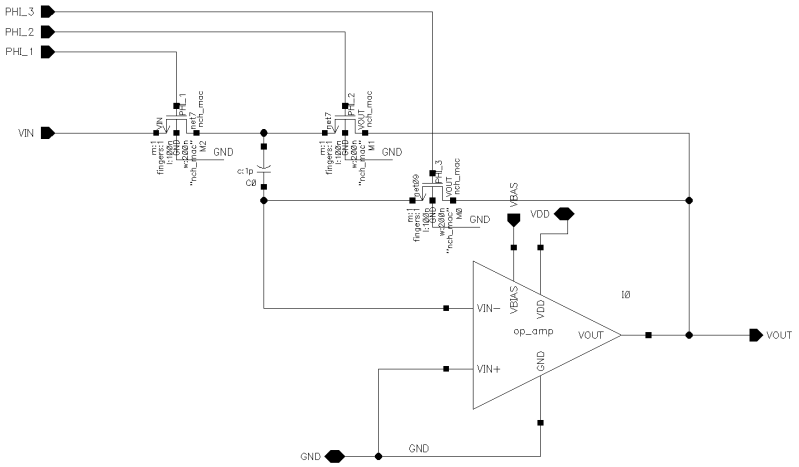

Figure 4: Sample and hold

Schematic: comparator

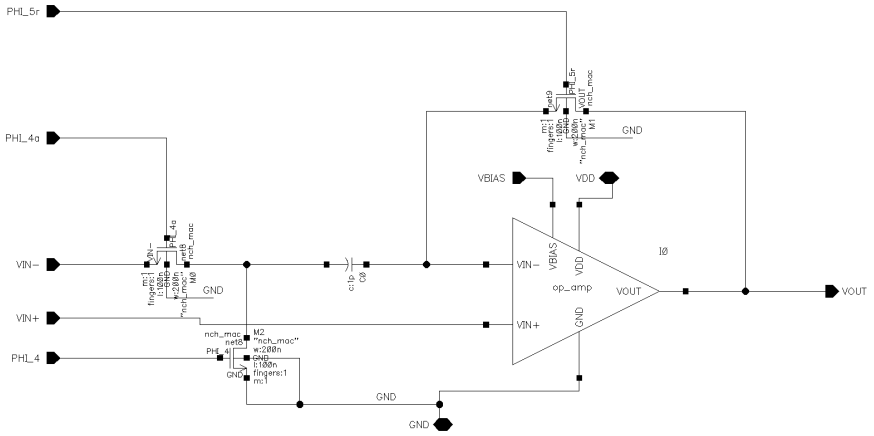

Figure 5: Comparator

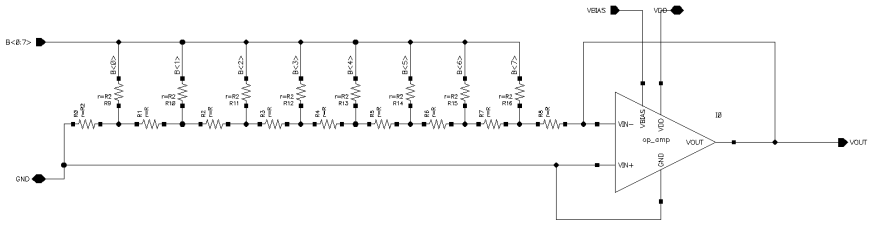

Figure 6: DAC

Schematic: SAR_logic

Schematic: dac

Schematic: op_amp

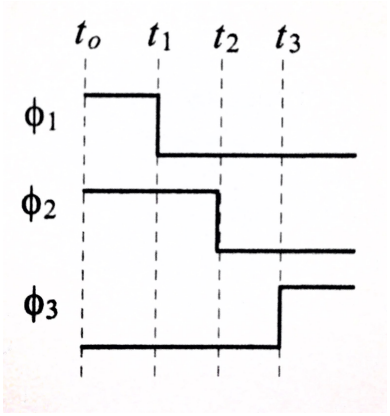

Figure 7: Single-ended S/H opartion [**CMOS-baker**]

4 Test bench

Schematic: SIM_system

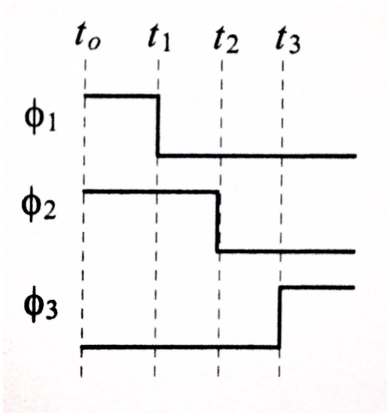

Figure 8: Single-ended S/H opartion [**CMOS-baker**]

Schematic: SIM_sample_hold

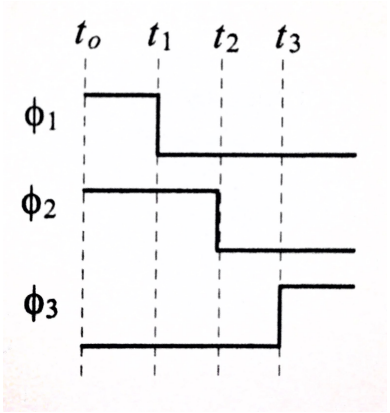

Figure 9: Single-ended S/H opartion [**CMOS-baker**]

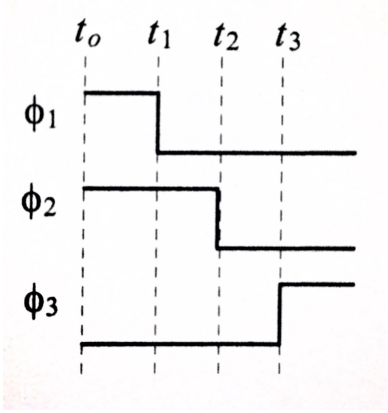

Figure 10: Single-ended S/H opartion **[CMOS-baker]**

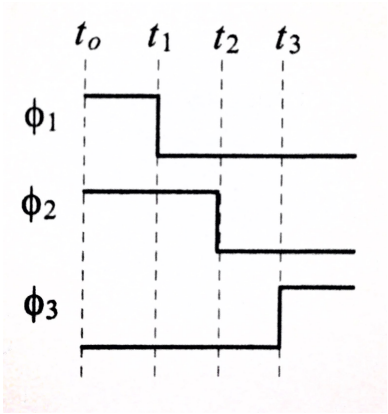

Figure 11: Single-ended S/H opartion **[CMOS-baker]**

Schematic: SIM_comparator

Schematic: SIM_SAR_logic

Schematic: SIM_dac

Schematic: SIM_op_amp

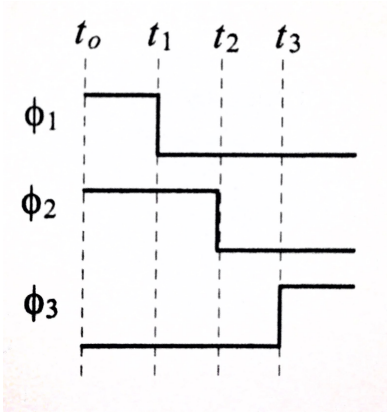

Figure 12: Single-ended S/H opartion **[CMOS-baker]**

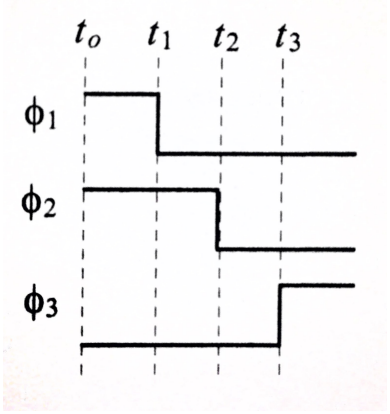

Figure 13: Single-ended S/H opartion **[CMOS-baker]**