Instruction	AU	MUX A/PC	MUX B/O	MUX AU/Mem	MEM Ctrl	Write Enable Registers	Notes
SUB	0011	Default	Default	Default	Default	A	
ADD	Default	Default	Default	Default	Default	A	
LDAC	Default	0010	0001	Default	Default	A	
LDBC	Default	0010	0001	Default	Default	B	
STAM	Default	0010	0001	Default	0101	Not Applicable	ADD O-reg + 0 to get to the correct address
LDAM	Default	0010	0001	0001	Default	A	ADD O-reg + 0 to get to the correct address
LDBM	Default	0010	0001	0001	Default	B	
LDAI	Default	Default	0001	0001	Default	A	ADD A+ O-reg to get to the correct address
Fetch	Default	0001	0010	0001	Default	Opcode O-reg	
PC+1	x100	0001	0010	Default	Default	PC	Performs PC + 0 + Carry

Overview of Computer Architecture