Gebze Technical University

Computer Engineering

CSE 331 – 2019

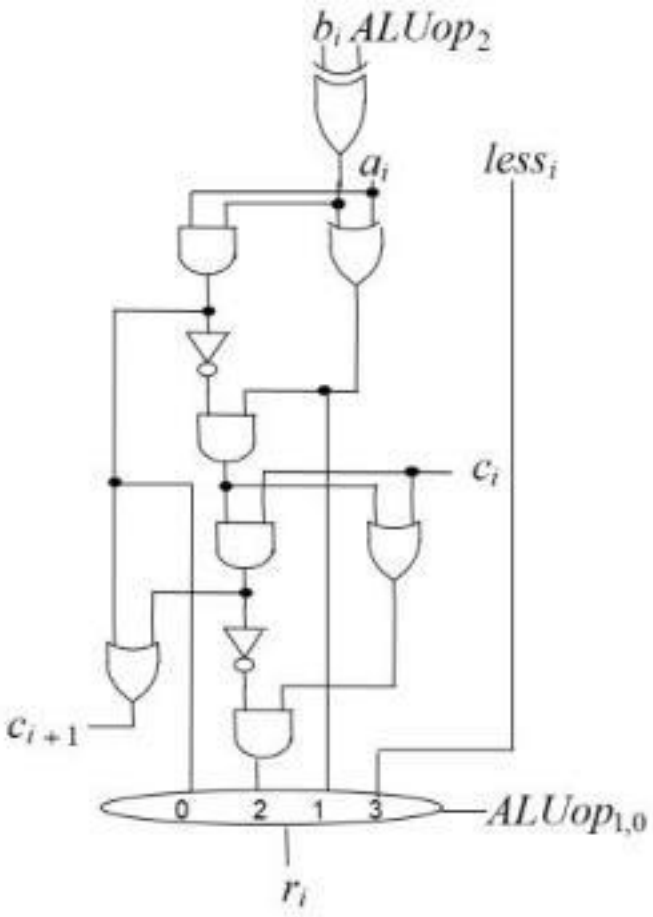
HOMEWORK 2 REPORT

FERHAT ÇELİK 151044014

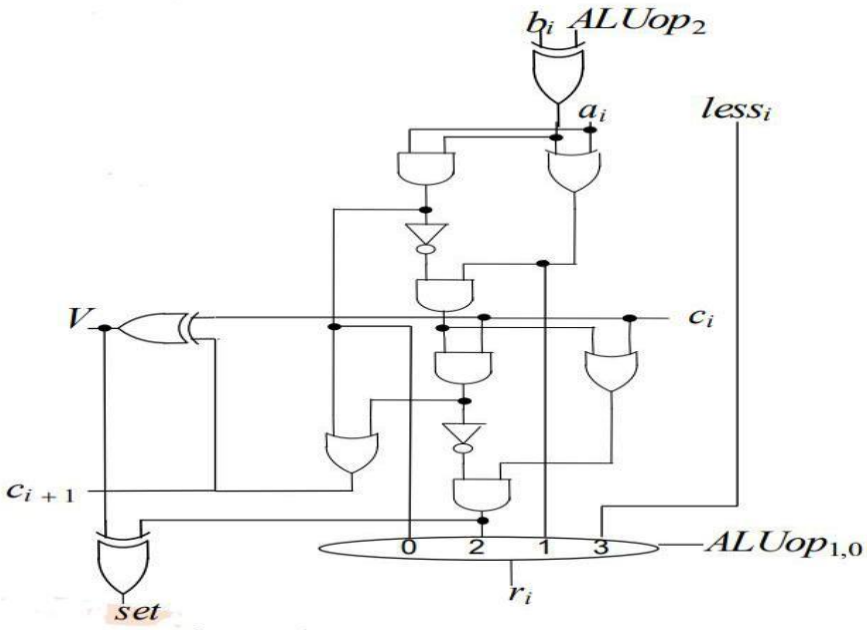
Course Assistant: Fatma Nur Esirci

Şematik Tasarımlar

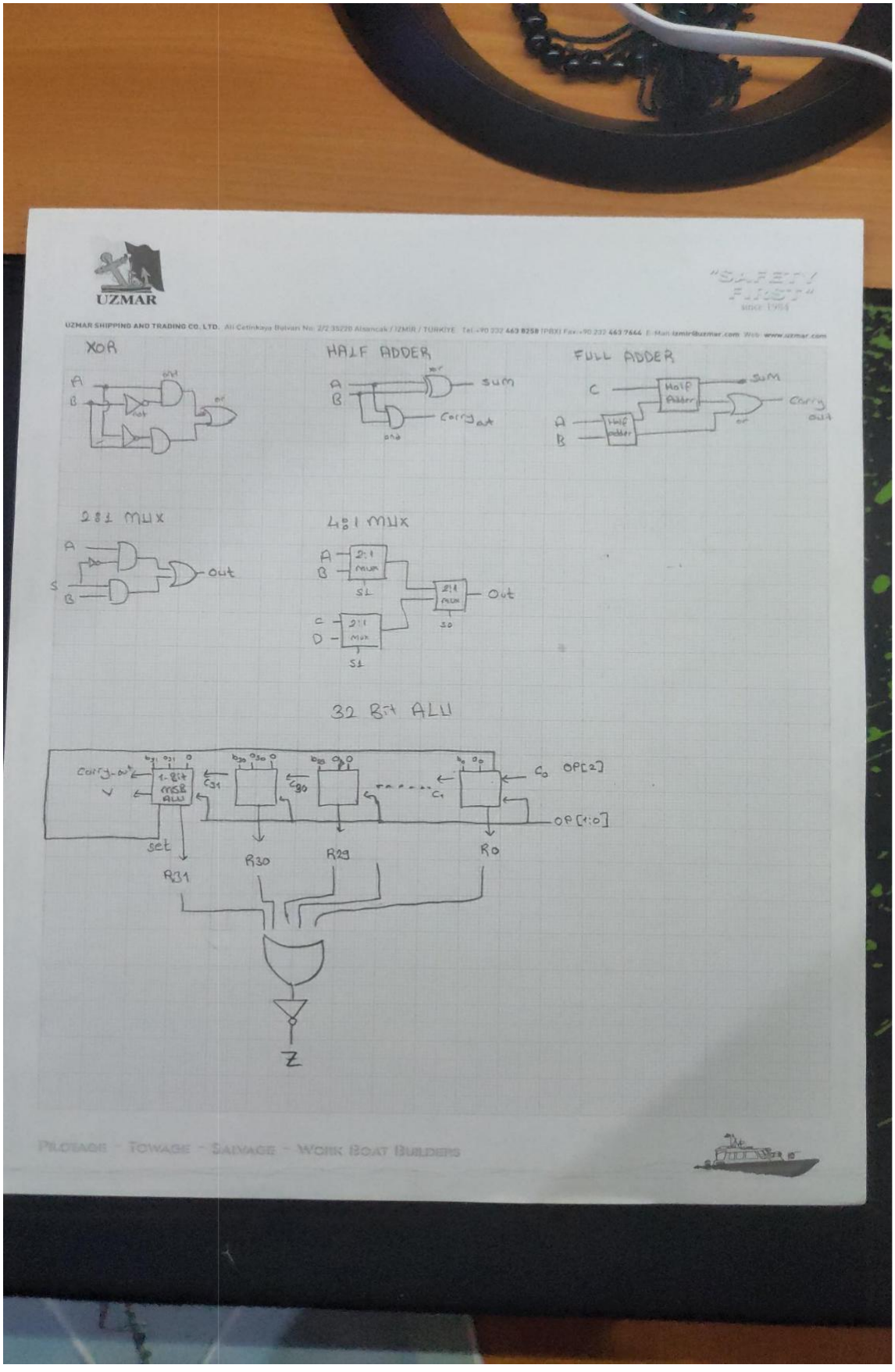
- 1 bit ALU



- 1 bit MSB ALU



- XOR / 2:1 4:1 MUX / 32 BIT ALU



VERİLOG MODÜLLERİ

Xor_module – 2 and 2 not ve bir or kapısı ile oluşturulmuş xor

kapısı _2mux – 1 Bitlik 2:1 Mux

_4mux – 3 adet 2:1 Mux ile oluşturulmuş 4 e 1 mux

_1bit_alu – Ders kitabında bulunan alu

_1bit_msb_alu – Overflow ve sign bit algılayan 1 bitlik alu

Alu32 – 31 adet 1 bit alu ve 1 adet 1 bit msb alu kullanılarak oluşturulmuş 32 bit işlem yapabilen alu

SİMÜLASYON SONUÇLARI

```
add wave -position insertpoint  \
sim:/_32bit_alu_testbench/a \
sim:/_32bit_alu_testbench/b \
sim:/_32bit_alu_testbench/select \
sim:/_32bit_alu_testbench/out \
sim:/_32bit_alu_testbench/v \
sim:/_32bit_alu_testbench/z \
sim:/_32bit_alu_testbench/carry_out
VSIM 5> step -current
# time =  0, Input1 = 00100100001010001110000000000100, Input2 = 00100100001010001110000000011110, select=000, out=00100100001010001110000000000100 ,v=0 ,z=0, carry_out=0
# time = 20, Input1 = 11111111111111111111111111111111, Input2 = 00000000000000000000000000000001, select=000, out=00000000000000000000000000000001 ,v=0 ,z=0, carry_out=1
# time = 40, Input1 = 10111010111101010111111110111100, Input2 = 10101111100101011111110101011110, select=000, out=10101010100101010111110100011100 ,v=1 ,z=0, carry_out=1
# time = 60, Input1 = 01000000000000000000000000000001, Input2 = 11000000000000000000000000000100, select=001, out=11000000000000000000000000000101 ,v=0 ,z=0, carry_out=1
# time = 80, Input1 = 11111111111111111111111111111111, Input2 = 00000000000000000000000000000001, select=001, out=11111111111111111111111111111111 ,v=0 ,z=0, carry_out=1
# time = 100, Input1 = 01000010000000001010110100000001, Input2 = 11010010111101111101010000000100, select=001, out=11010010111101111111111010000101 ,v=0 ,z=0, carry_out=1
# time = 120, Input1 = 01100011111111011010100000011100, Input2 = 10000010000010111000000000011000, select=010, out=11100110000010010010100000110100 ,v=0 ,z=0, carry_out=0
# time = 140, Input1 = 01000000000111010110000000000001, Input2 = 01111100000000000000011100000100, select=010, out=10111100000011101011001110000101 ,v=1 ,z=0, carry_out=0
# time = 160, Input1 = 11000000000000000000000000000001, Input2 = 01000000000000000000000000000100, select=010, out=00000000000000000000000000000101 ,v=0 ,z=0, carry_out=1
# time = 180, Input1 = 00000000000000000000000000000001, Input2 = 00000000000000000000000000000010, select=110, out=11111111111111111111111111111111 ,v=0 ,z=0, carry_out=0
# time = 200, Input1 = 01110110100000000000000000000001, Input2 = 00011011011111010111000000000100, select=110, out=01011011000000101000111111111101 ,v=0 ,z=0, carry_out=1
# time = 220, Input1 = 11000000000000000000000000000001, Input2 = 10000001111011011000000000000100, select=110, out=00111110000100100111111111111101 ,v=0 ,z=0, carry_out=1
# time = 240, Input1 = 01110101010101111111010101010101, Input2 = 11010111110110101111101010101010, select=111, out=00000000000000000000000000000000 ,v=1 ,z=1, carry_out=0
# time = 260, Input1 = 11000000000000000000000000000001, Input2 = 11000000000000000000000000000100, select=111, out=00000000000000000000000000000001 ,v=0 ,z=0, carry_out=0
# time = 280, Input1 = 01110101111101011111110000000001, Input2 = 10011101111101110000000000000100, select=111, out=00000000000000000000000000000000 ,v=1 ,z=1, carry_out=0
```

Tüm modüllerim düzgünce çalışıyor.Genel testbench hariç olarak bazı diğer modüllerim için de testbench yazdım.