

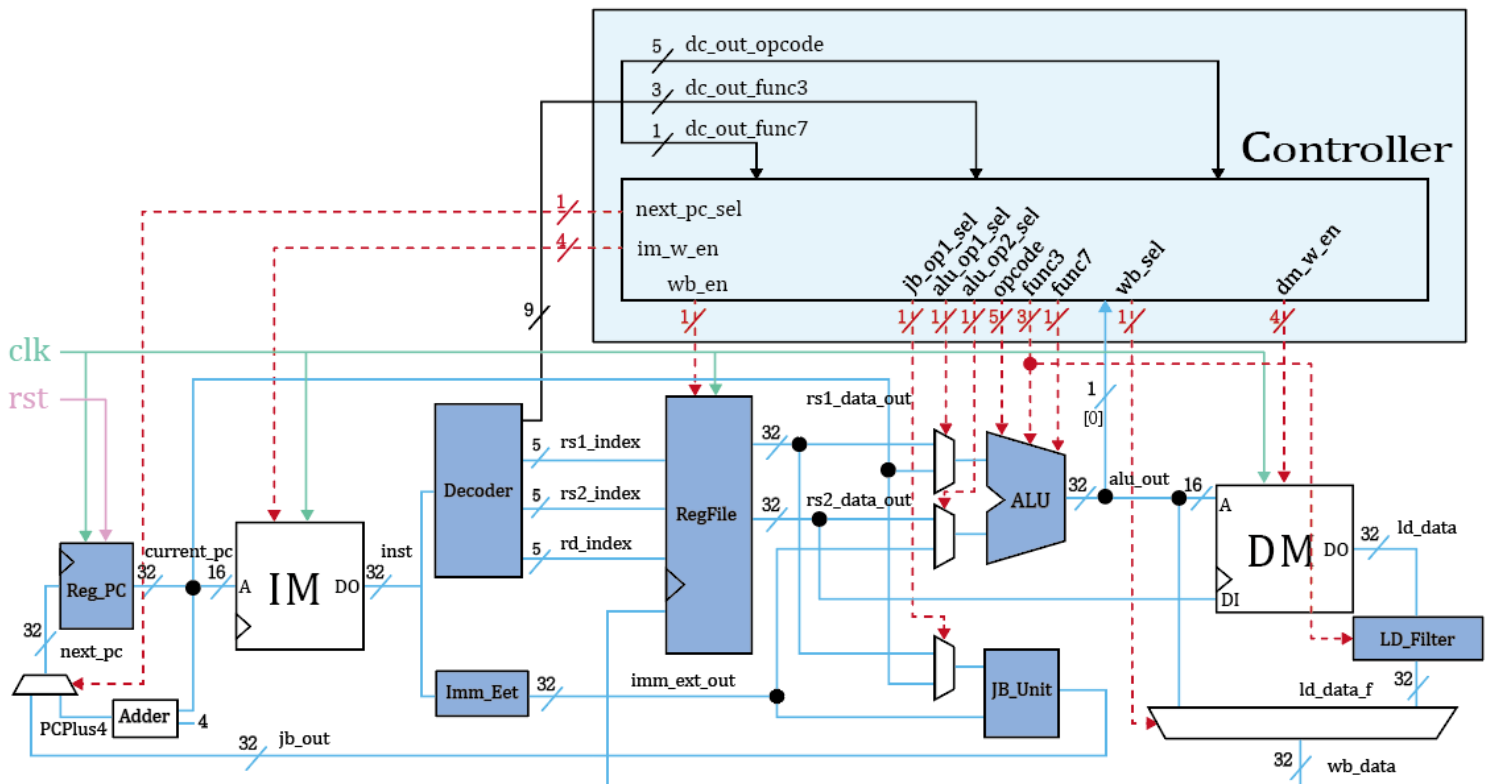
# 2022 計算機組織

## Computer Organization

### Lab 7 Report

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## 1. Architecture Diagram



## 2. Introduce each module (function / corner case / and so on...)

**Reg\_PC:** 控制 `current_pc`，當 `rst` 時，`current_pc` 為 0，其餘將 `next_pc` 賦值給 `current_pc`。

**SRAM:** 控制 instruction 的讀跟寫，一方面將 `mem[address]` 讀到 `read_data` 內，另一方面當 `clk` 正緣觸發時將 `write_data` 寫入 `mem[address]` 內，寫入訊號由 controller 輸出的 `w_en` 控制 (sb/sh/sw)，當 `w_en` 為 0 則不寫入。再在 `top.v` 內將 SRAM 分為 im 與 dm，im 將 `current_pc(address)` 從 mem 中讀指令出來，dm 做 load/store 指令。

**Adder:** 將 `current_pc(address)` 加 4 傳入 mux。

**Decoder:** 將 SRAM im 讀取出來的 instruction，分別輸出 `opcode`、`func3`、`func7`、`rs1_index`、`rs2_index`、`rd_index`。

**Imm\_Ext:** 將 SRAM im 讀取出來的 instruction 內包含的 `imm` 部分篩選出來，並擴展至 32 bits。

**RegFile:** 控制 register 的存 data 和取 data，一方面將 `registers[rs1_index]` 與 `registers[rs2_index]` 讀到 `rs1_data_out` 與 `rs2_data_out` 內，另一方面當 `clk` 正緣觸發時將 Mux 篩選出來的 `wb_data` 寫入 `registers[rd_index]` 內，寫入訊號由 controller 輸出的 `wb_en` 控制 (sb/sh/sw)，當 `w_en` 為 0 則不寫入。

**JB\_Unit:** 控制跳轉指令(branch/jal/jalr)，將 Mux 的 output 與 `imm_ext_out` 相加再 and (~32'd)。

**ALU**：運算單元做指令的運算，將 Mux output 的 operand1 與 operand2 以 opcode、func3、func7 來分類指令再作相對應的運算。

**LD\_Filter**：作為 load 指令的篩選器，以 func3 來分別做 lb /lh/lw/lbu/lhu。

**Controller**：控制 Mux 的選擇訊號輸出、ALU 與 LD\_Filter 的指令分類，以及 SRAM im/dm 與 RegFile 的寫入訊號。

**Mux**：控制所有 multiplexer 的輸出(alu\_operand1、alu\_operand2、jb\_operand1、wb\_data、next\_pc)。

### 3. Screenshot the successful result of prog0

```
DM['h9000'] = ffffffff0, pass
DM['h9004'] = ffffffff8, pass
DM['h9008'] = 00000008, pass
DM['h900c'] = 00000001, pass
DM['h9010'] = 00000001, pass
DM['h9014'] = 78787878, pass
DM['h9018'] = 000091a2, pass
DM['h901c'] = 00000003, pass
DM['h9020'] = fefcfefd, pass
DM['h9024'] = 10305070, pass
DM['h9028'] = cccccccc, pass
DM['h902c'] = fffffffc, pass
DM['h9030'] = ffffcccc, pass
DM['h9034'] = 000000cc, pass
DM['h9038'] = 0000cccc, pass
DM['h903c'] = 00000d9d, pass
DM['h9040'] = 00000004, pass
DM['h9044'] = 00000003, pass
DM['h9048'] = 000001a6, pass
DM['h904c'] = 00000ec6, pass
DM['h9050'] = 2468b7a8, pass
DM['h9054'] = 5dbf9f00, pass
DM['h9058'] = 00012b38, pass
DM['h905c'] = fa2817b7, pass
DM['h9060'] = ff000000, pass
DM['h9064'] = 12345678, pass
DM['h9068'] = 0000f000, pass
DM['h906c'] = 00000f00, pass
DM['h9070'] = 000000f0, pass
DM['h9074'] = 0000000f, pass
DM['h9078'] = 56780000, pass
DM['h907c'] = 78000000, pass
DM['h9080'] = 00005678, pass
DM['h9084'] = 00000078, pass
DM['h9088'] = 12345678, pass
DM['h908c'] = ce780000, pass
DM['h9090'] = fffff000, pass
DM['h9094'] = fffff000, pass
DM['h9098'] = fffff000, pass
DM['h909c'] = fffff000, pass
DM['h90a0'] = fffff000, pass
DM['h90a4'] = fffff000, pass
DM['h90a8'] = 13579d7c, pass
DM['h90ac'] = 13578000, pass
DM['h90b0'] = fffff004, pass

*****
**                               **
** Waku Waku !!                 **
**                               **
** Simulation PASS !!           **
**                               **
*****

Simulation complete via $finish(1) at time 6225 NS + 2
./top_tb.sv:114 $finish;
```

**4.** Screenshot the successful result of prog1

```

DM['h9000'] = 00000000, pass
DM['h9004'] = 00000001, pass
DM['h9008'] = 00000001, pass
DM['h900c'] = 00000003, pass
DM['h9010'] = 00000003, pass
DM['h9014'] = 00000006, pass
DM['h9018'] = 00000008, pass
DM['h901c'] = 0000000a, pass
DM['h9020'] = 0000000a, pass
DM['h9024'] = 0000000b, pass
DM['h9028'] = 0000000c, pass
DM['h902c'] = 0000000f, pass
DM['h9030'] = 00000010, pass
DM['h9034'] = 00000012, pass
DM['h9038'] = 00000012, pass
DM['h903c'] = 00000017, pass
DM['h9040'] = 00000017, pass
DM['h9044'] = 00000017, pass
DM['h9048'] = 00000018, pass
DM['h904c'] = 0000001b, pass
DM['h9050'] = 0000001e, pass
DM['h9054'] = 00000025, pass
DM['h9058'] = 00000025, pass
DM['h905c'] = 00000026, pass
DM['h9060'] = 00000027, pass
DM['h9064'] = 00000028, pass
DM['h9068'] = 00000028, pass
DM['h906c'] = 00000029, pass
DM['h9070'] = 0000002b, pass
DM['h9074'] = 0000002d, pass
DM['h9078'] = 0000002d, pass
DM['h907c'] = 0000002e, pass
DM['h9080'] = 0000002f, pass
DM['h9084'] = 00000031, pass
DM['h9088'] = ffffffff, pass
DM['h908c'] = ffffffff, pass
DM['h9090'] = ffffffff1, pass
DM['h9094'] = ffffffff1, pass
DM['h9098'] = ffffffff2, pass
DM['h909c'] = ffffffff2, pass
DM['h90a0'] = ffffffff9, pass
DM['h90a4'] = ffffffff9a, pass
DM['h90a8'] = ffffffff9b, pass
DM['h90ac'] = ffffffffed, pass
DM['h90b0'] = ffffffffef, pass
DM['h90b4'] = ffffffffef, pass
DM['h90b8'] = ffffffffef, pass
DM['h90bc'] = ffffffffef, pass
DM['h90c0'] = ffffffffef, pass
DM['h90c4'] = ffffffffef, pass
DM['h90c8'] = ffffffffef, pass
DM['h90cc'] = ffffffffef, pass
DM['h90d0'] = 00000000, pass
DM['h90d4'] = ffffffffef, pass
DM['h90d8'] = ffffffffef, pass
DM['h90dc'] = ffffffffef, pass
DM['h90e0'] = ffffffffef, pass
DM['h90e4'] = ffffffffef, pass
DM['h90e8'] = ffffffffef, pass
DM['h90ec'] = ffffffffef, pass
DM['h90f0'] = ffffffffef, pass
DM['h90f4'] = ffffffffef, pass
DM['h90f8'] = ffffffffef, pass
DM['h90fc'] = ffffffffef, pass
DM['h9100'] = ffffffffef, pass
DM['h9104'] = ffffffffef, pass
DM['h9108'] = ffffffffef, pass
DM['h910c'] = ffffffffef, pass
DM['h9110'] = ffffffffef, pass
DM['h9114'] = ffffffffef, pass
DM['h9118'] = 00000000, pass
DM['h911c'] = 00000000, pass
DM['h9120'] = 00000000, pass
DM['h9124'] = 00000003, pass
DM['h9128'] = 00000009, pass
DM['h912c'] = 0000000f, pass
DM['h9130'] = 00000013, pass
DM['h9134'] = 00000016, pass
DM['h9138'] = 00000017, pass
DM['h913c'] = 00000017, pass
DM['h9140'] = 00000023, pass
DM['h9144'] = 0000002e, pass

```

```

#####
*****
**                                     **
** Waku Waku !!                       **
** Simulation PASS !!                 **
**                                     **
*****
Simulation complete via $finish(1) at time 203835 NS + 2
./top_tb.sv:114      $finish;
xcelium> exit
TOOL:   xmverilog    22.03-s003: Exiting on Jan 17, 2023 at 14:28:
user:~/C02022_Lab7/Lab7>

```