Sitronix

ST7579

68 x 102 Dot Matrix LCD Controller/Driver

1. INTRODUCTION

The ST7579 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 102 segment and 67 common with 1 ICON driver circuits. This chip is connected directly to a microprocessor, accepts 3-line or 4-line serial peripheral interface (SPI), I^2C interface or 8-bit parallel interface, display data can stores in an on-chip display data RAM of 68 x 102 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Single-chip LCD controller & driver

Driver Output Circuits

102 segment / 67 common+1 ICON common (1/68 duty)

102 segment / 32 common+1 ICON common (1/33 duty)

102 segment / 16 common+1 ICON common (1/17 duty)

(1/33 duty and 1/17 duty are under partial screen mode)

On-chip Display Data Ram

- Capacity: 68X102=6,936 bits

Microprocessor Interface

- 8-bit parallel bi-directional interface with 6800-series or 8080-series
- 4-line SPI (serial peripheral interface) available (only write operation)
- 3-line SPI (serial peripheral interface) available
- I^2C (Inter-Integrated Circuit) Interface

On-chip Low Power Analog Circuit

- Generation of LCD supply voltage
- Generation of intermediate LCD bias voltages
- Oscillator requires no external components (external clock also possible)
- Voltage converter (X2,X3,X4 (partial display); X5 (normal display))
- Voltage follower
- On-chip electronic contrast control function (255 steps)

External RESB (reset) pin

Logic supply voltage range

- V_{DD1} -V_{SS} : 1.8 to 3.3V
- V_{DD2} -V_{SS} : 2.4 to 3.3V

Display supply voltage range (V0)

- Application Vop range: 4V-9.5V
- External V0: 10.5V

Temperature range: -40 to +85 degree

ST7579	**6800 , 8080 , 4-Line , 3-Line interface (without I^2C interface)**	ST
ST7579i	**I^2C interface**	I^2C BUS

3. ST7579 Pad Arrangement

Chip Size: 5570 um ×770 um

Bump Height: 15 um

Chip Thickness: 480 um

Bump Pitch: (minimum) **Unit: um**

PAD Number	Pitch	PAD Number	Pitch
1~27, 130~156, 157~163, 243~250:	37.20	212~213	46.65
28~129:	33.00	213~216,218~221	33.30
27~28	62.90	216~217,217~218	38.80
129~130	60.69	221~222	46.30
163~164	329.57	228~229	66.40
164~207, 208~211,222~228,229~235,236~242	59.30	235~236	62.45
207~208	131.83	242~243	79.90
211~212	71.30		

*** Refer to "Pad Center Coordinates" section for ITO layout.**

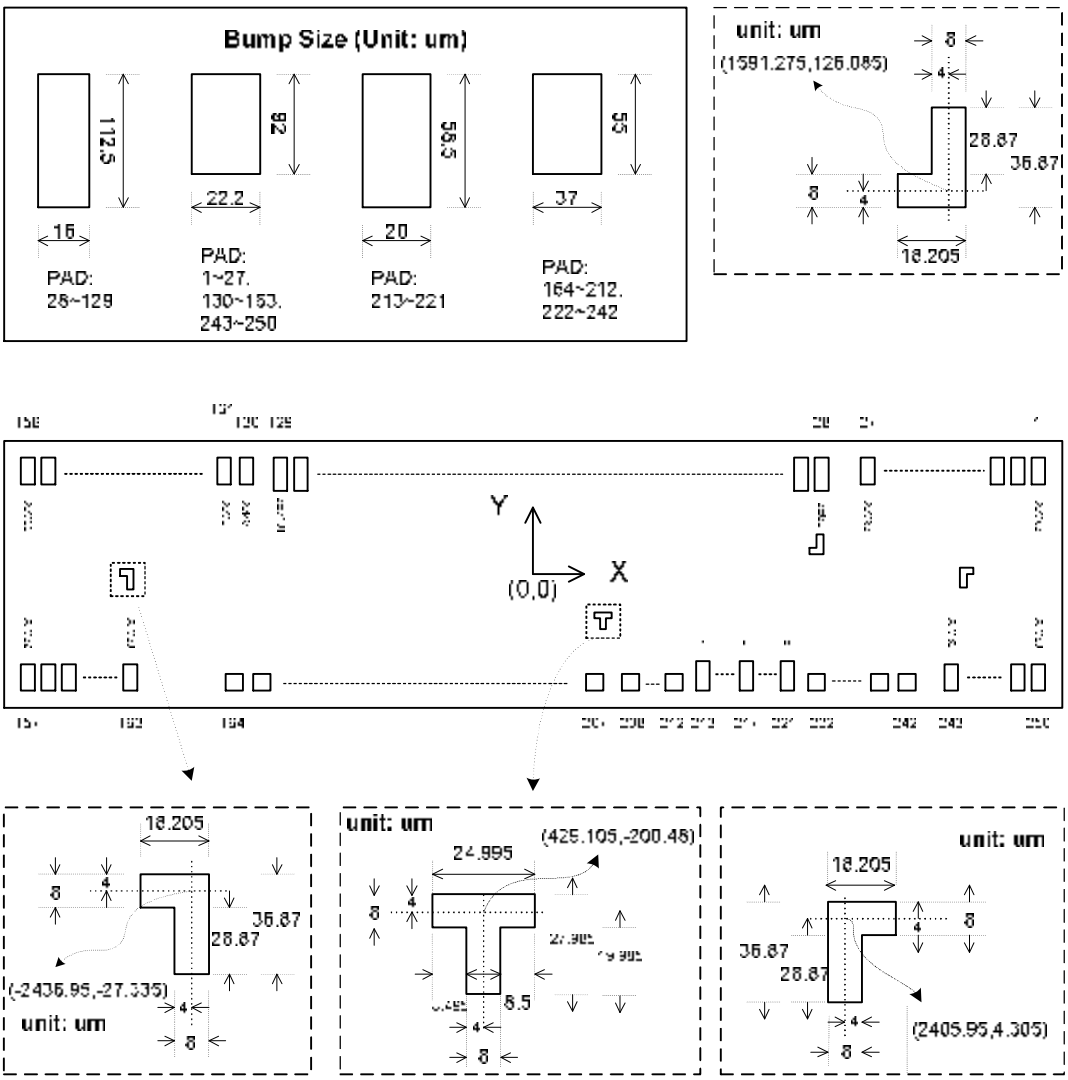


Fig 1

Pad Center Coordinates

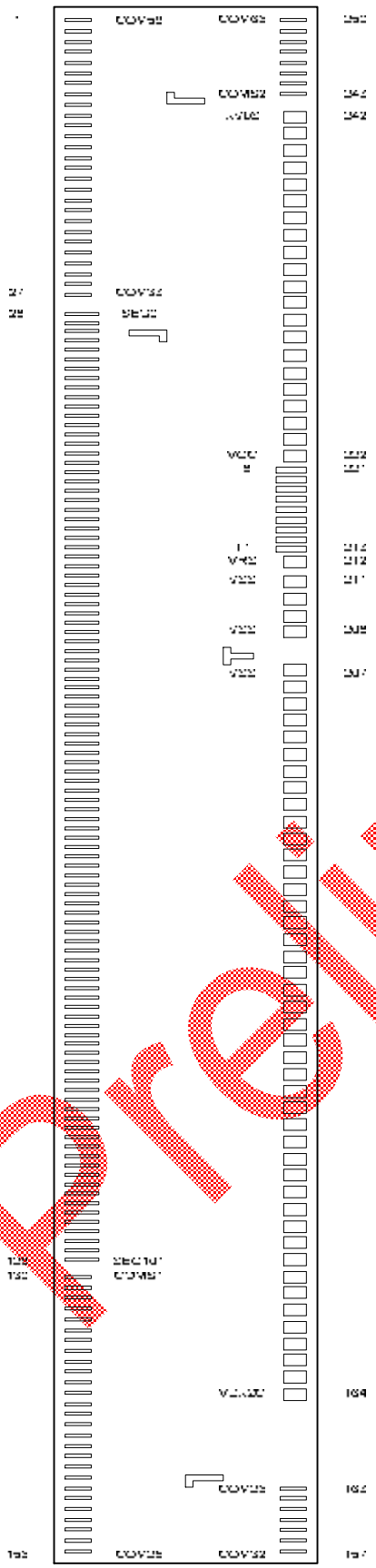


Fig 2

68 Duty (MY=0)

PAD NO.	PIN Name	X	Y
1	COM[59]	2695.50	293.00
2	COM[58]	2658.30	293.00
3	COM[57]	2621.10	293.00
4	COM[56]	2583.90	293.00
5	COM[55]	2546.70	293.00
6	COM[54]	2509.50	293.00
7	COM[53]	2472.30	293.00
8	COM[52]	2435.10	293.00
9	COM[51]	2397.90	293.00
10	COM[50]	2360.70	293.00
11	COM[49]	2323.50	293.00
12	COM[48]	2286.30	293.00
13	COM[47]	2249.10	293.00
14	COM[46]	2211.90	293.00
15	COM[45]	2174.70	293.00
16	COM[44]	2137.50	293.00
17	COM[43]	2100.30	293.00
18	COM[42]	2063.10	293.00
19	COM[41]	2025.90	293.00
20	COM[40]	1988.70	293.00
21	COM[39]	1951.50	293.00
22	COM[38]	1914.30	293.00
23	COM[37]	1877.10	293.00
24	COM[36]	1839.90	293.00
25	COM[35]	1802.70	293.00
26	COM[34]	1765.50	293.00
27	COM[33]	1728.30	293.00
28	SEG[0]	1665.39	282.75
29	SEG[1]	1632.39	282.75
30	SEG[2]	1599.39	282.75

PAD NO.	PIN Name	X	Y
31	SEG[3]	1566.39	282.75
32	SEG[4]	1533.39	282.75
33	SEG[5]	1500.39	282.75
34	SEG[6]	1467.39	282.75
35	SEG[7]	1434.39	282.75
36	SEG[8]	1401.39	282.75
37	SEG[9]	1368.39	282.75
38	SEG[10]	1335.39	282.75
39	SEG[11]	1302.39	282.75
40	SEG[12]	1269.39	282.75
41	SEG[13]	1236.39	282.75
42	SEG[14]	1203.39	282.75
43	SEG[15]	1170.39	282.75
44	SEG[16]	1137.39	282.75
45	SEG[17]	1104.39	282.75
46	SEG[18]	1071.39	282.75
47	SEG[19]	1038.39	282.75
48	SEG[20]	1005.39	282.75
49	SEG[21]	972.39	282.75
50	SEG[22]	939.39	282.75
51	SEG[23]	906.39	282.75
52	SEG[24]	873.39	282.75
53	SEG[25]	840.39	282.75
54	SEG[26]	807.39	282.75
55	SEG[27]	774.39	282.75
56	SEG[28]	741.39	282.75
57	SEG[29]	708.39	282.75
58	SEG[30]	675.39	282.75
59	SEG[31]	642.39	282.75
60	SEG[32]	609.39	282.75

PAD NO.	PIN Name	X	Y
61	SEG[33]	576.39	282.75
62	SEG[34]	543.39	282.75
63	SEG[35]	510.39	282.75
64	SEG[36]	477.39	282.75
65	SEG[37]	444.39	282.75
66	SEG[38]	411.39	282.75
67	SEG[39]	378.39	282.75
68	SEG[40]	345.39	282.75
69	SEG[41]	312.39	282.75
70	SEG[42]	279.39	282.75
71	SEG[43]	246.39	282.75
72	SEG[44]	213.39	282.75
73	SEG[45]	180.39	282.75
74	SEG[46]	147.39	282.75
75	SEG[47]	114.39	282.75
76	SEG[48]	81.39	282.75
77	SEG[49]	48.39	282.75
78	SEG[50]	15.39	282.75
79	SEG[51]	-17.60	282.75
80	SEG[52]	-50.60	282.75
81	SEG[53]	-83.60	282.75
82	SEG[54]	-116.60	282.75
83	SEG[55]	-149.60	282.75
84	SEG[56]	-182.60	282.75
85	SEG[57]	-215.60	282.75
86	SEG[58]	-248.60	282.75
87	SEG[59]	-281.60	282.75
88	SEG[60]	-314.60	282.75
89	SEG[61]	-347.60	282.75
90	SEG[62]	-380.60	282.75

PAD NO.	PIN Name	X	Y
91	SEG[63]	-413.60	282.75
92	SEG[64]	-446.60	282.75
93	SEG[65]	-479.60	282.75
94	SEG[66]	-512.60	282.75
95	SEG[67]	-545.60	282.75
96	SEG[68]	-578.60	282.75
97	SEG[69]	-611.60	282.75
98	SEG[70]	-644.60	282.75
99	SEG[71]	-677.60	282.75
100	SEG[72]	-710.60	282.75
101	SEG[73]	-743.60	282.75
102	SEG[74]	-776.60	282.75
103	SEG[75]	-809.60	282.75
104	SEG[76]	-842.60	282.75
105	SEG[77]	-875.60	282.75
106	SEG[78]	-908.60	282.75
107	SEG[79]	-941.60	282.75
108	SEG[80]	-974.60	282.75
109	SEG[81]	-1007.60	282.75
110	SEG[82]	-1040.60	282.75
111	SEG[83]	-1073.60	282.75
112	SEG[84]	-1106.60	282.75
113	SEG[85]	-1139.60	282.75
114	SEG[86]	-1172.60	282.75
115	SEG[87]	-1205.60	282.75
116	SEG[88]	-1238.60	282.75
117	SEG[89]	-1271.60	282.75
118	SEG[90]	-1304.60	282.75
119	SEG[91]	-1337.60	282.75
120	SEG[92]	-1370.60	282.75

PAD NO.	PIN Name	X	Y
121	SEG[93]	-1403.60	282.75
122	SEG[94]	-1436.60	282.75
123	SEG[95]	-1469.60	282.75
124	SEG[96]	-1502.60	282.75
125	SEG[97]	-1535.60	282.75
126	SEG[98]	-1568.60	282.75
127	SEG[99]	-1601.60	282.75
128	SEG[100]	-1634.60	282.75
129	SEG[101]	-1667.60	282.75
130	COMS1	-1728.30	293.00
131	COM[0]	-1765.50	293.00
132	COM[1]	-1802.70	293.00
133	COM[2]	-1839.90	293.00
134	COM[3]	-1877.10	293.00
135	COM[4]	-1914.30	293.00
136	COM[5]	-1951.50	293.00
137	COM[6]	-1988.70	293.00
138	COM[7]	-2025.90	293.00
139	COM[8]	-2063.10	293.00
140	COM[9]	-2100.30	293.00
141	COM[10]	-2137.50	293.00
142	COM[11]	-2174.70	293.00
143	COM[12]	-2211.90	293.00
144	COM[13]	-2249.10	293.00
145	COM[14]	-2286.30	293.00
146	COM[15]	-2323.50	293.00
147	COM[16]	-2360.70	293.00
148	COM[17]	-2397.90	293.00
149	COM[18]	-2435.10	293.00
150	COM[19]	-2472.30	293.00

PAD NO.	PIN Name	X	Y
151	COM[20]	-2509.50	293.00
152	COM[21]	-2546.70	293.00
153	COM[22]	-2583.90	293.00
154	COM[23]	-2621.10	293.00
155	COM[24]	-2658.30	293.00
156	COM[25]	-2695.50	293.00
157	COM[32]	-2695.50	-293.00
158	COM[31]	-2658.30	-293.00
159	COM[30]	-2621.10	-293.00
160	COM[29]	-2583.90	-293.00
161	COM[28]	-2546.70	-293.00
162	COM[27]	-2509.50	-293.00
163	COM[26]	-2472.30	-293.00
164	VDX2O	-2142.72	-311.50
165	VDX2O	-2083.42	-311.50
166	VDX2O	-2024.11	-311.50
167	VSS2	-1964.81	-311.50
168	T11	-1905.50	-311.50
169	T12	-1846.19	-311.50
170	BR	-1786.89	-311.50
171	CP	-1727.58	-311.50
172	T9	-1668.28	-311.50
173	T10	-1608.97	-311.50
174	PS2	-1549.67	-311.50
175	PS1	-1490.36	-311.50
176	PS0	-1431.06	-311.50
177	VMO	-1371.75	-311.50
178	VMO	-1312.45	-311.50
179	VMO	-1253.14	-311.50
180	VSS2	-1193.84	-311.50

PAD NO.	PIN Name	X	Y
181	VDD1	-1134.54	-311.50
182	VDD1	-1075.23	-311.50
183	VDD1	-1015.92	-311.50
184	VDD1	-956.62	-311.50
185	VDD2	-897.32	-311.50
186	VDD2	-838.01	-311.50
187	VDD2	-778.70	-311.50
188	VDD2	-719.40	-311.50
189	RESB	-660.09	-311.50
190	CSB	-600.79	-311.50
191	RWR	-541.48	-311.50
192	ERD	-482.18	-311.50
193	A0	-422.88	-311.50
194	VDD1	-363.57	-311.50
195	D7	-304.27	-311.50
196	D6	-244.96	-311.50
197	D5	-185.66	-311.50
198	D4	-126.35	-311.50
199	D3	-67.05	-311.50
200	D2	-7.74	-311.50
201	D1	51.56	-311.50
202	D0	110.87	-311.50
203	OSC	170.17	-311.50
204	VSS2	229.47	-311.50
205	VSS2	288.78	-311.50
206	VSS2	348.09	-311.50
207	VSS2	407.39	-311.50
208	VSS1	539.23	-311.50
209	VSS1	598.53	-311.50
210	VSS1	657.84	-311.50

PAD NO.	PIN Name	X	Y
211	VSS1	717.15	-311.50
212	VRS	788.45	-311.50
213	T1	835.10	-307.75
214	T2	868.40	-307.75
215	T3	901.70	-307.75
216	T4	935.00	-307.75
217	T0	973.80	-307.75
218	T5	1012.60	-307.75
219	T6	1045.90	-307.75
220	T7	1079.20	-307.75
221	T8	1112.50	-307.75
222	VGO	1158.81	-311.50
223	VGO	1218.11	-311.50
224	VGI	1277.42	-311.50
225	VGI	1336.72	-311.50
226	VGI	1396.03	-311.50
227	VGI	1455.33	-311.50
228	VGS	1514.64	-311.50
229	V0O	1581.08	-309.75
230	V0O	1640.38	-309.75
231	V0I	1699.69	-309.75
232	V0I	1759.00	-309.75
233	V0I	1818.30	-309.75
234	V0I	1877.60	-311.50
235	V0S	1936.91	-311.50
236	XV0O	1999.36	-311.50
237	XV0O	2058.67	-311.50
238	XV0I	2117.98	-311.50
239	XV0I	2177.28	-311.50
240	XV0I	2236.58	-311.50

PAD NO.	PIN Name	X	Y
241	XV0I	2295.89	-311.50
242	XV0S	2355.20	-311.50
243	COMS2	2435.10	-293.00
244	COM[60]	2472.30	-293.00
245	COM[61]	2509.50	-293.00
246	COM[62]	2546.70	-293.00
247	COM[63]	2583.90	-293.00
248	COM[64]	2621.10	-293.00
249	COM[65]	2658.30	-293.00
250	COM[66]	2695.50	-293.00

68 Duty (MY=1)

PAD NO.	PIN Name	X	Y
1	COM[7]	2695.50	293.00
2	COM[8]	2658.30	293.00
3	COM[9]	2621.10	293.00
4	COM[10]	2583.90	293.00
5	COM[11]	2546.70	293.00
6	COM[12]	2509.50	293.00
7	COM[13]	2472.30	293.00
8	COM[14]	2435.10	293.00
9	COM[15]	2397.90	293.00
10	COM[16]	2360.70	293.00
11	COM[17]	2323.50	293.00
12	COM[18]	2286.30	293.00
13	COM[19]	2249.10	293.00
14	COM[20]	2211.90	293.00
15	COM[21]	2174.70	293.00
16	COM[22]	2137.50	293.00
17	COM[23]	2100.30	293.00
18	COM[24]	2063.10	293.00
19	COM[25]	2025.90	293.00
20	COM[26]	1988.70	293.00
21	COM[27]	1951.50	293.00
22	COM[28]	1914.30	293.00
23	COM[29]	1877.10	293.00
24	COM[30]	1839.90	293.00
25	COM[31]	1802.70	293.00
26	COM[32]	1765.50	293.00
27	COM[33]	1728.30	293.00
28	SEG[0]	1665.39	282.75
29	SEG[1]	1632.39	282.75
30	SEG[2]	1599.39	282.75

PAD NO.	PIN Name	X	Y
31	SEG[3]	1566.39	282.75
32	SEG[4]	1533.39	282.75
33	SEG[5]	1500.39	282.75
34	SEG[6]	1467.39	282.75
35	SEG[7]	1434.39	282.75
36	SEG[8]	1401.39	282.75
37	SEG[9]	1368.39	282.75
38	SEG[10]	1335.39	282.75
39	SEG[11]	1302.39	282.75
40	SEG[12]	1269.39	282.75
41	SEG[13]	1236.39	282.75
42	SEG[14]	1203.39	282.75
43	SEG[15]	1170.39	282.75
44	SEG[16]	1137.39	282.75
45	SEG[17]	1104.39	282.75
46	SEG[18]	1071.39	282.75
47	SEG[19]	1038.39	282.75
48	SEG[20]	1005.39	282.75
49	SEG[21]	972.39	282.75
50	SEG[22]	939.39	282.75
51	SEG[23]	906.39	282.75
52	SEG[24]	873.39	282.75
53	SEG[25]	840.39	282.75
54	SEG[26]	807.39	282.75
55	SEG[27]	774.39	282.75
56	SEG[28]	741.39	282.75
57	SEG[29]	708.39	282.75
58	SEG[30]	675.39	282.75
59	SEG[31]	642.39	282.75
60	SEG[32]	609.39	282.75

PAD NO.	PIN Name	X	Y
61	SEG[33]	576.39	282.75
62	SEG[34]	543.39	282.75
63	SEG[35]	510.39	282.75
64	SEG[36]	477.39	282.75
65	SEG[37]	444.39	282.75
66	SEG[38]	411.39	282.75
67	SEG[39]	378.39	282.75
68	SEG[40]	345.39	282.75
69	SEG[41]	312.39	282.75
70	SEG[42]	279.39	282.75
71	SEG[43]	246.39	282.75
72	SEG[44]	213.39	282.75
73	SEG[45]	180.39	282.75
74	SEG[46]	147.39	282.75
75	SEG[47]	114.39	282.75
76	SEG[48]	81.39	282.75
77	SEG[49]	48.39	282.75
78	SEG[50]	15.39	282.75
79	SEG[51]	-17.60	282.75
80	SEG[52]	-50.60	282.75
81	SEG[53]	-83.60	282.75
82	SEG[54]	-116.60	282.75
83	SEG[55]	-149.60	282.75
84	SEG[56]	-182.60	282.75
85	SEG[57]	-215.60	282.75
86	SEG[58]	-248.60	282.75
87	SEG[59]	-281.60	282.75
88	SEG[60]	-314.60	282.75
89	SEG[61]	-347.60	282.75
90	SEG[62]	-380.60	282.75

PAD NO.	PIN Name	X	Y
91	SEG[63]	-413.60	282.75
92	SEG[64]	-446.60	282.75
93	SEG[65]	-479.60	282.75
94	SEG[66]	-512.60	282.75
95	SEG[67]	-545.60	282.75
96	SEG[68]	-578.60	282.75
97	SEG[69]	-611.60	282.75
98	SEG[70]	-644.60	282.75
99	SEG[71]	-677.60	282.75
100	SEG[72]	-710.60	282.75
101	SEG[73]	-743.60	282.75
102	SEG[74]	-776.60	282.75
103	SEG[75]	-809.60	282.75
104	SEG[76]	-842.60	282.75
105	SEG[77]	-875.60	282.75
106	SEG[78]	-908.60	282.75
107	SEG[79]	-941.60	282.75
108	SEG[80]	-974.60	282.75
109	SEG[81]	-1007.60	282.75
110	SEG[82]	-1040.60	282.75
111	SEG[83]	-1073.60	282.75
112	SEG[84]	-1106.60	282.75
113	SEG[85]	-1139.60	282.75
114	SEG[86]	-1172.60	282.75
115	SEG[87]	-1205.60	282.75
116	SEG[88]	-1238.60	282.75
117	SEG[89]	-1271.60	282.75
118	SEG[90]	-1304.60	282.75
119	SEG[91]	-1337.60	282.75
120	SEG[92]	-1370.60	282.75

PAD NO.	PIN Name	X	Y
121	SEG[93]	-1403.60	282.75
122	SEG[94]	-1436.60	282.75
123	SEG[95]	-1469.60	282.75
124	SEG[96]	-1502.60	282.75
125	SEG[97]	-1535.60	282.75
126	SEG[98]	-1568.60	282.75
127	SEG[99]	-1601.60	282.75
128	SEG[100]	-1634.60	282.75
129	SEG[101]	-1667.60	282.75
130	COMS1	-1728.30	293.00
131	COM[66]	-1765.50	293.00
132	COM[65]	-1802.70	293.00
133	COM[64]	-1839.90	293.00
134	COM[63]	-1877.10	293.00
135	COM[62]	-1914.30	293.00
136	COM[61]	-1951.50	293.00
137	COM[660	-1988.70	293.00
138	COM[59]	-2025.90	293.00
139	COM[58]	-2063.10	293.00
140	COM[57]	-2100.30	293.00
141	COM[56]	-2137.50	293.00
142	COM[55]	-2174.70	293.00
143	COM[54]	-2211.90	293.00
144	COM[53]	-2249.10	293.00
145	COM[52]	-2286.30	293.00
146	COM[51]	-2323.50	293.00
147	COM[50]	-2360.70	293.00
148	COM[49]	-2397.90	293.00
149	COM[48]	-2435.10	293.00
150	COM[47]	-2472.30	293.00

PAD NO.	PIN Name	X	Y
151	COM[46]	-2509.50	293.00
152	COM[45]	-2546.70	293.00
153	COM[44]	-2583.90	293.00
154	COM[43]	-2621.10	293.00
155	COM[42]	-2658.30	293.00
156	COM[41]	-2695.50	293.00
157	COM[34]	-2695.50	-293.00
158	COM[35]	-2658.30	-293.00
159	COM[36]	-2621.10	-293.00
160	COM[37]	-2583.90	-293.00
161	COM[38]	-2546.70	-293.00
162	COM[39]	-2509.50	-293.00
163	COM[40]	-2472.30	-293.00
164	VDX2O	-2142.72	-311.50
165	VDX2O	-2083.42	-311.50
166	VDX2O	-2024.11	-311.50
167	VSS2	-1964.81	-311.50
168	T11	-1905.50	-311.50
169	T12	-1846.19	-311.50
170	BR	-1786.89	-311.50
171	CP	-1727.58	-311.50
172	T9	-1668.28	-311.50
173	T10	-1608.97	-311.50
174	PS2	-1549.67	-311.50
175	PS1	-1490.36	-311.50
176	PS0	-1431.06	-311.50
177	VMO	-1371.75	-311.50
178	VMO	-1312.45	-311.50
179	VMO	-1253.14	-311.50
180	VSS2	-1193.84	-311.50

PAD NO.	PIN Name	X	Y
181	VDD1	-1134.54	-311.50
182	VDD1	-1075.23	-311.50
183	VDD1	-1015.92	-311.50
184	VDD1	-956.62	-311.50
185	VDD2	-897.32	-311.50
186	VDD2	-838.01	-311.50
187	VDD2	-778.70	-311.50
188	VDD2	-719.40	-311.50
189	RESB	-660.09	-311.50
190	CSB	-600.79	-311.50
191	RWR	-541.48	-311.50
192	ERD	-482.18	-311.50
193	A0	-422.88	-311.50
194	VDD1	-363.57	-311.50
195	D7	-304.27	-311.50
196	D6	-244.96	-311.50
197	D5	-185.66	-311.50
198	D4	-126.35	-311.50
199	D3	-67.05	-311.50
200	D2	-7.74	-311.50
201	D1	51.56	-311.50
202	D0	110.87	-311.50
203	OSC	170.17	-311.50
204	VSS2	229.47	-311.50
205	VSS2	288.78	-311.50
206	VSS2	348.09	-311.50
207	VSS2	407.39	-311.50
208	VSS1	539.23	-311.50
209	VSS1	598.53	-311.50
210	VSS1	657.84	-311.50

PAD NO.	PIN Name	X	Y
211	VSS1	717.15	-311.50
212	VRS	788.45	-311.50
213	T1	835.10	-307.75
214	T2	868.40	-307.75
215	T3	901.70	-307.75
216	T4	935.00	-307.75
217	T0	973.80	-307.75
218	T5	1012.60	-307.75
219	T6	1045.90	-307.75
220	T7	1079.20	-307.75
221	T8	1112.50	-307.75
222	VGO	1158.81	-311.50
223	VGO	1218.11	-311.50
224	VGI	1277.42	-311.50
225	VGI	1336.72	-311.50
226	VGI	1396.03	-311.50
227	VGI	1455.33	-311.50
228	VGS	1514.64	-311.50
229	V0O	1581.08	-309.75
230	V0O	1640.38	-309.75
231	V0I	1699.69	-309.75
232	V0I	1759.00	-309.75
233	V0I	1818.30	-309.75
234	V0I	1877.60	-311.50
235	V0S	1936.91	-311.50
236	XV0O	1999.36	-311.50
237	XV0O	2058.67	-311.50
238	XV0I	2117.98	-311.50
239	XV0I	2177.28	-311.50
240	XV0I	2236.58	-311.50

PAD NO.	PIN Name	X	Y
241	XV0I	2295.89	-311.50
242	XV0S	2355.20	-311.50
243	COMS2	2435.10	-293.00
244	COM[6]	2472.30	-293.00
245	COM[5]	2509.50	-293.00
246	COM[4]	2546.70	-293.00
247	COM[3]	2583.90	-293.00
248	COM[2]	2621.10	-293.00
249	COM[1]	2658.30	-293.00
250	COM[0]	2695.50	-293.00

4. BLOCK DIAGRAM

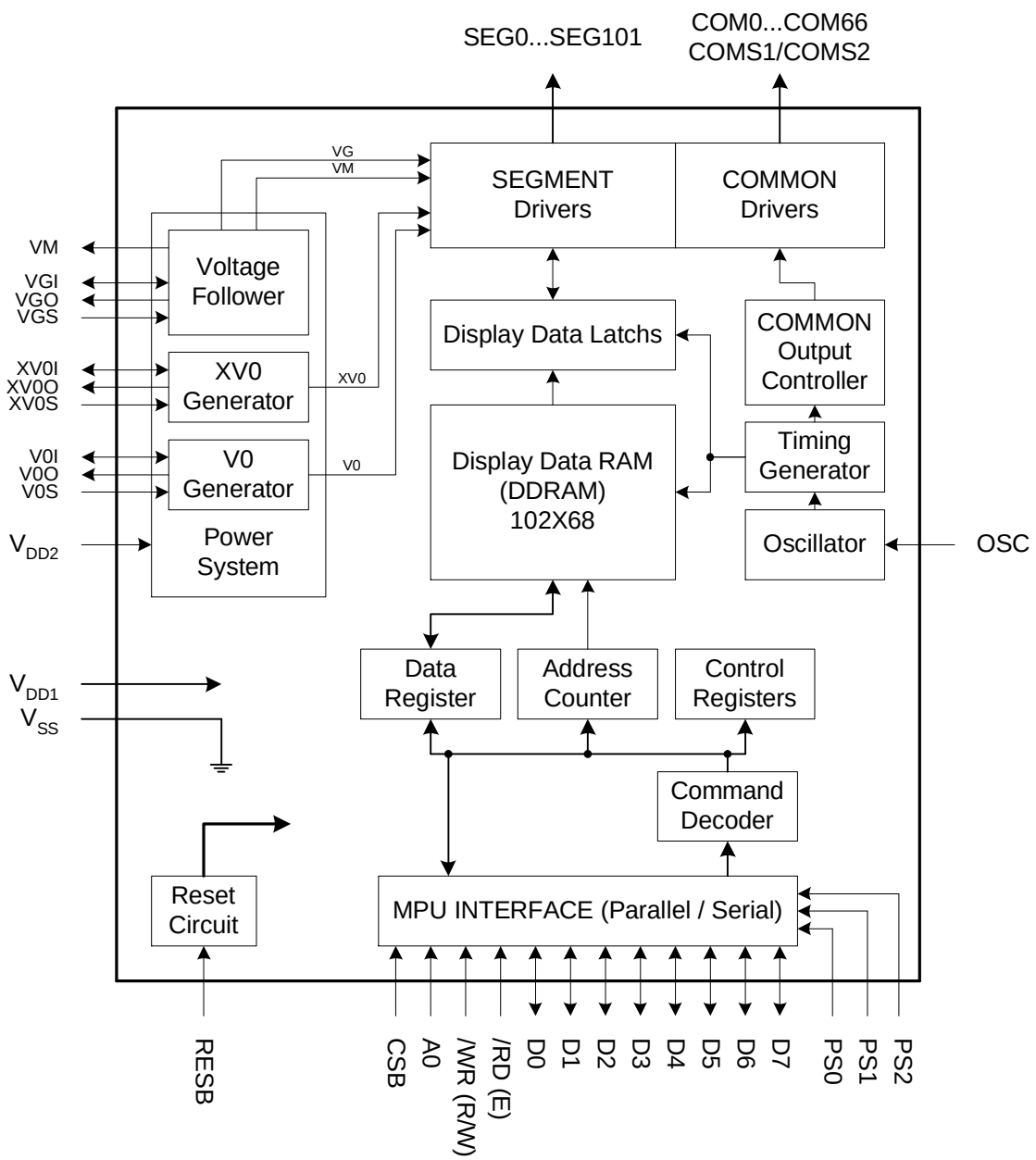


Fig 3 Block diagram

5. PINNING DESCRIPTIONS

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td colspan="4">Lcd driver outputs</td></tr>
<tr><td>SEG0 to SEG101</td><td>O</td><td>LCD segment driver outputs
This display data and the M signal control the output voltage of segment driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">Frame</td><td colspan="2">Segment drover output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>VG</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>H</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>L</td><td>VG</td><td>VSS</td></tr>
<tr><td colspan="2">Power save mode</td><td>VSS</td><td>VSS</td></tr>
</table></td><td>102</td></tr>
<tr><td>COM0 to COM66</td><td>O</td><td>LCD column driver outputs
This internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">Frame</td><td colspan="2">Common drover output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">XV0</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">VM</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">VM</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">VSS</td></tr>
</table></td><td>67</td></tr>
<tr><td>COMS</td><td>O</td><td>Common output for the icons
The output signals of two pins are same. When not used, this pin should be left open.</td><td>2</td></tr>
<tr><td colspan="4">MICROPROCESSOR INTERFACE</td></tr>
<tr><td>PS[2:0]</td><td>I</td><td>Microprocessor interface select input pin
<table>
<tr><td>PS2</td><td>PS1</td><td>PS0</td><td>State</td></tr>
<tr><td>“ L “</td><td>“ L “</td><td>“ L “</td><td>4 Pin-SPI MPU interface</td></tr>
<tr><td>“ H “</td><td>“ L “</td><td>“ L “</td><td>3 Pin-SPI MPU interface</td></tr>
<tr><td>“ L “</td><td>“ H “</td><td>“ L “</td><td>8080-series parallel MPU interface</td></tr>
<tr><td>“ H “</td><td>“ H “</td><td>“ L “</td><td>6800-series parallel MPU interface</td></tr>
<tr><td>“ H “</td><td>“H”</td><td>“ H “</td><td>I^2C interface</td></tr>
</table></td><td>3</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pins
Data/instruction I/O is enabled only when CSB is “L”. When chip select is non-active, DB0 to DB7 is high impedance.
There is no CSB pin in I^2C interface, so this pin can fix to ” H”</td><td>1</td></tr>
<tr><td>RESB</td><td>I</td><td>Reset input pin
When RESB is “L”, initialization is executed.</td><td>1</td></tr>
<tr><td>A0</td><td>I</td><td>It determines whether the data bits are data or a command.
A0=”H“: Indicates that D0 to D7 are display data.
A0=”L“: Indicates that D0 to D7 are control data.
There is no A0 pin in three line or I^2C interface, so this pin can fix to ” H”</td><td>1</td></tr>
</table>

<table>
<tr>
<td>RWR</td>
<td>I</td>
<td>Read/Write execution control pin (PS[0:1]=[L:H])
<table>
<tr><th>PS2</th><th>MPU type</th><th>/WR(R/W)</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>R/W</td><td>Read/Write control input pin
R/W=”H“: read
R/W=”L”: write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on D0 to D7 are latched at the rising edge of the /WR signal</td></tr>
</table>
When in the serial interface must fix to ”H”</td>
<td>1</td>
</tr>
<tr>
<td>ERD</td>
<td>I</td>
<td>Read/Write execution control pin (PS[0:1]=[L:H])
<table>
<tr><th>PS2</th><th>MPU Type</th><th>/RD (E)</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read/Write control input pin
R/W=”H“: When E is “H”, D0 to D7 are in an output status.
R/W=”L“: The data on D0 to D7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, D0 to D7 are in an output status.</td></tr>
</table>
When in the serial interface must fix to ” H”</td>
<td>1</td>
</tr>
<tr>
<td>D7 to D4
D1 to D3 (SDA)
D0(SCLK)</td>
<td>I/O</td>
<td>When using 8-bit parallel interface: 6800 . 8080
8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus.
When chip select is not active, D0 to D7 is high impedance.

When using serial interface: 4-LINE
D0: serial input clock (SCLK)
D1,D2, D3 : serial input data (SDA), must be connected together
D4, D5, D6, D7 : must fix to ”H”
When chip select is not active, D0 to D7 is high impedance.

When using serial interface: 3-LINE
D0 : serial input clock (SCLK)
D1 : serial input data (SDA_IN)
D2, D3 : serial data output for read ID function(SDA_OUT)
Suggest D1~D3 be connected together;
When chip select is not active, D0 to D7 is high impedance.</td>
<td>8</td>
</tr>
</table>

D7 to D6 (SA) D5 to D4(X) D3 to D2 (SDA_OUT) D1 (SDA_IN) D0 (SCLK)		**When using I^2C interface** D0: serial clock input (SCLK) D1: serial input data (SDA_IN) D2, D3: (SDA_OUT) serial data acknowledge for the I^2C interface. By connecting SDA_OUT to SDA_IN externally, the SDA line becomes fully I^2C interface compatible. Having the acknowledge output separated from the serial data line is advantageous in chip on glass (COG) applications. In COG application where the track resistance from the SDA_OUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the ITO track resistance. It is possible the during the acknowledge cycle the ST7579 will not be able to create a valid logic 0 level. By splitting the SDA_IN input from the SDA_OUT output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDA_OUT pad to the system SDA line to guarantee a valid low level. **D1,D2,D3 must be connected together (SDA)** D4, D5: must fix to "H" D6, D7: Are slave address (SA) bit0, 1, must fix to "H" or "L" Chip select pin "CSB" is not used and must fix to "H".	
LCD DRIVER SUPPLY			
OSC	**I**	**When the on-chip oscillator is used, this input must be connected to V_{DD1}.** An external clock signal, if used, is connected to this input. If the oscillator and external clock are both inhibited by connecting the OSC pin to VSS the display is not clocked and may be left in a DC state. To avoid this, the chip should always be put into Power Down Mode before stopping the clock.	**1**
Power Supply Pins			
VSS1	**Power**	Digital ground: must be connected with VSS2	**4**
VSS2	**Power**	Analog ground: must be connected with VSS1	**6**
VDX2	**Power**	VDD*2 Testing mode power. Must be floating.	**1**
VDD1	**Power**	Digital Supply voltage:1.8V~3.3V The 2 supply rails V_{DD1} and V_{DD2} could be connected together. If Digital Option pin is high, must be this level	**5**
VDD2	**Power**	Analog Supply voltage:2.4V~3.3V The 2 supply rails V_{DD1} and V_{DD2} could be connected together.	**4**
XV0	**Power**	Negative LCD driver supply voltage XV0O, XV0I & XV0S should be separated in ITO layout. XV0O, XV0I & XV0S should be connected together in FPC layout.	**7**
V0	**Power**	Positive LCD driver supply voltage V0 ≥ VG ≥ VM ≥ VSS ≥ XV0 V0O, V0I & V0S should be separated in ITO layout. V0O, V0I & V0S should be connected together in FPC layout.	**7**
VG	**Power**	LCD driving voltage for segments VGO, VGI & VGS should be separated in ITO layout. VGO, VGI & VGS should be connected together in FPC layout.	**7**
VMO	**Power**	VM output. LCD driving voltage for commons.	**4**
VRS	**Power**	Monitor Voltage Regulator level, must be left open.	**1**

Configuration Pins			
CP	**I**	Set Booster stages. (“L”=4X; “H”=5X) CP pin set the default value of booster stages after reset , and booster stage can be changed by software instruction	**1**
BR	**I**	Set LCD bias ratio. (“L”=1/7; “H”=1/9) BR pin set the default value of bias ratio after reset , and bias ratio can be changed by software instruction	**1**
Test Pin			
T0~T10	**T**	Do NOT use. Reserved for testing. Must be floating	**11**
T11	**T**	Do NOT use. Reserved for testing. Must be pull high	**1**
T12	**T**	Do NOT use. Reserved for testing. Must be pull high	**1**

ST7579 I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
PS[2:0], OSC, CP, BR, T11, T12	**No Limitation**
T0~T10, VRS, VDX2	**Floating**
VDD1, VDD2, VSS	**<100Ω**
V0, VG, VM, XV0	**<500Ω**
A0, /WR, /RD, CSB, D7…D0	**<1KΩ**
RESB	**RESB<10KΩ**

6. FUNCTIONS DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There is CSB pin for chip selection. The ST7579 can interface with an MPU when CSB is "L". When CSB is “H”, these pins are set to any other combination, A0, /RD(E), and /WR(R/W) inputs are disabled and D0 to D7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

ST7579 has five types of interface with an MPU, which are three serial and two parallel interfaces. This parallel or serial interface is determined by PS [0:2] pin as shown in table 1.

Table 1. Parallel/Serial Interface Mode

PS2	PS1	PS0	CSB	A0	State
" L "	" L "	" L "	CSB	A0	4 Pin-SPI MPU interface
" H "	" L "	" L "	CSB	" * "	3 Pin-SPI MPU interface
" L "	" H "	" L "	CSB	A0	8080-series parallel MPU interface
" H "	" H "	" L "	CSB	A0	6800-series parallel MPU interface
" H "	" H "	" H "	" * "	" * "	I^2C interface

Parallel Interface

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS2 as shown in table 2. The type of data transfer is determined by signals at A0, /RD (E) and /WR(R/W) as shown in table 3.

Table 2. Microprocessor Selection for Parallel Interface

PS2	PS1	PS0	CSB	A0	/RD (E)	/WR (R/W)	D0 to D7	MPU bus
H	H	L	CSB	A0	E	R/W	D0 to D7	6800-series
L	H	L	CSB	A0	/RD	/WR	D0 to D7	8080-series

Table 3. Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E (/RD)	R/W (/WR)	/RD (E)	/WR (R/W)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

NOTE: When /RD (E) pin is always pulled high for 6800-series interface, it can be used CSB for enable signal. In this case, interface data is latched at the rising edge of CSB and the type of data transfer is determined by signals at A0, /WR(R/W) as in case of 6800-series mode.

Serial Interface

Serial Mode	PS2	PS1	PS0	CSB	A0
4-line SPI interface	L	L	L	CSB	Used
3-line SPI interface	H	L	L	CSB	Not Used Fix to “H”
I^2C interface	H	H	H	Not Used Fix to “H”	Not Used Fix to “H”

PS2= “L”, PS1= “L”, PS0= “L”: 4-line SPI interface

When the ST7579 is active (CSB=”L”), serial data (D1) and serial clock (D0) inputs are enabled. When CSB is “High”, the internal 8-bit shift register and the 3-bit counter are reset. The display data/command indication is controlled by the register selection pin (A0). The signals transferred on data bus will be display data when A0 is high and will be instruction when A0 is low. The read feature is not supported in this mode. Serial data on SDA (D1) is latched at the rising edge of serial clock on SCLK (D0). After the eighth serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.

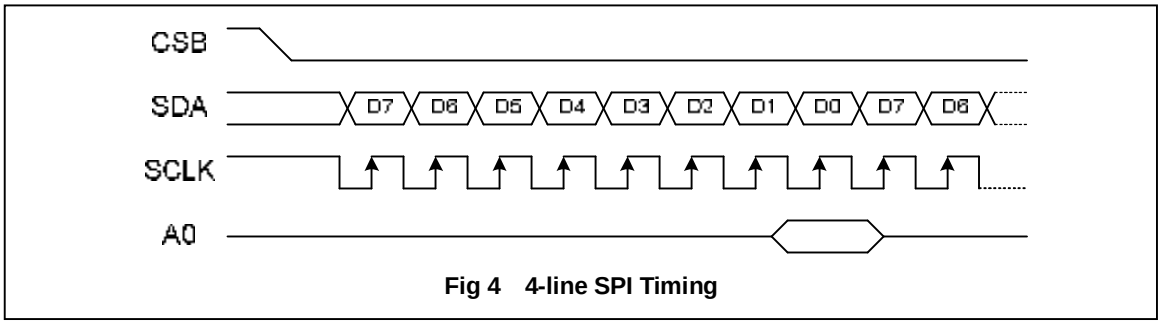


Fig 4 4-line SPI Timing

PS2= “L”, PS1= “L”, PS0= “H”: 3-line SPI interface

When ST7579 is active (CSB=”L”), SDA-out, SDA-in and SCL inputs are enabled. When ST7579 is not active (CSB=”H”), the internal 8-bit shift register and the 3-bit counter are reset. The A0 pin is not available in this mode. Before issuing serial data, an A0 bit is required to indicate the access is data or instruction. The read feature is not supported in this mode except ID code read feature. Serial data on SDA (D1) is latched at the rising edge of serial clock on SCLK (D0). After the eighth serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.

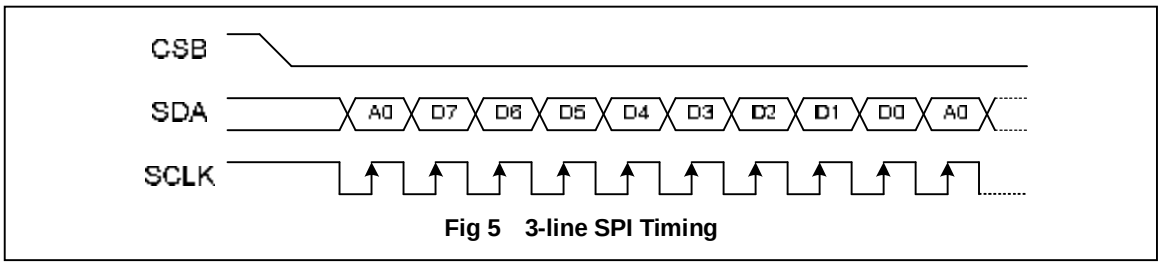


Fig 5 3-line SPI Timing

PS2= "H", PS1= "H", PS0= "H": I²C Interface

The I²C interface receives and executes the commands sent via the I²C Interface. It also receives RAM data and sends it to the RAM.

The I²C Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.6.

START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.7.

SYSTEM CONFIGURATION

The system configuration is illustrated in Fig.8.

- Transmitter: the device, which sends the data to the bus
- Receiver: the device, which receives the data from the bus
- Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating a acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I²C Interface is illustrated in Fig.9.

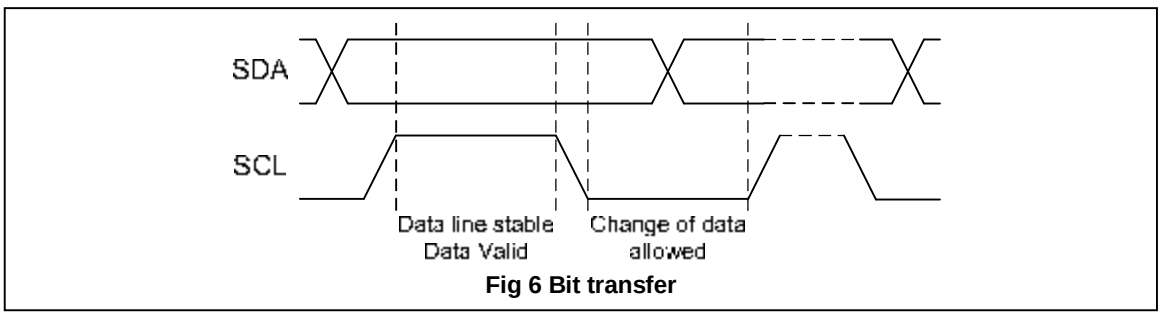


Fig 6 Bit transfer

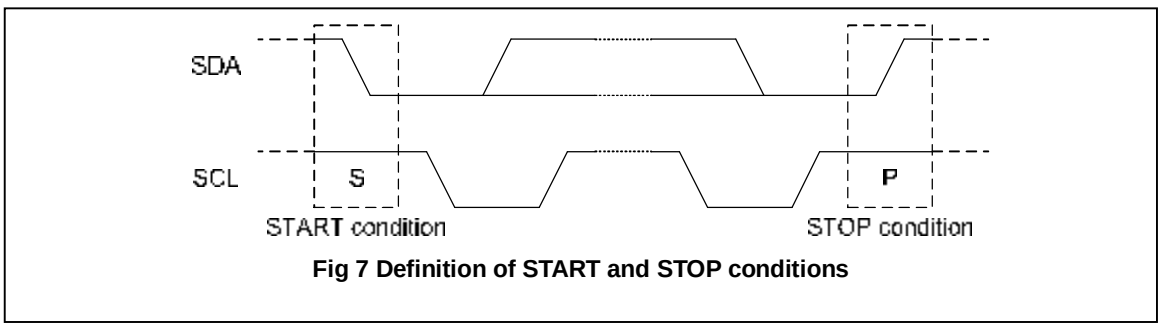


Fig 7 Definition of START and STOP conditions

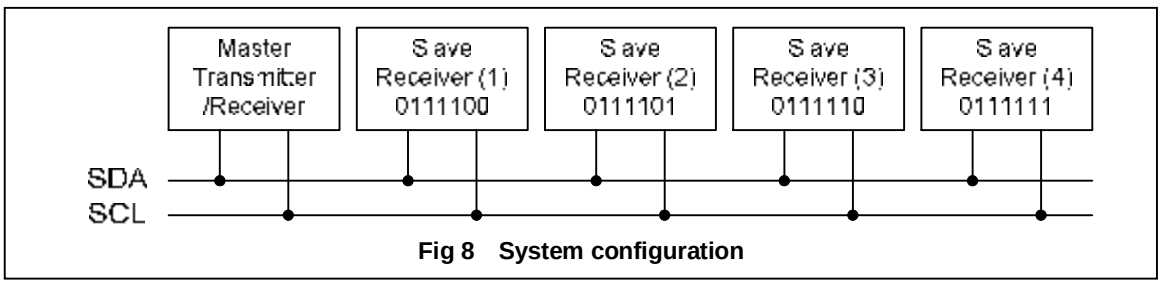


Fig 8 System configuration

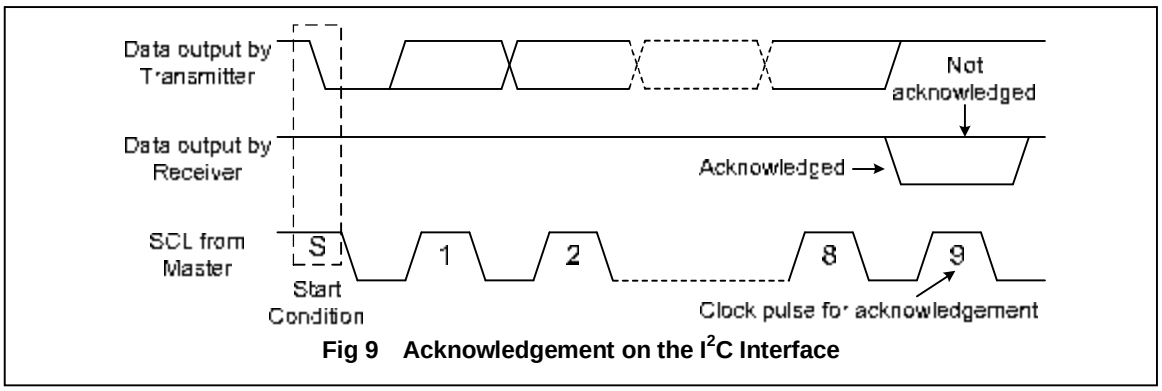


Fig 9 Acknowledgement on the I²C Interface

I²C Interface protocol

The ST7579 supports command, data write addressed slaves on the bus.

Before any data is transmitted on the I²C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100,0111101, 0111110 and 0111111) are reserved for the ST7579. The least significant bit of the slave address is set by connecting the input SA0 and SA1 to either logic 0 or logic 1 (V_{DD1}).

The I²C Interface protocol is illustrated in Fig.10.

The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.

A command word consists of a control byte, which defines Co and A0, and a data byte.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended ST7579 device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

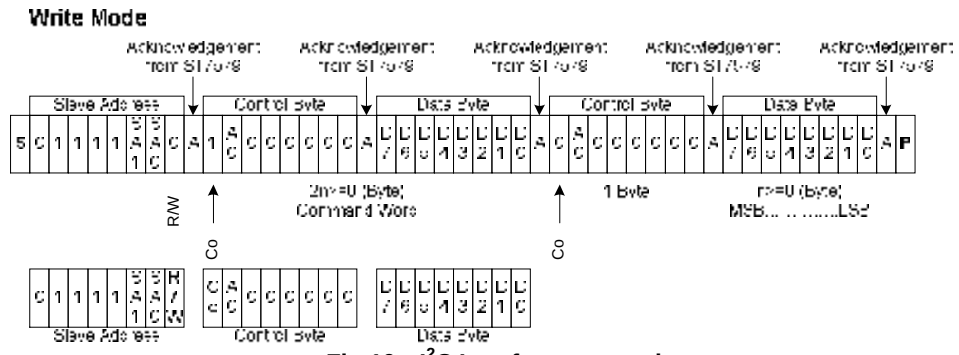


Fig 10 I²C Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by s STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

Data Transfer

The ST7579 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Fig. 11. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in Fig. 12. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

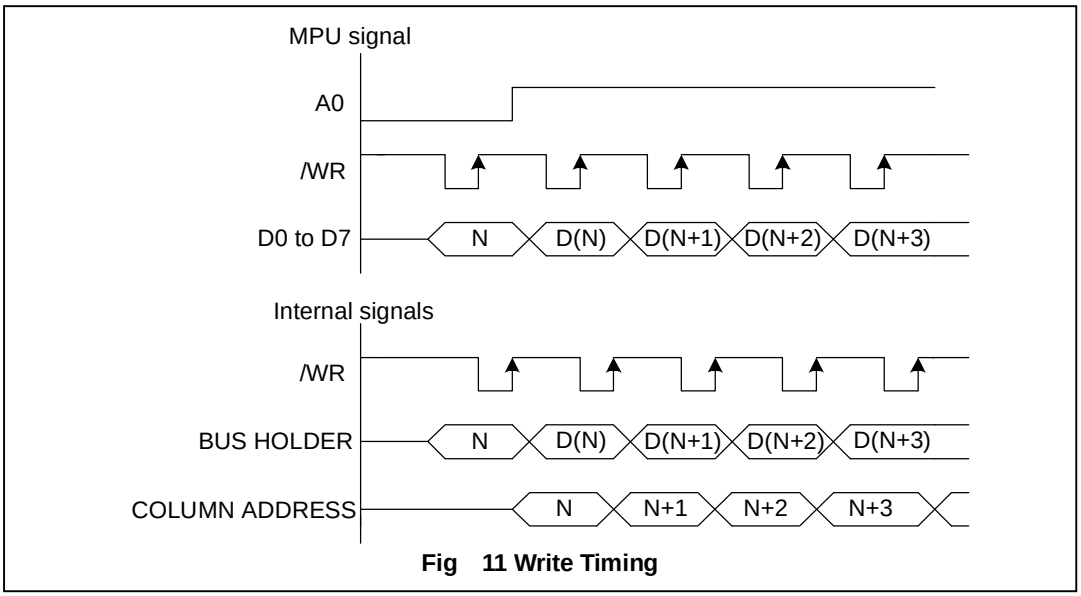


Fig 11 Write Timing

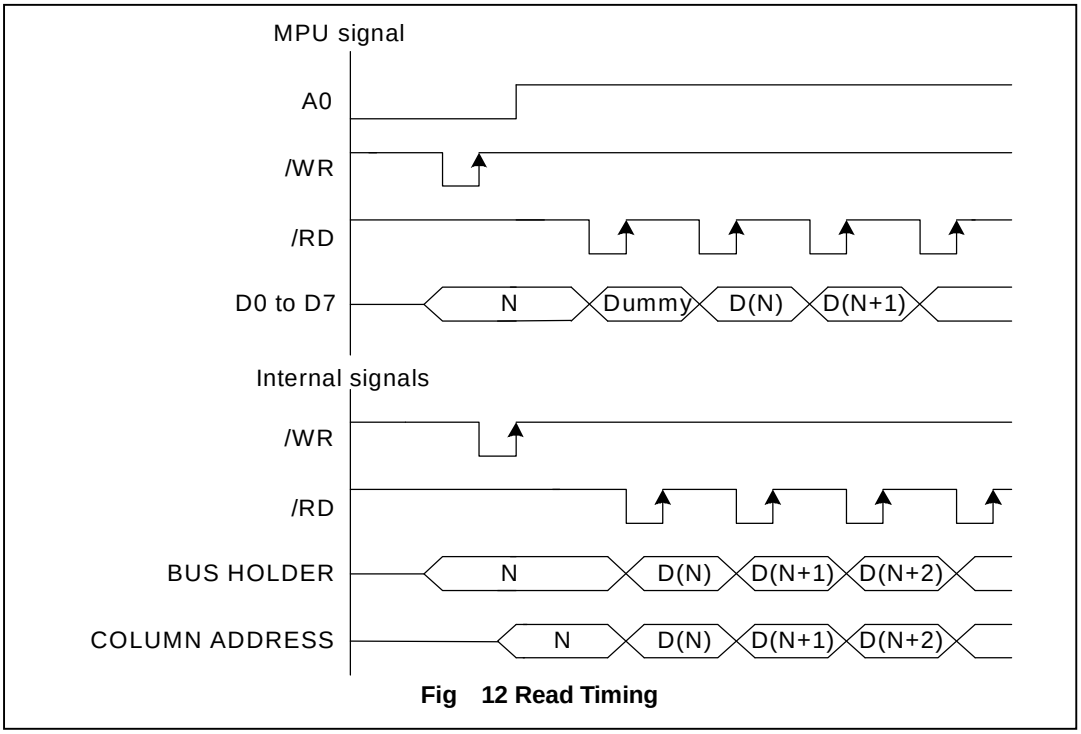


Fig 12 Read Timing

DISPLAY DATA RAM (DDRAM)

The ST7579 contains a 68X102 bit static RAM that stores the display data. The display data RAM store the dot data for the LCD. It has a 68(8 pageX8 bit +1 pageX3 bit +1 pageX1 bit) X 102 . There is a direct correspondence between X-address and column output number. It is 68-row by 102-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines (0~63 COM) and 8th page with three line (D0 ~D2) (64~ 66 COM) and 9th page with a single line (D0 only)(67 row—COMS (ICON). Data is read from or written to the 8 lines of each page directly through D0 to D7. The display data of D0 to D7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM. It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 9 is a special RAM area for the icons and display data D0 is only valid.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in Fig. 10. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 102-bit RAM data to the display data latch circuit. When icon is selected by setting icon page address, display data of icons are not scrolled because the MPU cannot access Line Address of icons.

Column Address Circuit

Column Address Circuit has an 8-bit preset counter that provides Column Address to the Display Data RAM as shown in figure16. The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously.

Register MX and MY selection instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing MX select instruction. Refer to the following tables.

SEG Output

SEG Output MX	SEG0	SEG101
"0"	SEG0 à Segment Address à	SEG101
"1"	SEG101 ß Segment Address ß	SEG0

Com Output

SEG Output MY	Common output pins COM0	COM66	COMS
"0"	COM0 à Common Address à	COM66	COMS
"1"	COM66 ß Common Address ß	COM0	COMS

ADDRESSING

Data is downloaded in bytes into the RAM matrix of ST7579 as indicated in Figs. 13~15. The display RAM has a matrix of 68 by 102 bits. The address pointer addresses the columns. The address ranges are: X 0 to 101 (1100101), Y 0 to 9 (1001) .Addresses outside these ranges are not allowed.

In horizontal addressing mode the X address increments after each byte (see Fig.14). After the last X address (X = 101) X wraps around to 0 and Y increments to address the next row.

After the very last address (X = 101, Y = 9) the address pointers wrap around to address (X = 0, Y =0)

Data structure

Fig 13 RAM format, if DO=0

Fig 14 RAM format, if DO=1

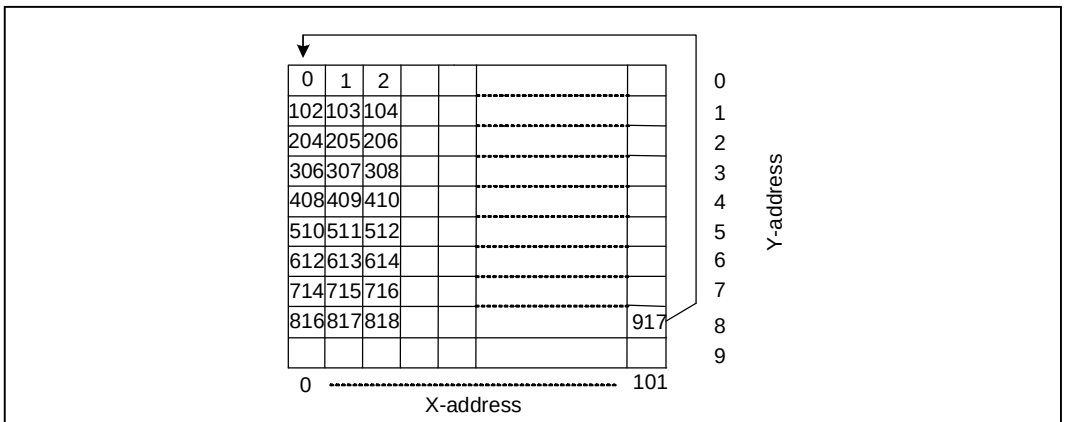
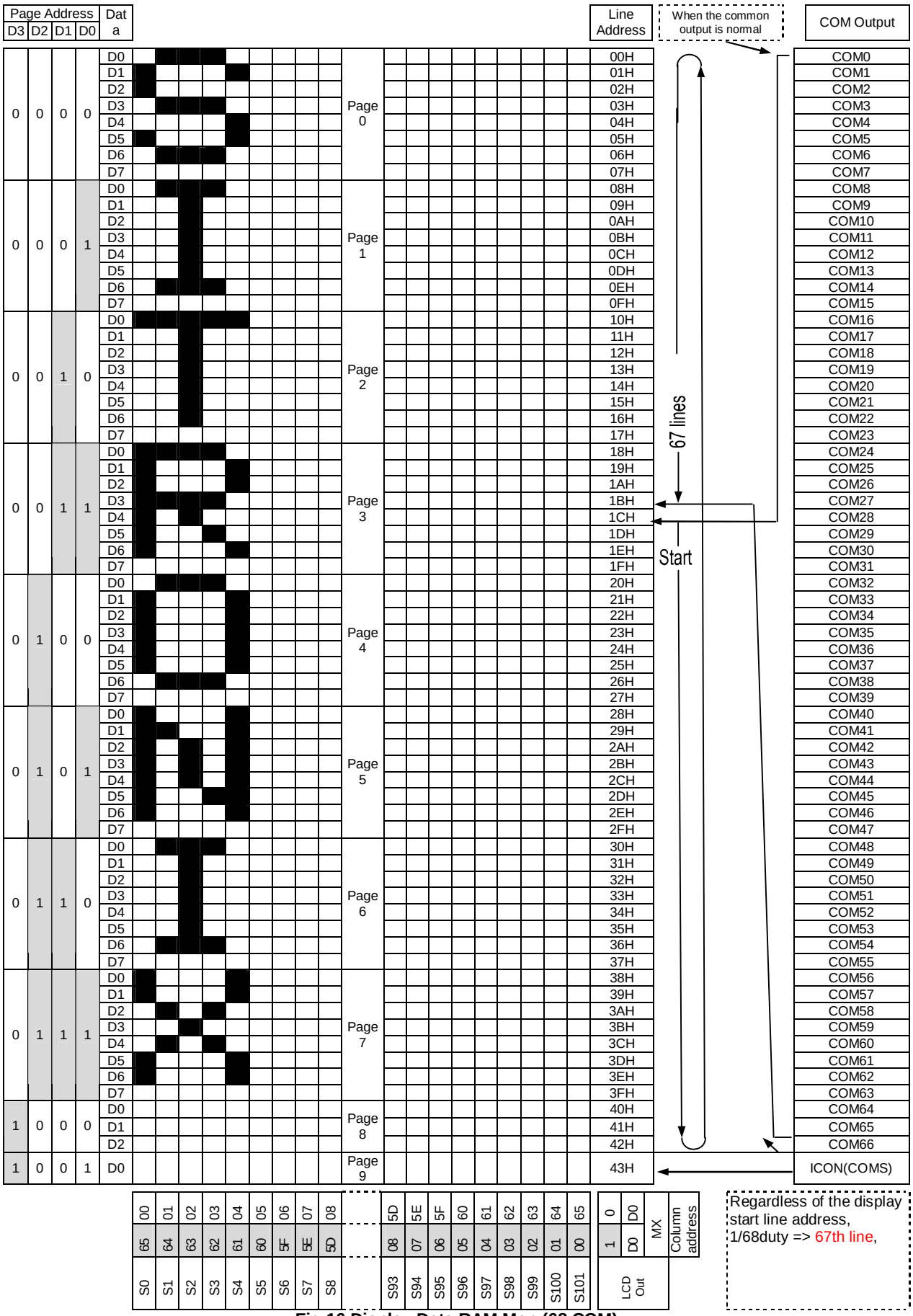


Fig 15 RAM addressing when segment write: horizontal addressing



Partial Display on LCD

The ST7579 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages.

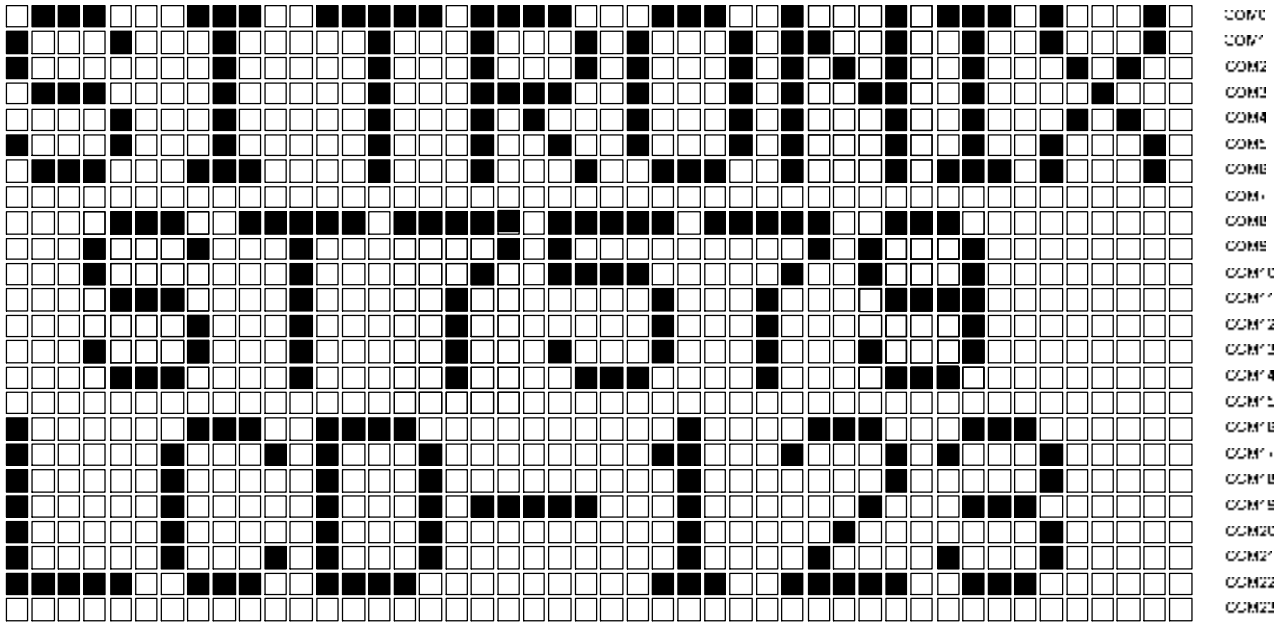


Fig 18 Reference Example for Partial Display

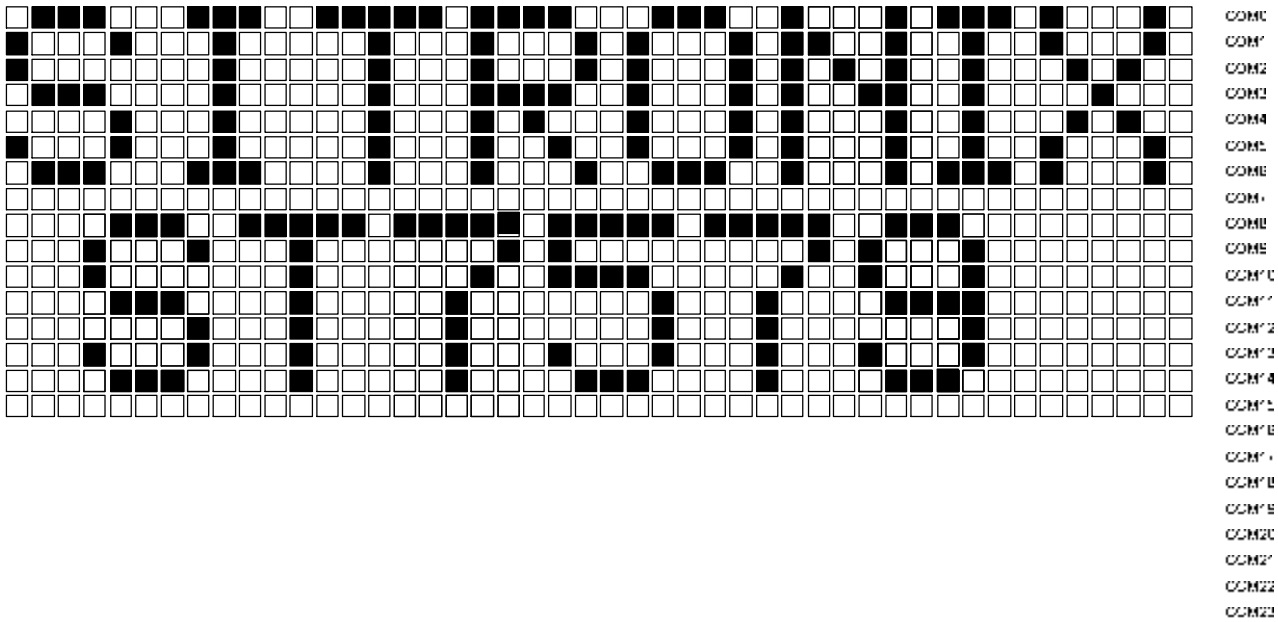


Fig 19 Partial Display (Partial Display Duty=16, initial COM0=0)

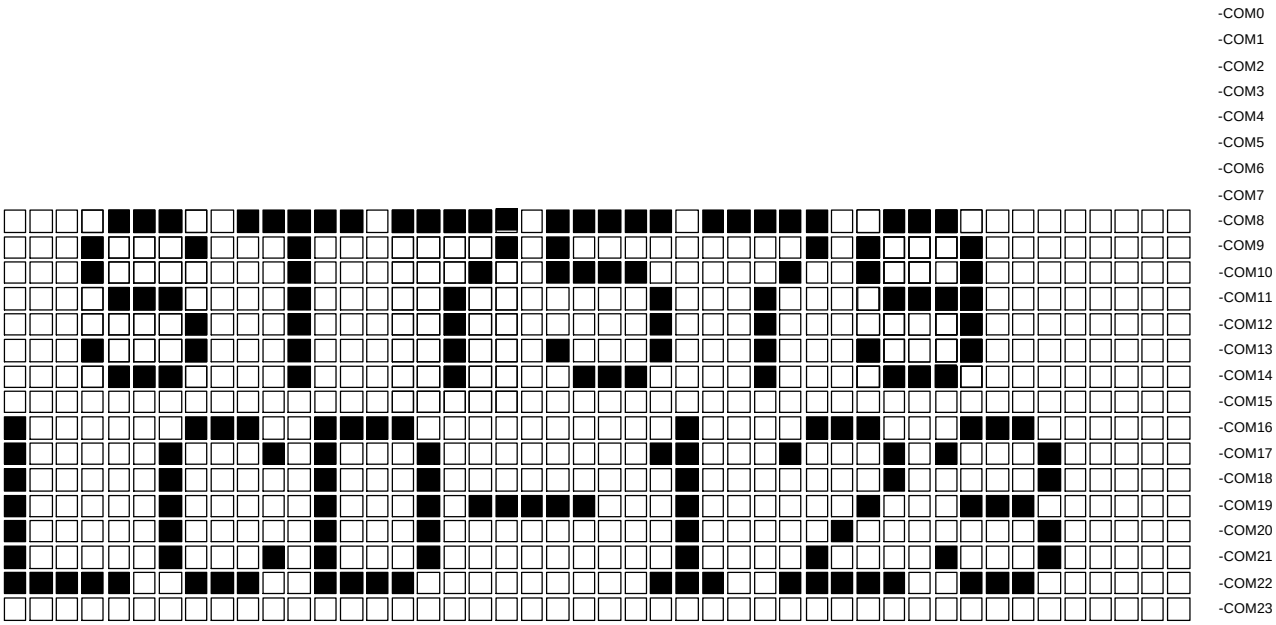


Fig 20 Moving Display (Partial Display Duty=16, Initial COM0=8)

Liquid Crystal Driver Power Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction.

External Power Components

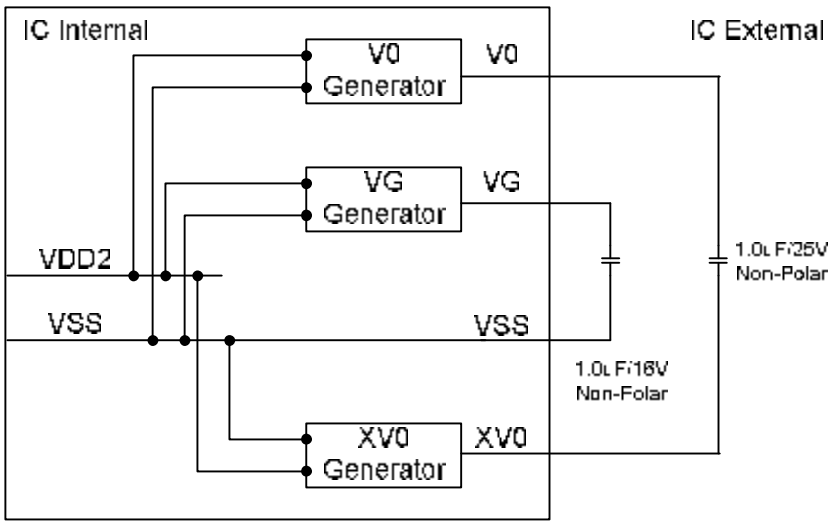


Fig 17 Power Circuit

7. RESET CIRCUIT

Setting RESB to “L” or Reset instruction can initialize internal function.

When RESB becomes “L”, following procedure is occurred.

Page address: 0

Column address: 0

Display control: Display blank

COM Scan Direction MY: 0

SEG Select Direction MX: 0

DO=0

Oscillator: OFF

N-line inversion register: 0 (disable)

Power down mode (PD = 1)

normal instruction set (H[1:0] = 00)

Display blank (E = D = 0)

Address counter X [6:0] = 0, Y [3:0] = 0

Bias system: depend on Hardware (BR) setting

Booster efficiency (BE [1:0] = [1,0])

Booster stage: depend on Hardware (CP) setting

V0 is equal to 0; the HV generator is switched off (VOP [6:0] = 0)

After power-on, RAM data are undefined

While RESB is “L” or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at D0. After D0 becomes ”L”, any instruction can be accepted. RESB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESB is essential before used.

8. INSTRUCTION TABLE

INSTRUCTION	A0	WR (R/W)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
H independent instruction											
NOP	0	0	0	0	0	0	0	0	0	0	No operation
Reserved	0	0	0	0	0	0	0	0	0	1	Do not use
Function set	0	0	0	0	1	MX	MY	PD	H1	H0	Power-down; entry mode; Extended instruction control
Read status byte	0	1	PD	0	0	D	E	MX	MY	DO	Read status byte
Read data	1	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Read data to RAM
Write data	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Write data to RAM

INSTRUCTION	A0	WR (R/W)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
H[1:0]=[0:0]											
Reserved	0	0	0	0	0	0	0	0	1	X	Do not use
Set V_{LCD} range	0	0	0	0	0	0	0	1	0	PRS	V_{LCD} range L/H select
END	0	0	0	0	0	0	0	1	1	0	Release read/modify/write
Read/modify/write	0	0	0	0	0	0	0	1	1	1	RAM address at R:+0 , W:+1
Display control	0	0	0	0	0	0	1	D	0	E	Sets display configuration
Reserved	0	0	0	0	0	1	0	0	X	X	Do not use
Set Y address of RAM	0	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0	Sets Y address of RAM $0 \leqq Y \leqq 9$
Set X address of RAM	0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Sets X address of RAM $0 \leqq X \leqq 101$
H[1:0]=[0:1]											
Reserved	0	0	0	0	0	0	0	0	1	X	Do not use
Display configuration	0	0	0	0	0	0	1	DO	X	X	Top/bottom row mode set data order
Bias system	0	0	0	0	0	1	0	BS_2	BS_1	BS_0	Sets bias system (BSx)
Set Start line S6	0	0	0	0	0	0	0	1	0	S6	Specify the initial display line S6
Set Start line	0	0	0	1	S5	S4	S3	S2	S1	S0	Specify the initial display line to realize vertical scrolling
Set V_{OP}	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	Write V_{OP} to register

INSTRUCTION	A0	WR (R/W)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
H[1:0]=[1:0]											
Reserved	0	0	0	0	0	0	0	0	1	X	Do not use
Partial screen mode	0	0	0	0	0	0	0	1	0	PS	Partial screen enable
Partial screen size	0	0	0	0	0	0	1	0	0	WS	Set partial screen size
Display part	0	0	0	0	0	1	0	DP2	DP1	DP0	Set display part for partial screen mode
H[1:0]=[1:1]											
Test command mode	0	0	0	0	0	0	0	0	0	TEN	Test command enable/disable
RESET	0	0	0	0	0	0	0	0	1	1	Software reset
Display control	0	0	0	0	0	0	1	FR2	FR1	FR0	Frame rate control
N line inversion	0	0	0	1	0	NL4	NL3	NL2	NL1	NL0	Sets N line inversion
Booster Efficiency &Booster Stage(2)	0	0	1	0	0	1	BE1	BE0	PC1	PC0	Booster Efficiency Set
Reserved	0	0	1	X	X	X	X	X	X	X	Do not use

9. INSTRUCTION DESCRIPTION

Function Set

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	MX	MY	PD	H1	H0

Flag	Description
MX	SEG bi-direction selection MX=0:normal direction (SEG0->SEG101) MX=1:reverse direction (SEG101->SEG0)
MY	COM bi-direction selection MY=0:normal direction (COM0->COM66) MY=1:reverse direction (COM66->COM0)
PD	All LCD outputs at V_{SS} (display off), bias generator and V0 generator off, V_{OUT} can be disconnected, oscillator off (external clock possible), RAM contents not cleared; RAM data can be written. PD=0:chip is active PD=1:chip is in power down mode
H0.H1	H0.H1 are used to select different instruction block Follow the instruction table

Read status byte

Indicates the internal status of the ST7579

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	PD	0	0	D	E	MX	MY	DO

Flag			Description
PD			PD=0:chip is active PD=1:chip is in power down mode
D,E	D	E	The bits D and E select the display mode.
	0	0	Display OFF
	0	1	All display segments on
	1	0	Normal mode
	1	1	Inverse video mode
DO			DO=0:LSB is on top DO=1:MSB is on top See page 20

Read data

8-bit data of Display Data from the RAM location specified by the column address and page address can be read to the microprocessor.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	Read data							

Write data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Write data							

H[1:0]=[0:0]

Set V0 range

V0 range L/H select

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	PRS

PRS=0: V0 programming range LOW

PRS=1: V0 programming range HIGH

Display Control

This bits D and E selects the display mode.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	D	0	E

Flag	Description		
D,E	D	E	The bits D and E select the display mode.
	0	0	Display OFF
	1	0	Normal display
	0	1	All display segments on
	1	1	Inverse video mode

Set Y address of RAM

Y [3:0] defines the Y address vector address of the display RAM.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	Y_3	Y_2	Y_1	Y_0

Y_3	Y_2	Y_1	Y_0	CONTENT	ALLOWED X-RANGE	Valid Bit
0	0	0	0	Page0 (display RAM)	0 to 101	D0~ D7
0	0	0	1	Page1 (display RAM)	0 to 101	D0~ D7
0	0	1	0	Page2 (display RAM)	0 to 101	D0~ D7
0	0	1	1	Page3 (display RAM)	0 to 101	D0~ D7
0	1	0	0	Page4 (display RAM)	0 to 101	D0~ D7
0	1	0	1	Page5 (display RAM)	0 to 101	D0~ D7
0	1	1	0	Page6 (display RAM)	0 to 101	D0~ D7
0	1	1	1	Page7 (display RAM)	0 to 101	D0~ D7
1	0	0	0	Page8 (display RAM)	0 to 101	D5~ D7
1	0	0	1	Page9 (display RAM)	0 to 101	D7

Set X address of RAM

The X address points to the columns. The range of X is 0…101.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0

X_6	X_5	X_4	X_3	X_2	X_1	X_0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	1	0	0	0	1	0	98
1	1	0	0	0	1	1	99
1	1	0	0	1	0	0	100
1	1	0	0	1	0	1	101

END

This command releases the read/modify/write mode, and returns the column and row address to the address it was at when the mode was entered.

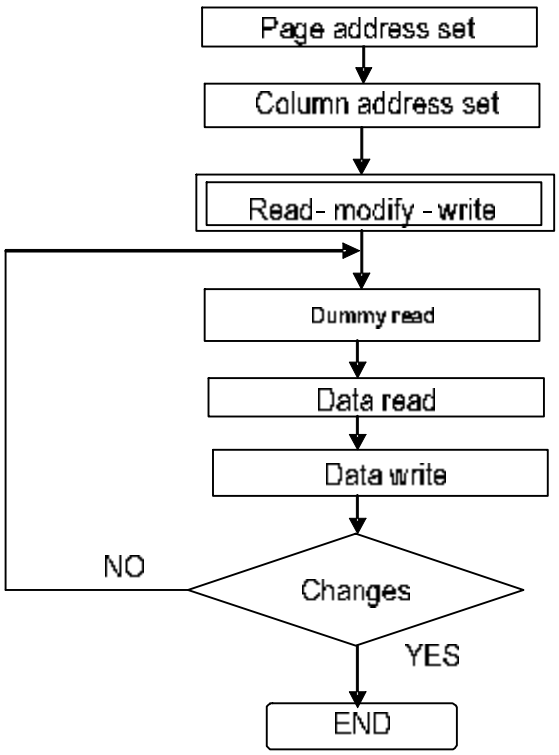
A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	1	0

Read/modify/write

This command is used paired with the “END” instruction. Once this command has been input, the display data read command does not change the column and row address, but only the display data write command increments (+1) the address depend on V register setting. This mode is maintained until the END command is input. When the END command is input, the address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	1	1

* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used.



H[1:0]=[0:1]

Display configuration

Top/bottom row mode set data order

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	DO	X	X

Flag	Description
DO	DO=0:LSB is on top DO=1:MSB is on top See page 20

System Bias

Select LCD bias ratio of the voltage required for driving the LCD.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	BS_2	BS_1	BS_0

BS_2	BS_1	BS_0	Bias
0	0	0	11
0	0	1	10
0	1	0	9
0	1	1	8
1	0	0	7
1	0	1	6
1	1	0	5
1	1	1	4

LCD bias voltage

Symbol	Bias voltage for 1/9 bias
V0	V0
VG	2/9 x V0
VM	1/9 x V0
VSS	VSS

* **VG operating range: 1.4 < VG < (VDD2-0.2)**

Set start line

Sets the line address of display RAM to determine the initial display line instruction. The RAM display data is displayed at the top of row (COM0) of LCD panel. The S_6 must be defined first, and then defined S_5 to S_0.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	S_6

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	S_5	S_4	S_3	S_2	S_1	S_0

S_6	S_5	S_4	S_3	S_2	S_1	S_0	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	63
1	0	0	0	0	0	0	64
1	0	0	0	0	0	1	65
1	0	0	0	0	1	0	66
1	0	0	0	0	1	1	No used
:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	No used

Set V0 value:

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	V_{06}	V_{05}	V_{04}	V_{03}	V_{02}	V_{01}	V_{00}

The operation voltage V0 can be set by software.

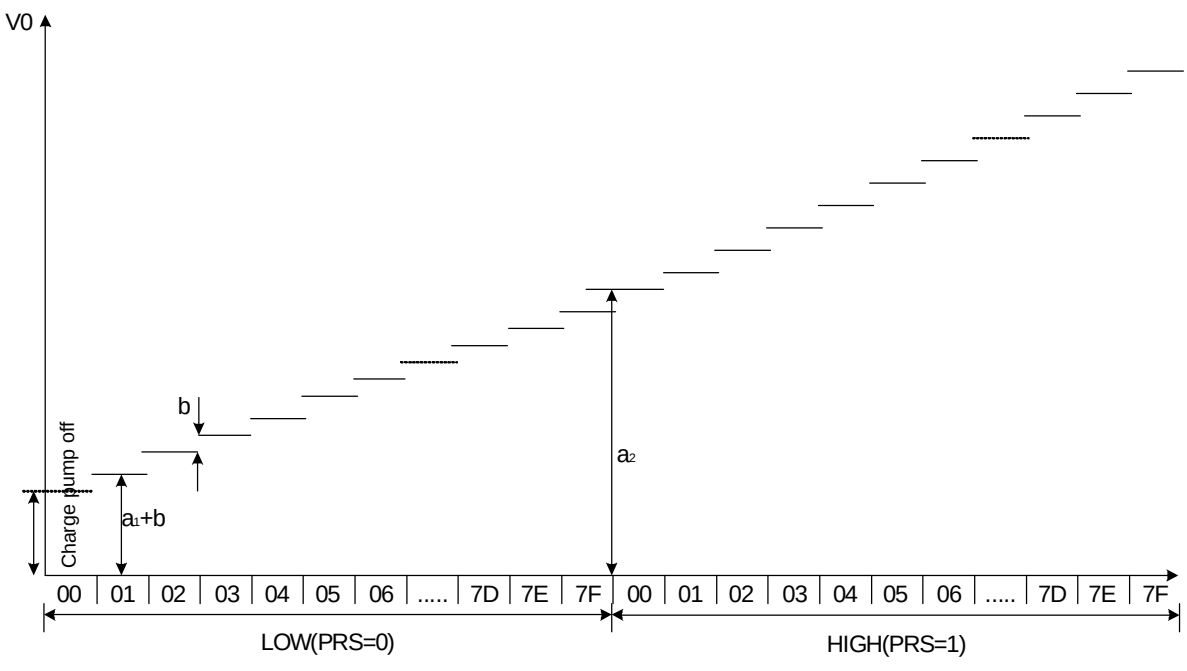
$$V0=V_{OP}=(a + V_{0x} X b) \quad (1)$$

The parameters are explained in table 4.The maximum voltage that can be generated is depending on the V_{DD1} voltage and the display load current. Two overlapping V0 ranges are selectable via the command “Booster control”. For the LOW (PRS=0) range a=a1 and for the HIGH (PRS=1) range a=a2 with steps equal to “b” in both ranges. Note that the charge pump is turned off if V0 [6;0] and the bit PRS are all set to zero.

* **The Vop must be operated in the range of 4V to 9.5V for the normal or partial display mode application, so that customer have some range(<4V; >9.5V) to adjust contrast by themselves.**

Table 4 Typical values for parameter for the HV-Generator programming

SYMBOL	VALUE	UNIT
a1	2.94(PRS=0)	V
a2	6.75(PRS=1)	V
b	0.03	V



V0 [6:0](programmed) {00 hex… 7F hex}

Fig 21 Vop programming of ST7579

H[1:0]=[1:0]

Partial screen mode

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	PS

Flag	Description
PS	Full display mode or partial screen mode selection PS=0:Full display mode with MUX 1:68 PS=1:Partial screen mode with MUX 1:17 or MUX 1:33

When enter Partial screen mode, COMS also works. The DDRAM position of COMS is at page9(D0)

Partial screen size

This instruction can select partial screen size

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	0	0	WS

Flag	Description
WS	WS=0:partail screen mode with MUX 1:17(16 Common + COMS) WS=1:Partial screen mode with MUX 1:33(32 Common + COMS)

Display part

This instruction can select partial screen modes

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	DP_2	DP_1	DP_0

Flag	Status			Description	
				Display common	DDRAM position
DP_2 DP_1 DP_0	0	0	0	Start from common 0	Start from page 0
	0	0	1	Start from common 8	Start from page 1
	0	1	0	Start from common 16	Start from page 2
	0	1	1	Start from common 24	Start from page 3
	1	0	0	Start from common 32	Start from page 4
	1	0	1	Start from common 40	Start from page 5
	1	1	0	Start from common 48	Start from page 6
	1	1	1	Start from common 56	Start from page 7

The range of display common and DDRAM depends on the “WS” register . For example , if WS=1 and DP[2:0]=001 ,then display common is common 8 to common 39 and DDRAM position is page 1 to page4 and COMS is at page 9 . Moreover the bottom of DP[2:0] is common 66, when the range is over common66,there will be no more common output to display

H[1:0]=[1:1]

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status .This instruction cannot initialize the LCD power supply, which is initialized by the RESB pin.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	1	1

Frame frequency

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	FR2	FR1	FR0

This command is used to set the frame frequency.

FR_2	FR_1	FR_0	FR frequency
0	0	0	55 Hz ±15%
0	0	1	65 Hz ±15%
0	1	0	68 Hz ±15%
0	1	1	70 Hz ±15%
1	0	0	73 Hz ±10%
1	0	1	76 Hz ±15%
1	1	0	80 Hz ±15%
1	1	1	137 Hz ±15%

Release N-line inversion

ST7579 returns to the frame inversion condition from the N-line inversion condition.

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	NL4	NL3	NL2	NL1	NL0

Set N-line inversion

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (M)

Note: The N-line inversion mode will be disabled when partial display mode enter. After the partial display mode end, the N-line inversion mode will return as it was.

NL4	NL3	NL2	NL1	NL0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
0	0	0	1	1	5-line inversion
:	:	:	:	:	:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion

Booster Efficiency & Booster stages

A0	WR(R/W)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	BE1	BE0	PC1	PC0

Booster Efficiency

The ST7579 incorporates software configurable Booster Efficiency. It could be used with Voltage multiplier to get the suitable V_{OUT} and Power consumption .Using lower Booster Efficiency level will get the lower V_{OUT} & lower Power consumption. *Default setting is Level 2.(suggest level)*

Flag	Description		
BE[1:0]	BE_1	BE_0	
	0	0	Booster Efficiency Level 4
	0	1	Booster Efficiency Level 3
	1	0	Booster Efficiency Level 2(default)
	1	1	Booster Efficiency Level 1

Booster stages

The ST7579 incorporates a software configurable voltage multiplier. After reset (RESB), the default voltage multiplier is related to “CP” pin(see page 11). Other voltage multiplier factors are set via this command .

Flag	Description		
PC_1, PC0	PC_1	PC_0	
	0	0	2*voltage multiplier(Booster X2)
	0	1	3*voltage multiplier(Booster X3)
	1	0	4*voltage multiplier(Booster X4)
	1	1	5*voltage multiplier(Booster X5)

10. COMMAND DESCRIPTION

Referential Instruction Setup Flow: Initializing with the built-in Power Supply Circuits

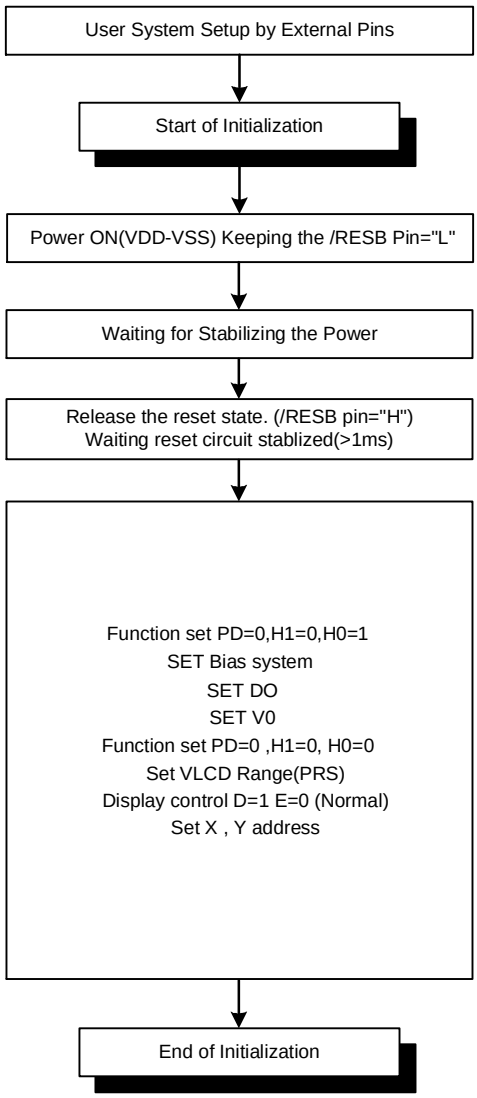


Fig 22 Initializing with the Built-in Power Supply Circuits

11. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	V_{DD1}	-0.3 ~ 3.6	V
Power supply voltage	V_{DD2}	-0.3 ~ 3.6	V
LCD Power supply voltage	V0	-0.3~10.5	V
LCD Power supply voltage	XV0-VG	-10.5~0.3	V
LCD Power driving voltage	VG, VM	-0.3 ~ VDD2	V
Operating temperature	TOPR	–40 to +85	°C
Storage temperature	TSTR	–65 to +150	°C

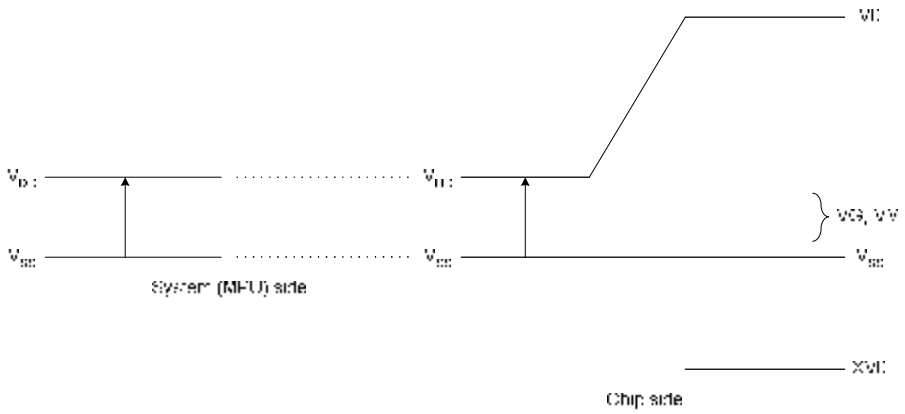


Fig 23

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. Insure that the voltage levels of VG, VM, VSS, and XV0 are always such that

   V0 ≧VDD2≧ VG ≧ VM ≧ VSS ≧ XV0

12. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see “Handling MOS devices”).

13. DC CHARACTERISTICS

V_{DD1} = 1.8V to 3.3V; V_{SS} = 0V; T_{amb} = -40℃ to +85℃; unless otherwise specified.

Item	Symbol	Condition	Rating			Units	Applicable Pin
			Min.	Typ.	Max.		
Operating Voltage (1)	V_{DD1}		1.8	—	3.3	V	V_{DD1}
Operating Voltage (2)	V_{DD2}	(Relative to VSS)	2.4	—	3.3	V	V_{DD2}
High-level Input Voltage	V_{IHC}		0.7 x V_{DD1}	—	V_{DD1}	V	
Low-level Input Voltage	V_{ILC}		V_{SS}	—	0.3 x V_{DD1}	V	
High-level Output Voltage	V_{OHC}	I_{OUT}=-500uA; V_{DD1}=1.7V	0.7 x V_{DD1}	—	V_{DD1}	V	
Low-level Output Voltage	V_{OLC}	I_{OUT}=500uA; V_{DD1}=1.7V	V_{SS}	—	0.3 x V_{DD1}	V	
Input leakage current	I_{LI}		–1.0	—	1.0	μA	
Output leakage current	I_{LO}		–3.0	—	3.0	μA	
Liquid Crystal Driver ON Resistance	R_{ON}	Ta = 25°C, Vop= 9.0 V, △V=0.9V	—	0.7	—	KΩ	COMn SEGn
		Ta = 25°C, VG = 2.0 V, △V=0.2V	—	0.7	—		
Frame frequency	FR	FR default (1,0,0)	65.7	73	80.3	Hz	

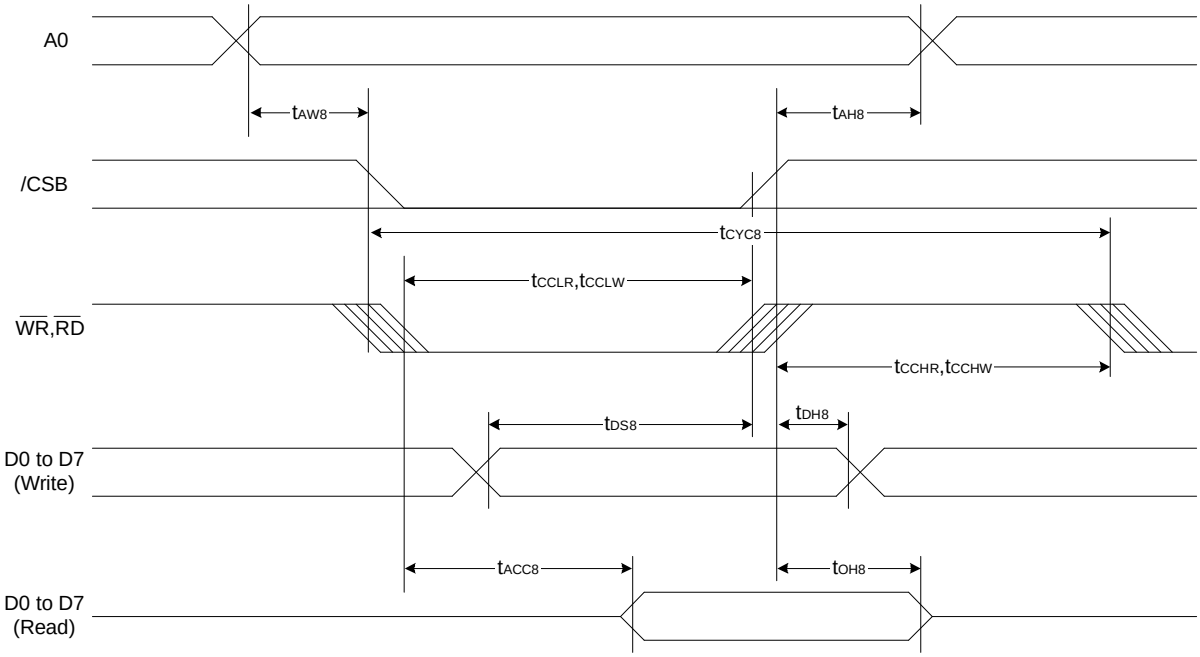
Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Internal Power	Positive power for common driver	V0	(Relative to VSS)	3	—	13	V	V0
	Negative power for common driver	XV0	(Relative to VSS)	3	—	13	V	XV0

Dynamic consumption current: During Display, with Internal Power Supply ON, current consumed by whole IC (bare die).

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern SNOW (static)	I_{SS}	V_{DD} = 3.0 V, Booster X5 V0 – V_{SS} = 9.0 V Bias=1/9	—	110	150	μA	
Power Down	I_{SS}	Ta = 25°C	—	0.7	3	μA	
Display Pattern SNOW (dynamic)	I_{SS}	V_{DD} = 3.0 V, Booster X5 V0 – V_{SS} = 9.0 V Bias=1/9 Data write frequency: 1M Hz	—			μA	

14. TIMING CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)



(VDD = 3.3V , Ta =-40~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		10	—	ns
Address setup time		tAW8		80	—	
System cycle time	WR	tCYC8		350	—	
Enable L pulse width (WRITE)	WR	tCCLW		70	—	
Enable H pulse width (WRITE)		tCCHW		50	—	
Enable L pulse width (READ)	RD	tCCLR		120	—	
Enable H pulse width (READ)		tCCHR		50		
WRITE Data setup time	D0 to D7	tDS8		60	—	
WRITE Data hold time		tDH8		10	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	10	50	

(VDD = 2.8V , Ta =-40~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		15	—	ns
Address setup time		tAW8		120	—	
System cycle time	WR	tCYC8		450	—	
Enable L pulse width (WRITE)	WR	tCCLW		120	—	
Enable H pulse width (WRITE)		tCCHW		100	—	
Enable L pulse width (READ)	RD	tCCLR		120	—	
Enable H pulse width (READ)		tCCHR		100	—	
WRITE Data setup time	D0 to D7	tDS8		90	—	
WRITE Address hold time		tDH8		15	—	
READ access time		tACC8	CL = 100 pF	—	140	
READ Output disable time		tOH8	CL = 100 pF	10	100	

(VDD = 1.8V , Ta =-40~85°C)

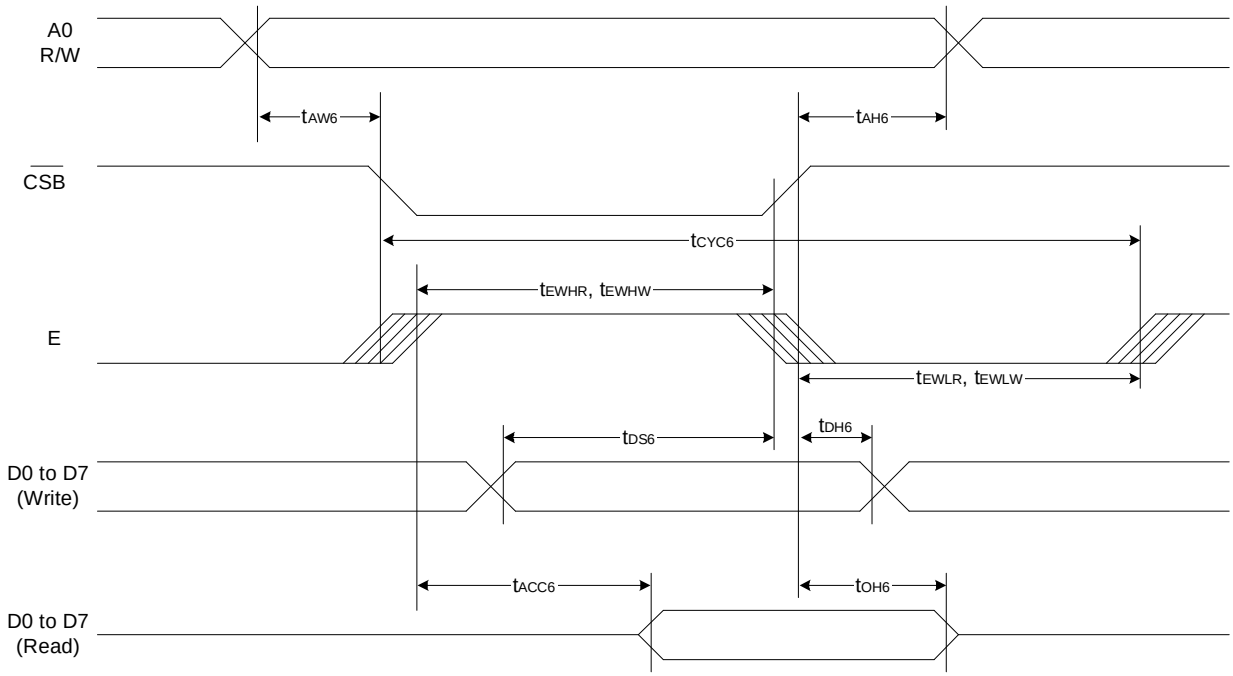
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		30	—	ns
Address setup time		tAW8		150	—	
System cycle time	WR	tCYC8		550	—	
Enable L pulse width (WRITE)	WR	tCCLW		170	—	
Enable H pulse width (WRITE)		tCCHW		150	—	
Enable L pulse width (READ)	RD	tCCLR		170	—	
Enable H pulse width (READ)		tCCHR		150		
WRITE Data setup time	D0 to D7	tDS8		120	—	
WRITE Address hold time		tDH8		30	—	
READ access time		tACC8	CL = 100 pF	—	240	
READ Output disable time		tOH8	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) $\leqq$ (tCYC8 – tCCLW – tCCHW) for (tr + tf) $\leqq$ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tCCLW and tCCLR are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)



(VDD = 3.3V , Ta =-40~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		10	—	ns
Address setup time		tAW6		80	—	
System cycle time		tCYC6		240	—	
Enable L pulse width (WRITE)	WR	tEWLW		70	—	
Enable H pulse width (WRITE)		tEWHW		50	—	
Enable L pulse width (READ)	RD	tEWLR		70	—	
Enable H pulse width (READ)		tEWHR		130		
WRITE Data setup time	D0 to D7	tDS6		60	—	
WRITE Data hold time		tDH6		10	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	10	50	

(VDD = 2.8V , Ta =-40~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		15	—	ns
Address setup time		tAW6		100	—	
System cycle time		tCYC6		340	—	
Enable L pulse width (WRITE)	WR	tEWLW		120	—	
Enable H pulse width (WRITE)		tEWHW		100	—	
Enable L pulse width (READ)	RD	tEWLR		120	—	
Enable H pulse width (READ)		tEWHR		100	—	
WRITE Data setup time	D0 to D7	tDS6		120	—	
WRITE Address hold time		tDH6		15	—	
READ access time		tACC6	CL = 100 pF	—	140	
READ Output disable time		tOH6	CL = 100 pF	10	100	

(VDD = 1.8V , Ta =-40~85°C)

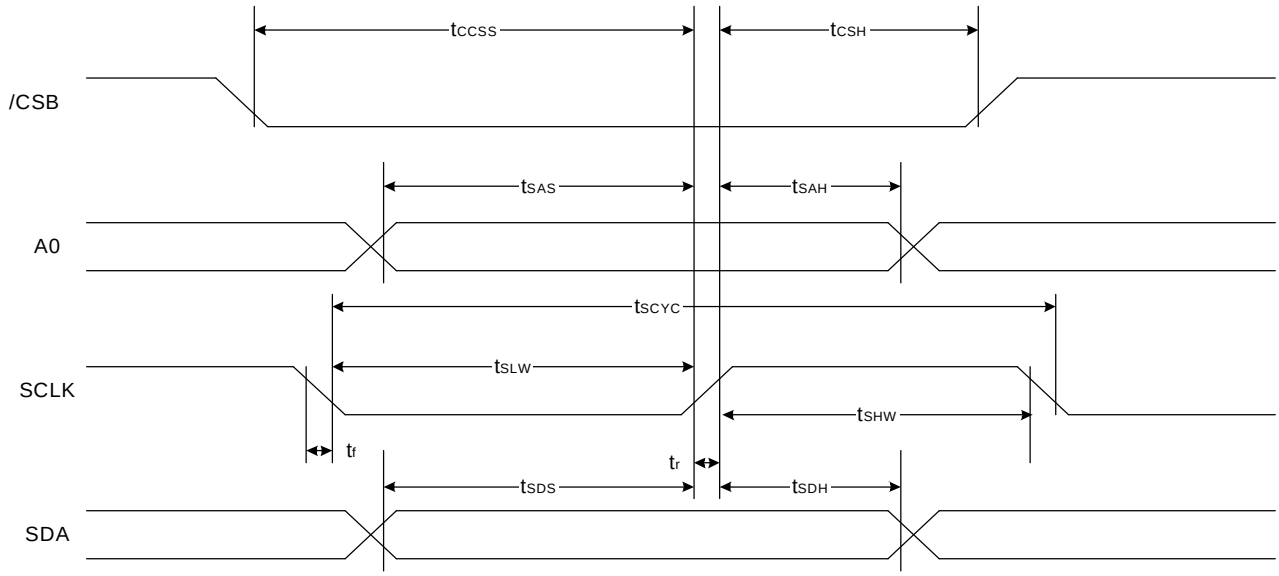
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		30	—	ns
Address setup time		tAW6		150	—	
System cycle time		tCYC6		440	—	
Enable L pulse width (WRITE)	WR	tEWLW		170	—	
Enable H pulse width (WRITE)		tEWHW		150	—	
Enable L pulse width (READ)	RD	tEWLR		170	—	
Enable H pulse width (READ)		tEWHR		150	—	
WRITE Data setup time	D0 to D7	tDS6		180	—	
WRITE Data hold time		tDH6		30	—	
READ access time		tACC6	CL = 100 pF	—	240	
READ Output disable time		tOH6	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) $\leqq$ (tCYC6 – tEWLW – tEWHW) for (tr + tf) $\leqq$ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CSB being “L” and E.

SERIAL INTERFACE(4-Line Interface)



(VDD = 3.3V , Ta =-40~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		120	—	ns
SCL “H” pulse width		tSHW		60	—	
SCL “L” pulse width		tSLW		60	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		90	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	CSB	tCSS		20	—	
CS-SCL time		tCSH		120	—	

(VDD = 2.8V , Ta =-40~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		200	—	ns
SCL “H” pulse width		tSHW		100	—	
SCL “L” pulse width		tSLW		100	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		120	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	CSB	tCSS		30	—	
CS-SCL time		tCSH		150	—	

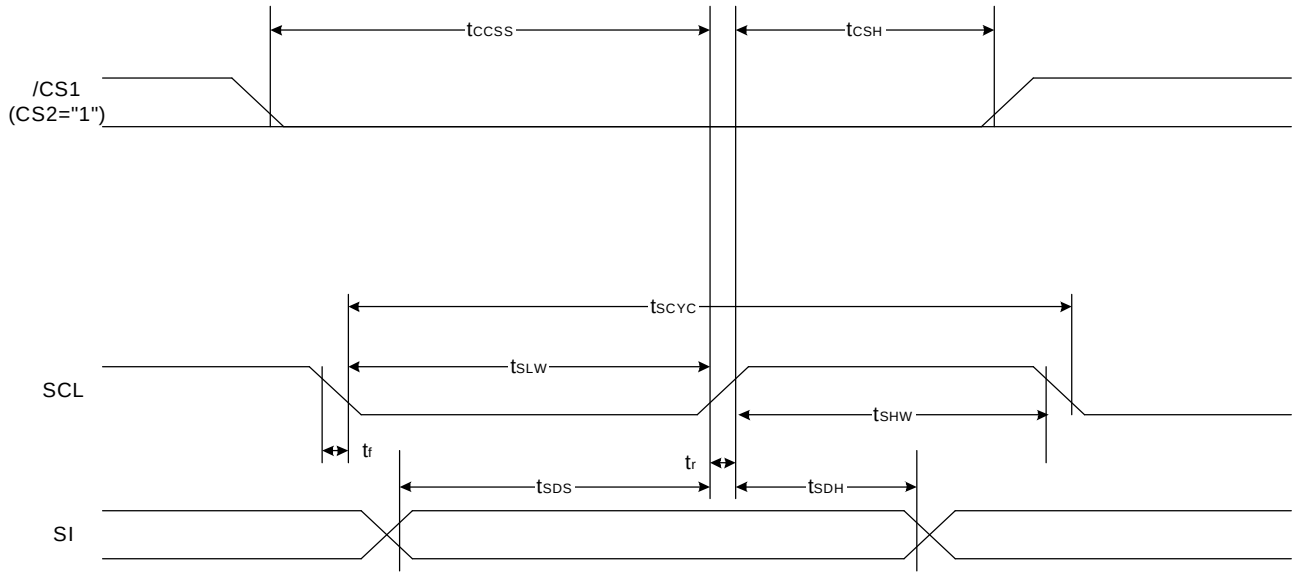
(V_{DD}=1.8V,Ta=-40~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		280	—	ns
SCL “H” pulse width		tSHW		140	—	
SCL “L” pulse width		tSLW		140	—	
Address setup time	A0	tSAS		50	—	
Address hold time		tSAH		150	—	
Data setup time	SI	tSDS		50	—	
Data hold time		tSDH		50	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		180	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD1 as the standard.

SERIAL INTERFACE (3-Line Interface)



(V_{DD}=3.3V,Ta=-40~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		120	—	ns
SCL “H” pulse width		tSHW		60	—	
SCL “L” pulse width		tSLW		60	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	CSB	tCSS		20	—	
CS-SCL time		tCSH		130	—	

(V_{DD}=2.8V,Ta=-40~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		180	—	ns
SCL “H” pulse width		tSHW		90	—	
SCL “L” pulse width		tSLW		90	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	CSB	tCSS		30	—	
CS-SCL time		tCSH		160	—	

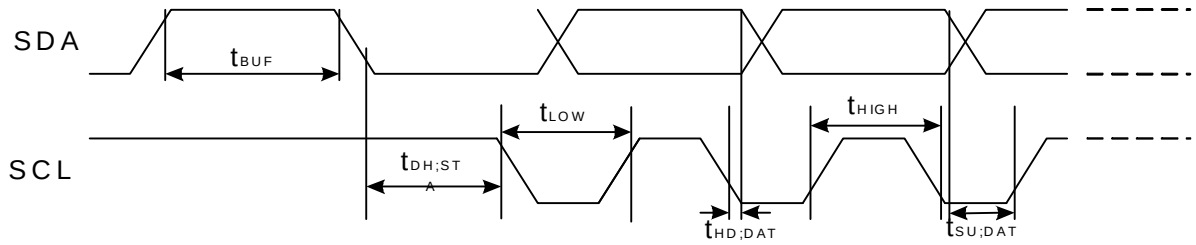
(V_{DD}=1.8V,Ta=-40~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		240	—	ns
SCL “H” pulse width		tSHW		120	—	
SCL “L” pulse width		tSLW		120	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		50	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		190	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD1 as the standard.

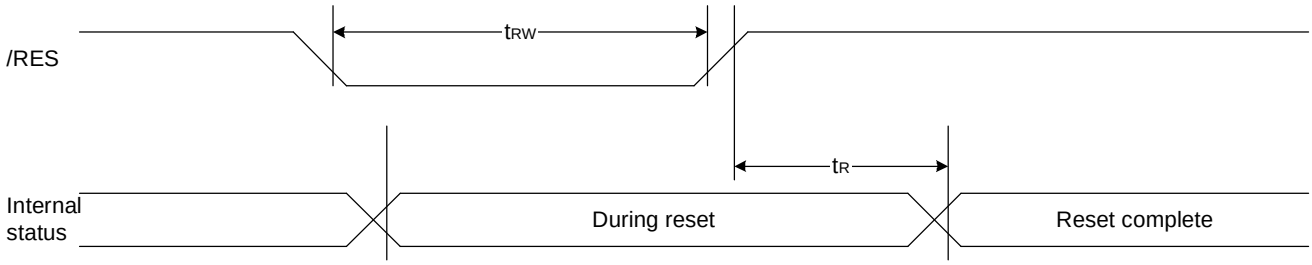
SERIAL INTERFACE(I²C Interface)



(V_{DD}=3.3V,Ta=-40~85℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	FSCLK		-	4	MHZ
SCL clock low period	SCL	TLOW		150	-	ns
SCL clock high period	SCL	THIGH		100	-	ns
Data set-up time	SI	TSU;Data		100	-	ns
Data hold time	SI	THD;Data		0	0.9	us
SCL,SDA rise time	SCL	TR		20+0.1Cb	300	ns
SCL,SDA fall time	SCL	TF		20+0.1Cb	300	ns
Capacitive load represented by each bus line		Cb		-	400	pF
Setup time for a repeated START condition	SI	TSU;SUA		400	-	ns
Start condition hold time	SI	THD;STA		400	-	ns
Setup time for STOP condition		TSU;STO		0.6	-	us
Tolerable spike width on bus		TSW		-	50	ns
BUS free time between a STOP and START condition	SCL	TBUF		600		ns

15. RESET TIMING



(VDD = 3.3V , Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1.5	us
Reset “L” pulse width	RESB	tRW		1.5	—	—	us

(VDD = 2.8V , Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	2.0	us
Reset “L” pulse width	RESB	tRW		2.0	—	—	us

(VDD = 1.8V , Ta = –40 to 85°C)

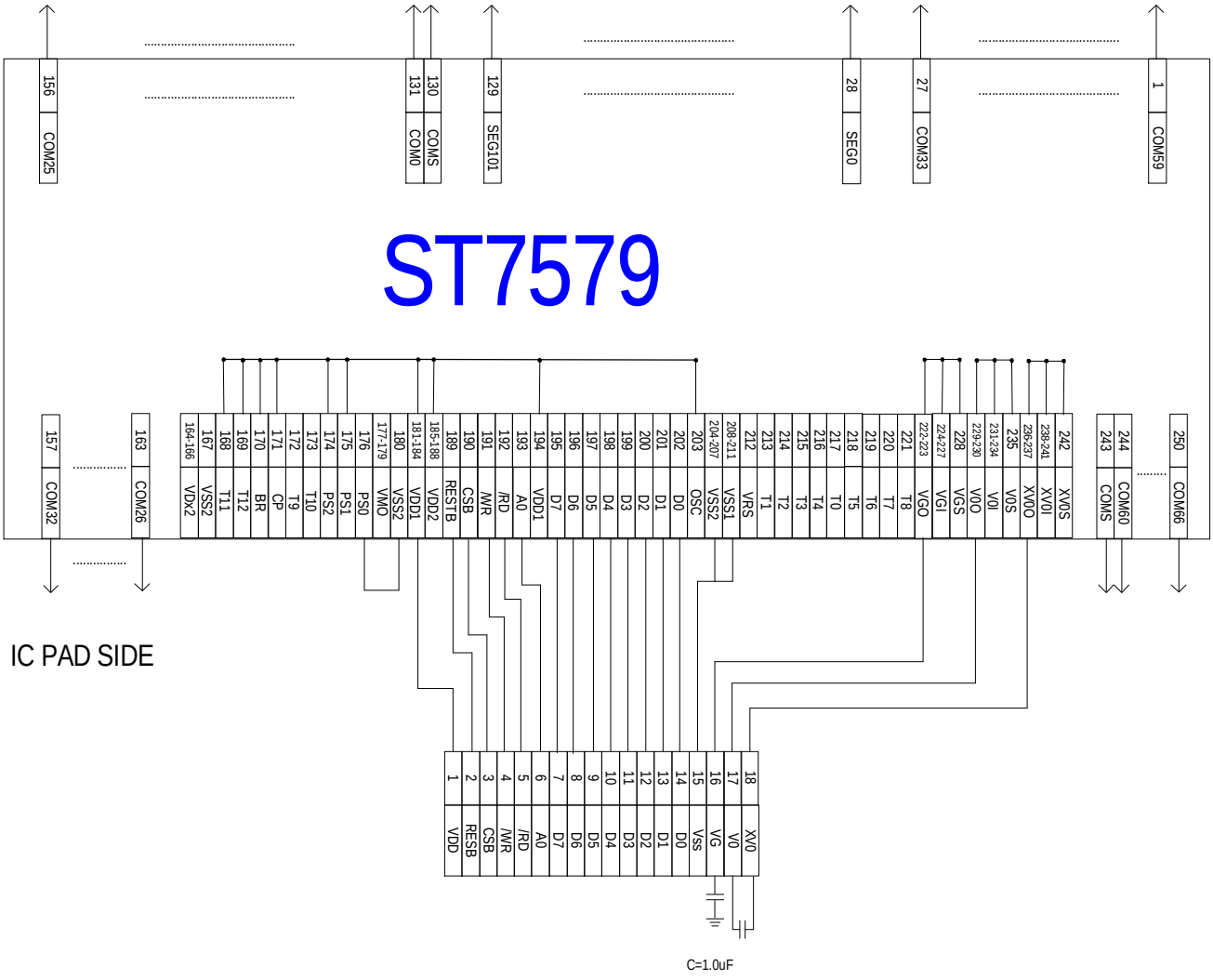
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	3.0	us
Reset “L” pulse width	RESB	tRW		3.0	—	—	us

APPLICATION NOTE

ST7579

Resolution : 68(67COM+ICON)*102(SEG)
Interface : 6800 series
Internal analog circuit
Internal OSC
Booster : X5
Bias ratio default : 1/9
(bias ratio can be changed by instruction)
C=1.0 uF

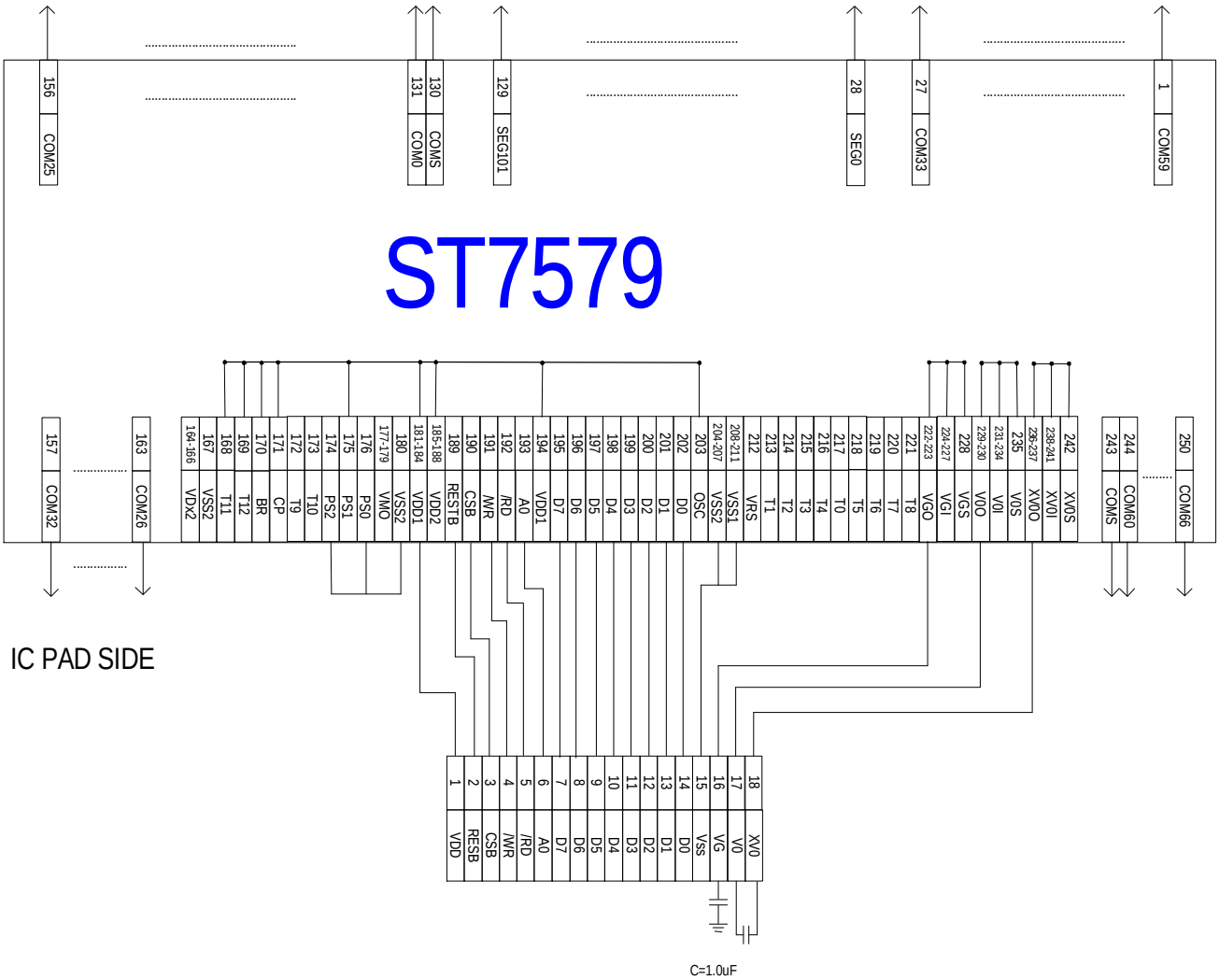
OSC : Vdd1
T11:Vdd1
T12:Vdd1
PS0 : Vss
PS1 : Vdd1
PS2 : Vdd1
CP : Vdd1
BR : Vdd1



ST7579

Resolution : 68(67COM+ICON)*102(SEG)
Interface: 8080
Internal analog circuit
Internal OSC
Booster : X5
Bias ratio default : 1/9
(bias ratio can be changed by instruction)
C=1.0 uF

OSC : Vdd1
T11:Vdd1
T12:Vdd1
PS0 : Vss
PS1 : Vdd1
PS2:Vss
CP : Vdd1
BR : Vdd1

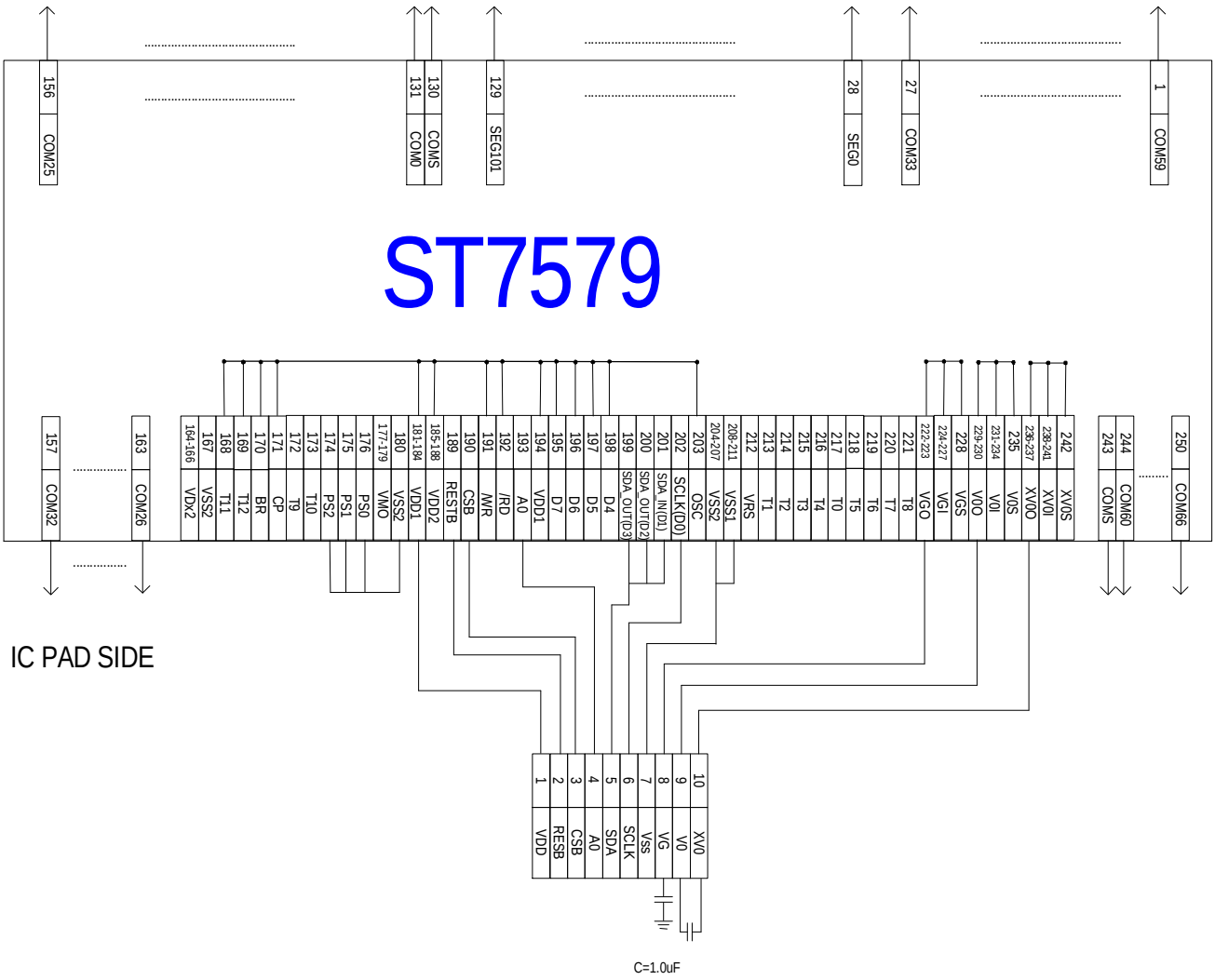


IC PAD SIDE

ST7579

Resolution : 68(67COM+ICON)*102(SEG)
Interface:4-line
Internal analog circuit
Internal OSC
Booster : X5
Bias ratio default : 1/9
(bias ratio can be changed by instruction)
C=1.0 uF

OSC : Vdd1
T11:Vdd1
T121:Vdd1
PS0 : Vss
PS1:Vss
PS2:Vss
CP : Vdd1
BR : Vdd1

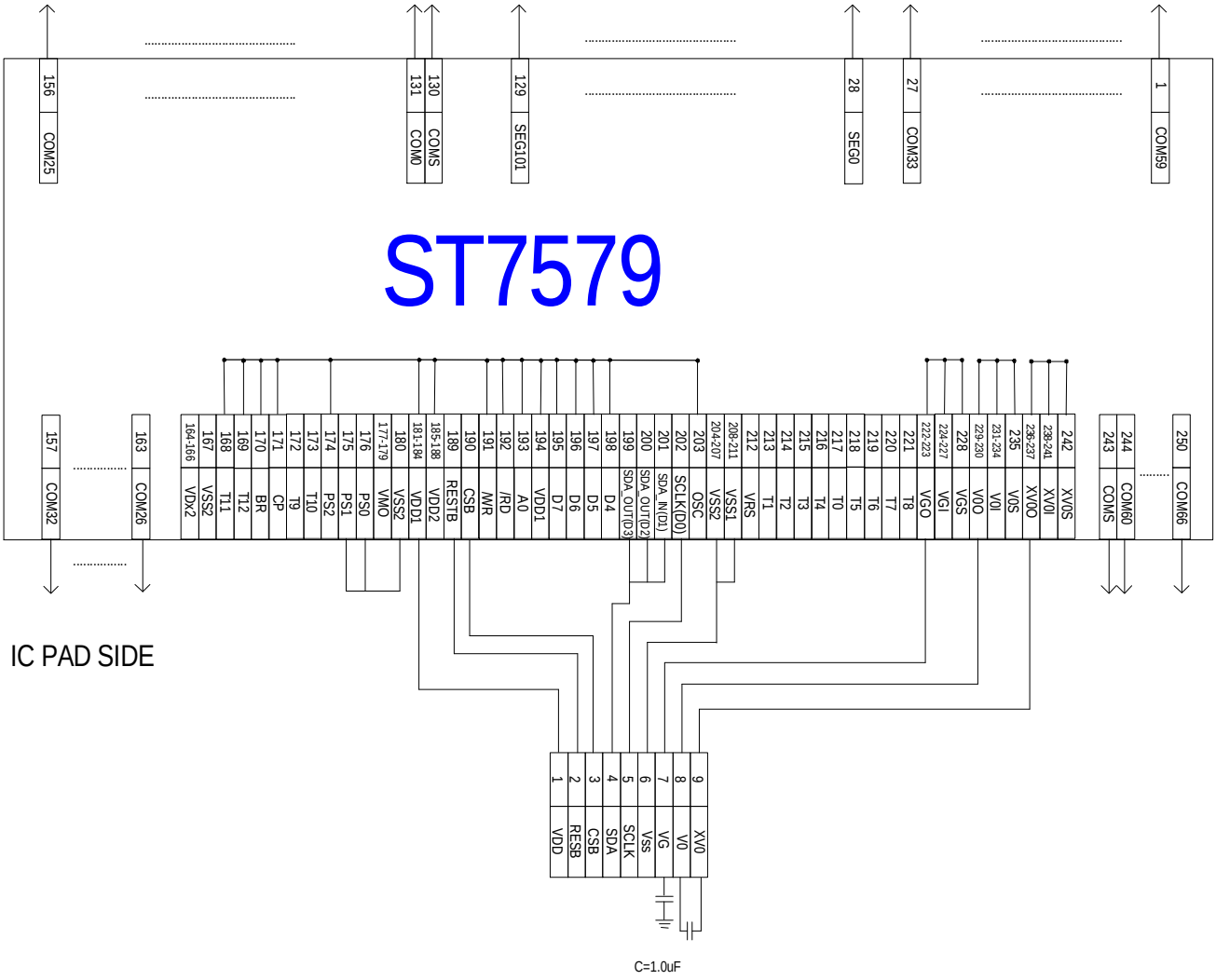


IC PAD SIDE

ST7579

Resolution : 68(67COM+ICON)*102(SEG)
Interface:3-line
Internal analog circuit
Internal OSC
Booster : X5
Bias ratio default : 1/9
(bias ratio can be changed by instruction)
C=1.0 uF

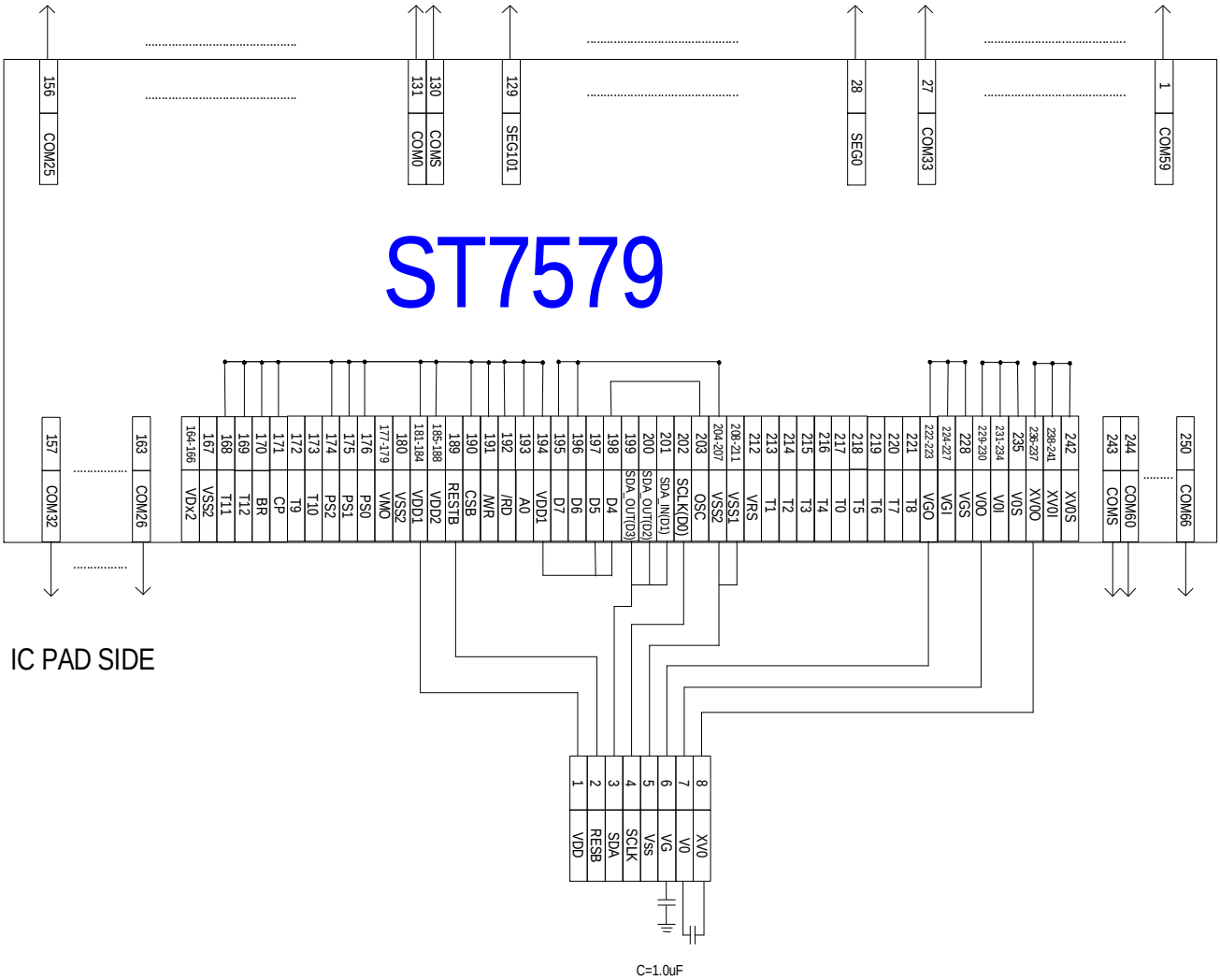
OSC : Vdd1
T11:Vdd1
T12:Vdd1
PS0 : Vss
PS1:Vss
PS2:Vdd1
CP : Vdd1
BR : Vdd1



ST7579

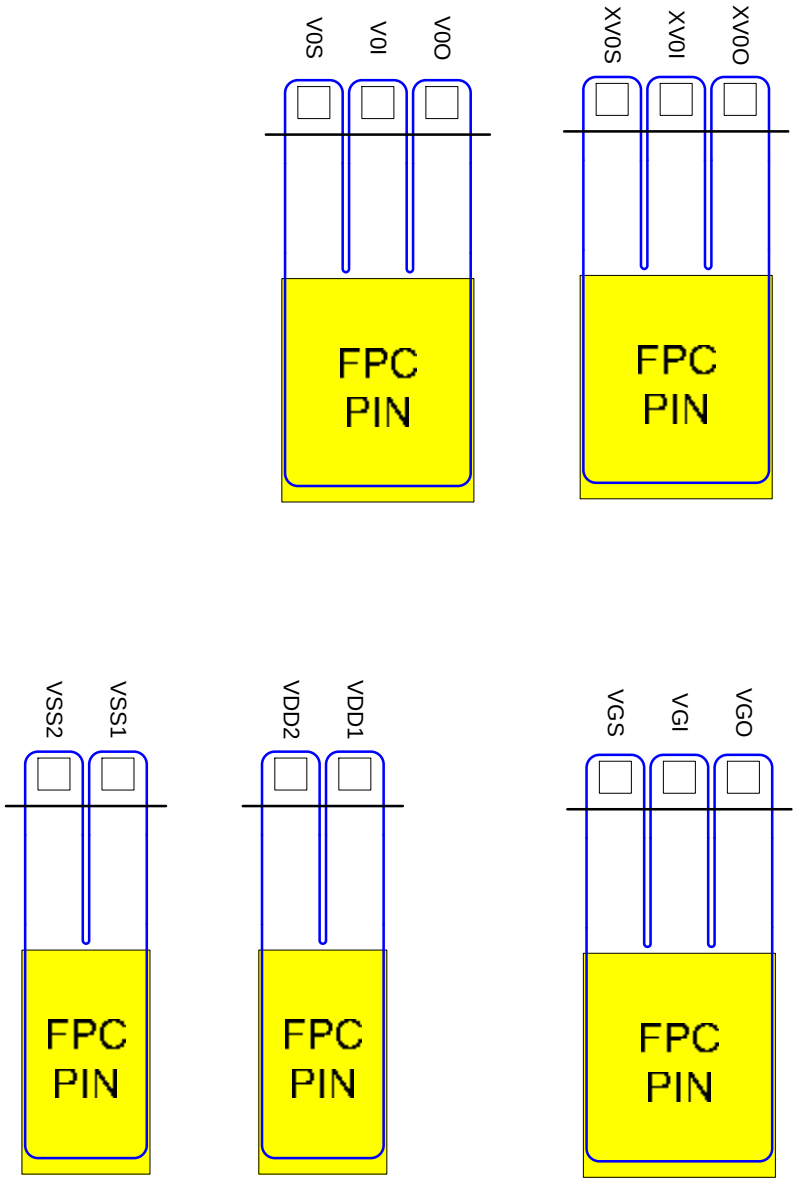
Resolution : 68(67COM+ICON)*102(SEG)
Interface:I2C
Internal analog circuit
Internal OSC
Booster : X5
Bias ratio default : 1/9
(bias ratio can be changed by instruction)
C=1.0 uF
SA[1:0]=(0,0)

OSC : Vdd1
T11:Vdd1
T12:Vdd1
PS0:Vdd1
PS1:Vdd1
PS2:Vdd1
CP : Vdd1
BR : Vdd1

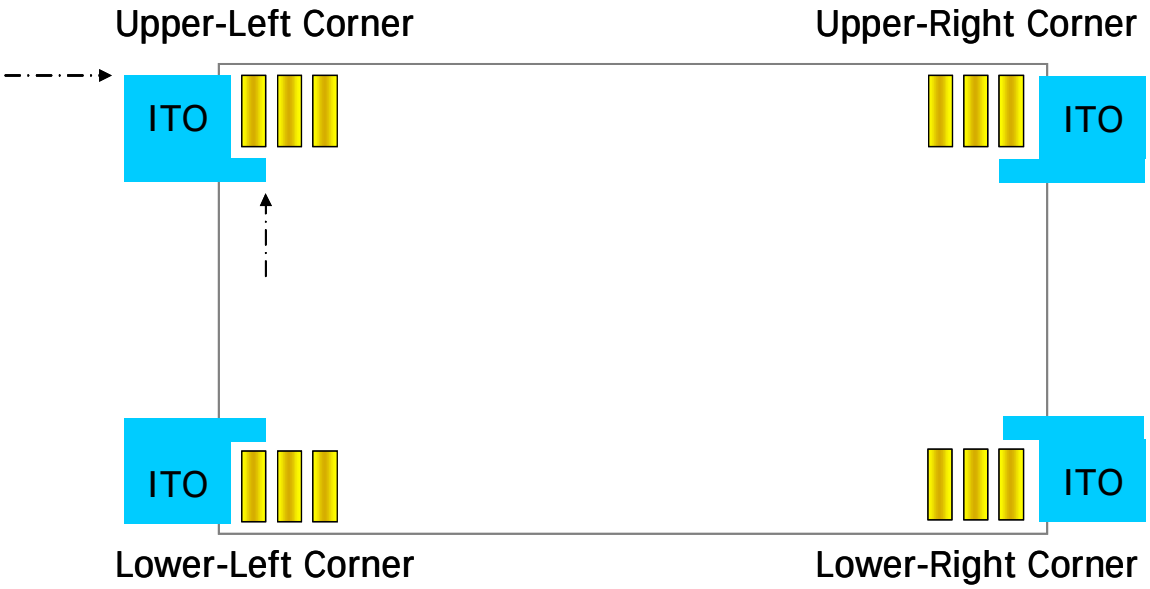


IC PAD SIDE

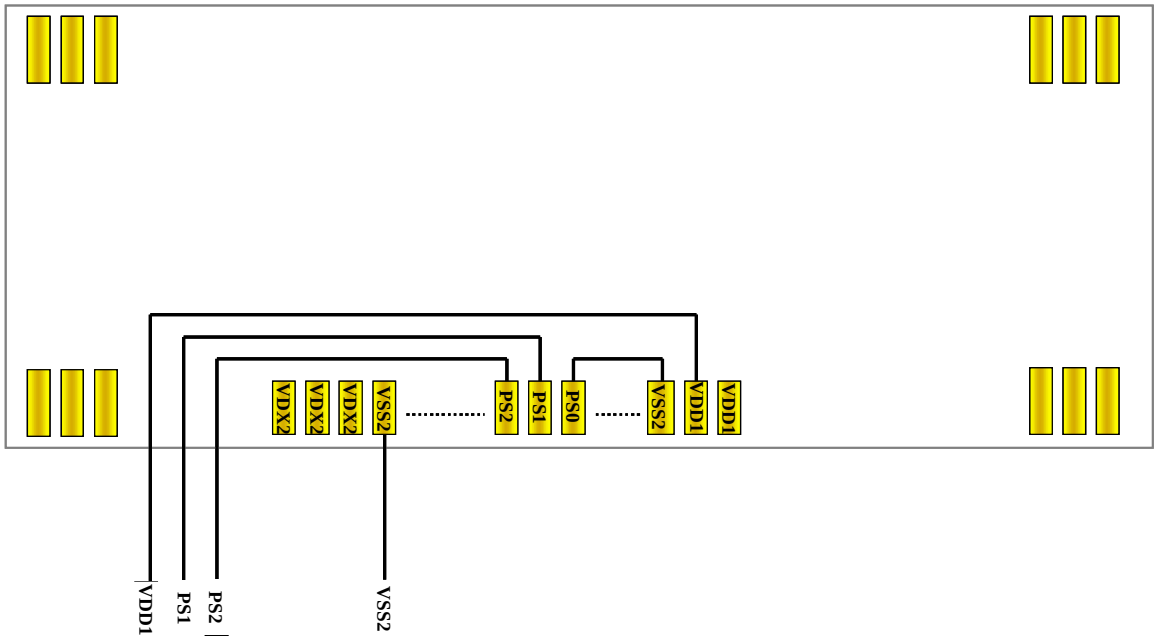
Reference to ITO Layout



For manual COG machine (reference ITO mark)



For some ST7549 replaced case (matching the PS1, PS2 pin out)



ST7579 Serial Specification Revision History		
Version	**Date**	**Description**
0.6	2006/05/04	All layer change
0.6b	2006/05/05	Fig arrange
0.6c	2006/05/10	Add reference to ITO layout
0.6d	2006/05/15	P18 => 6800 interface PS0='L' Test pin size reduce
0.6e	2006/05/24	P11
0.6f	2006/06/19	P6, Modify TMX,TMY=>T9,T10
0.7a	2006/0807	P1 : Voltage converter P16: VSS1, VSS2 P17: Mode0, Mode1=>T11,T12 P35 : limit Vop application range
0.7b	2006/08/14	P1 : Display supply voltage range P39-P50: timing, limited voltage, DC characteristic modify
0.9	2006/11/30	Add application note