Name: Dinesh Kotti
Email: dkotti@gmail.com
LinkedIn: linkedin.com/in/dinesh-kotti-2758ba2 (209 connections)
Facebook: facebook.com/dkotti
Twitter: twitter.com/dkotti
GitHub: github.com/dkotti

Summary:
Experienced Hardware Design Engineer with expertise in mixed signal design, NCSim, SOC, functional verification, RTL design, ASIC, systemverilog, IC, VLSI, CADENCE Virtuoso, SPICE, Verilog, ATPG, Formality, Linting, Code Coverage, Sub System, USB 2.0, DSP, Digital Signal Processors, FPGA, and other related technologies. Currently seeking new opportunities in the semiconductor industry.

Skills:
- Mixed signal design
- NCSim
- SOC design
- Functional verification
- RTL design
- ASIC design
- Systemverilog
- IC design
- VLSI design
- CADENCE Virtuoso
- SPICE simulation
- Verilog
- ATPG
- Formality
- Linting
- Code coverage
- Sub system design
- USB 2.0
- DSP and digital signal processors
- FPGA design

Location: Milpitas, California, United States (North America)
Industry: Semiconductors

Professional Experience:
[Open to new opportunities]

Education: [To be added if applicable]

Technical Proficiencies:
- Mixed signal design tools and methodologies
- CADENCE Virtuoso, SPICE, Verilog, Systemverilog, NCSim, Formality, Linting, ATPG, Code Coverage
- FPGA development tools (Xilinx, Altera)
- Digital signal processing software (Matlab, Simulink)

Certifications: [To be added if applicable]

Languages: English (Fluent), [Other languages if applicable]

References available upon request.

Note: Max Git forks and max stars not provided in the profile.