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BLG-322e Homework -2-

a-)

ADD R6, R7, R8	F	D	O	A	M												
NOP		N	N	N	N	N											
LD 0(R8), R1			F	D	O	A	M										
LD 0(R11), R2				F	D	O	A	M									
NOP					N	N	N	N	N								
NOP						N	N	N	N	N							
ADD R1, R2, R3							F	D	O	A	M						
NOP								N	N	N	N	N					
ADD R0, R3, R4									F	D	O	A	M				
ST 0(R12), R3										F	D	O	A	M			
BA L2											F	D	O	A	M		
NOP												N	N	N	N	N	
ADD R0, 0, R3													F	D	O	A	M

I added NOP if there is data or branch conflict. Like when a data is been readed before updated and also i added nope after branch for emptying the pipeline. And two NOP's added beacuse of waiting time of writing and reading from memory.

Since there is 5 NOP's there will be a 5 clock cycle penalty for this piece of code.

b-)

ADD R6, R7, R8	F	D	O	A	M										
LD 0(R11), R2		F	D	O	A	M									
LD 0(R8), R1			F	D	O	A	M								
NOP				N	N	N	N	N							
NOP					N	N	N	N	N						
ADD R1, R2, R3						F	D	O	A	M					
NOP							N	N	N	N	N				
ADD R0, R3, R4								F	D	O	A	M			
ST 0(R12), R3									F	D	O	A	M		
BA L2										F	D	O	A	M	
ADD R0, 0, R3											F	D	O	A	M

When software base solutions are applied the pipiline still get a penalty for memory access time and register write time but this time penalty is only 3 clock cyles.

Changes:

LD 0(R11), R2 - LD 0(R8), R1 Changed Places

ADD R0, 0, R3 - ADD R0, 0, R4 Changed Places