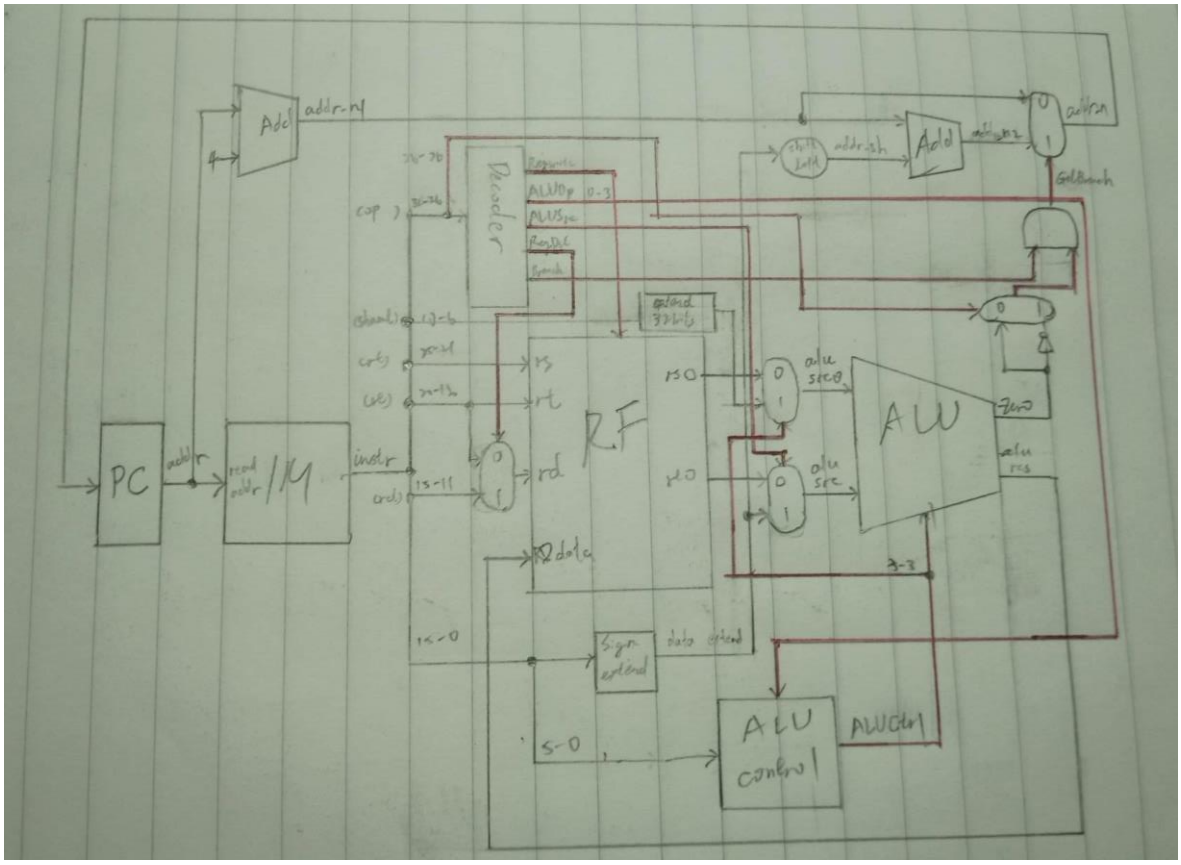
Computer Organization Lab 2: Simplified Single-cycle CPU

(1) Architecture diagram

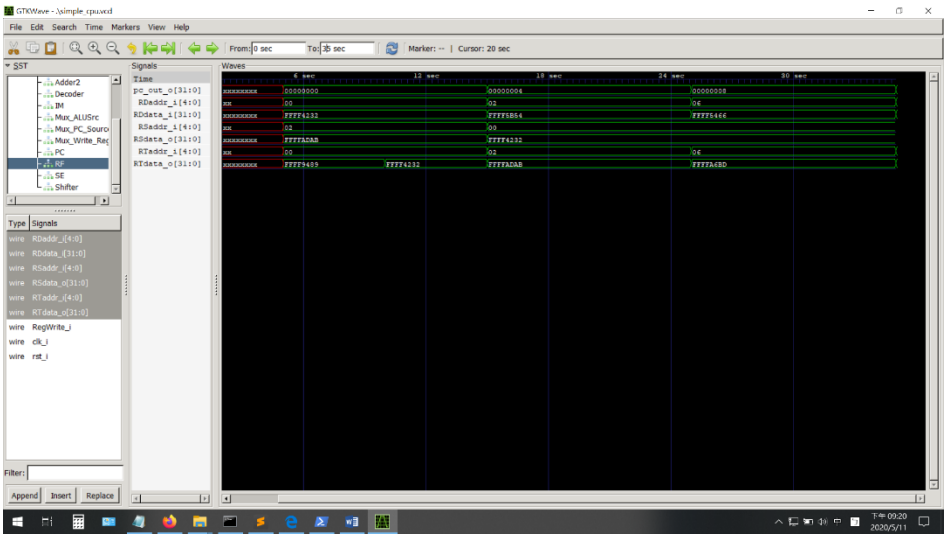


(2) Module description

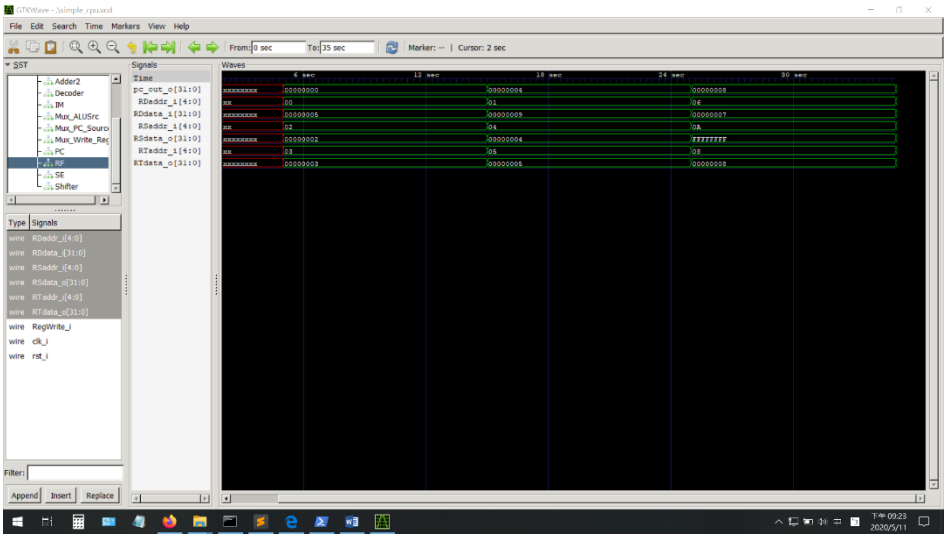
Adder: calculate the next address.
ALU: has function AND, OR, SUM, SUB, SLTIU, SR, LU, SLT.
ALU_Ctrl: output the signal to determine the which function of ALU should do.
Decoder: output control signals.
Instr_Memory: obtain instruction.
MUX_2to1: 2 to 1 multiplexer.
ProgramCounter: counter of address.
Reg_File: write data to register or read data from register.
Shift_Left_Two_32: output equal to input times 4.
Sign_Extend: extend input data to 32 bits.
Simple_Single_CPU: total structure.

(3) Waveform

addi:



addu:



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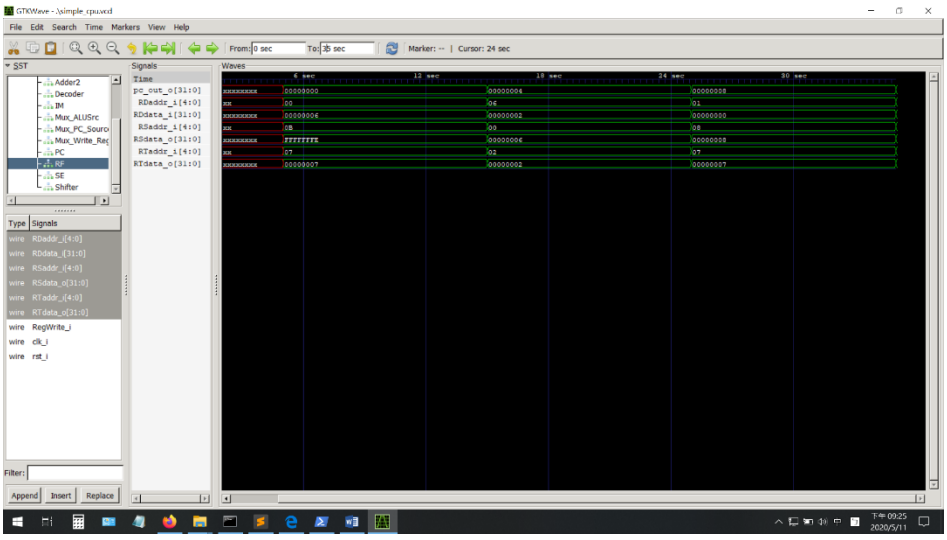
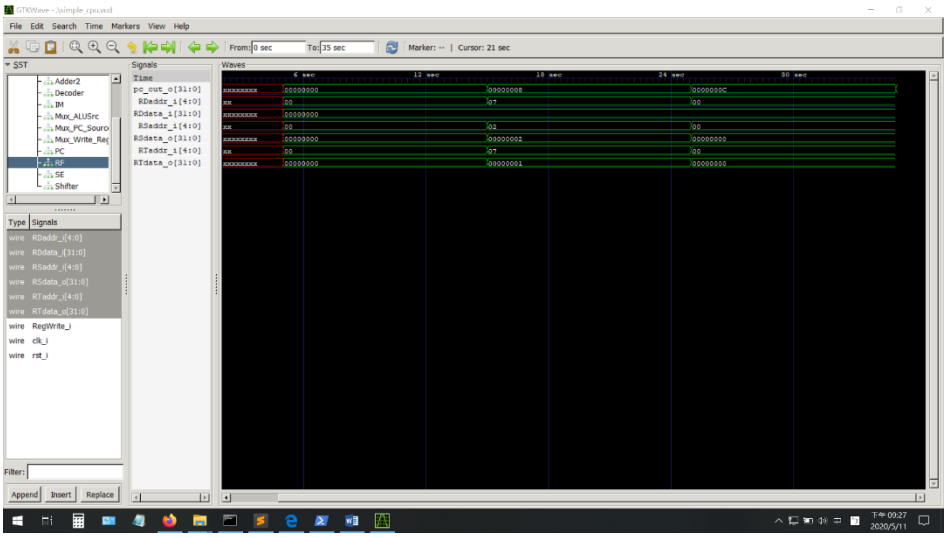
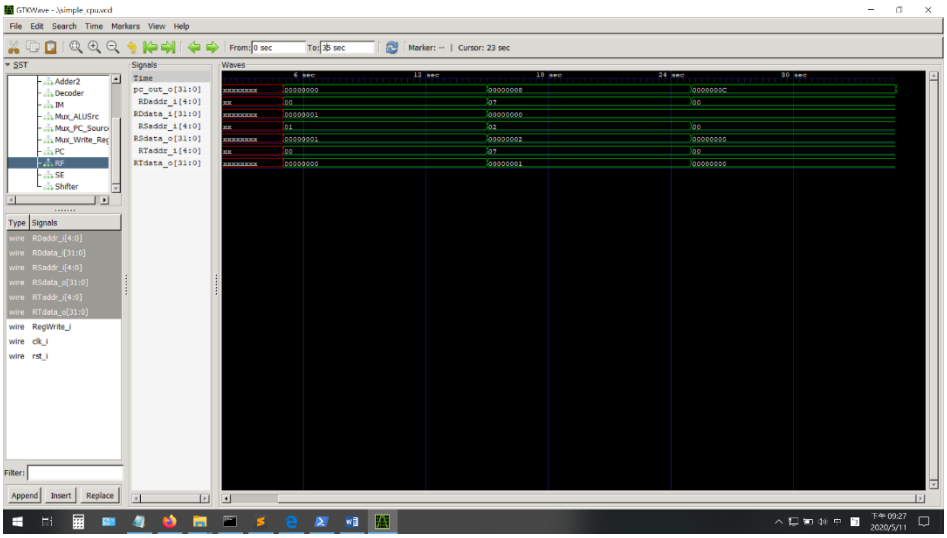


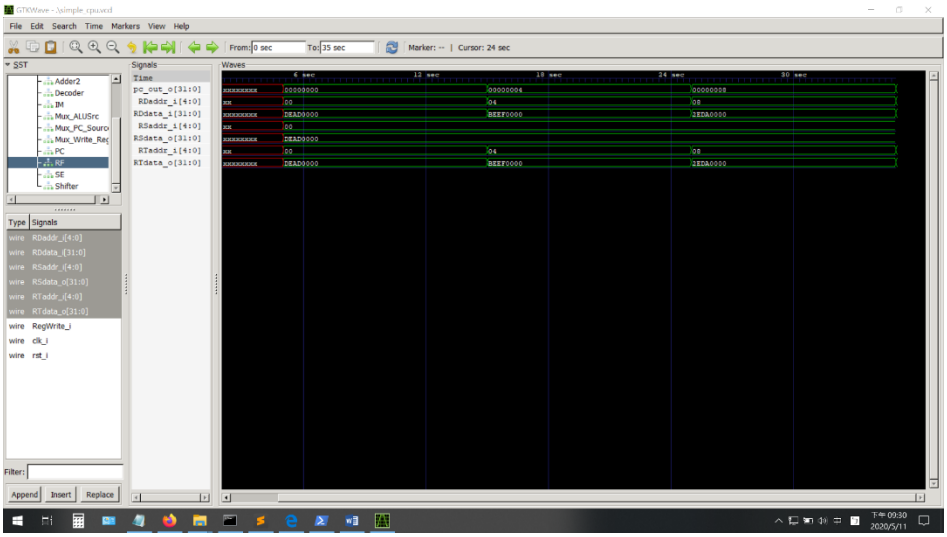
beq:



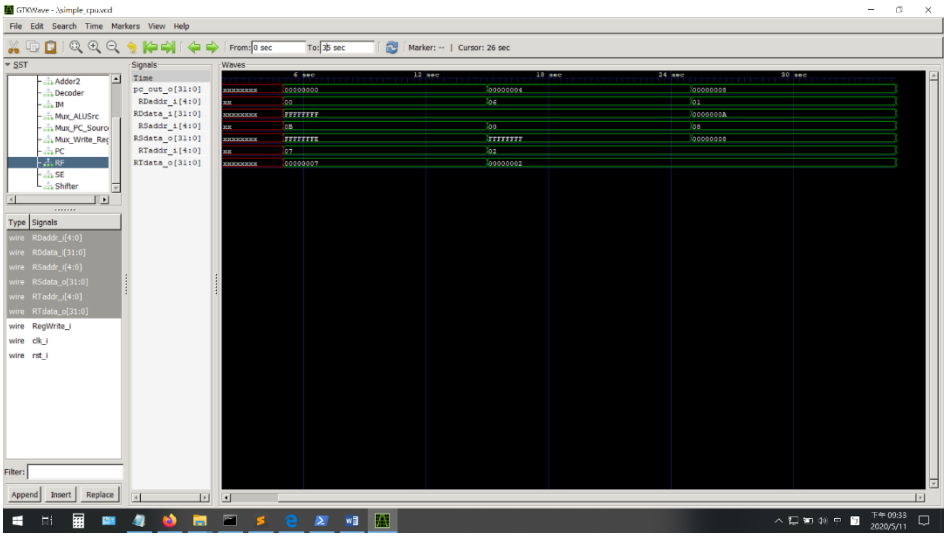
bne:



lui:



or:



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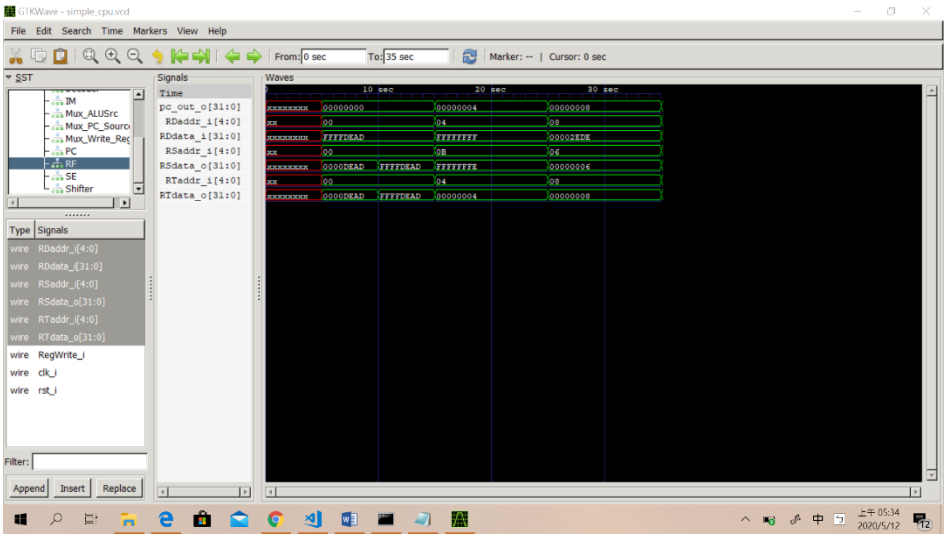
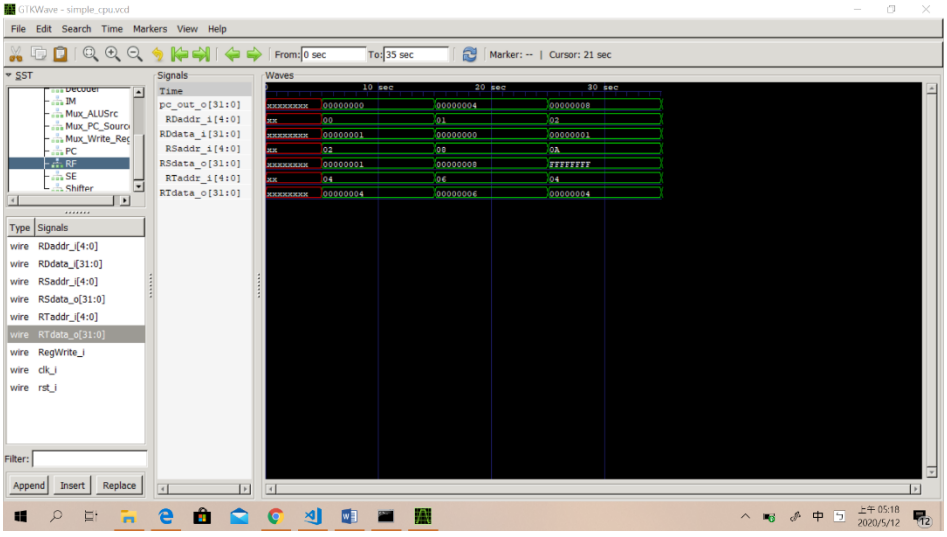
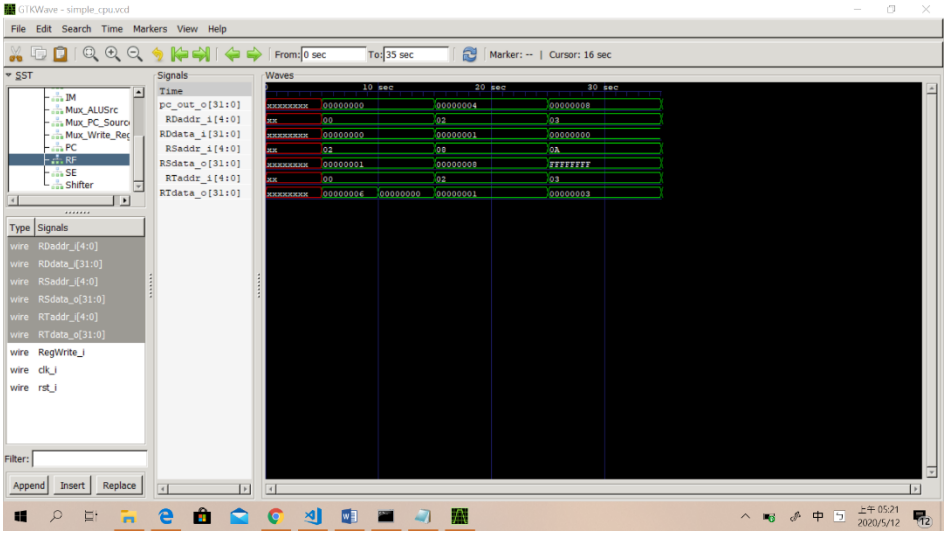


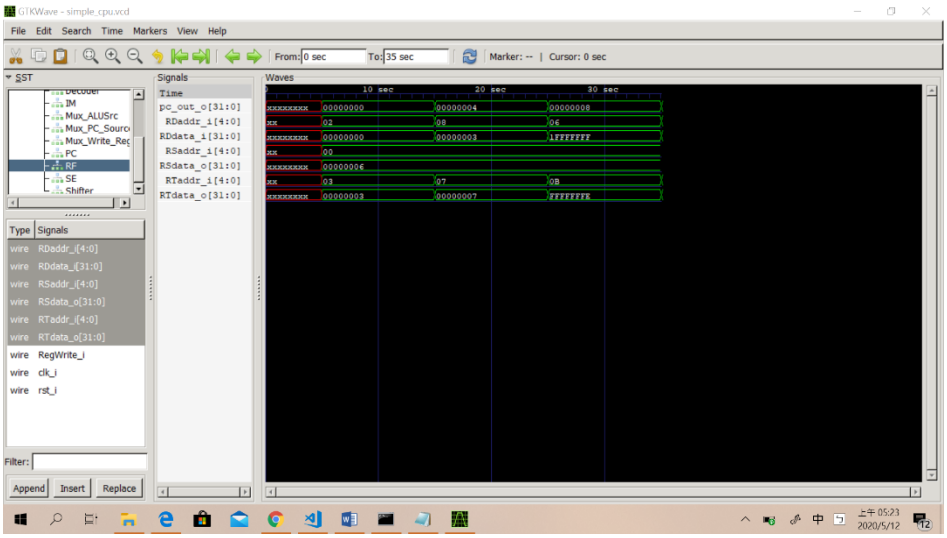
slt:



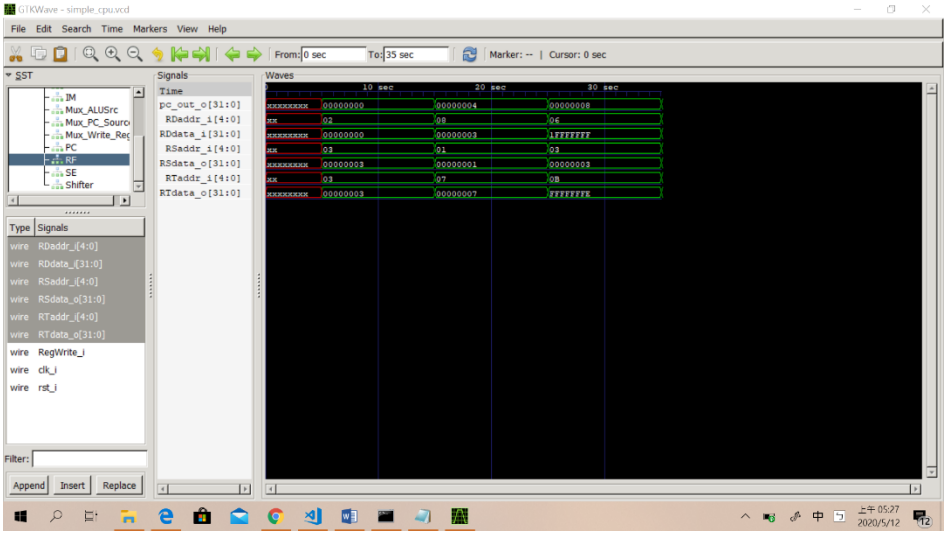
sltiu:



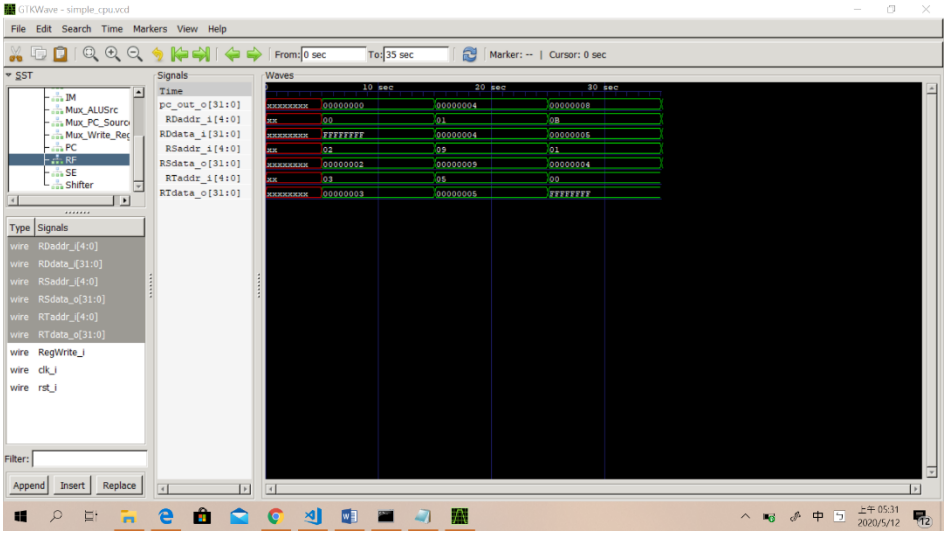
sra:



srav:



subu:



(4) Questions

1.

"input [15:0] input_0": a 16-bit variable

"input [0:15] input_0": 16 1-bit variables

2.

executing when the condition been modified.

3.

port connection by order: few code, but program crash if wrong order

port connection by name: more code, but less possibility of crash

(5) Contribution

Adder, ALU_Ctrl, Shift_Left_Two_32, Simple_Single_CPU, bug fixing, arrange ALU control code

(6) Discussions

There seems to have some different between datapath in ch4 and this project.