CO_Lab 1
ALU

TA: Yi, Lee

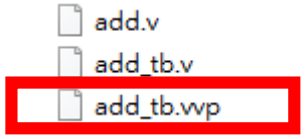
E-mail: nctubio@gmail.com

Installation of Icarus Varilog and GTKWave

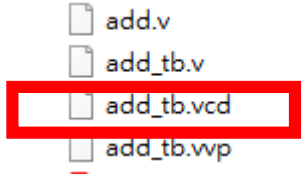
- Make sure that you install these softwares with administrator
- Open cmd.exe and move to directory the .v file you are working on
- Execute commands mentioned in the pdf file, then you will get corresponding files

```
C:\Users\cad633>cd C:\Users\cad633\Downloads\CO_2019\tool installation (2)\tool installation
```

```
C:\Users\cad633\Downloads\CO_2019\tool installation (2)\tool installation>iverilog -o add_tb.vvp add_tb.v add.v
```




```
C:\Users\cad633\Downloads\CO_2019\tool installation (2)\tool installation>vvp add_tb.vvp
VCD info: dumpfile add_tb.vcd opened for output.
```

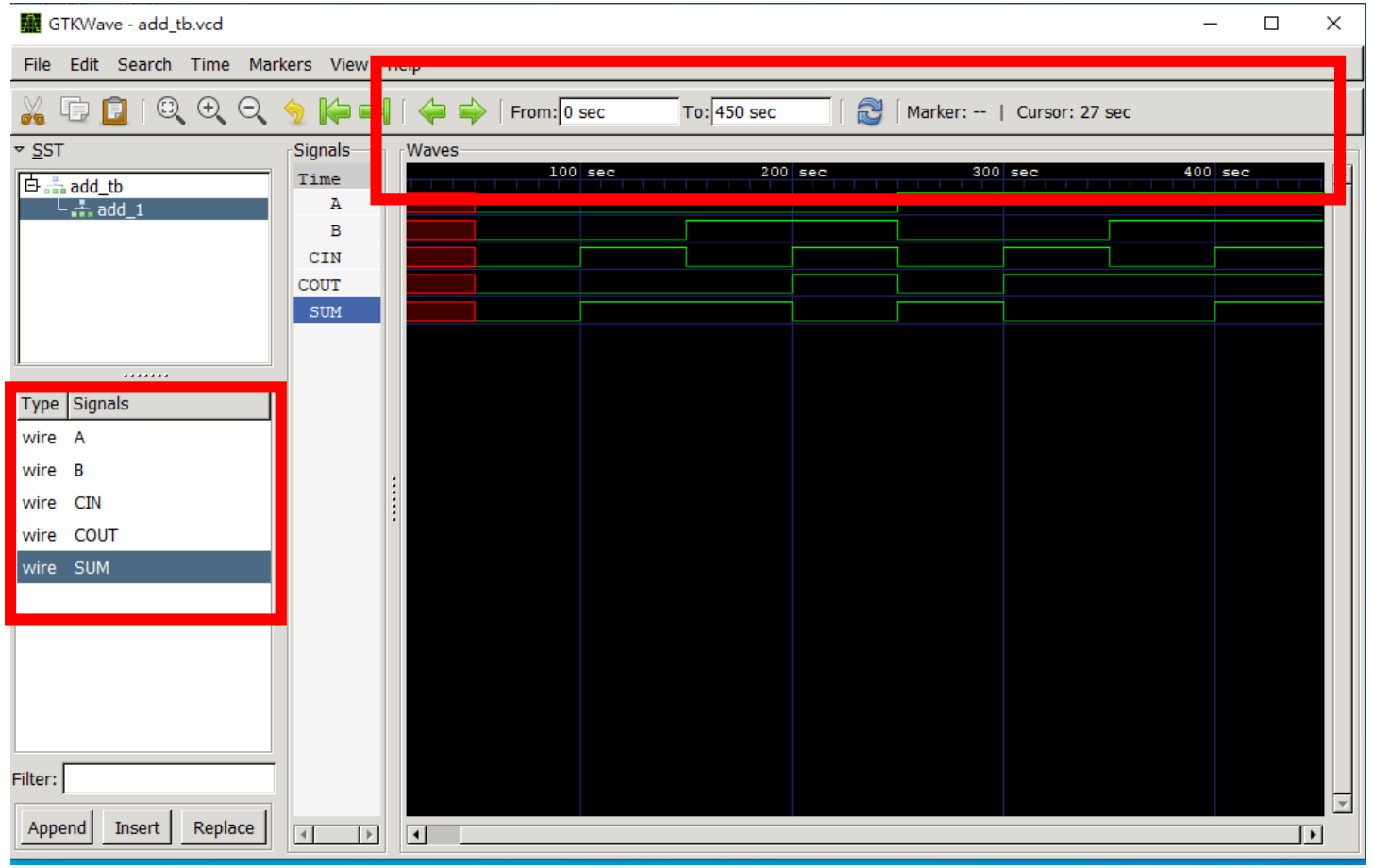


Execute gtkwave to see the results

```
C:\Users\cad633\Downloads\CO_2019\tool installation (2)\tool installation>gtkwave add_tb.vcd

GTKWave Analyzer v3.3.100 (w)1999-2019 BSI

[0] start time.
[450] end time.
```



- Double clicks these signals
- Look out for the time scale

Hint

- Complete this lab with 32 one-bit ALU is more recommended than one 32-bits ALU, which means that you will not get full scores if you do the latter one.
- Thus, knowing the concept of module would be helpful. It is also good for you to improve your coding style.

Example of module fulladder called by another module.

Module main is like a test bench to demonstrate the result.

```
module fulladder(input a,b,c_in, output sum, c_out);
    wire s1, c1,c3;
    xor g1(s1, a, b);
    xor g2(sum, s1, c_in);
    and g3(c1, a,b);
    and g4(c2, s1, c_in) ;
    xor g5(c_out, c2, c1) ;

endmodule

module adder_4bit(input [3:0] a, input [3:0] b, input c_in, output [3:0] sum, output c_out);
    wire [3:0] c;
    fulladder fa1(a[0],b[0],c_in,sum[0],c[1]);
    fulladder fa2(a[1],b[1],c[1],sum[1],c[2]);
    fulladder fa3(a[2],b[2],c[2],sum[2],c[3]);
    fulladder fa4(a[3],b[3],c[3],sum[3],c_out);
endmodule

module main;
reg [3:0] a;
reg [3:0] b;
wire [3:0] sum;
wire c_out;

adder_4bit demo (a, b, 1'b0, sum, c_out);

initial
begin
  a = 4'b0000;
  b = 4'b0000;
end

always #1 begin
  b=b+1;
  if (b==4'b1111)
    a=a+1;
  $monitor("%dns monitor: a=%d b=%d sum=%d", $stime, a, b, sum);
end

initial #256 $finish;

endmodule
```