Computer Organization Lab 4: Cache Simulator

Student ID: 0716085 Name: 賴品樺

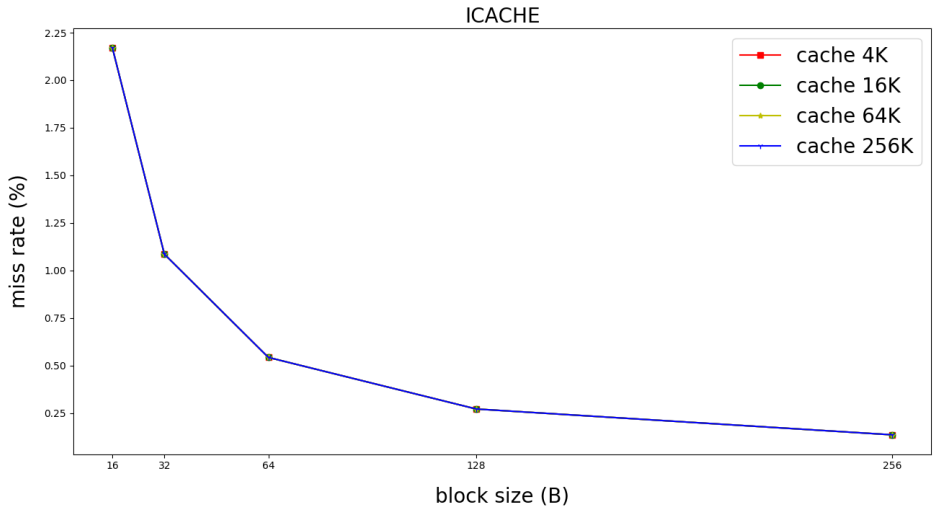
Teammate ID: 0716316 Name: 洪珩均

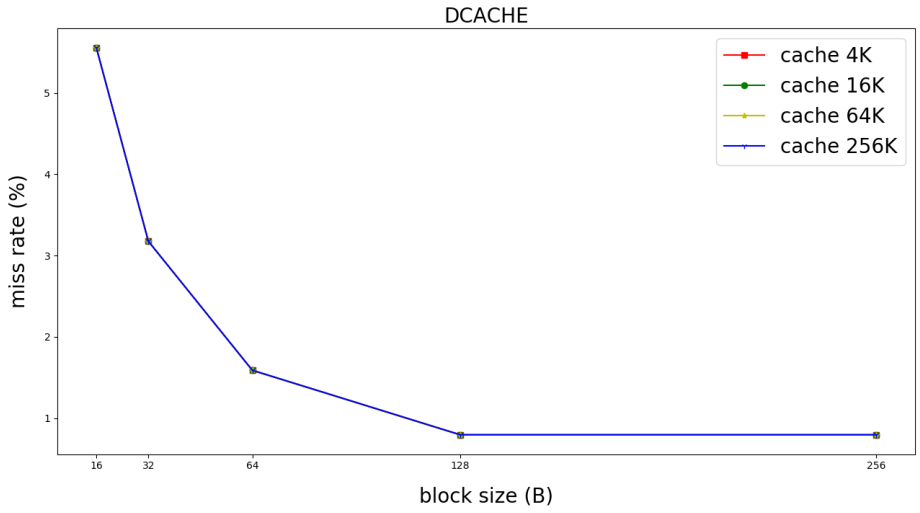
(1) Basic Problem

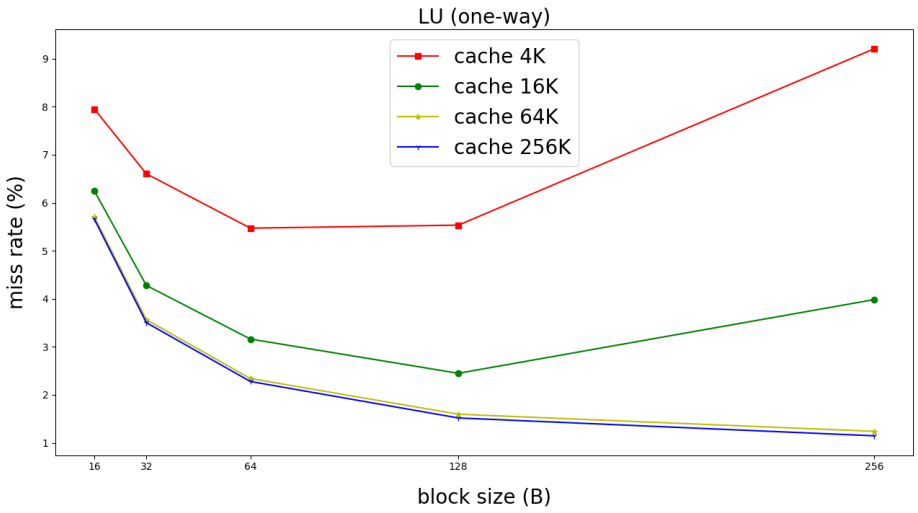
Verilog result:

```
系統管理員: Windows PowerShell
PS D:\NCTU\108_2\Computer Organization\Lab4\tmp> iverilog -o cpu.vvp *.v
PS D:\NCTU\108_2\Computer Organization\Lab4\tmp> vvp .\cpu.vvp
WARNING: Instruction_Memory.v:40: $readmemb(lab4_test_data.txt): Not enough words in the file for the requested range [0:64].
** VVP Stop(0) **
** Flushing output streams.
** Current simulation time is 20020000 ticks.
> finish
** Continue **
PS D:\NCTU\108_2\Computer Organization\Lab4\tmp>
```

direct_mapped_cache result:





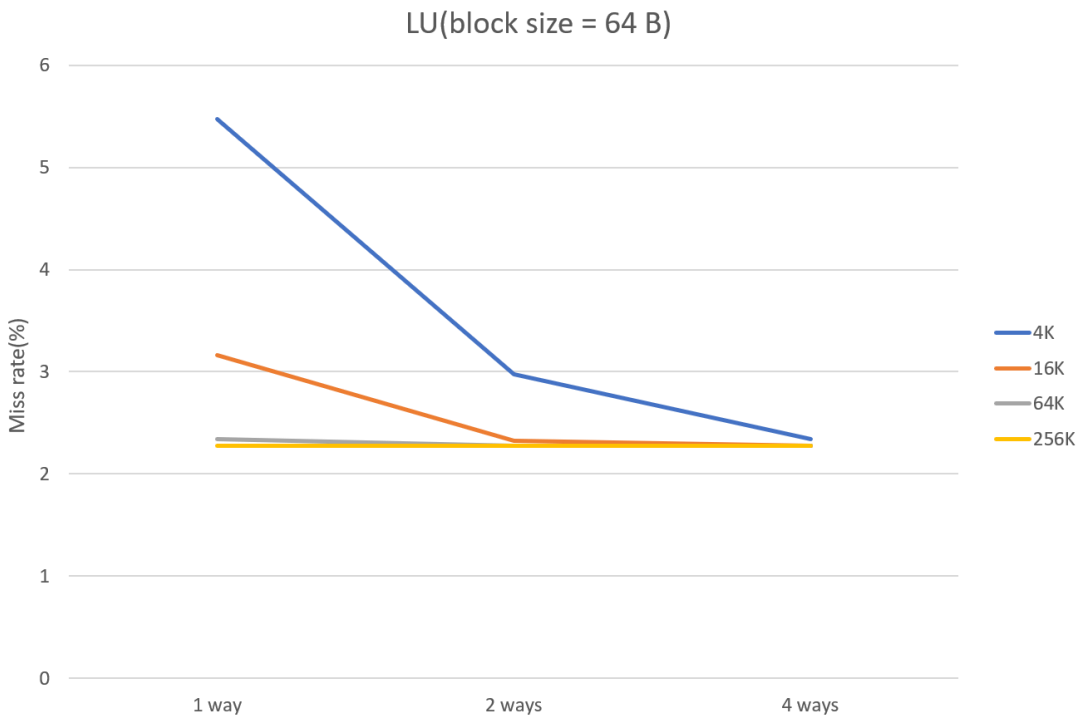


the reason of rise and fall of the lines:

When the block size rises and the cache size is fixed, the offset bit will reduce and the number of lines (blocks) in the cache will reduce. As the number of lines reduce, the rate of access an invalid block will reduce, which can greatly reduce miss rate. But the number of lines can't reduce without limited, the decreasing of number of lines can also cause the increase of miss rate (see LU (one-way)). It is because the over-decreasing of lines will increase the miss rate of tag unmatching.

(2) Advanced Problem

LU (block size = 64B):



CACHE SIZE	4K	16K	64K	256K
1 way	5.472%	3.1623%	2.3407%	2.2787%
2 ways	2.9763%	2.3252%	2.2787%	2.2787%
4 ways	2.3407%	2.2787%	2.2787%	2.2787%

RADIX (block size = 64B):

CACHE SIZE	4K	16K	64K	256K
1 way	19.2569%	7.3560%	1.0109%	0.7517%
2 ways	2.7117%	0.8093%	0.7517%	0.7517%
4 ways	1.1679%	0.7532%	0.7517%	0.7517%

(3) Execution Step

$ iverilog -o cpu.vvp *.v
$ vvp cpu.vvp
$ make
$ ./ direct_mapped_cache
$ ./ direct_mapped_cache_lru