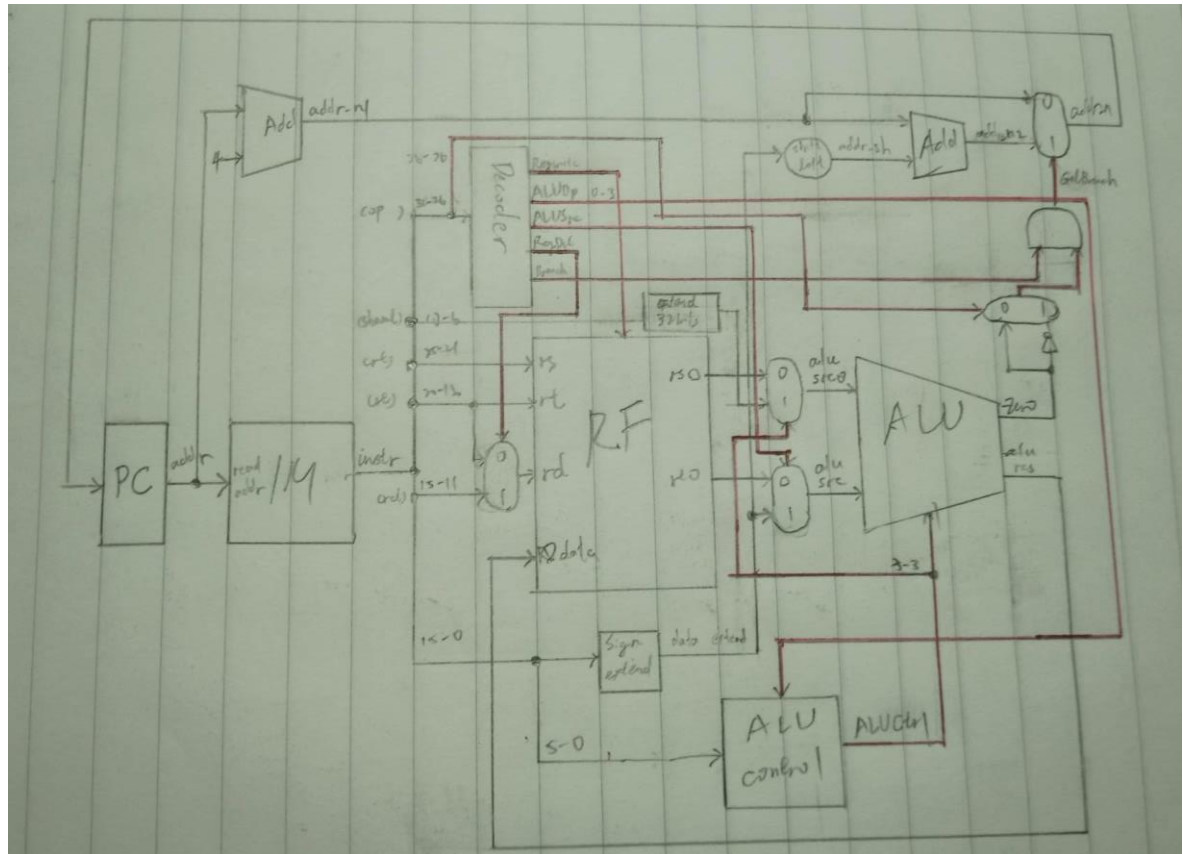


Computer Organization Lab 2: Simplified Single-cycle CPU

Student ID: 0716085 Name: 賴品樺

Teammate ID: 0716316 Name: 洪珩均

(1) Architecture diagram



(2) Module description

Adder: calculate the next address.

ALU: has function AND, OR, SUM, SUB, SLTIU, SR, LU, SLT.

ALU_Ctrl: output the signal to determine the which function of ALU should do.

Decoder: output control signals.

Instr Memory: obtain instruction.

MUX 2to1: 2 to 1 multiplexer.

ProgramCounter: counter of address.

Reg File: write data to register or read data from register.

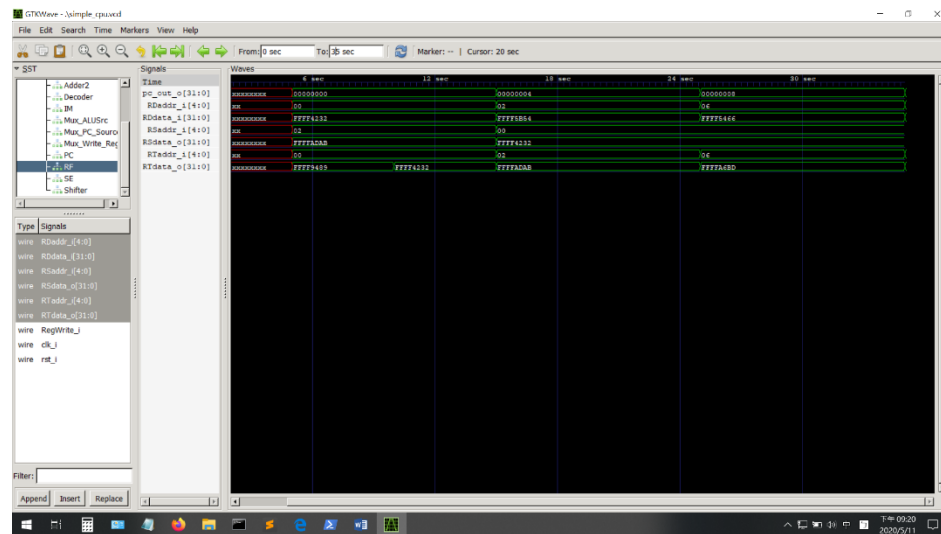
Shift Left Two 32: output equal to input times 4.

Sign Extend: extend input data to 32 bits.

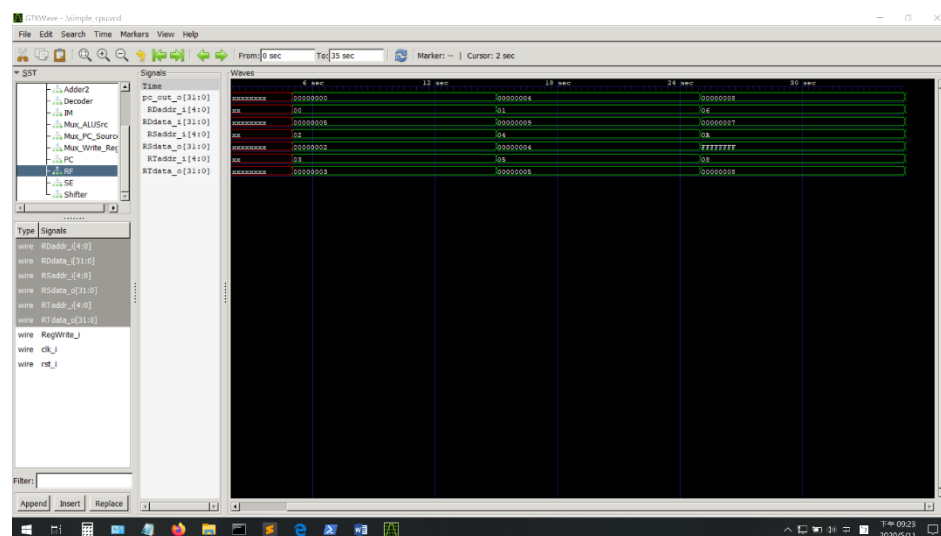
Simple Single CPU: total structure.

(3) Waveform

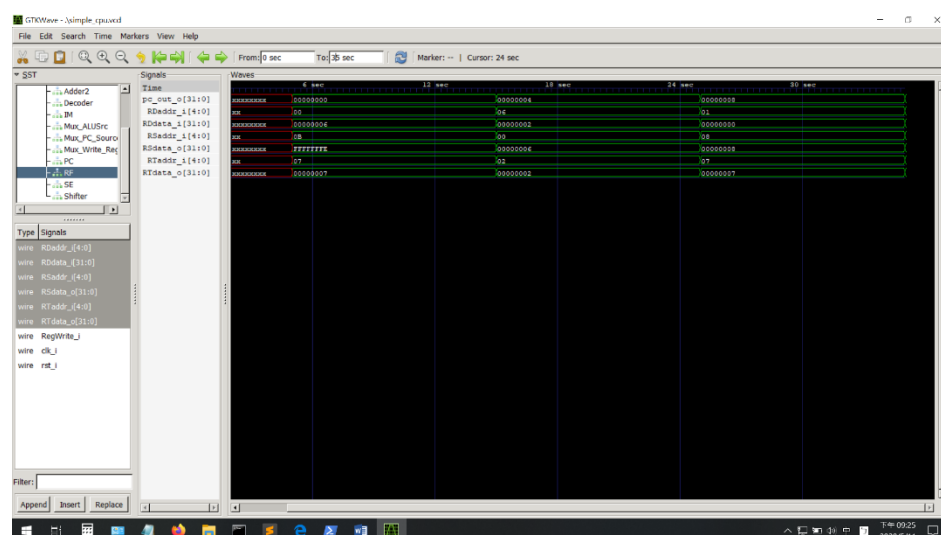
addi:



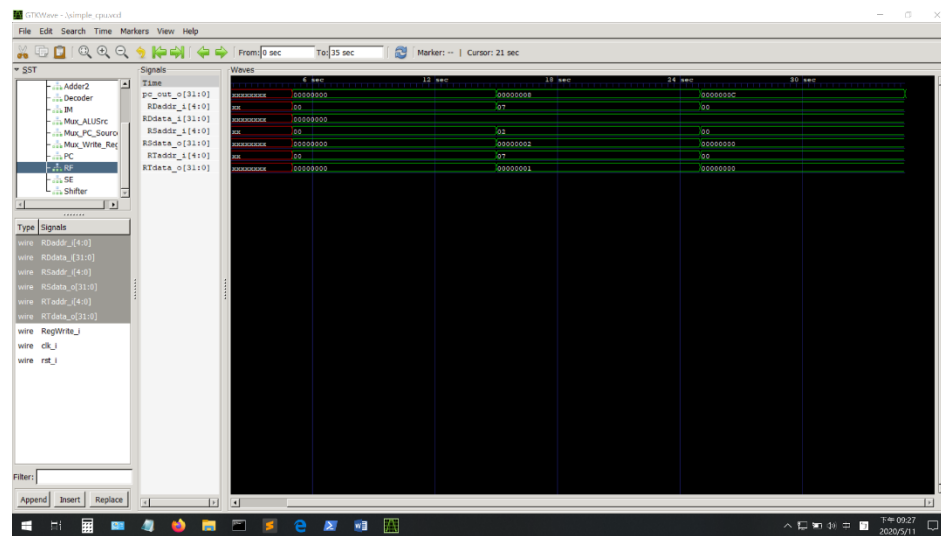
addu:



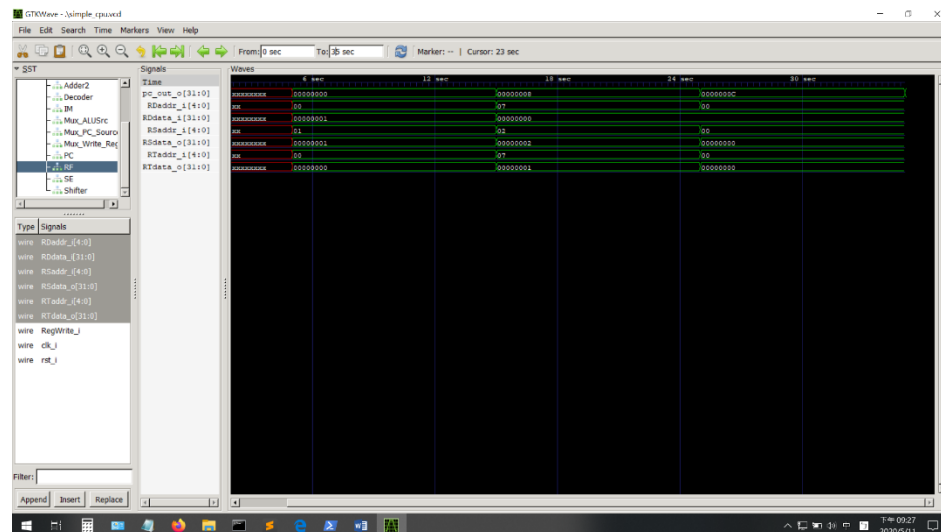
and:



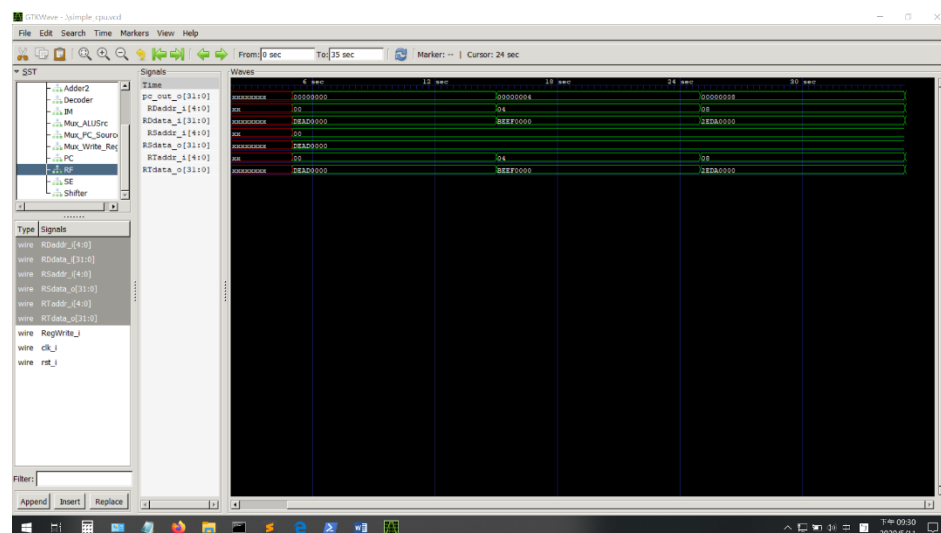
beq:



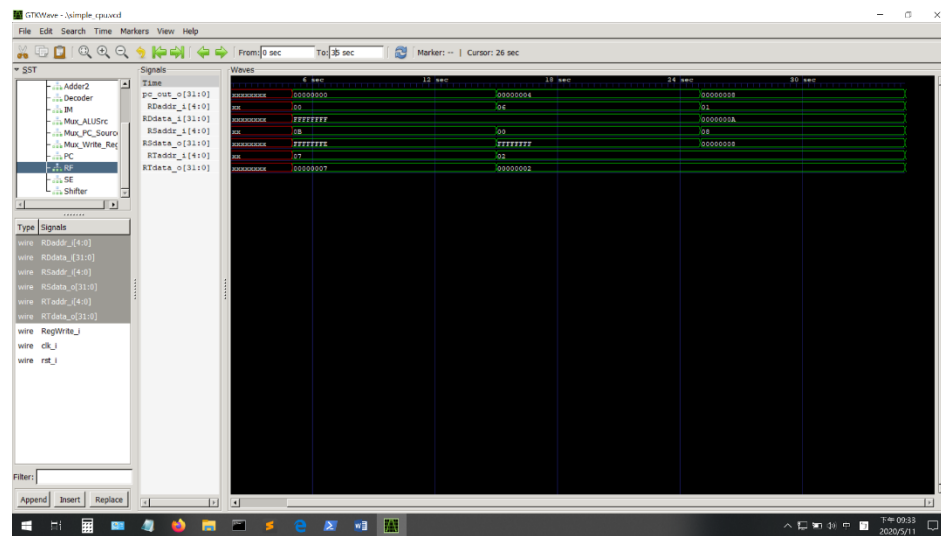
bne:



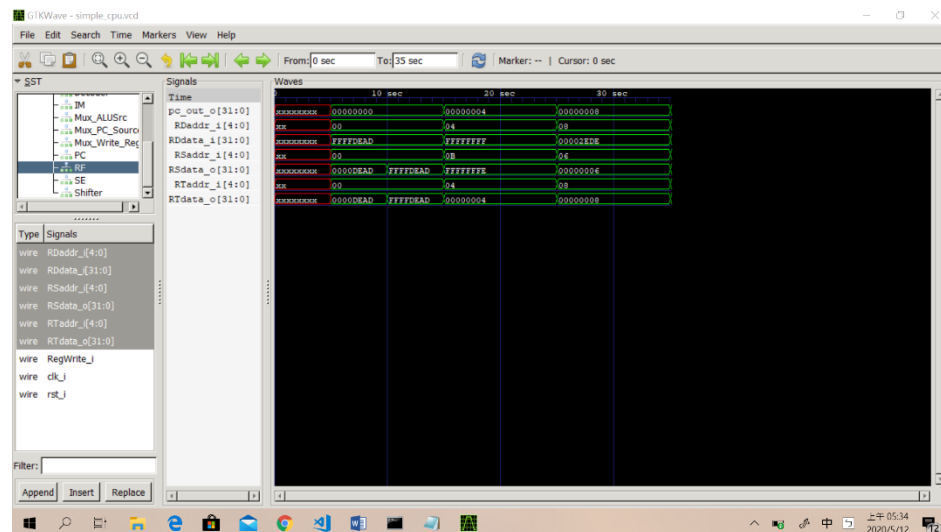
lui:



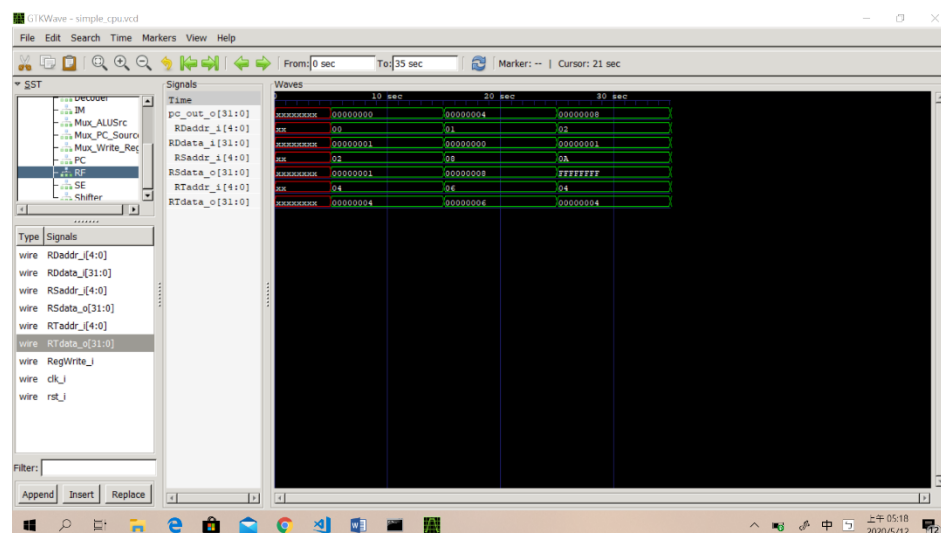
or:



ori:



slt:



The screenshot shows the GTKWave interface for a Verilog simulation. The top menu bar includes File, Edit, Search, Time, Markers, View, and Help. Below the menu is a toolbar with icons for file operations and simulation control. The main workspace is divided into three panels:

- SST (Signal Structure Tree):** Located on the left, it shows a hierarchical list of signals. The signal 'RegWrite_1' is currently selected.
- Signals:** Located in the center, it lists the signals present in the simulation. The signals listed are:
 - pc_out_o[31:0]
 - RDaddr_i[4:0]
 - RDdata_i[31:0]
 - RSaddr_i[4:0]
 - RSdata_o[31:0]
 - RTaddr_i[4:0]
 - RTdata_o[31:0]
- Waves:** Located on the right, it displays a waveform view. The waveform is organized into three columns representing time intervals: 10 sec, 20 sec, and 30 sec. The signals shown in the waveform are:
 - RDdata_i[31:0]: Shows a sequence of hexadecimal values (00000000, 00000004, 00000008, 00, 08, 06, 00, 0000000E, 00000007, 00000007, 00000007).
 - RSdata_o[31:0]: Shows a sequence of hexadecimal values (00000000, 00000003, 00000003, 00, 0000000E, 00000007, 00000007, 00000007).
 - RTdata_o[31:0]: Shows a sequence of hexadecimal values (00000000, 00000003, 00000003, 00, 0000000E, 00000007, 00000007, 00000007).

The bottom status bar shows the current time as 05:23 on 2020/5/12.

GTKWave - simple_cpu.gcd

File Edit Search Time Markers View Help

From: 0 sec To: 35 sec Marker: -- Cursor: 0 sec

SST

- BM
- Max_ALUSrc
- Max_PC_Souro
- Max_Write_Reg
- PC
- RF
- SE
- Shifter

Signals

Time

pc_out_o[31:0]

RDaddr_i[4:0]

RDdata_i[31:0]

RSaddr_i[4:0]

RSdata_o[31:0]

RTaddr_i[4:0]

RTdata_o[31:0]

Waves

10 sec 20 sec 30 sec

Signal	00000000	00000004	00000008
pc_out_o[31:0]	00000000	00000004	00000008
RDaddr_i[4:0]	00	08	06
RDdata_i[31:0]	00000000	00000003	11111111
RSaddr_i[4:0]	03	01	03
RSdata_o[31:0]	00000003	00000001	00000003
RTaddr_i[4:0]	03	07	0B
RTdata_o[31:0]	00000003	00000007	11111111

Type Signals

wire RDaddr_i[4:0]

wire RDdata_i[31:0]

wire RSaddr_i[4:0]

wire RSdata_o[31:0]

wire RTaddr_i[4:0]

wire RTdata_o[31:0]

wire RegWrite_i

wire clk_i

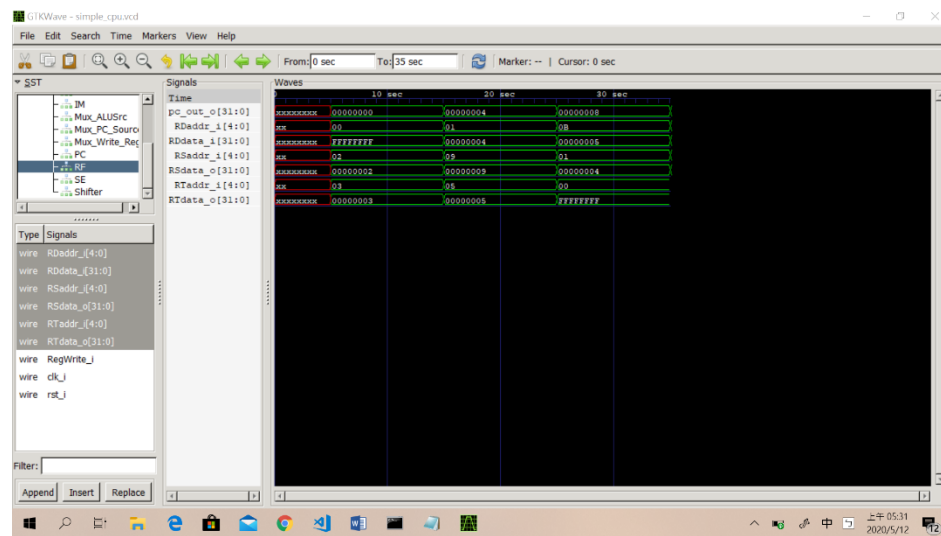
wire rst_i

Filter:

Append Insert Replace

2020/5/12 上午 05:27

subu:



(4) Questions

1.
"input [15:0] input_0": a 16-bit variable
"input [0:15] input_0": 16 1-bit variables
2.
executing when the condition been modified.
3.
port connection by order: few code, but program crash if wrong order
port connection by name: more code, but less possibility of crash

(5) Contribution

Adder, ALU_Ctrl, Shift_Left_Two_32, Simple_Single_CPU, bug fixing,
arrange ALU control code

(6) Discussions

There seems to have some different between datapath in ch4 and this project.