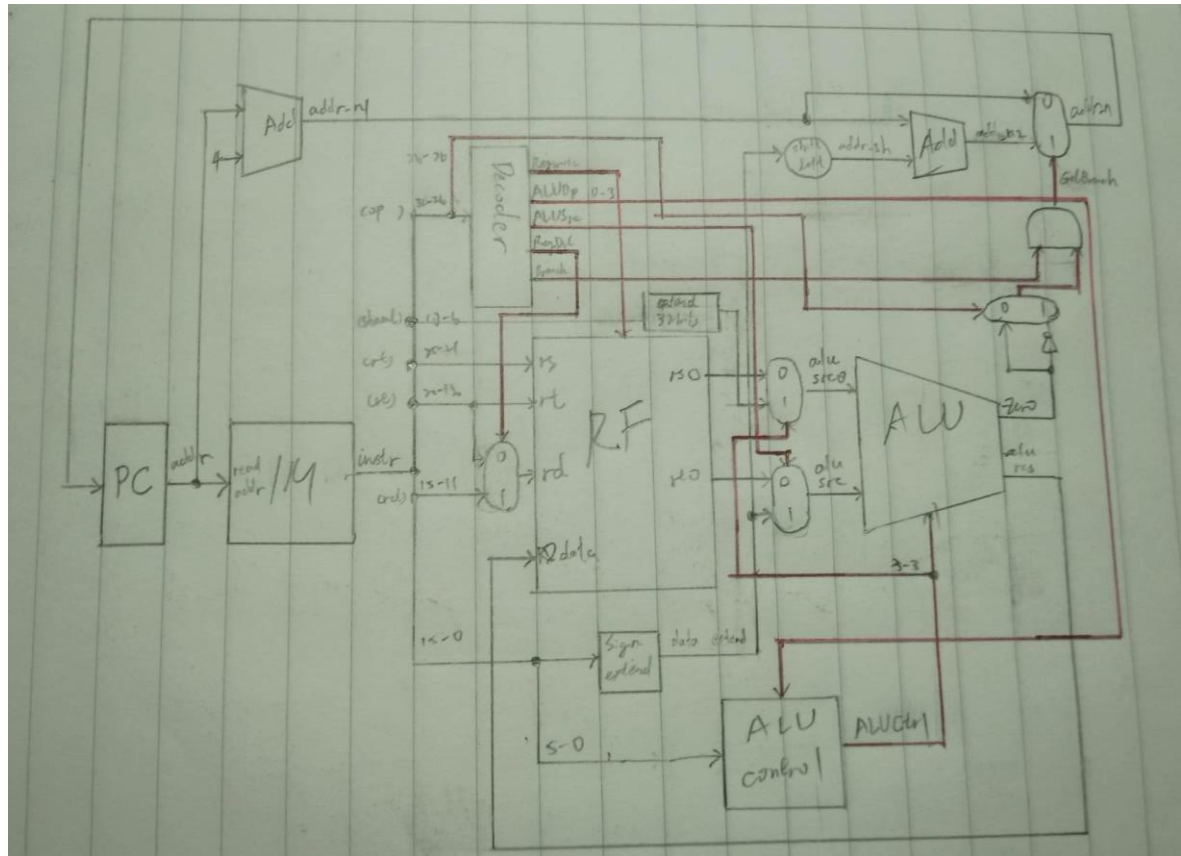


## Computer Organization Lab 2: Simplified Single-cycle CPU

### (1) Architecture diagram



## (2) Module description

Adder: calculate the next address.

ALU: has function AND, OR, SUM, SUB, SLTIU, SR, LU, SLT.

ALU\_Ctrl: output the signal to determine the which function of ALU should do.

Decoder: output control signals.

Instr Memory: obtain instruction.

MUX 2to1: 2 to 1 multiplexer.

ProgramCounter: counter of address.

Reg File: write data to register or read data from register.

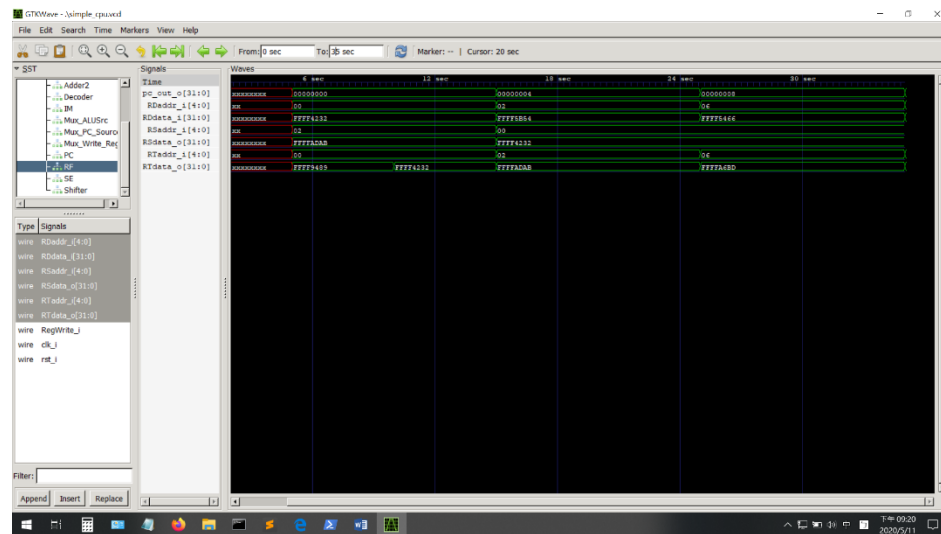
Shift Left Two 32: output equal to input times 4.

**Sign Extend:** extend input data to 32 bits.

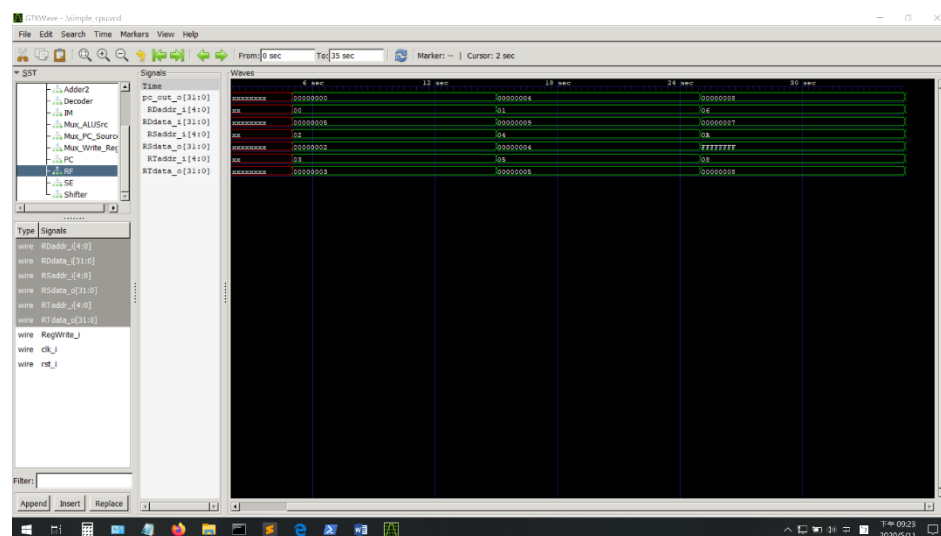
Simple Single CPU: total structure.

### (3) Waveform

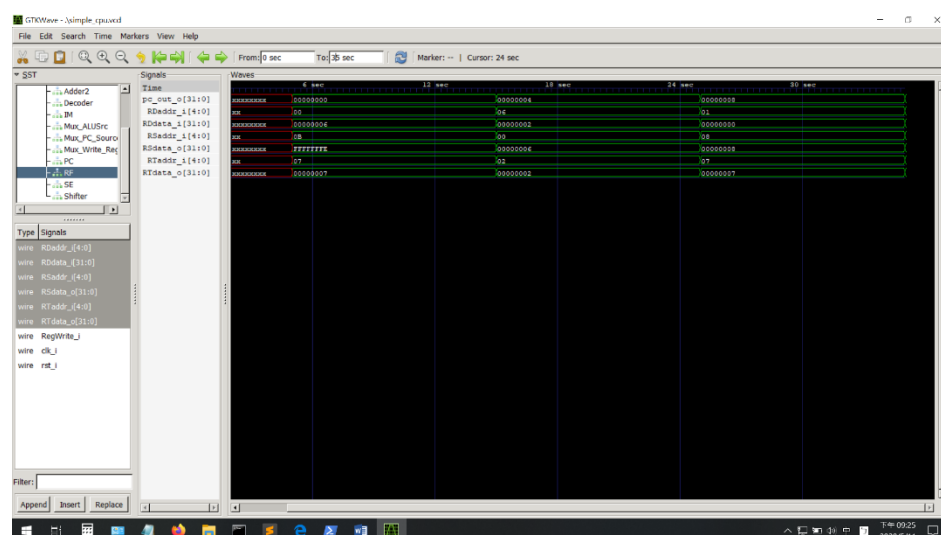
addi:



addu:



and:



GTWave - Jimple.rptuned

File Edit Search Time Markers View Help

From: 0 sec To: 30 sec Markers: -- | Cursor: 23 sec

SST

- Address2
  - Decoder
  - Mux
  - Max\_AliSrc
  - Max\_FC\_Souro
  - Max\_Write\_Ras
  - PC
  - SE
  - Shifter

Type Signals

- wire RbAddr\_[4:0]
- wire RbData\_[31:0]
- wire RbAddr\_o[4:0]
- wire RbData\_o[31:0]
- wire RTAddr\_o[4:0]
- wire RTData\_o[31:0]
- wire RegWrite\_i
- wire ck\_i
- wire rst\_i

Filter:

Append Insert Replace

Signals

Time

PC\_out\_o[31:0]

RbAddr\_i[4:0]

RbData\_i[31:0]

RbAddr\_o[31:0]

RbData\_o[31:0]

RTAddr\_i[4:0]

RTAddr\_o[31:0]

SE

Shifter

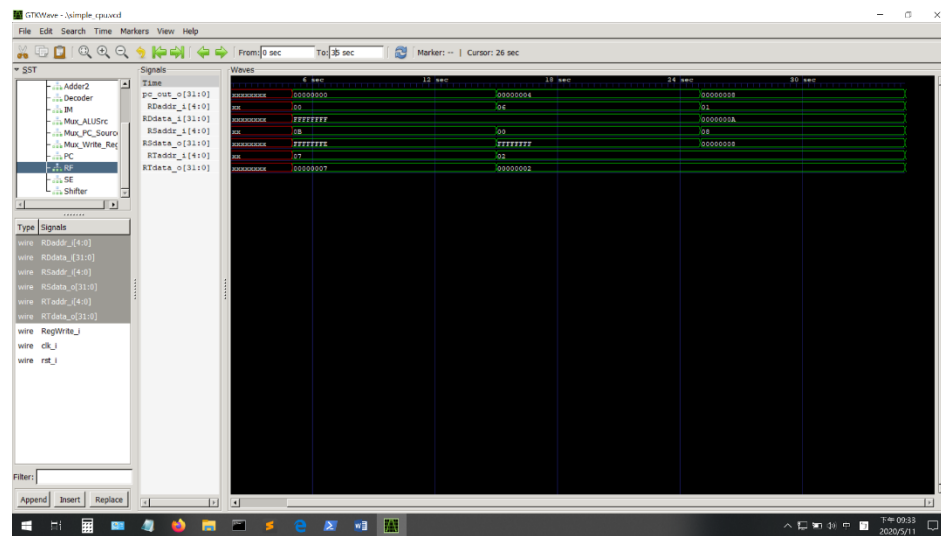
Values

4 sec	12 sec	18 sec	24 sec	30 sec
00000000	00000000	00000000	00000000	00000000
00	00	00	00	00
00000001	00000001	00000001	00000001	00000001
00	00	00	00	00
00000001	00000001	00000001	00000001	00000001
00	00	00	00	00
00000000	00000000	00000001	00000001	00000001

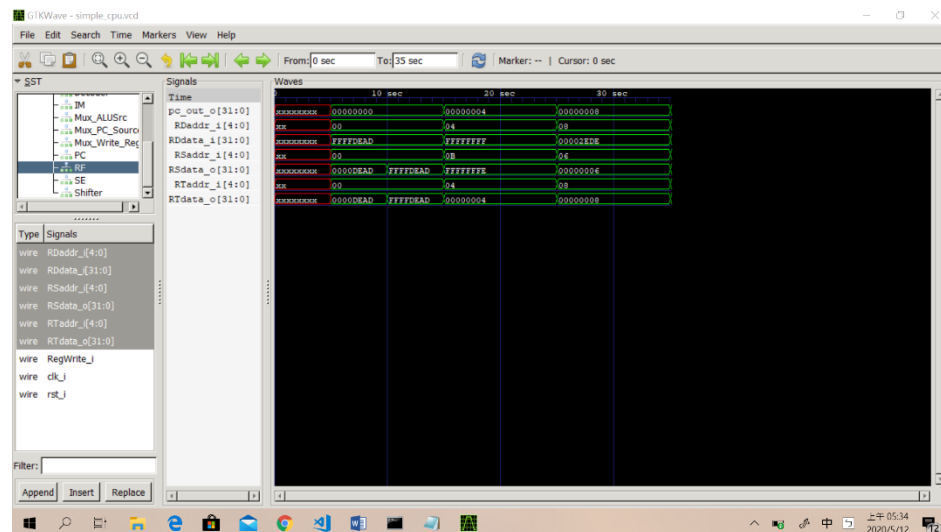
9:27 2024-02-11

[illegible]

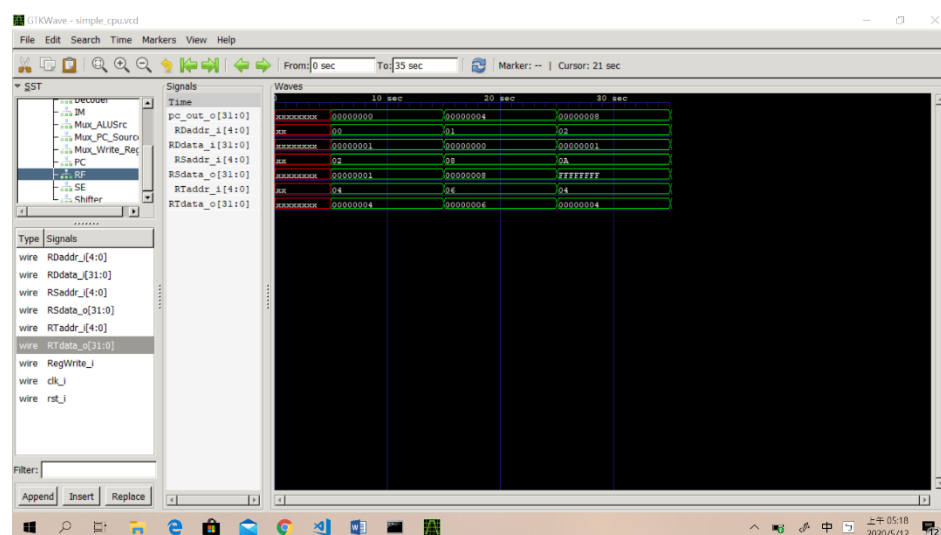
or:



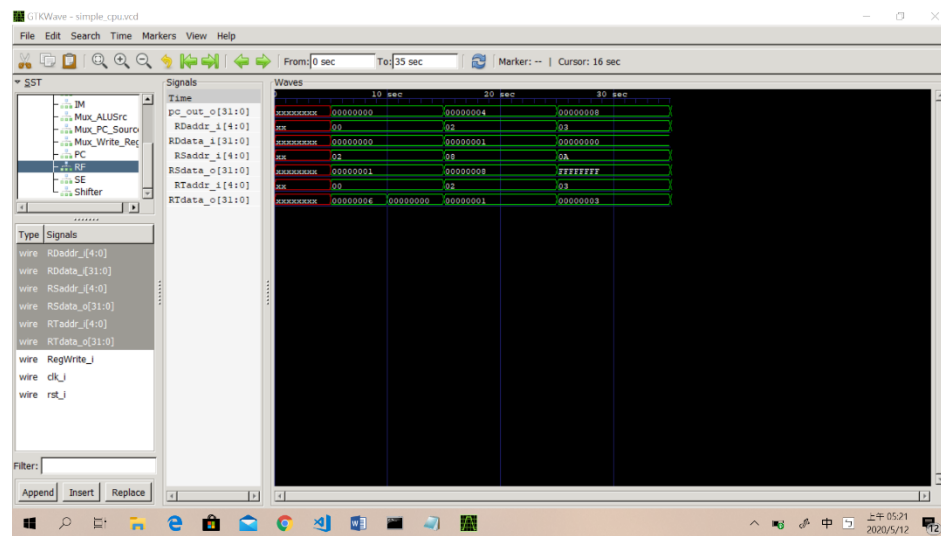
ori:



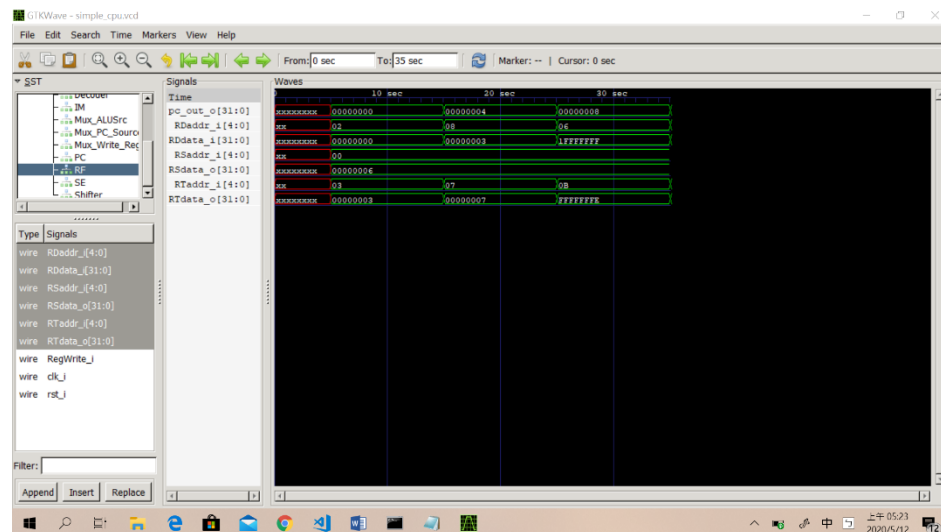
slt:



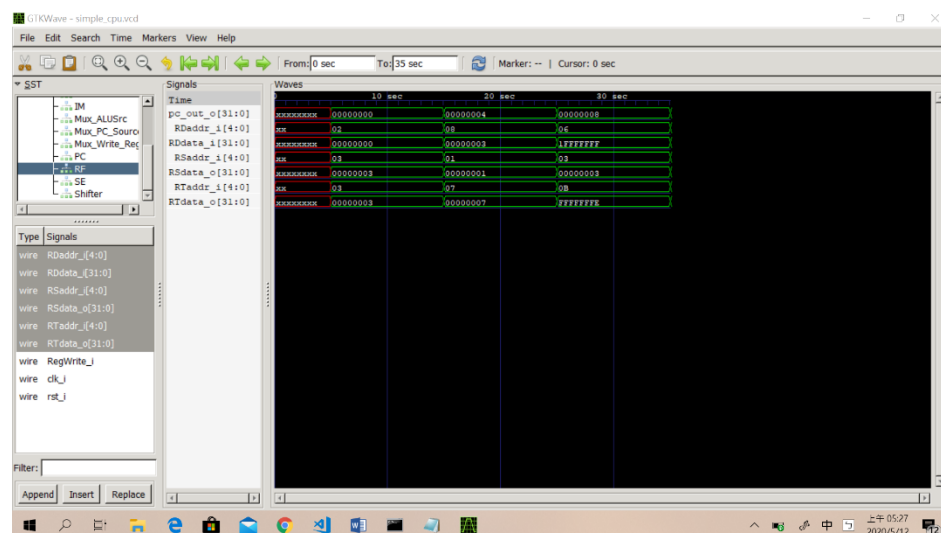
sltiu:



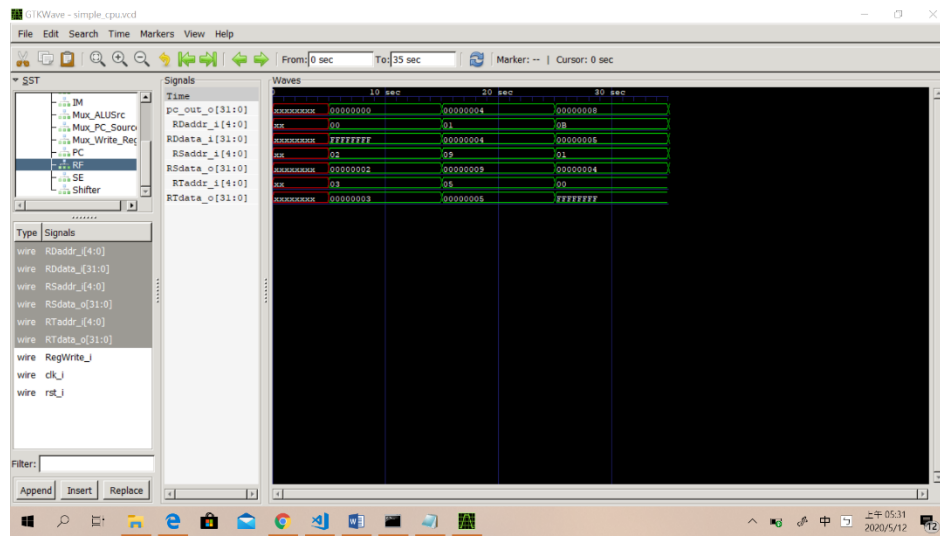
sra:



srav:



subu:



#### (4) Questions

1. "input [15:0] input\_0": a 16-bit variable  
"input [0:15] input\_0": 16 1-bit variables

2. executing when the condition been modified.

3. port connection by order: few code, but program crash if wrong order  
port connection by name: more code, but less possibility of crash

## (5) Contribution

Adder, ALU\_Ctrl, Shift\_Left\_Two\_32, Simple\_Single\_CPU, bug fixing,  
arrange ALU control code

## (6) Discussions

There seems to have some different between datapath in ch4 and this project.