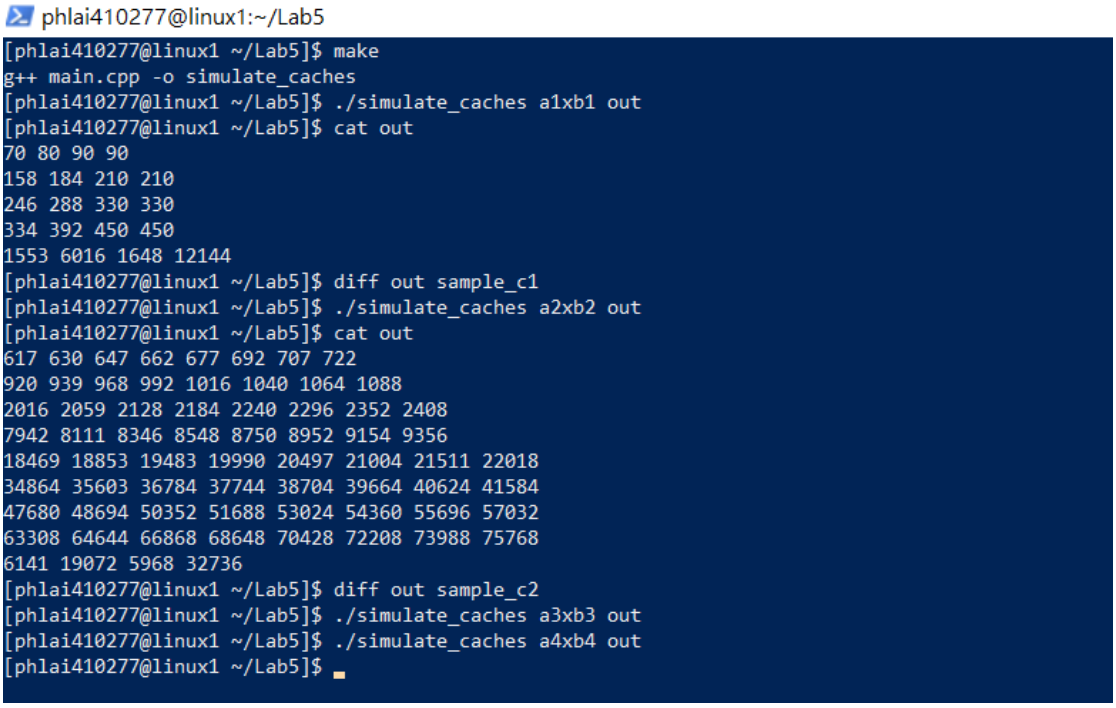
Computer Organization Lab 5: Cache Performance

Author ID: 0716316 Name: 洪珩均

Teammate ID: 0716085 Name:賴品樺

(1) Execution result



(2) Analysis and discussions for lab 5

Every time we access the cache, no matter hit or not, we should add up minimum memory stall cycle. We first check if the address hit or not. If miss, go to the next layer searching for the target address, add up miss penalty and also check if there is any invalid cache block. Our program will try to find the invalid slot which is nearest to the starting slot. If all slots are valid, replace the one that is least recently unused. Compare with case a and b, since the bandwidth in case b is 8-words wide, the miss penalty is less than in case a. Compare with case a and c, not only because the miss rate in L1 cache of case 3 is higher but also the block size of L2 cache is 32-word large, case 3 spend much more time on accessing memory and send a word to upper layer one at a time.