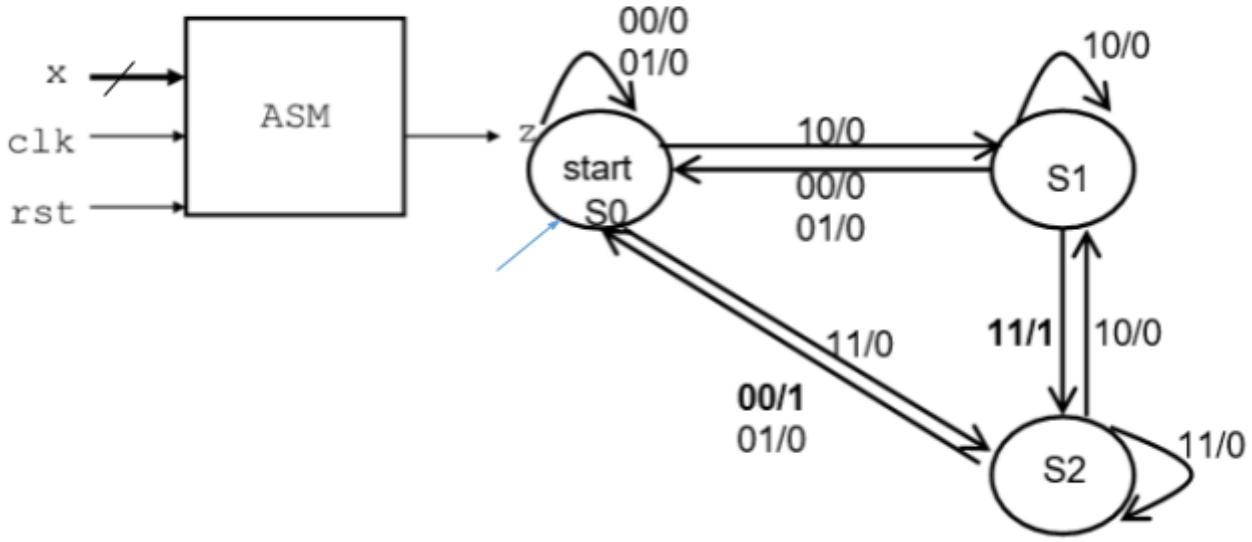
CME4456 Reconfigurable Computing – Homework 2

Due to: 14.04.2022

Write VHDL code (entity and architecture) for following State Machine. Using waveform show that state transitions and outputs are correct. Test your design with using Altera MuxPlus II or Quartus programme). X is an input port with two bits (X_1X_2), Z is an output port.

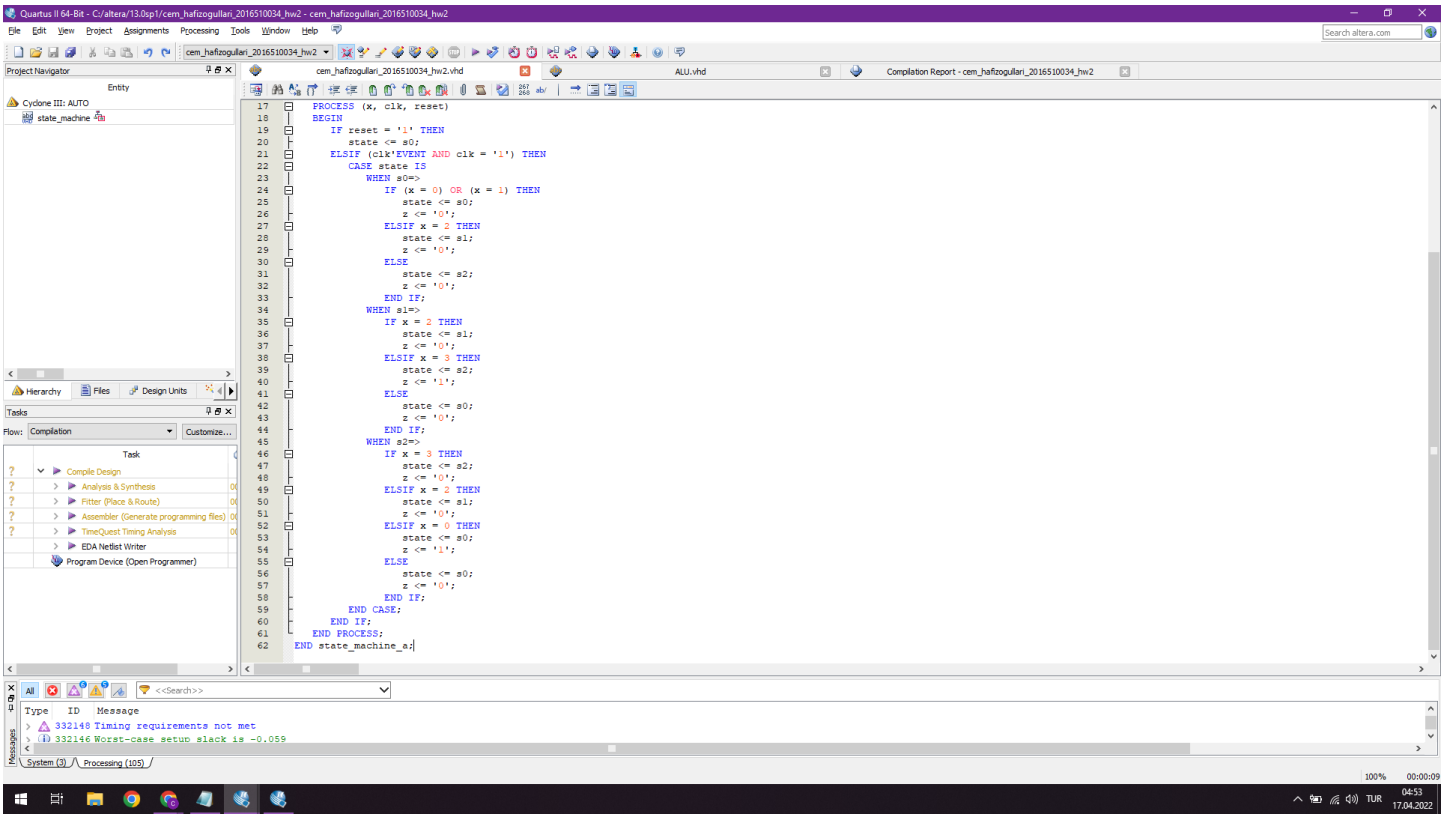



```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use ieee.numeric_std.all;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

ENTITY state_machine IS
  PORT(
    x : IN SIGNED(1 downto 0);
    clk, reset : IN STD_LOGIC;
                 z : OUT STD_LOGIC);
END state_machine;

ARCHITECTURE state_machine_a OF state_machine IS
  TYPE STATE_TYPE IS (s0, s1, s2);
  SIGNAL state : STATE_TYPE;
BEGIN
  PROCESS (x, clk, reset)
  BEGIN
    IF reset = '1' THEN
      state <= s0;
    ELSIF (clk'EVENT AND clk = '1') THEN
      CASE state IS
        WHEN s0=>
          IF (x = 0) OR (x = 1) THEN
            state <= s0;
                                                  z <= '0';
          ELSIF x = 2 THEN
            state <= s1;
                                                  z <= '0';
                                              ELSE
```

```
                                                    state <= s2;
                                                    z <= '0';
          END IF;
        WHEN s1=>
          IF x = 2 THEN
            state <= s1;
                                                    z <= '0';
          ELSIF x = 3 THEN
            state <= s2;
                                                    z <= '1';
                                                ELSE
                                                    state <= s0;
                                                    z <= '0';
          END IF;
        WHEN s2=>
          IF x = 3 THEN
            state <= s2;
                                                    z <= '0';
          ELSIF x = 2 THEN
            state <= s1;
                                                    z <= '0';
                                                ELSIF x = 0 THEN
                                                    state <= s0;
                                                    z <= '1';
                                                ELSE
                                                    state <= s0;
                                                    z <= '0';
          END IF;
      END CASE;
    END IF;
  END PROCESS;
END state_machine_a;
```


Quartus II 64-Bit - C:/altera/13.0sp1/cem_hafizogullari_2016510034_hw2 - cem_hafizogullari_2016510034_hw2
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Entity
Cyclone III: AUTO
state_machine
cem_hafizogullari_2016510034_hw2.vhd
ALU.vhd
Compilation Report - cem_hafizogullari_2016510034_hw2
PROCESS (x, clk, reset)
BEGIN
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state <= s0;
ELSIF (clk'EVENT AND clk = '1') THEN
CASE state IS
WHEN s0=>
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state <= s0;
z <= '0';
ELSIF x = 2 THEN
state <= s1;
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state <= s2;
z <= '1';
ELSE
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z <= '0';
END IF;
WHEN s2=>
IF x = 3 THEN
state <= s2;
z <= '0';
ELSIF x = 2 THEN
state <= s1;
z <= '0';
ELSIF x = 0 THEN
state <= s0;
z <= '1';
ELSE
state <= s0;
z <= '0';
END IF;
END CASE;
END IF;
END PROCESS;
END state_machine_a;
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Type ID Message
332148 Timing requirements not met
332146 Worst-case setup slack is -0.059
System (3)
Processing (105)
100%
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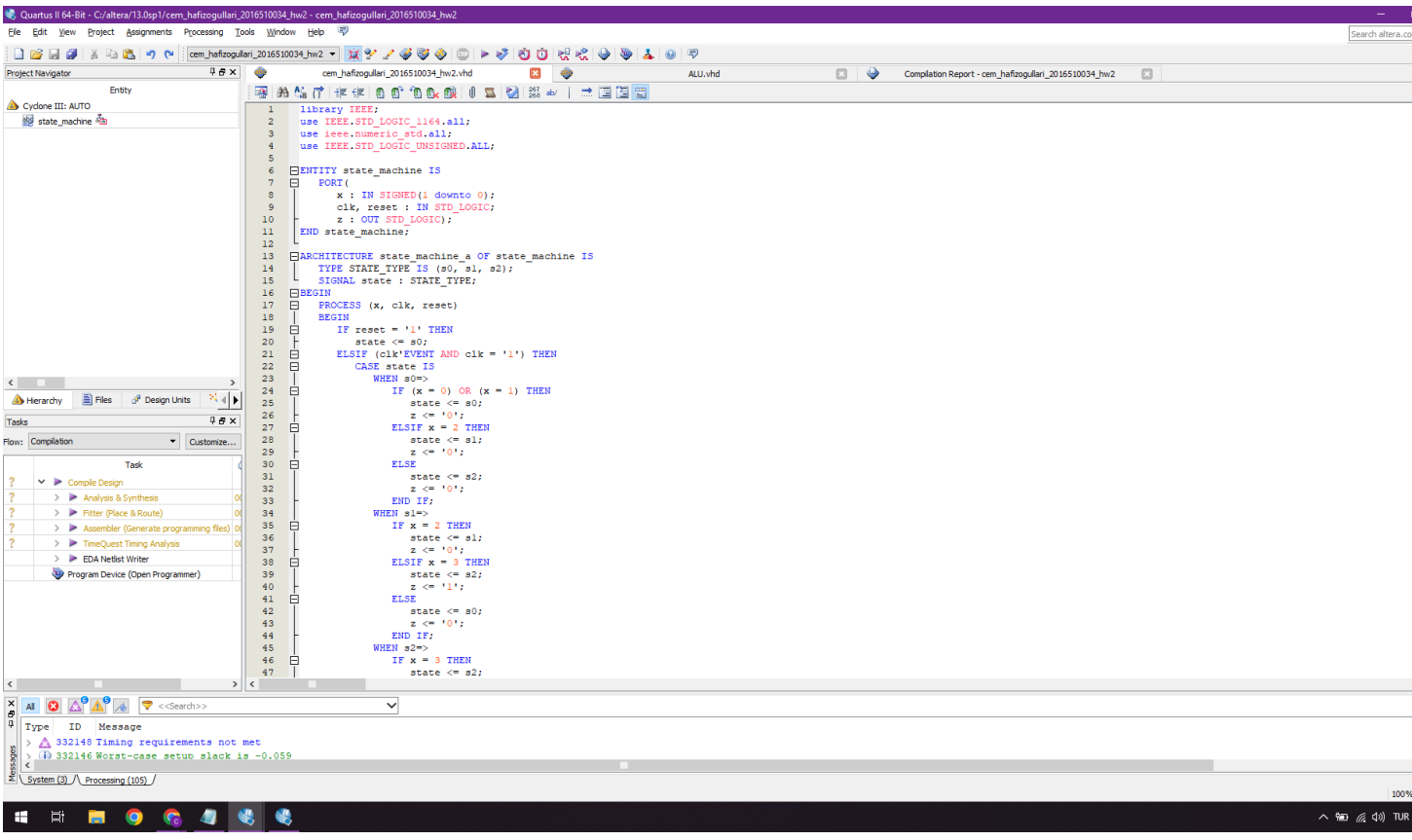
17.04.2022


Quartus II 64-Bit - C:/altera/13.0sp1/cem_hafizogullari_2016510034_hw2 - cem_hafizogullari_2016510034_hw2
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z <= '0';
ELSE
state <= s2;
z <= '0';
END IF;
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ELSIF x = 3 THEN
state <= s2;
z <= '1';
ELSE
state <= s0;
z <= '0';
END IF;
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IF x = 3 THEN
state <= s2;
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17.04.2022


Simulation Waveform Editor - [cem_hafizogullari_2016510034_hw2.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 5.63 ns
Interval: 5.63 ns
Start:
End:
Name
Value at 0 ps
clk
B 0
reset
B 0
x
B 00
z
B 0
0 ps
20.0 ns
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60.0 ns
80.0 ns
100.0 ns
120.0 ns
140.0 ns
160.0 ns
180.0 ns
200.0 ns
220.0 ns
240.0 ns
260.0 ns
280.0 ns
300.0 ns
320.0 ns
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400.0 ns
420.0 ns
440.0 ns
460.0 ns
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17.04.2022