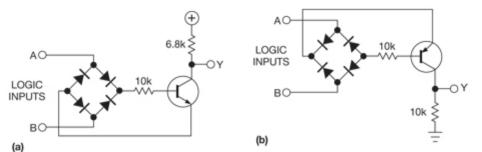
IMPORTANT: Besides your **calculator** and the sheets you use for calculations you are only allowed to have an A4 sized "copy sheet" during this exam. Notes, problems and alike are not permitted. **Please submit your "copy sheet" along with your solutions**. You may get your "copy sheet" back after your solutions have been graded. **Do not forget to write down units and convert units carefully! Cell phones are not allowed and should be placed on the front desk before the exam.**

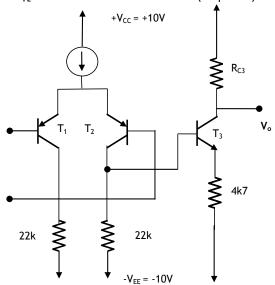
ELE222E INTRODUCTION TO ELECTRONICS (21071) Midterm Exam #1 25 March 2013 9.30-11.30 inci ÇİLESİZ, PhD, Hacer ATAR YILDIZ, MSE

- 1. You have a diode with the following doping properties: $N_D = 10^{18}$ /cm³, and $N_A = 10^{15}$ /cm³. Other important parameters to consider are $n_i = 1.5 \ 10^{10}$ /cm³, $q = 1.602 \ 10^{-19}$ C, $\epsilon_r = 12$, $\mu_n = 1600 \ cm^2$ /Vs, $\mu_p = 400 \ cm^2$ /Vs, $\epsilon_o = 8.85 \ 10^{-12}$ F/m, $\nu_T = 25 \ mV$. (35 points)
 - a. Find majority and minority carrier concentrations in n- and p-type doped silicon. (6 points)
 - b. Find the barrier voltage. (5 points)
 - c. Calculate the specific conductivities of n- and p-type doped silicon. (2x3 points)
 - d. Determine the depletion zone width. How large is the depletion zone in n- and p-typed doped silicon around the junction? (7 points)
 - e. What is the maximum value of the electrical field in unbiased state? (6 points)
 - f. Calculate the junction capacitance for a junction area of 1 mm². (5 points)
- 2. Look at the circuits below and complete look-up tables (like the one shown) for both (a) and (b). Assuming $| logic 0 \equiv low \ voltage$; such as $0 \ V$ and $| logic 1 \equiv high \ voltage$; such as $5 \ V$ Which logic functions do these circuits realize? You need to analyze states for A < B, A > B, and A = B with $V_D = 0.6 \ V$, $V_+ = 5 \ V$. (30 points)



A↓\B→	Logic 0	Logic 1
Logic 0		
Logic 1		

3. Study DC characteristics of the 2-stage BJT amplifier circuit shown on the right with $|\mathbf{V}_{BE}| = 0.6 \text{ V}$, and $\mathbf{h}_{FE} = 200 \text{ for all three transistors.}$ (35 points)



- a. Design a current source that will provide 0,4 mA biasing current to the differential stage. (10 points)
- b. Choose \mathbf{R}_{C3} such that \mathbf{V}_{o} = 0V. Do NOT neglect base currents. (25 points)

SOLUTIONS:

1. Using the given parameters

a.		
region	Majority carriers	Mainority carriers
n-type	$n_n = N_D = 10^{18} / cm^3$	$p_n = n_i^2/N_D = 225 / cm^3$
р-уре	$p_p = N_A = 10^{15} / cm^3$	$n_p = n_i^2/N_A = 2,25 \cdot 10^5/cm^3$
		·

b.
$$V_B = -V_T \cdot \ln \left(\frac{n_i^2}{N_A \cdot N_D} \right) = \underline{728mV}$$

c.
$$\sigma_n = q\mu_n N_D = 256 \Omega \cdot cm; \sigma_p = q\mu_p N_A = 0.06 \Omega \cdot cm$$

d. Since
$$x_n N_D = x_p N_A$$
 and $x_D N_A = 1000 \Rightarrow w \cong x_p$, that is $x_p N_A = 1000 \Rightarrow w \cong x_p$
$$w = \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_r \cdot V_B}{q}} \left[\frac{1}{N_D} + \frac{1}{N_A} \right] = \underbrace{0.98 \mu m}_{p} \Rightarrow x_p \cong \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} \Rightarrow x_n = \underbrace{x_p N_A}_{p} = \underbrace{0.98 \mu m}_{p} =$$

e. We need to find the electrical field at the junction
$$V_p(x) = \frac{q \cdot N_A}{2 \cdot \epsilon_o \cdot \epsilon_r} x^2 - \frac{q \cdot N_A}{\epsilon_o \cdot \epsilon_r} x_p \cdot x$$
. Thus,

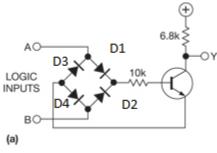
f.
$$C = \varepsilon_o \cdot \varepsilon_r \frac{A}{w} = \underline{130nF}$$

2. Lookup tables

A↓\B→	Logic 0	Logic1
Logic 0	1	0
Logic1	0	1

A↓\B→	Logic 0	Logic1
Logic 0	0	1
Logic1	1	0

It looks like (a) realizes an XNOR and (b) realizes an XOR functions. Let us see how this works:



LOGIC INPUTS D4 D2 10k S

With AB, 00, none of the diodes are conducting, thus, the transistor is obviously in cut off. With no collector current flowing Y = 5 V (logic 1)

Likewise with AB, 11.

With AB, 10, D1 and D4 are conducting, a base current flows. The collector is at a higher voltage than the base of the npn, thus collector current flows. The collector current initiates a voltage drop on 6k8 and $Y \rightarrow 0$ (logic 0)

With AB, 01, D2 and D3 are conducting a base current flows. The collector is at a higher voltage than the base of the npn, thus collector current flows. The collector current initiates a voltage drop on 6k8 and Y→0 (logic 0)

With AB, 00, none of the diodes are conducting, thus, the transistor is obviously in cut off. With no collector current flowing Y = 0 V (logic 0) Likewise with AB, 11.

With AB, 10, D3 and D2 are conducting, a base current flows. The collector is at a lower voltage than the base of the pnp, thus collector current flows. The collector current initiates a voltage drop on 10k and Y increases (logic 1)

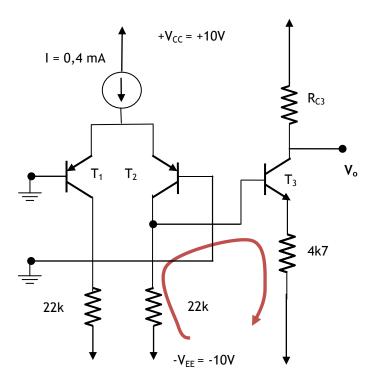
With AB, O1, D1 and D4 are conducting, a base current flows. The collector is at a lower voltage than the base of the pnp, thus collector current flows. The collector current initiates a voltage drop on 10k and Y increases (logic 1).

For more information look at http://jjackson.eng.ua.edu/courses/ece380/lectures/lect11-4.pdf

3. Exactly the same problem as in ELE222E INTRODUCTION TO ELECTRONICS (11245) Midterm Exam #2.... You can easily design the current mirror. So this part is left to you. Without neglecting the base currents of the differential (the very first) stage, for $V_i = 0 \text{ V}$

$$I_{C1} = I_{C2} = \frac{h_{FE}}{h_{FE} + 1} \cdot \frac{I_{ref}}{2} = \frac{200}{200 + 1} \cdot \frac{0.4mA}{2} \Rightarrow I_{C1} = I_{C2} = \underbrace{0.199mA}_{C1}$$

Following the brown loop shown in the sketch $-(I_{C2}-I_{B3})22k+V_{BE3}+(h_{FE}+1)I_{B3}4k7=0$



$$I_{C3} = h_{FE} \frac{22k * I_{C2} - V_{BE3}}{(h_{FE} + 1)4k7 + 22k} = 200 \frac{22k * 0,199mA - 0,6V}{(200 + 1)4k7 + 22k} = \underline{0,782mA}$$

$$V_o = 0V \Rightarrow I_{C3}R_{C3} = V_{CC} = 10V \Rightarrow R_{C3} = \frac{V_{CC} - V_o}{I_{C3}} = \frac{10V}{0.782mA} = 12k8$$