BLG322E HW3
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1)

T(ns)	50	40	50	40
CPU	FI 50 ns	DI 20 ns	FO 50 ns	EX 30 ns
DMAC		1 byte 40 ns		1 byte 40ns

1 CPU instruction, 2 bytes DMAC transfer

a. When T = 50+40 = 90 ns, DMAC transfers first byte. Since CPU needs bus in FI and FO phases and not DI and EX, DMAC takes bus while CPU operates DI and EX operations.

b. When T = 50+40+50+40 = 180 ns, CPU finishes first instruction. DI and EX operations take 40 ns because CPU needs to wait of transfers between I/O and Memory.

c. In this modified cycle above, 16 instructions and 32 byte DMAC transfers finishes when T = 16 * 180 ns = 2880 ns

d. 20 instruction = 16 instruction and 32 byte transfer + 4 normal instruction cycles.
T = 16*180 + 4*(50+20+50+30) = 2880 + 600 = 3480 ns

2)

T(ns)	50	20	50	30	150	800
CPU	FI	DI	FO	EX	Intr Prep	ISR

1 CPU instruction, 8 bytes DMAC transfer

a. For 32 byte DMA transfer, 4 cycles with interrupt required.
T = 4*(50+20+50+30+150+800) = 4400 ns

b. 20 instruction = 4 instruction and 32 byte transfer + 16 normal instruction cycles
T = 4*1100 + 16*(50+20+50+30) = 6800 ns