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EHB322E Digital Electronic Circuits
MIDTERM I

Duration: 120 Minutes

Grading: 1) 30%, 2) 30%, 2) 40%

Exam is in closed-notes and closed-books format; calculators are allowed

For your answers please use the space provided in the exam sheet

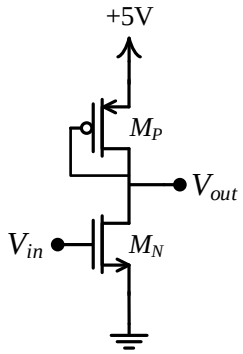
GOOD LUCK!

1) Consider a pseudo NMOS inverter shown below. Use the following equations for your calculations.

Saturation region current-voltage equation: $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} (V_{GS} - V_{T0\,p,n})^2$

Linear region current-voltage equation: $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} \left[2(V_{GS} - V_{T0\,p,n})V_{DS} - V_{DS}^2\right]$

Transistor parameters: $k_p' = \mu_p c_{ox} = 55\text{uA/V}^2$, $k_n' = \mu_n c_{ox} = 100\text{uA/V}^2$, $V_{TN}=1\text{V}$, $V_{TP}=-1\text{V}$, $W_N=12\text{u}$, $L_P=1\text{u}$, $L_N=1\text{u}$.



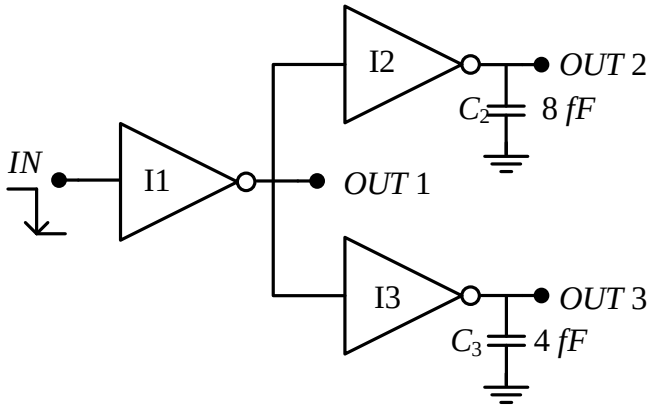
Pseudo NMOS Inverter

a) Find the value of $\mathbf{W_P}$ if $\mathbf{V_{OL} = 0.25V}$.

b) Find the static power consumption of the inverter for $\boldsymbol{V_{in}}$**=0V** and $\boldsymbol{V_{in}}$**=5V**.

c) Derive an expression of the **output capacitor** in terms of C_{GS} and C_{GD} capacitors.

2) Consider a circuit with three CMOS inverters and three outputs shown below. A capacitor of 8*fF* is connected to the output-2; A capacitor of 4*fF* is connected to the output-3. A signal switching from high to low is applied to the input.
Transistor parameters: c_{ox}=1 fF/um2, $\tau_n = \tau_p$=1ps, W_{N1}=5u, W_{P2}=6u, W_{P3}=4u, $L_{N1}=L_{P1}=L_{N2}=L_{P2}=L_{N3}=L_{P3}$=1u.



Digital circuit with three CMOS inverters

Propagation delays of an inverter are formulized as follows. C_L represents the load capacitor of the inverter. Neglect C_{GD} capacitors in your calculations.

$t_{PHL} = (C_L/C_N)\,\tau_n$ $\quad C_N = c_{ox} W_N L_N$

$t_{PLH} = (C_L/C_P)\,\tau_p$ $\quad C_P = c_{ox} W_P L_P$

If **the total propagation delay** is 2ps at output-1, 4ps at output-2, and 4ps at output-3,

a) Find the value of $\mathbf{W_{N2}}$ and $\mathbf{W_{N3}}$.

b) Find the value of $\mathbf{W_{P1}}$.

3) For a specific technology and a specific supply voltage, a CMOS inverter with parameters W_P=1u, W_N=1u, L_P=1u, L_N=1u, and a load capacitor of 1 *fF* has t_{PHL} =1ns and t_{PLH} =2ns. Considering the same technology and the supply voltage,

a) Implement $f = x_1(x_2+x_3) + \bar{x}_1 x_4$ with a **CMOS circuit**. How many PMOS and NMOS transistors do you use?

b) Select W_P=4u for all PMOS transistors and W_N=2u for all NMOS transistors of your CMOS circuit. Find the **worst case (largest)** t_{PHL} **and** t_{PLH} values if a load capacitor of 2 *fF* is connected to the output.

c) Select W_P=4u for all PMOS transistors and W_N=2u for all NMOS transistors of your CMOS circuit. Find the **best case (smallest)** t_{PHL} **and** t_{PLH} values if a load capacitor of 2 *fF* is connected to the output.