# ELE 222E INTRODUCTION TO ELECTRONICS (21604)
## Midterm Exam #2 ✐ 16 April 2003 🕙 10.00-12.00
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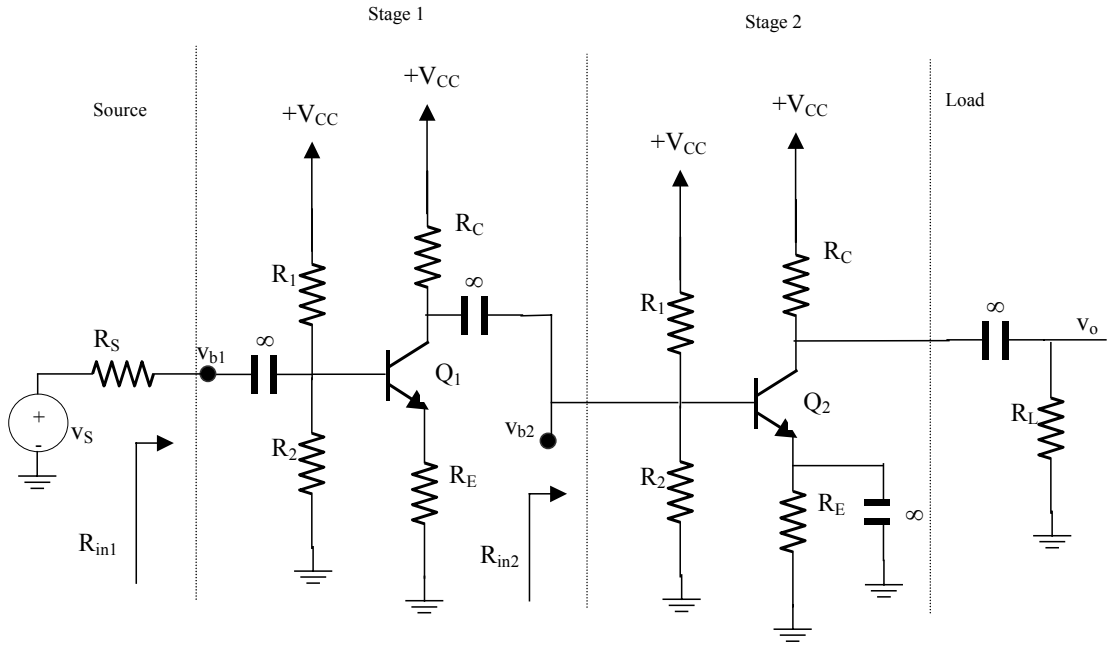
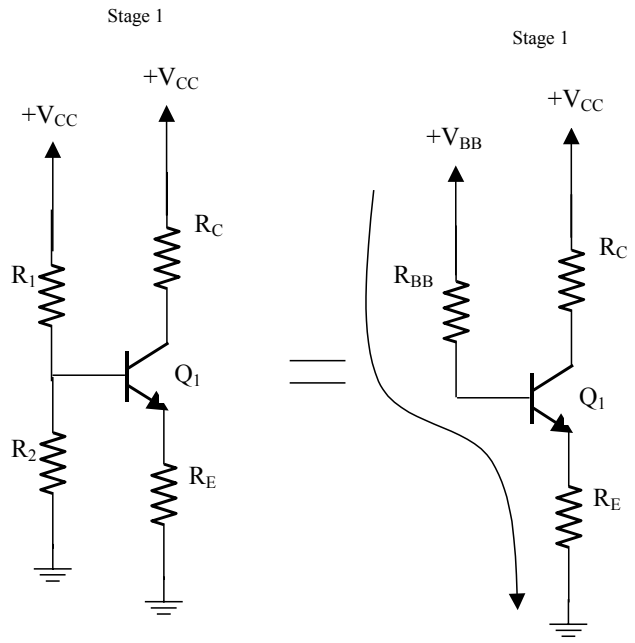
## SOLUTIONS

1. The amplifier shown below consists of two identical common-emitter amplifiers connected in cascade. Recall, that the input resistance of the second stage, $R_{in2}$, constitutes the load resistance of the first stage.




a. For $V_{CC}$ = 15 V, $R_1$ = 100k, $R_2$ = 47k, $R_E$ = 3k9, $R_C$ = 6k8 and $h_{FE}$ = 100, find the DC collector currents and DC collector voltages of each transistor. (10 points)




Both stages can be simplified for DC analysis as we did in class. In the equivalent circuit shown

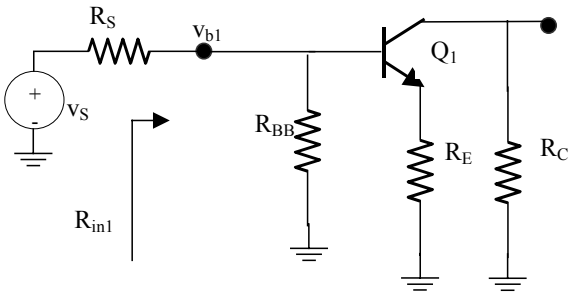
$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC}$$ and

$R_{BB} = R_1 \,||\, R_2$. With the values given, $R_{BB}$ = 32k and $V_{BB}$ = 4,8 V for both stages. Using the stretch from $+V_{BB}$ to ground, for the first stage

$$V_{BB1} - R_{BB1} I_{B1} - V_{BE1} - R_E I_{B1} (h_{FE1} + 1) = 0$$

$I_{C1} = h_{FE1}\dfrac{V_{BB1} - V_{BE1}}{R_{BB} + (1 + h_{FE1})R_E} = 100\dfrac{4{,}8V - 0{,}6V}{32k + 101 \cdot 3k9} \cong 1mA$. Note that, the second stage is identical for DC biasing conditions. Thus $I_{C1} = I_{C2} = I_C \cong 1mA$ and also $V_{C1} = V_{C2} = V_{CC} - R_C I_C = 8{,}2V$ and $r_{e1} = r_{e2} = \dfrac{V_T}{I_C} = 25\Omega$.

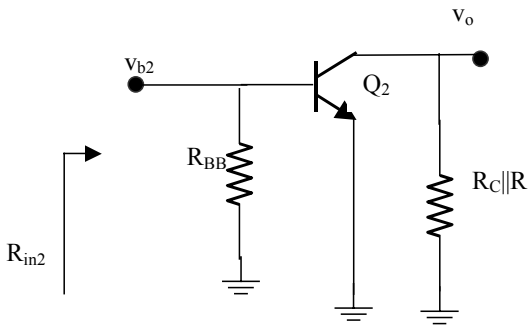
b. Find $R_{in1}$ and $v_{b1}/v_s$ for $R_s$ = 5k. (5 points)




When a small (AC) signal is applied, all capacitors are shorted as seen on the left. We see that $R_{in1} = R_{BB} \,||\, r_{i1}$ where $r_{i1} = h_{fe}(r_{e1} + R_E) = 392{,}5k$ for common emitter amp $\rightarrow R_{in1} = 29k6$.

$\dfrac{v_{b1}}{v_s} = \dfrac{R_{in1}}{R_{in1} + R_S} = 0{,}86 < 1$, high as preferred!

c. Find $R_{in2}$ and $v_{b2}/v_{b1}$. (10 points)




When a small (AC) signal is applied, the emitter is shorted to ground. We now see that $R_{in2} = R_{BB} \,||\, r_{i2}$ where $r_{i2} = h_{fe} r_{e2} = 2k5$ $\rightarrow R_{in2} = 2k3$. For common emitter amp:

$\dfrac{v_{b2}}{v_{b1}} = -\dfrac{R_C^{'}}{R_e + r_{e1}} = -\dfrac{R_{in2} \,||\, R_C}{R_E + r_{e1}} = -0{,}44$, or as expressed differently, $\left|\dfrac{v_{b2}}{v_{b1}}\right| = 0{,}44 < 1$, gain is less than 1, something you did not anticipate when you started working on this problem. Do you see the effect of the presence of the "AC resistor" in the emitter? Without it the gain of this first stage would have been $\dfrac{v_{b2}{}^*}{v_{b1}} = -\dfrac{R_C^{'}}{R_e + r_{e1}} = -\dfrac{R_{in2} \,||\, R_C}{r_{e1}} = -68{,}7$.

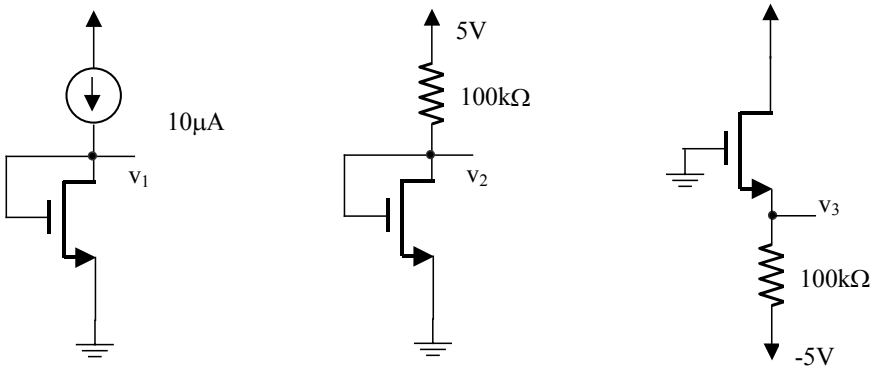
d. Find $v_o/v_{b2}$ for $R_L$ = 2k. (10 points)

For common emitter amplifier: $\dfrac{v_o}{v_{b2}} = -\dfrac{R_C^{'}}{R_e + r_{e2}} = -\dfrac{R_L \,||\, R_C}{r_{e2}} \cong -62$

e. Find the overall voltage gain $v_o/v_s$. (5 points)

$\dfrac{v_o}{v_S} = \dfrac{v_o}{v_{b2}} \cdot \dfrac{v_{b2}}{v_{b1}} \cdot \dfrac{v_{b1}}{v_S} = 0{,}86 \cdot (-0{,}44) \cdot (-62) = 23{,}46V/V$

2. For each of the circuits shown in (left), (middle), and (right) find the labeled node voltages. For all NMOS transistors $V_t$ = 2V, $\mu_n C_{ox}(W/L)$ = 0,5 mA/V², and λ = 0. (30 points)



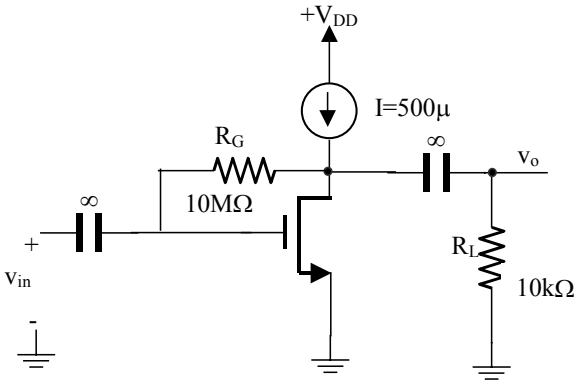

In the first two MOSFETs gate and drain are shorted, no current flows into the gate and the MOSFETs operate in saturation mode, $I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_t)^2$ with $V_{GS} = V_{DS} = V_D$. We also have to make sure that $V_{GS} - V_t = V_{DS} - V_t \geq 0 \Leftrightarrow V_D \geq V_t$.

Left: $10\mu A = 0{,}25mA/V^2(V_{DS} - 2V)^2$ → $V_{1.1} = V_{DS1}$ = 2,02 V; $V_{1.2} = V_{DS2}$ = 1,98 V. For $V_{GS} - V_t \geq 0$ to be valid, $V_1$ = 2,02 V.

Middle: $I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{DS} - 2V)^2$ and also $I_D = \frac{5V - V_{DS}}{100k}$. From combination of these two equations and substitution of $V_{DS}$ by $V_2$ we obtain the second order equation $25V_2^2 - 99V_2 + 95 = 0$. → $V_{2.1} = V_{DS1}$ = 2,33 V; $V_{2.2} = V_{DS2}$ = 1,63 V. Hereby, $V_{GS} - V_t \geq 0$ is no more valid for the second solution, thus $V_2$ = 2,33 V!

Right: This one is a bit complicated, because we cannot say for sure whether it operates in saturation. $V_G$ = 0, $V_{GS}$ = -$V_3$ and $I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(-V_3 - 2V)^2 = \frac{V_3 - (-5V)}{100k}$. Solution of the second order equation $25V_3^2 + 99V_3 + 95 = 0$ yields $V_{3.1}$ = -1,63 V; $V_{3.2}$ = -2,33 V. Using $V_{GS}$ = -$V_3$, $V_{GS1}$ = 1,63 V and $V_{GS2}$ = 2,33 V. For $V_{GS} - V_t \geq 0$ to be valid, i.e., for operation in saturation, $V_3$ = 2,33 V!

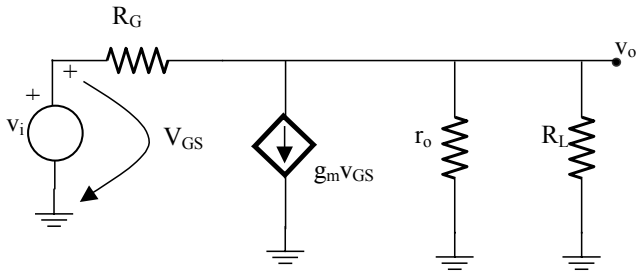
3. The NMOS transistor below has the following parameters, $|V_t|$ = 0,9 V, $V_A$ = 50 V and operates with $V_D$ = 2 V. What is the voltage gain $v_o/v_i$? What do $V_D$ and the gain become for I increased to 1 mA? (30 points)




IMPORTANT HINT: In this specific design, no current flows over $R_G$.

Since the DC gate current is zero, there will be no DC voltage drop across $R_G$, thus $V_{GS} = V_{DS} = V_D$. Substitution of the given values above and $\lambda = \frac{1}{V_A} = 0{,}02V^{-1}$ in $I_D = \frac{k_n'}{2}\frac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS}) = \frac{\beta}{2}(V_{DS}-V_t)^2(1+\lambda V_{DS})$ we obtain $\beta \cong 0{,}8mA/V^2$. Since channel length modulation effect, $(1+\lambda V_{DS}) = 1{,}04 \approx 1$, can be neglected, $g_m \approx \sqrt{2\beta I_D} = \sqrt{2\beta\frac{\beta}{2}(V_{DS}-V_t)^2} = \beta(V_{DS}-V_t) = 0{,}87mA/V$.

For small signals the equivalent circuit is:




Since $R_G$ is very large, the small signal current through $R_G$ is negligible as given in the HINT. The current though $R_G$ is negligible because it is much smaller than the controlled current source $g_m v_{GS}$. We find $r_o = \frac{V_A}{I_D} = 100k$

$v_o = -g_m v_{GS}(r_o \parallel R_L) = -g_m v_i(r_o \parallel R_L)$. Therefore, $\frac{v_o}{v_i} = -g_m(r_o \parallel R_L) = -7{,}9V/V$

Neglecting channel length modulation effect, $I_D = \frac{\beta}{2}(V_D - V_t)^2$. For $I_D$ = 500 µA, we find $V_D$ = 2,48 V and $r_o = \frac{V_A}{I_D} = 50k$ Therefore, $\frac{v_o}{v_i} = -g_m(r_o \parallel R_L) = -10{,}5V/V$