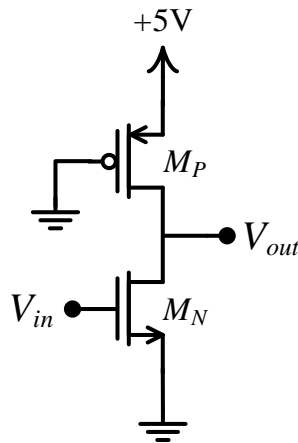# EHB322E Digital Electronic Circuits
Homework 1
Deadline: 17/03/2014 (before the lecture)

Consider the pseudo NMOS inverter shown below.

Pseudo NMOS Inverter

1. **CALCULATION:** Use the following parameters for your calculations. Neglect Early effect (V_A is infinite).
   Transistor parameters: $k_p'=\mu_p c_{ox}=50\text{uA/V}^2$, $k_n'=\mu_n c_{ox}=100\text{uA/V}^2$, $V_{TN}=1V$, $V_{TP}=-1V$, $W_P=1u$, $L_P=1u$, $L_N=1u$.

   a) Find the minimum value of $\mathbf{W_N}$ to satisfy that $V_{OL}<0.1V$.
   b) Suppose that a load capacitor of 10pF is connected to the output. Find the value of the propagation delay $\mathbf{t_{PLH}}$.
   c) Find the static power consumption of the inverter for $\boldsymbol{V_{in}=0V}$ and $\boldsymbol{V_{in}=5V}$.

2. **SIMULATION:** Construct the above circuit using SPICE. Connect body terminals of transistor to their source terminals. Select $W_P=1u$, $L_P=1u$, $L_N=1u$. Use T15DN and T15DP spice models for NMOS and PMOS transistors, respectively. For details of using LTspice check out the tutorial attached to the homework.

   a) Find the minimum value of $\mathbf{W_N}$ to satisfy that $V_{OL}<0.1V$.
   b) Sketch voltage transfer curve of the inverter; find noise margin values of $\mathbf{NM_L}$ and $\mathbf{NM_H}$; find the switching threshold value of $\mathbf{V_M}$.
   c) Suppose that a load capacitor of 10pF is connected to the output. Find the value of the propagation delay $\mathbf{t_{PLH}}$.

Grading: 1(a)20%, 1(b)15%, 1(c)15%, 2(a)15 %, 2(b)20, 2(c)15%

Note: *Do not forget to attach SPICE **output file** prints to your homework!*

**Mini LTspice Tutorial**

Model parameters for NMOS and PMOS transistors are given below.

```
.MODEL T15DN NMOS (                    LEVEL = 3
+ TOX   = 1.4E-8       NSUB  = 1E17        GAMMA = 0.5483559
+ PHI   = 0.7          VTO   = 0.7640855    DELTA = 3.0541177
+ UO    = 662.6984452   ETA   = 3.162045E-6   THETA = 0.1013999
+ KP    = 1.259355E-4   VMAX  = 1.442228E5    KAPPA = 0.3
+ RSH   = 7.513418E-3   NFS   = 1E12         TPG   = 1
+ XJ    = 3E-7          LD    = 1E-13        WD    = 2.334779E-7
+ CGDO  = 2.15E-10      CGSO  = 2.15E-10     CGBO  = 1E-10
+ CJ    = 4.258447E-4   PB    = 0.9140376    MJ    = 0.435903
+ CJSW  = 3.147465E-10  MJSW  = 0.1977689    )
*
.MODEL T15DP PMOS (                    LEVEL = 3
+ TOX   = 1.4E-8       NSUB  = 1E17        GAMMA = 0.6243261
+ PHI   = 0.7          VTO   = -0.9444911   DELTA = 0.1118368
+ UO    = 250          ETA   = 0           THETA = 0.1633973
+ KP    = 3.924644E-5   VMAX  = 1E6          KAPPA = 30.1015109
+ RSH   = 33.9672594    NFS   = 1E12         TPG   = -1
+ XJ    = 2E-7          LD    = 5E-13        WD    = 4.11531E-7
+ CGDO  = 2.34E-10      CGSO  = 2.34E-10     CGBO  = 1E-10
+ CJ    = 7.285722E-4   PB    = 0.96443      MJ    = 0.5
+ CJSW  = 2.955161E-10  MJSW  = 0.3184873    )
```

In order to use the parameter sets, shown above, in Ltspice, please follow these steps:

1- Create a .txt file named T15D_models.txt.

2- Copy parameters above and paste them into T15D_models.txt file.

3- Then place T15D_models.txt file into the LTspice folder.

4- After click on the .op tab as shown in figure below (circled red), write T15D_models.txt into the opened window. After pressing OK, you will see a rectangle information bar. Paste it somewhere in the schematic.
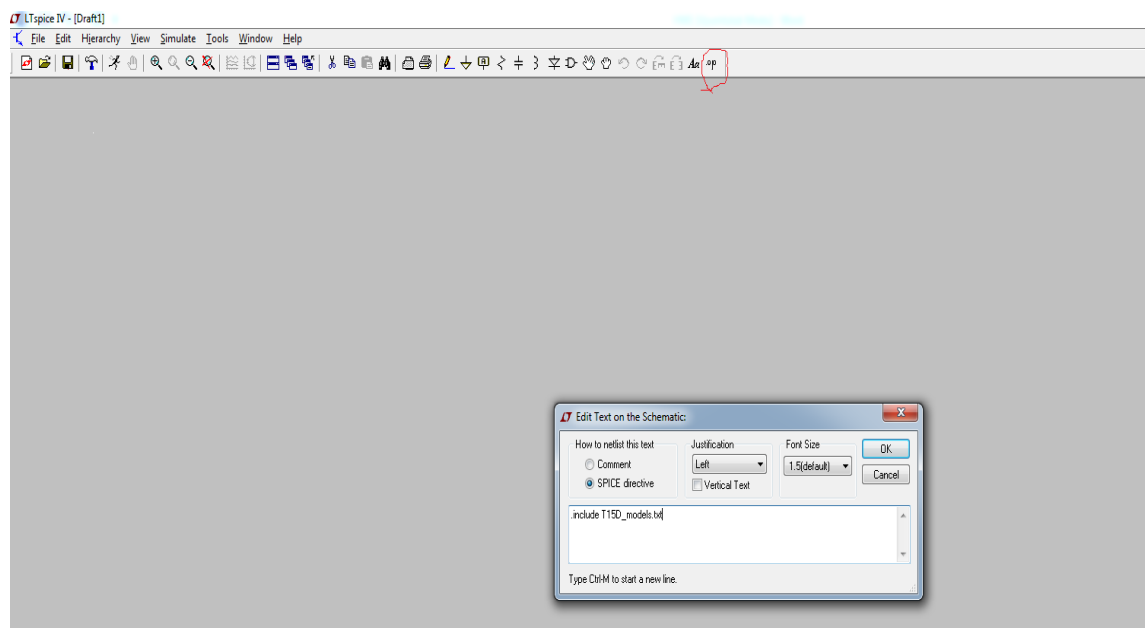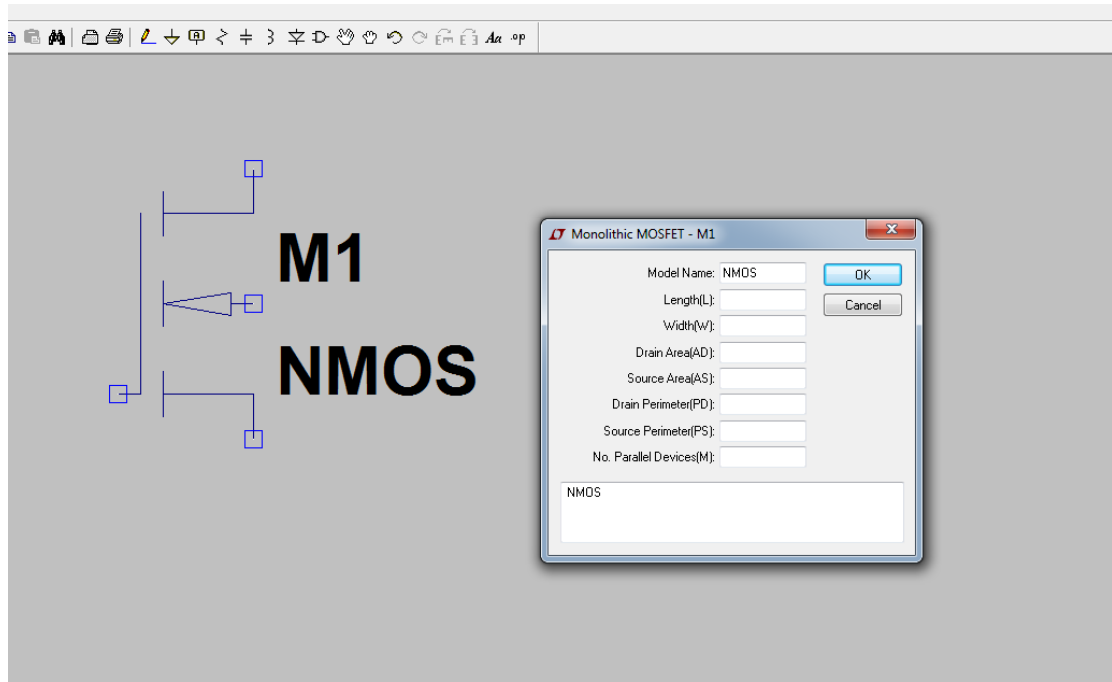
5- To add MOS transistors, click on the component tab shown below (circled red), then select NMOS4 and PMOS4.
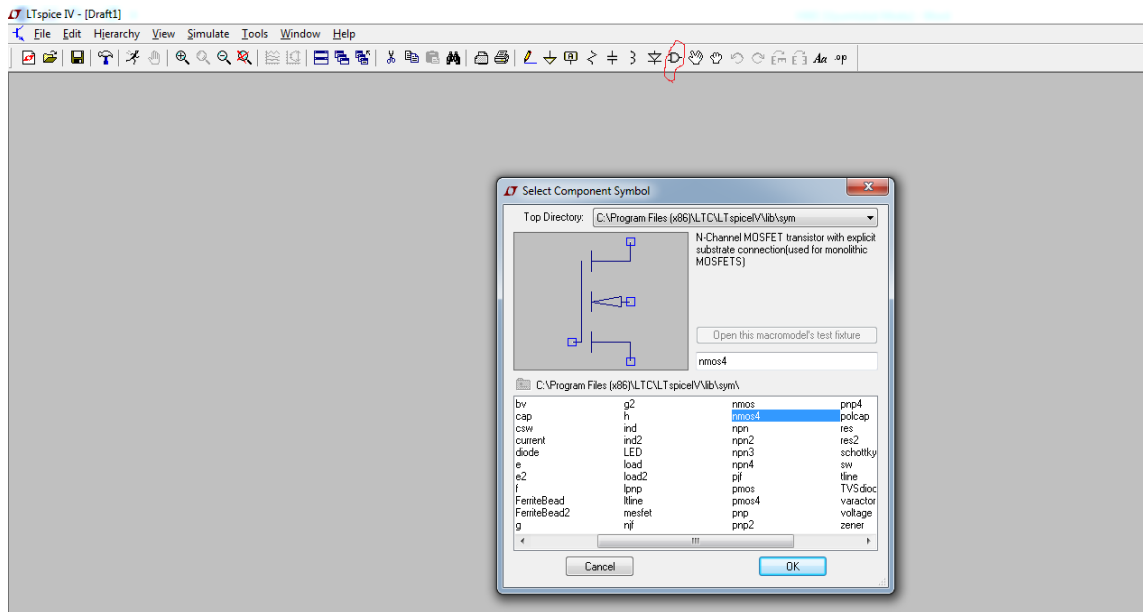
6- After selecting the transistor, right click on the transistor; name it as T15DN for NMOS and T15DP for PMOS.
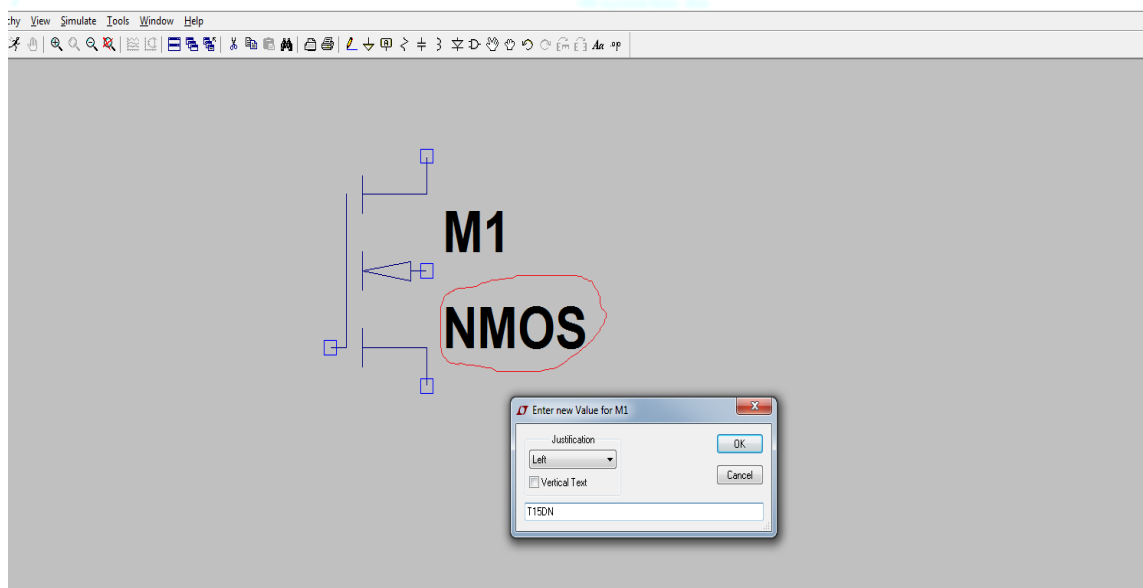
7- To enter W and L parameter values, right click on the transistor and write W and L values.

Note: Your simulation results can be slightly different from hand calculations because of probable mismatches between calculation and simulation parameters.