Number:
Name Surname:

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DIGITAL CIRCUITS 2nd MIDTERM EXAM (Question 1)

Regulations:
1. Duration is 100 minutes.
2. Asking questions to proctors is not allowed.
3. Any cheating or any attempt to cheat will be subject to the University disciplinary proceedings. Cell phones are prohibited on the desk, they must be switched off.

QUESTION 1 (30 Points):

a. Design and draw a **full adder** by using only 4:1 multiplexers and only one NOT gate.

b. Design and draw a **full adder** by using only one decoder of a proper size, and 2-input NAND gates. Use minimum number of 2-input NAND gates.

Solution:

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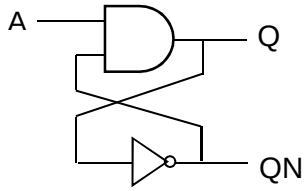
DIGITAL CIRCUITS 2nd MIDTERM EXAM (Question 2)

QUESTION 2 (30 Points):



a. Analyze the given circuit by giving different input values. Can this circuit be used as a memory unit? Explain?

b. Assume that you have a positive edge triggered T (toggle) Flip-flop. It is not possible to modify the internal structure of this flip-flop.

i) Connect necessary logic gates to a **T flip-flop** to obtain a positive edge triggered **D (Delay) flip-flop**. Use minimum number of logic gates.

iii) Connect necessary logic gates to a **T flip-flop** to obtain a positive edge triggered **T flip-flop** with an **enable input (EN)**. If EN=0 the flip-flop preserves its value, otherwise it operates normally.

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DIGITAL CIRCUITS 2nd MIDTERM EXAM (Question 3)

QUESTION 3 (40 Points):

a. Analyze the given clocked synchronous circuit with two inputs (A,B) and one output (Z) and construct the State/Output table. Draw the state diagram of the circuit.

b. Under the assumption that the circuit is in state Q1=1, Q0=0, draw the timing diagram that shows the values of Q1, Q0 and Z, when the input sequence is AB=01,00,00,11.