İ.T.Ü. Faculty of Computer and Informatics – Microprocessor Systems Midterm 2
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04.24.2012
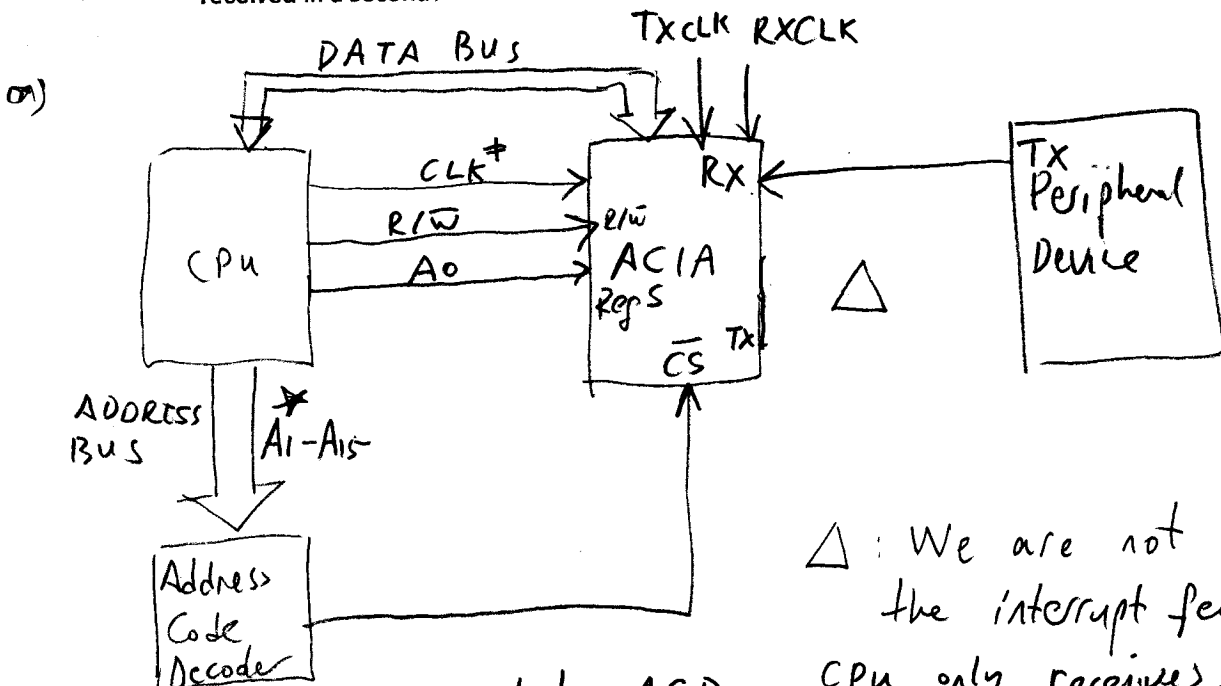Time: 120 mins.

Student #	Name	Signature

Q1	Q2
50 %	50 %

Do not use any reference other than the approved printouts.
Write your name on all answer sheets.
Good Luck

Q1) The EDU-CPU receives data from a peripheral device via the ACIA interface. The ACIA is connected to the CPU at the base address of $A0A0. The transmission rate is 19.2Kbps with data and receive clock running at the same rate (TX / RX clock ratio is 1/1). The data is in the form of 7-bit ASCII characters with an additional 8th bit as the even parity bit. The communication protocol uses one start bit, and one stop bit.

The CPU stores the received data on memory locations between $1000 and $12FF. In addition, the CPU checks the parity of the received characters and counts the number of parity errors for every 255 characters, and stores the number of parity errors at the C register. The error counter restarts after 255 characters are received.

20 pts a. Design and draw the hardware, clearly showing the CPU-ACIA connections at the receive side, and the connection to the transmitting ACIA. Indicate the peripheral device on the drawing.

20 pts b. Write the program for the receiver without using the interrupt features of the ACIA.

10 pts c. With this serial interface, what would be the maximum number of characters that can be received in a second?

a)

DATA BUS   TxCLK RXCLK

CPU — CLK* / R/W̄ / Ao → ACIA Regs, CS̄, RX, Tx

ADDRESS BUS / A1–A15

Address Code Decoder

Tx Peripheral Device

△ : We are not using the interrupt features and CPU only receives. ACIA TX, RDY, Data Valid need not be connected.

⚹ Notes: Ao is not an input to ACD
╪ CLK ≠ TXCLK ≠ RXCLK

b) ACIA : TX/RX address $A0A0 } R/W̄ determines which is selected!
: Status/control address $A0A1

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          YÜK   A    $20
          YAZ   A    $A0A1        : control register

          YÜK   SK   $1000

CLR       SIL   C                 : Counter for parity error
          SIL   D
REW       YÜK   A    $A0A1        : status register

          SIN   A    $01          : Did the ACIA receive data?

          DEE   REW
          ART   D
          DEE   CLR               : If D=0 after increment,
                                  : 255 characters have been received
                                    clear the counters

          SIN   A , $04           : Is there parity error?

          DEE   FWD

          ART   C                 : If Parity error, increase parity
                                    error counter.

FWD       YÜK   A    $A0A0

          YAZ   A    <SK+00> + 01

          KAR   SK   $1300        : Check if reached the
                                    end of allocated memory
          DEE   FINISH             for data?

          BRA   REW
```

FINISH   KES

c) 7 bit ASCII + 1 bit parity + 1 start bit + 1 stop bit
= 10 bits/character.
19.2kbps = 19200 bits per second
⟹ max. of 19200/10 = 1920 characters/second