IMPORTANT: Besides your calculator and the sheets you use for calculations you are only allowed to have an A4 sized "copy sheet" during this exam. Notes, problems and alike are not permitted. Please submit your "copy sheet" along with your solutions. You may get your "copy sheet" back after your solutions have been graded. **Do not forget to write down units!**

ELE222E INTRODUCTION TO ELECTRONICS (21618)
Midterm Exam #1 ✎ 21 March 2005 🕙 10.00-12.00
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1. What is a semi-conductor? What are similarities and differences between conductors and semi-conductors? Explain within a maximum of 4 to 5 sentences. (10 points)

2. Assume you are to create a diode using n- and p-typed doped silicon with the following possible doping parameters: N_D : 10^{15} 1/cm^3 , 10^{17} 1/cm^3 , and N_A : 10^{16} 1/cm^3 , 10^{18} 1/cm^3. Study the four possible pn junction combinations, find barrier voltages and saturation currents for let's say a junction area of 1 mm^2.

   a. Which unbiased pn junction (N_D = ?, N_A = ?) has the lowest barrier potential? Why? (10 points)

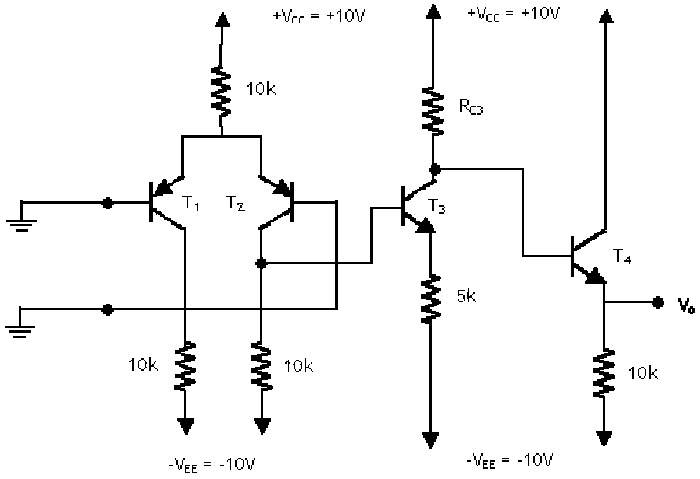
   b. Which unbiased pn junction (N_D = ?, N_A = ?) has the smallest saturation current? Why? (10 points)

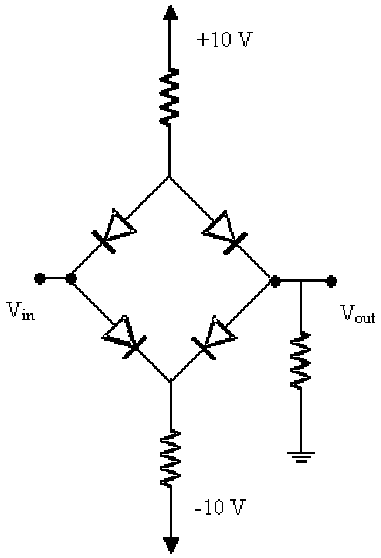
   c. Which unbiased pn junction (N_D = ?, N_A = ?) has the largest depletion capacitance? Why? (10 points)

   NOTE: L_n = 10 μm, L_p = 5 μm,
   μ_n = 1350 cm^2/Vs, μ_p = 480 cm^2/Vs.
   n_i = 1.5 10^{10} 1/cm^3,
   q = 1.602 10^{-19} C, ε_r = 12,
   ε_o = 8.85 10^{-12} F/m, V_T = 25 mV.

3. Study the 3-stage amplifier circuit on the right at DC. For h_{FE} = 100, V_T = 25 mV, $|V_{BE}|$ = 0,6 V,

   a. Find the collector currents of all 4 transistors and value of R_{c3} such that V_0 = 0V. (30 points)





   b. design a BJT based current mirror that will provide the current provided by the 10k resistor connected to the common emitters of the differential stage. (10 points)

4. For the circuit shown on the left sketch V_{out} as a function of V_{in} for V_{in}: -10 V to +10 V assuming all three resistors are 10k and the voltage drop across conducting diodes are constant at 0,6 V. (20 points)
   HINT: Analyze the circuit first at V_{in} = 0V; then at +10 V and –10 V, and finally at values in between.

GOOD LUCK!

SOLUTIONS TO PROBLEMS OF MIDTERM EXAM ON 21 MARCH 2005

1.

CONDUCTORS		SEMI-CONDUCTORS
Charged carriers conduct current.	**similarity**	Charged carriers conduct current.
Charged carriers are electrons ONLY.	**difference**	Charged carriers are electrons AND holes.
Electron density is ~ $10^{23}/cm^3$.	**difference**	Electron or hole density in intrinsic semiconductor silicon is about $10^{10}/cm^3$.
Electron density is the same all the time.	**difference**	Electron/hole density may be increased by doping the intrinsic semiconductor.
…	…	…

For more information consult your textbooks.

2. From Einstein Relation, $D_{p/n} = V_T \cdot \mu_{p/n}$, one can calculate $\mathbf{D_p}$ = 12 cm^2/s and $\mathbf{D_n}$ = 33.8 cm^2/s.

   Using the formulae $V_B = -V_T \cdot \ln\left(\frac{n_i^2}{N_A \cdot N_D}\right)$, $I_o = A \cdot q \cdot n_i^2 \cdot \left[\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right]$,

   $w = \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_r \cdot V_B}{q \cdot}\left[\frac{1}{N_A} + \frac{1}{N_D}\right]}$, and $C = \varepsilon_o \cdot \varepsilon_r \frac{A}{w}$, we cay say that

   a. The unbiased pn junction **A** has the lowest barrier potential because barrier potential is proportional to doping ratios, and junction **A** has the lowest doping ratios $\mathbf{N_D}$ and $\mathbf{N_A}$.

   b. The unbiased pn junction **D** has the smallest saturation current because saturation current is inversely proportional to doping ratios, and junction **D** has the highest doping ratios $\mathbf{N_D}$ and $\mathbf{N_A}$.

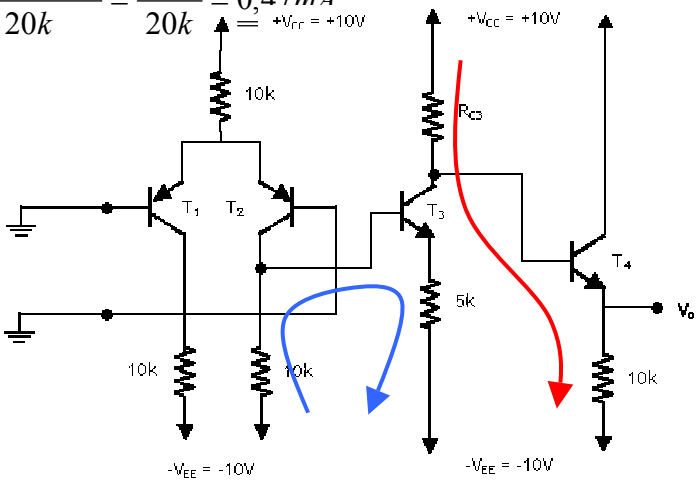
   c. The unbiased pn junction **D** has the largest depletion capacitance because it has the smallest depletion width which is inversely proportional to the sum of doping ratios $\mathbf{N_D}$ and $\mathbf{N_A}$.

   The table below shows it in figures:

	A	B	C	D
$\mathbf{N_D}$ [1/cm^3]	10^{15}	10^{15}	10^{17}	10^{17}
$\mathbf{N_A}$ [1/cm^3]	10^{16}	10^{18}	10^{16}	10^{18}
$\mathbf{V_B}$ [mV]	***613***	*728*	*728*	*843*
$\mathbf{I_o}$ [fA]	*987*	*866*	*2500*	***9,9***
$\mathbf{w_{depletion}}$ [nm]	*945*	*983*	*326*	*111*
$\mathbf{C_{depletion}}$ [pF]	*112*	*108*	*326*	***958***

3. The first stage of the 3-stage amplifier is a differential stage. Since both transistors are ideal, their collector currents are the same and equal to

$$I_{C1} = I_{C2} = \frac{V_{CC} - V_{EB1}}{2R_E} = \frac{10V + V_{BE1}}{20k} = \frac{10V - 0{,}6V}{20k} = \frac{9{,}4V}{20k} = 0{,}47mA$$



Now, following the blue loop

$$-(I_{C2} - I_{B3})10k + V_{BE3} + (h_{FE} + 1)I_{B3}5k = 0$$

$$I_{C3} = h_{FE}\frac{10k * I_{C2} - V_{BE3}}{(h_{FE} + 1)5k + 10k} = \underline{\underline{0{,}8mA}}$$

We are told that V_0 = 0V. Thus

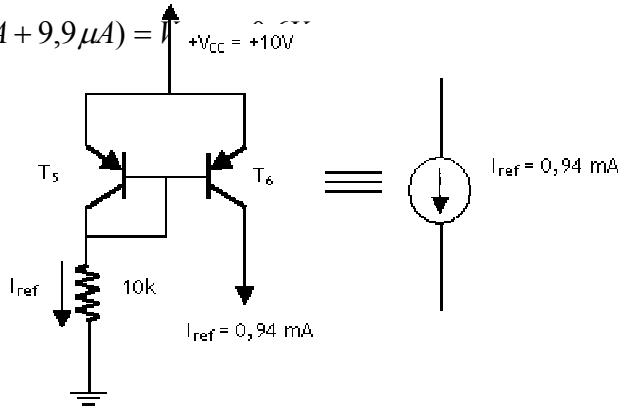
$$I_{E4} = \frac{0V - (-V_{EE})}{10k} \text{ or}$$

$$(h_{FE4} + 1)I_{B4}10k = 10V$$

$$\Rightarrow I_{C4} = h_{FE4}I_{B4} = \underline{\underline{0{,}99mA}}$$

Also,

$$V_{B4} = +V_{CC} - R_{C3} * (I_{C3} + I_{B4}) = +10V - R_{C3} * (0{,}91mA + 9{,}9\mu A) =$$



Therefore, $R_{C3} = \frac{10V - 0{,}6V}{0{,}8mA + 9{,}9\mu A} = \underline{\underline{11k6}}$

<u>BJT based current mirror design:</u>

$I_{ref} = 2I_{C1} = 2I_{C2}$ = 0,94 mA.

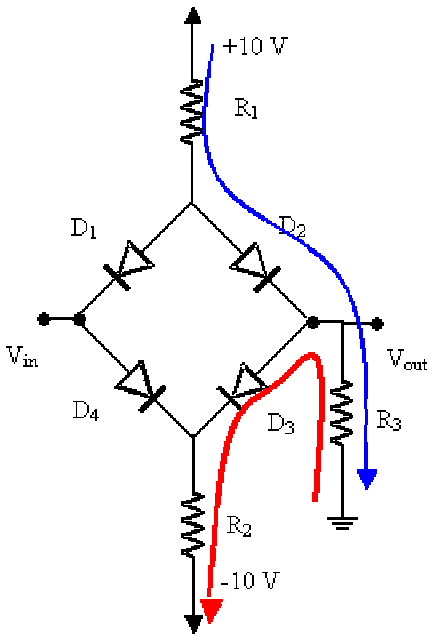
On the right is my design. NOTE that the collector of T_6 is connected to the common emitters of the differential stage. At DC $V_{E1} = V_{E2}$ = 0,6 V, that means, V_{C6} = 0,6 V. This voltage should keep T_6 in active mode! Does it?

V_{B6} = 9,4 V. For BC junction to be reverse biased,

$V_{C6} \leq V_{B6}$ - 0,6 V that is $V_{C6} \leq$ 8,8 V.

V_{C6} = 0,6 V < 8,8 V and THUS this condition is satisfied.

4. Assume there is no V_{in}. V_{out} = 0V because of the symmetry of the circuit, and because all diodes are conducting. This is the same as V_{in} = 0V.



Now assume V_{in} = 10V. We can easily see that D_1 and D_3 are reverse biased because most of the voltage drop from +10 V to -10 V is over the resistors R_1 and R_2. In other words, the anode of D_1 is much less than +10V whereas the cathode is at +10V (reverse bias). Also, D_4 is conducting, thus, the cathode of D_3 is at 9,4V wheras the anode of D_3 is much less than +9,4V. That means current flows (a) from +10V over R_1, D_2 , and R_3 to ground (**follow blue line**), and (b) from V_{in} over D_4 and R_4 to -10V. Since only 0,6V drops on the conducting diodes 9,4V drops over the two resistors R_1 and R_3. Since R_1 and R_3 have equal values, we divide the voltage drop by 2 and this

is V_{out} = 4.7V.

Now assume V_{in} = -10V. Similar to the observations above, D_4 and D_2 are reverse biased because most of the voltage drop from +10 V to –10 V is again over the resistors R_1 and R_2.
In other words, the cathode of D_4 is much higher than -10V whereas the anode is at -10V (reverse bias again). Also, D_1 is conducting, thus, the anode of D_2 is at -9,4V wheras the cathode of D_2 is much higher than -9,4V. That means current flows (a) from the ground over R_3, D_3 , and R_2 to –10V (**follow red line**), and (b) from +10V over R_1 and D_1 to V_{in}. Since only 0,6V drops on the conducting diodes 9,4V drops over the two resistors R_2 and R_3. Since R_2 and R_3 have equal values, we divide the voltage drop by 2 and this is V_{out} = 4.7V.

Finally, we need to consider the output for 0V ≥ V_{in} ≥ -10V and 0V ≤ V_{in} ≤ +10V. One sees easily that when all the 4 diodes are conducting, the output V_{out} follows the input V_{in} because the circuit is symmetrical. When do all the 4 diodes conduct? See the sketch below….Capito????