IMPORTANT: Besides your calculator and the sheets you use for calculations you are only allowed to have an A4 sized "copy sheet" during this exam. Notes, problems and alike are not permitted. Please submit your "copy sheet" along with your solutions. You may get your "copy sheet" back after your solutions have been graded. **Do not forget to write down units!**

ELE222E INTRODUCTION TO ELECTRONICS (20748)
Midterm Exam #1 ✐ 17 March 2008 🕙 10.00-12.00
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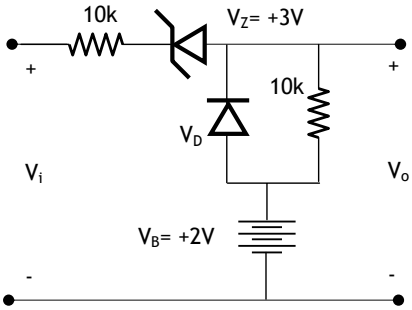
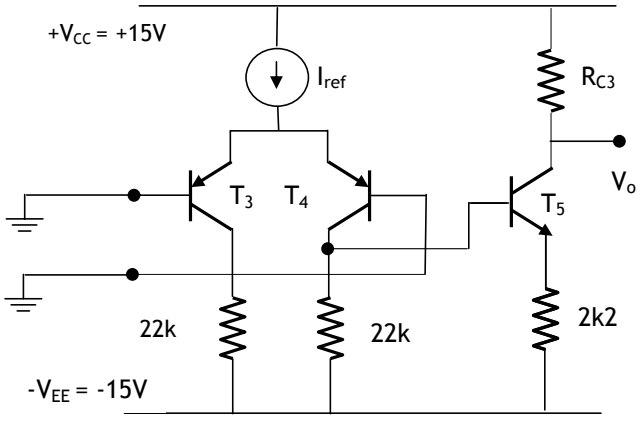
1. Assume you are to create a diode using n- and p-typed doped silicon with the following doping parameters: $N_D = 3\ 10^{17}$ /cm^3 , and $N_A = 10^{15}$ /cm^3.

   a. Find the barrier voltage and saturation current for a junction area of 0,1 mm^2. (7 points)
   b. Calculate the specific conductivities of n- and p-type doped silicon. (6 points)
   c. Determine the depletion zone width in unbiased state, when the junction is reverse biased at 3,5 V and when it is forward biased at 0,35 V. (6 points)
   d. Calculate the junction capacitances for the cases in (c). (6 points)

   $L_n = 10\ \mu m$, $L_p = 5\ \mu m$, $\mu_n = 1400$ cm^2/Vs, $\mu_p = 500$ cm^2/Vs.
   $n_i = 1.5\ 10^{10}$ 1/cm^3, $q = 1.602\ 10^{-19}$ C, $\varepsilon_r = 12$, $\varepsilon_o = 8.85\ 10^{-12}$ F/m,
   $V_T = 25$ mV.

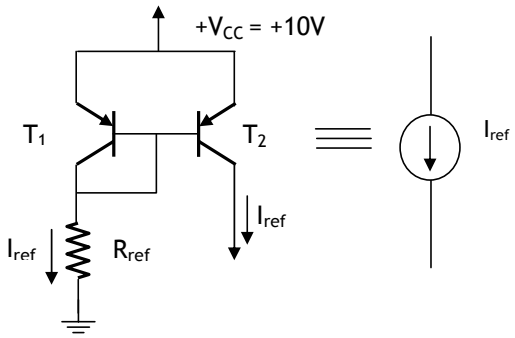
2. Consider the circuit on the right. Study and plot the output voltage V_o as a function of the input voltage V_i over the range -10V to +10V. You may assume the diodes are ideal, i.e., $V_D = 0$ V when they are forward biased. (25 points)





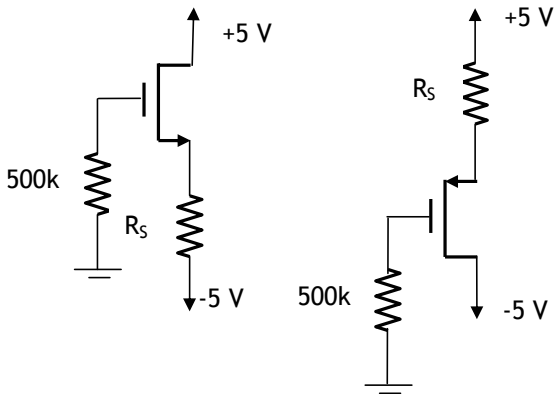
3. Study DC characteristics of the 3-stage BJT amplifier circuit on the left for $|V_{BE}| = 0{,}6$ V, $h_{FE} = 100$.

   a. Design a current source like that shown below that will provide 0,5 mA biasing current to the differential stage. (10 points)



   b. How should R_{C3} be chosen, such that, waveform distortion at the output V_o is minimum and symmetrical, i.e. $V_o = 0$V? (20 points)

4. The MOS transistors shown on the right have the following parameters:
   $|V_{th}| = 2$ V, $\mu_n C_{ox}(W/L) = \mu_p C_{ox}(W/L) = 2$ mA/V^2.
   Determine the source resistances, such that, when the MOS transistors are working in saturation $I_D = 1$ mA.
   (20 points)



GOOD LUCK!

SOLUTIONS:

1. Using Einstein Equation , i.e., $D_{p/n} = V_T \cdot \mu_{p/n}$, we find D_p = 12,5 cm^2/s and D_n = 35 cm^2/s.

   a. $V_B = V_T \cdot \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right)$ =698 mV; $I_o = A \cdot q \cdot n_i^2 \cdot \left[\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right]$ = 1,26 pA

   b. $\sigma_p = q \cdot \left(\frac{n_i^2}{N_A}\mu_n + N_A \mu_p\right) \cong qN_A\mu_p$ = 0,08 /(Ω cm)

   $\sigma_n = q \cdot \left(N_D \mu_n + \frac{n_i^2}{N_D}\mu_p\right) \cong qN_D\mu_n$ = 67,3 /(Ω cm)

   c. unbiased $w_{dep} = \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_r \cdot V_B}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)}$ =0,96 µm

   with reverse bias at 3,5 V, $w_{dep} = \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_r \cdot (V_B + V_{bias})}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)}$ = 2,36 µm

   with forward bias at 0,35 V, $w_{dep} = \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_r \cdot (V_B - V_{bias})}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)}$ = 0,68 µm

   d. Thus, $C = \varepsilon_o \cdot \varepsilon_r \frac{A}{w} = \begin{cases} 11{,}02\,pF, unbiased \\ 4{,}49\,pF, reverse@3{,}5V \\ 15{,}61pF, \ forward@0{,}35V \end{cases}$

2. The circuit has to be analyzed in three parts. The plot is placed at the bottom.

   a. **-10 V < V_{in} < 2 V**: Both the regular diode and the Zener diode are forward biased. As they are ideal, they effectively create electrical shorts. That is,

      i. The 10k resistor at the input is directly connected to the output and the 2V power supply.

      ii. V_o = 2 V

   b. **+5V < V_{in} < +10 V**: Both the regular diode and the Zener diode are reverse biased.

      i. the Zener diode is in the Zener zone and 3 V drops across it.

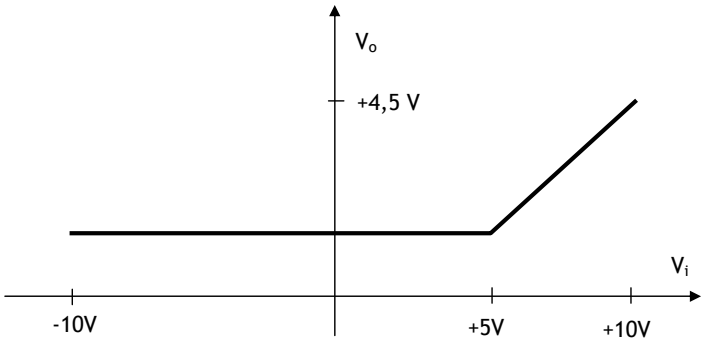
      ii. the regular diode is in cut off.

      iii. current flows over 10k resistor on the left, the Zener diode and 10k resistor on the right. Thus $I = \frac{V_i - V_Z - 2V}{20k}$

      iv. $V_o = 2V + 10k * I$. If this current changes linearly, then V_o changes linearly.

   c. **2 V < V_{in} < +5 V**: Both the regular diode and the Zener diode are reverse biased, yet, the Zener diode is not in Zener zone.

      i. no current flows over R_1, the Zener diode, the regular diode and R_2.
      V_o = 2 V



3. .

a. $R_{ref} = \dfrac{V_{CC} - V_{EB1}}{I_{ref}} = \dfrac{15V - 0{,}6V}{0{,}5mA} = \underline{\underline{28k8}}$ However, we also need to make sure that T_2 operates in the normal operating region, i.e., $V_{C2} < V_{B2}$. The current mirror is connected to the common emitters of T_1 and T_2. The emitter voltage of the differential stage is

$V_E = V_B + V_{EB} = 0 + 0{,}6\ V = 0{,}6\ V.$

On the other hand $V_{B2} = V_{CC} - V_{BE1} = 10v - 0{,}6\ V = 9{,}4\ V > 0{,}6\ V.$
This satisfies the condition $V_{C2} < V_{B2}$.

b. From the loop of 22k resistance connected to the collector of T_4, V_{BE5} and the 2k2 resistor:

$$-22k*(I_{C4} - I_{B5}) + V_{BE5} + 2k2*(1+h_{FE5})I_{B5} = 0 \quad I_{C4} = \frac{I_{ref}}{2}\cdot\frac{h_{FE}}{h_{FE}+1} = \underline{\underline{0{,}247mA}}$$

$$I_{C5} = h_{FE5}\frac{22k*I_{C4} - V_{BE5}}{(h_{FE5}+1)2k2 + 22k} = 100\frac{22k*0{,}25mA - 0{,}6V}{(100+1)2k2 + 22k} = \underline{\underline{1{,}98mA}}$$

Since $V_0 = +V_{CC} - R_{C3}*I_{C5} = 0V$ we find $R_{C3} = \underline{\underline{7k55}}$.

Hereby note we did NOT neglect the base currents of the differential stage because h_{FE} is only 100!

4. Let's first take the circuit with NMOS:

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[V_{GS} - V_{th}\right]^2 \Rightarrow V_{GS} = V_{th} \pm \sqrt{\frac{I_D}{\frac{\mu_n C_{ox}}{2}\frac{W}{L}}} = 2V \pm \sqrt{\frac{1mA}{1mA/V^2}} = \begin{cases} 3V \\ 1V \end{cases}$$

Since $V_{GS} \geq V_{th}$ for channel creation, $V_{GS} = \underline{\underline{3V}}$.

As $V_G = 0V \Rightarrow V_S = V_G - V_{GS} = -3V$ thus $R_S = \dfrac{V_S - (-5V)}{1mA} = \underline{\underline{2k}}$

Now the circuit with PMOS:

$$I_D = \frac{\mu_p C_{ox}}{2}\frac{W}{L}\left[V_{GS} - V_{th}\right]^2 \Rightarrow V_{GS} = V_{th} \pm \sqrt{\frac{I_D}{\frac{\mu_n C_{ox}}{2}\frac{W}{L}}} = -2V \pm \sqrt{\frac{1mA}{1mA/V^2}} = \begin{cases} -1V \\ -3V \end{cases}$$

Since $V_{GS} \leq V_{th}$ for channel creation, $V_{GS} = \underline{\underline{-3V}}$.

As $V_G = 0V \Rightarrow V_S = V_G - V_{GS} = +3V$ thus $R_S = \dfrac{+5V - 3V}{1mA} = \underline{\underline{2k}}$