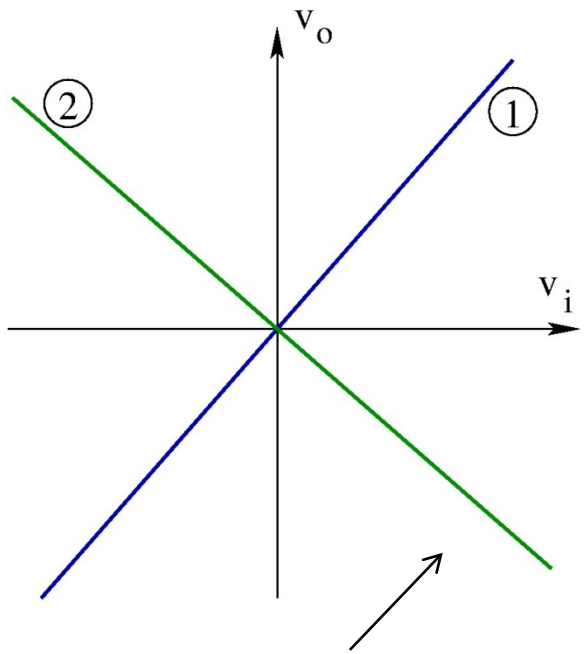
Introduction to Transistor Amplifiers: Concept & Biasing

Lecture notes: Sec. 5

Sedra & Smith (6th Ed): Sec. 5.4-5.4.6 & 6.3-6.4
Sedra & Smith (5th Ed): Sec. 4.4-4.4.6 & 5.3-5.4

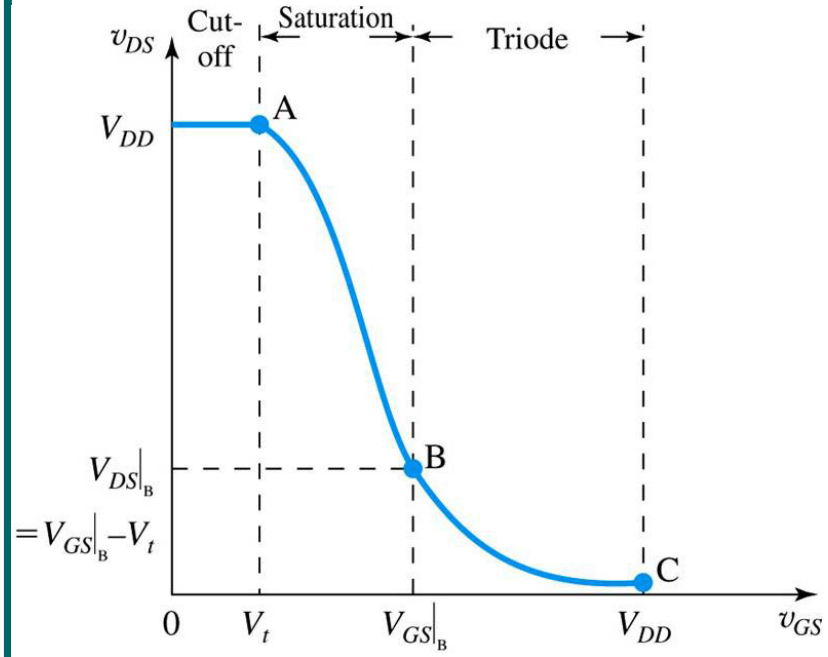
Foundation of Transistor Amplifiers (1)

- A voltage amplifier requires $v_o/v_i = \text{const.}$ (2 examples are shown below)



- v_o/v_i can be negative (minus sign represents a 180^o phase shift)

- MOS transfer function is NOT linear

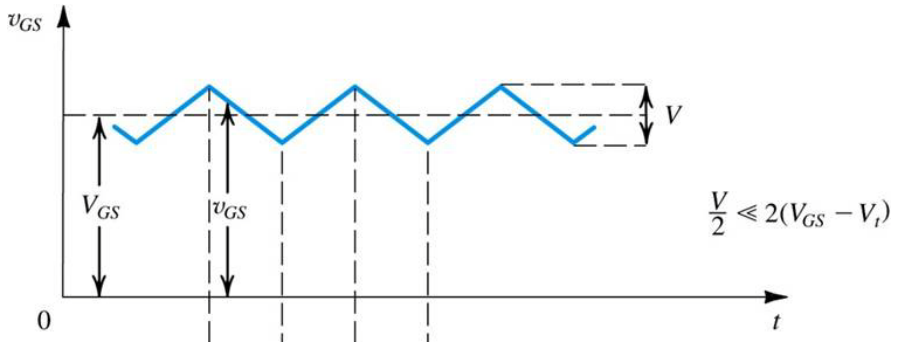


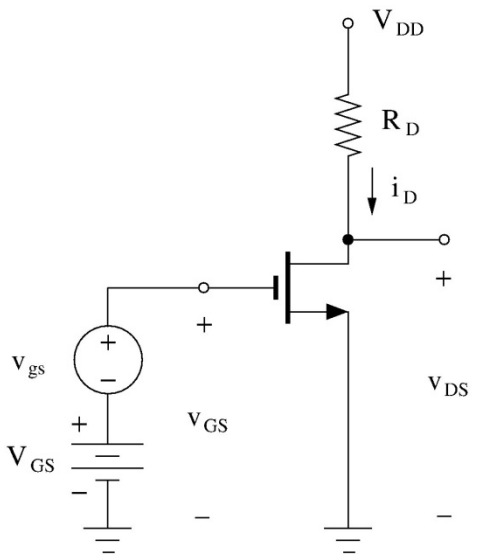
- In saturation, however, transfer function looks linear (but shifted)

Foundation of Transistor Amplifiers (2)

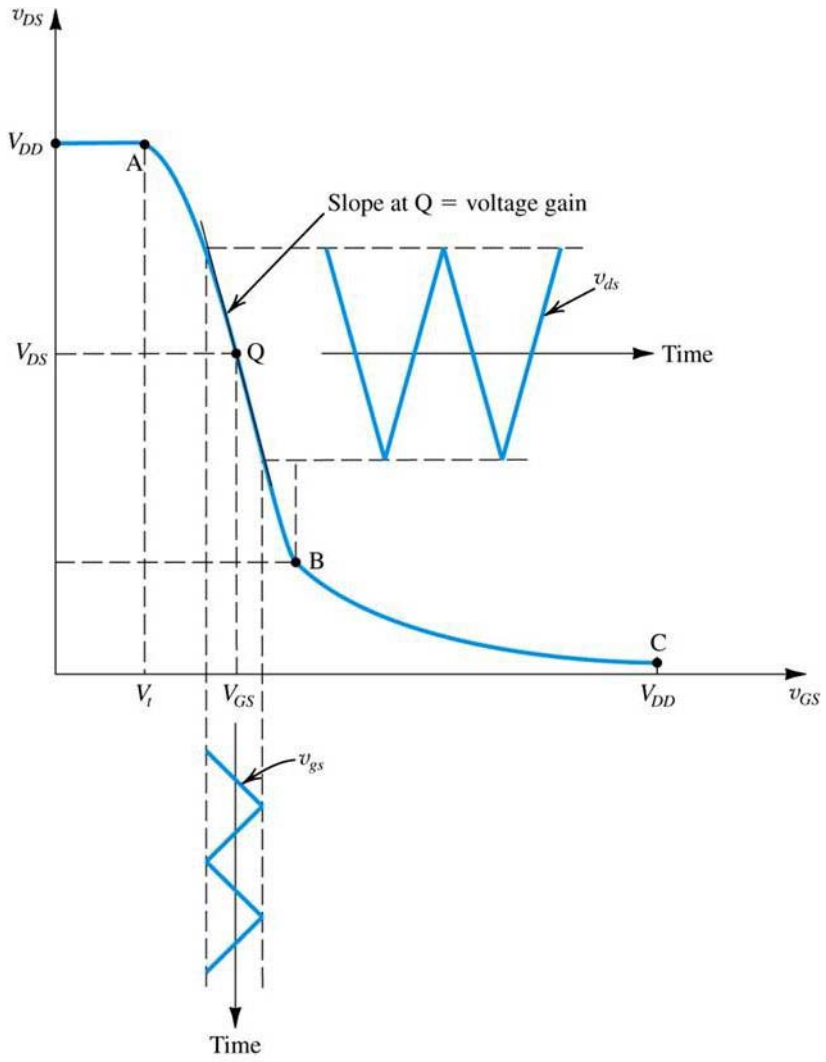
- Let us consider the response if NMOS remain in saturation at all times:
  - v_{GS} should be a combination of a constant value (V_{GS}) and a signal (v_{gs}).

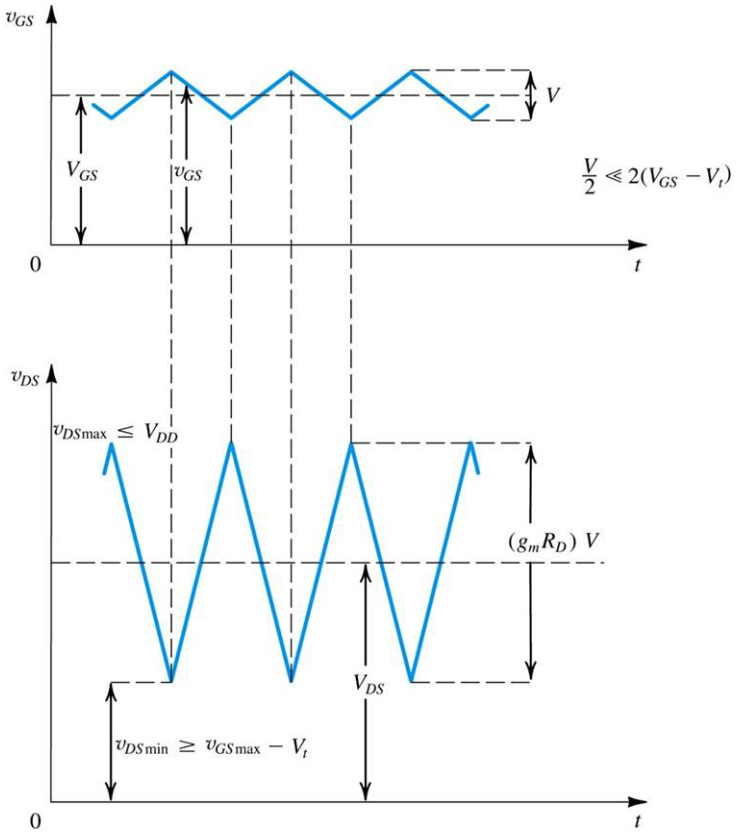
$$v_{GS} = V_{GS} + v_{gs}$$



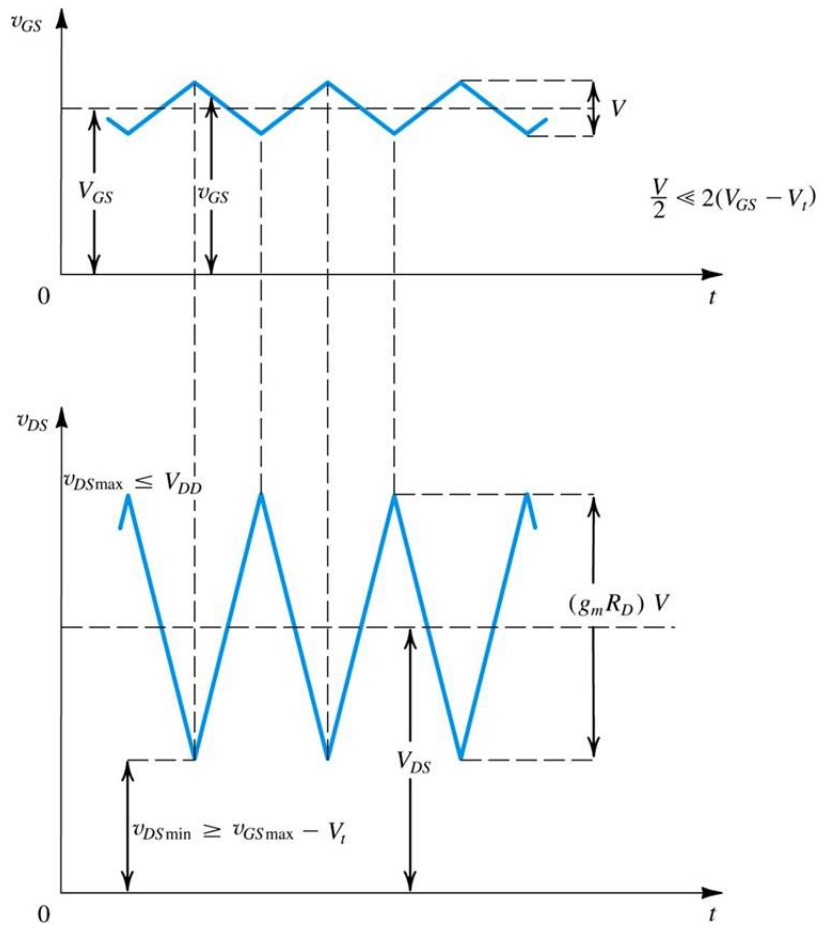


The response to a combination of $v_{GS} = V_{GS} + v_{gs}$ can be found from the transfer function





Response to the signal appears to be linear!



- Response ($v_o = v_{DS}$) is also made of a constant part (V_{DS}) and a signal response part (v_{ds}).
- Constant part of the response, V_{DS}, is ONLY related to V_{GS}, the constant part of the input (Q point on the transfer function of previous slide).
  - i.e., if $v_{gs} = 0$, then $v_{ds} = 0$
- The shape of the time varying portion of the response (v_{ds}) is similar to v_{gs}.
  - i.e., v_{ds} is proportional to the input signal, v_{gs}
- **While overall response is non-linear, response to the signal appears to be linear!**

Although the overall response is non-linear, the transfer function for the signal is linear!

Constant: Bias

Signal and response

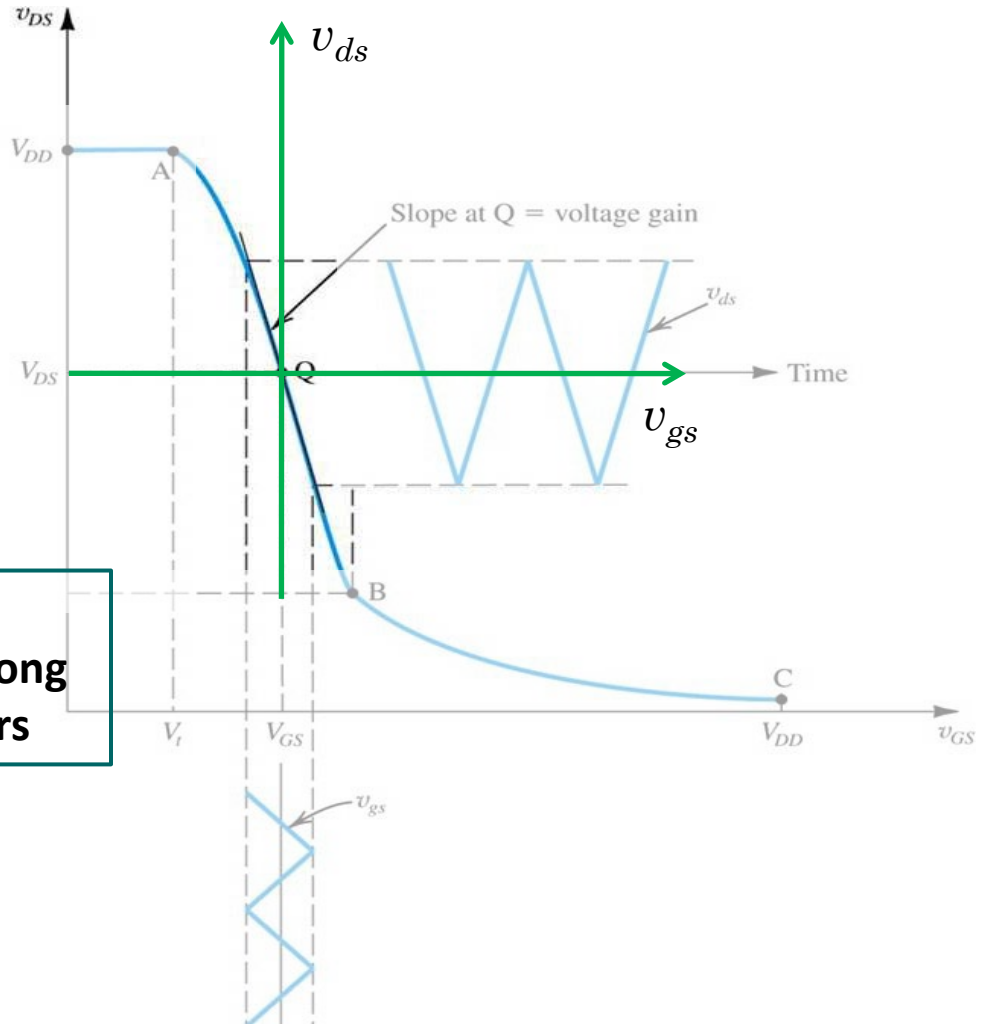
$$v_{GS} = V_{GS} + v_{gs}$$

$$v_{DS} = V_{DS} + v_{ds}$$

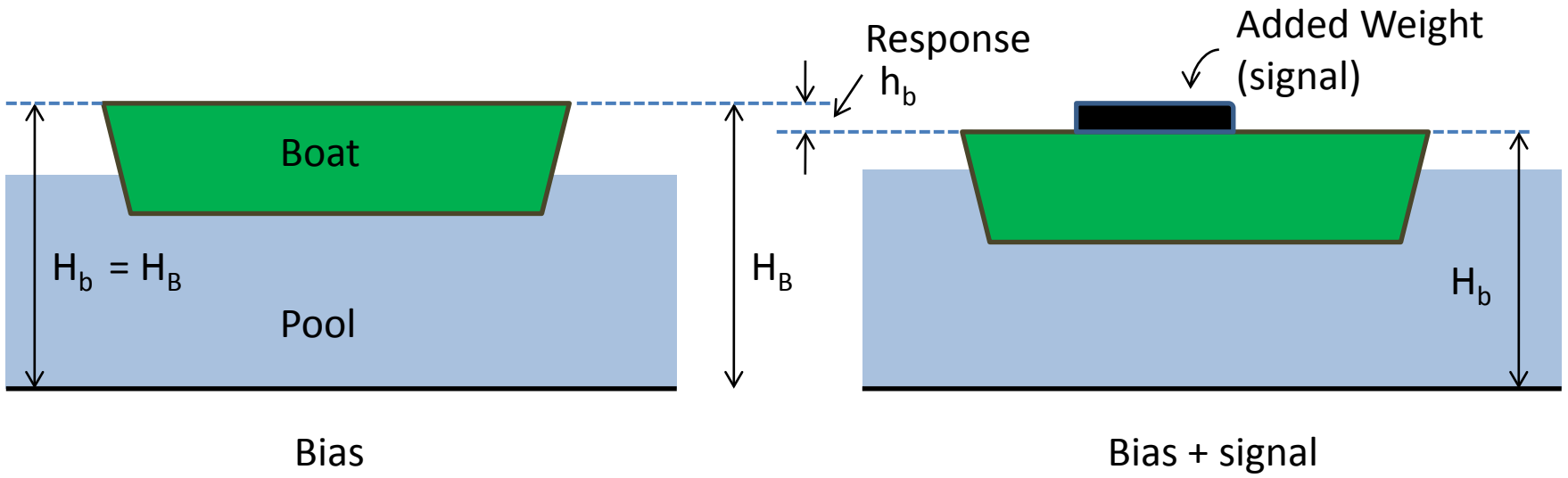
$$i_D = I_D + i_d$$

Non-linear relationship among these parameters

Linear relationship among these parameters

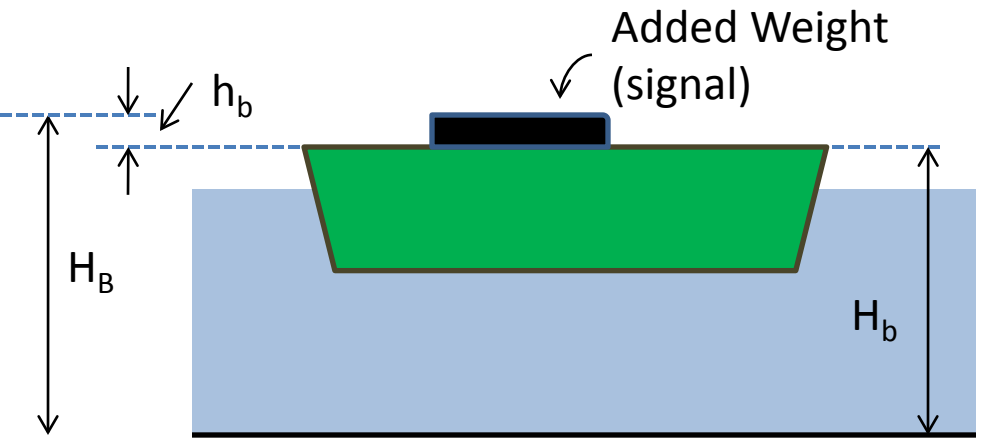


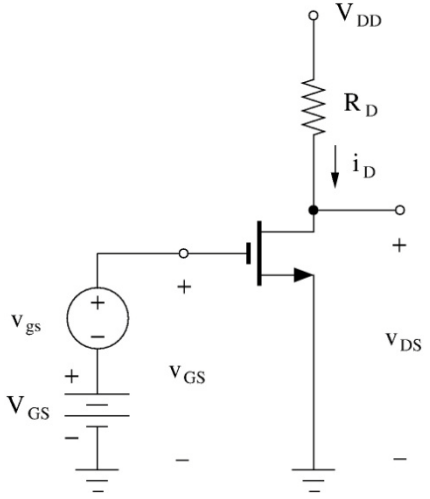
An Analogy: How much water is under the keel of a boat?



- Total Height, H_b = Bias (H_B) + response to the added weight (h_b)
- Complicated correlation between the total height, H_b , and the weight of the boat.
- Simple correlation between h_b and the added weight

An Analogy (2)





- Bias: zero added weight & H_B
- Bias + Signal: total weight & H_b
- Signal & response: added weight & h_b

- Bias: V_{GS} , V_{DS} , I_D
- Bias + Signal: v_{GS} , v_{DS} , i_D
- Signal & response: v_{gs} , v_{ds} , i_d

- Non-linear correlations among Bias + Signal: v_{GS} , v_{DS} , i_D
- Simple (and linear) correlation between signal and response to the signal: v_{gs} , v_{ds} , i_d

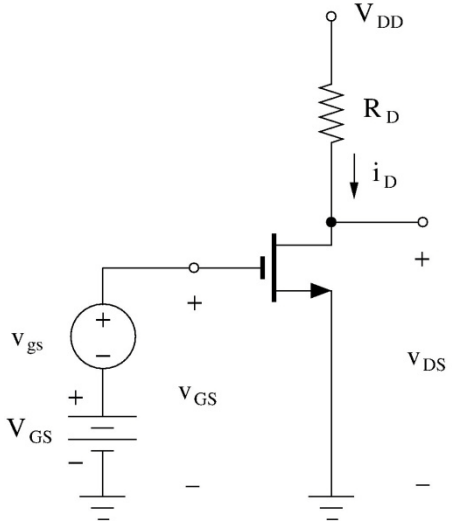
Important Observations!

- **Signal:** We want the response of the circuit to this input.
- **Bias:** State of the system when there is no signal (current and voltages in all elements).
  - Bias is constant in time (may vary very slowly compared to the signal)
  - Purpose of the bias is to ensure that MOS is in saturation at all times.
- **Response** of the circuit (and elements within) to the signal is different than the response of the circuit and its elements to Bias (or to Bias + signal):
  - Different transfer function for the circuit
  - Different iv characteristics for elements, i.e. relationships among v_{gs} , v_{ds} , i_d are different than relationships among v_{GS} , v_{DS} , i_D .

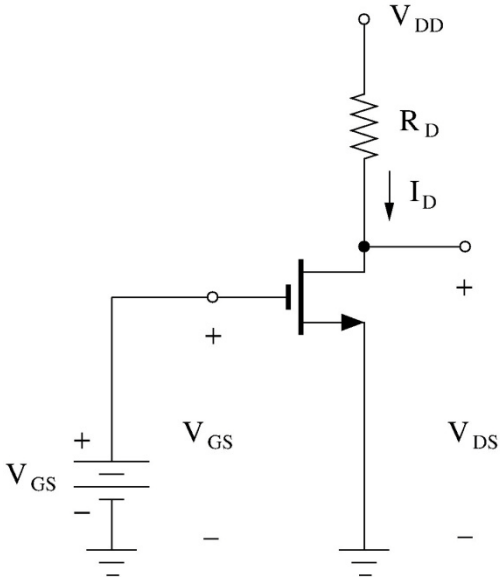
Above observations & conclusions equally apply to a BJT in the active mode!

Transistor Amplifier Development

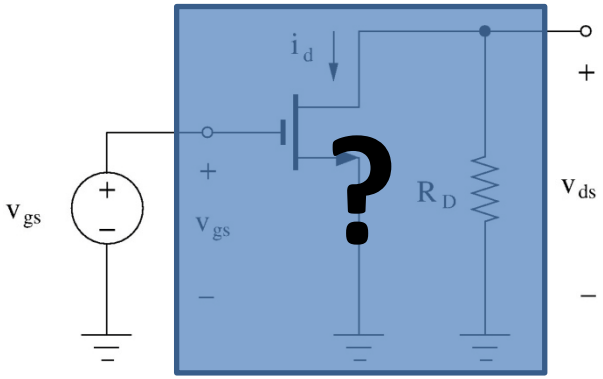
Bias & Signal



Bias



Signal only
= (Bias + Signal) - Bias



MOS : $v_{GS}, v_{DS}, i_D,$

$(v_{GS} = V_{GS} + v_{gs}, \ldots)$

R_D : $v_R = V_R + v_r$

$i_R = I_R + i_r$

.....

MOS : $V_{GS}, V_{DS}, I_D,$

R_D : V_R, I_R

.....

MOS : $v_{gs}, v_{ds}, i_d,$

R_D : v_r, i_r

.....

Issues in developing a transistor amplifier:

1. **Establish a Bias point** (bias is the state of the system when there is no signal).
   - Stable and robust bias point should be resilient to variations in β, $\mu_n C_{ox}(W/L), V_t$, … due to temperature and/or manufacturing variability.
2. **Find the iv characteristics of the elements for the signal** (which can be different than their characteristics equation for bias).
   - This will lead to different circuit configurations for bias versus signal: **Signal circuit**
3. **Compute circuit response to the signal & develop transistor amplifier circuits**

Transistor Biasing
(Bias is the state of the circuit when there is no signal)

1. **Purpose:** BJT should be in active (or MOS should in saturation) at all times.
   - Bias point impacts the small-signal parameters.
   - Bias point impacts how large a signal can be amplified
2. Bias point should be resilient to variations in β, $\mu_n C_{ox}(W/L)$, V_t , … due to temperature and/or manufacturing variability.

BJT biasing with Base Voltage (Fixed Bias)

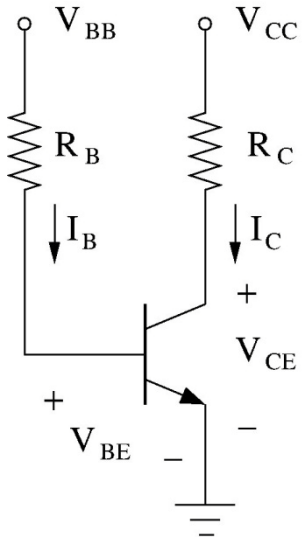
$$\text{BE}-\text{KVL}: \quad V_{BB} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{BB} - V_{D0}}{R_B}$$

$$I_C = \beta I_B = \beta \frac{V_{BB} - V_{D0}}{R_B}$$

$$\text{CE}-\text{KVL}: \quad V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - \frac{\beta R_C}{R_B}(V_{BB} - V_{D0})$$



* Typically $V_{BB} = V_{CC}$ in order to reduce the need for additional reference voltages.

Exercise 1: Find R_C and R_B such that BJT would be in active with $I_C =$ 25 mA, $V_{CE} = 5$ V. ($V_{CC} = 15$ V, Si BJT with $\beta = 100$ and $V_A = \infty$).

BJT is in Active since $I_C > 0$ and $V_{CE} = 5 \geq V_{D0} = 0.7$ V

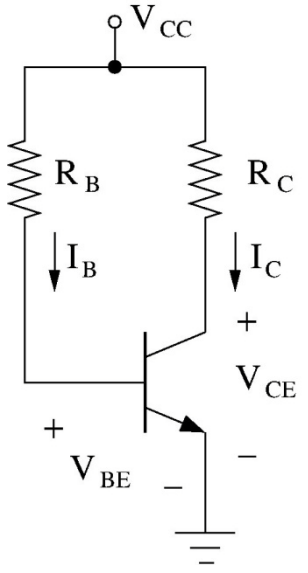
$$I_B = I_C / \beta = 0.25 \text{ mA}$$

$$\text{BE} - \text{KVL}: \quad 15 = I_B R_B + V_{BE} = 0.25 \times 10^{-3} R_B + 0.7$$

$$R_B = 57.2 \text{ k}$$

$$\text{CE} - \text{KVL}: \quad 15 = I_C R_C + V_{CE} = 25 \times 10^{-3} R_C + 5$$

$$R_C = 400 \ \Omega$$



Exercise 2: Consider the circuit designed in Exercise 1 ($R_C = 400$, R_B = 57.2 k, $V_{CC} = 15$ V). Find the operating point of BJT if $\beta = 200$.

Assume BJT is in Active:

$V_{BE} = 0.7\ \text{V},\ I_C > 0$ and $V_{CE} \geq 0.7\ \text{V}$

$$\text{BE}-\text{KVL}: \quad 15 = I_B R_B + V_{BE} = 57.2\times 10^3 I_B + 0.7$$

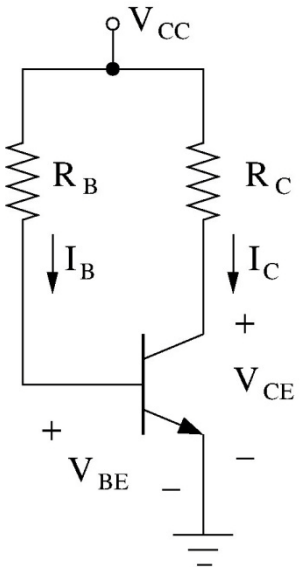
$$I_B = 0.25\ \text{mA}$$

$$I_C = \beta I_B = 50\ \text{mA}$$

$$\text{CE}-\text{KVL}: \quad 15 = I_C R_C + V_{CE} = 50\times 10^{-3}\times 400 + V_{CE}$$

$$V_{CE} = -5\ \text{V}$$

BJT in saturation!

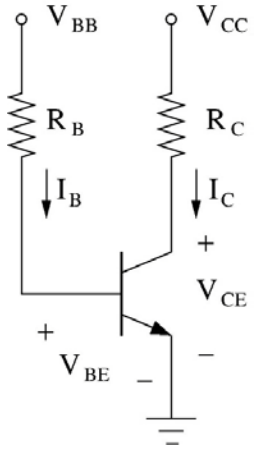


Note, compared to Exercise 1:

- I_B is the same.
- I_C increased.
- V_{CE} decreased.

Why biasing with base voltage (fixed bias) does not work?

- Changes in BJT β changes the bias point drastically.
  - BJT can end up in saturation or in cut-off easily.
- In fixed bias, I_B is set through $I_B = \dfrac{V_{BB} - V_{D0}}{R_B}$
- BJT β then sets $I_C = \beta I_B$ (I_C changes with β).
  - CE circuit then sets V_{CE}.



- But, requirements for BJT in active are on I_C and V_{CE} and NOT on I_B
  - $I_C > 0$, $V_{CE} > V_{D0}$
- **To make bias point independent of changes in β, the bias circuit should "set" I_C and NOT I_B!**

Biasing with Emitter Degeneration

Requires a resistor in the emitter circuit!

$$\text{BE}-\text{KVL}: \quad V_{BB} = I_B R_B + V_{BE} + I_E R_E$$

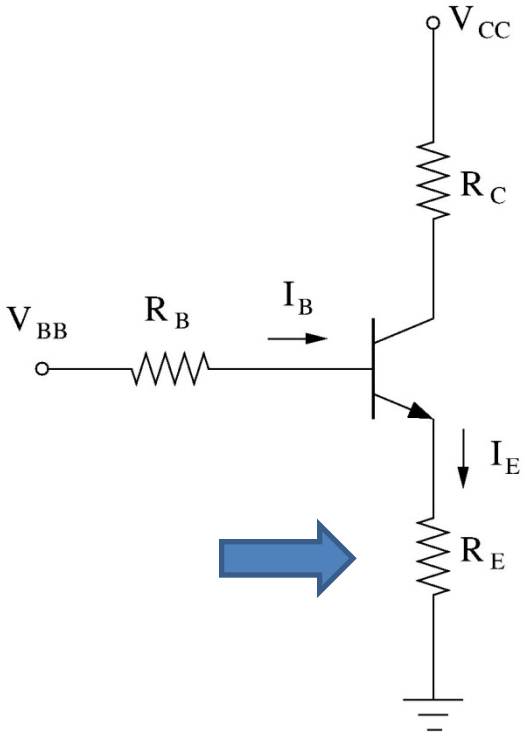
$$V_{BB} - V_{D0} = I_E \left[\frac{R_B}{\beta + 1} + R_E \right]$$

$$\text{If}: \quad R_B << (\beta + 1) R_E$$

$$V_{BB} - V_{D0} \approx I_E R_E$$

$$I_C \approx I_E \approx \frac{V_{BB} - V_{D0}}{R_E}$$

Independent of β!

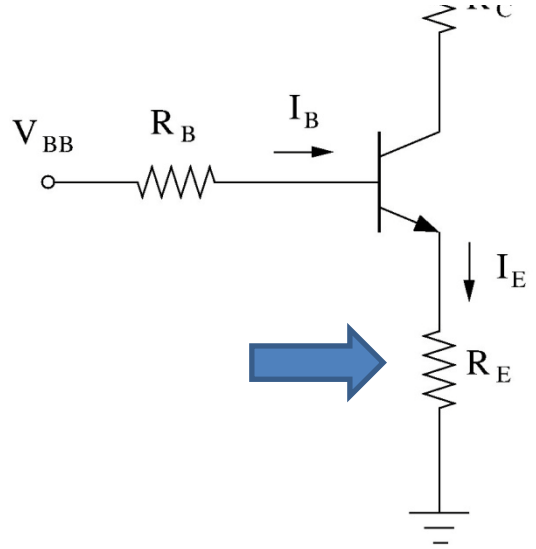


Condition of $R_B << (\beta + 1) R_E$ means that the voltage drop across R_B is small and the bias voltage $V_{BB} - V_{D0}$ appears across R_E, setting $I_E \approx I_C$.

Emitter resistor provides negative feedback!

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E$$

$$I_B \propto e^{V_{BE}/V_T}$$



Negative Feedback:

- If $I_C \approx I_E \uparrow$ (because $\beta \uparrow$), $\xrightarrow{\text{BE -KVL}} V_{BE} \downarrow \xrightarrow{\text{BE junction}} I_B \downarrow \xrightarrow{\beta} I_C \approx I_E \downarrow$
- If $I_C \approx I_E \downarrow$ (because $\beta \downarrow$), $\xrightarrow{\text{BE -KVL}} V_{BE} \uparrow \xrightarrow{\text{BE junction}} I_B \uparrow \xrightarrow{\beta} I_C \approx I_E \uparrow$

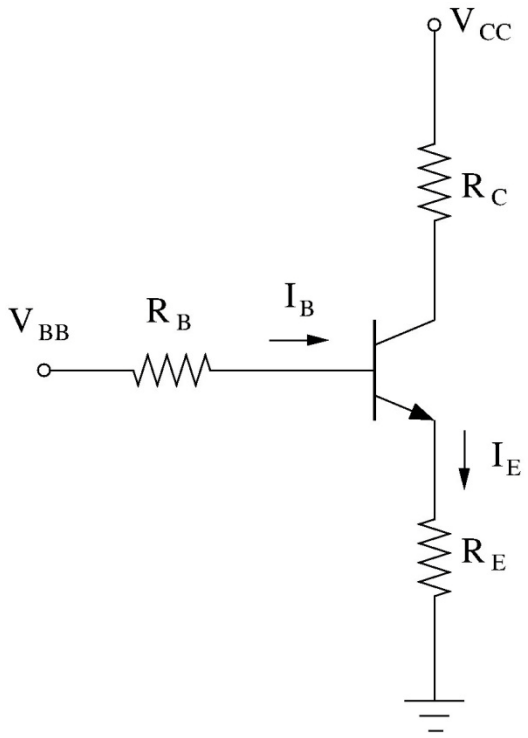
Requirements for Biasing with Emitter Degeneration

- Requires a resistor in the emitter circuit.
- The bias voltage $V_{BB} - V_{D0}$ should appear across R_E to set $I_E \approx I_C$:

$$V_{BB} - V_{BE} = I_B R_B + I_E R_E$$

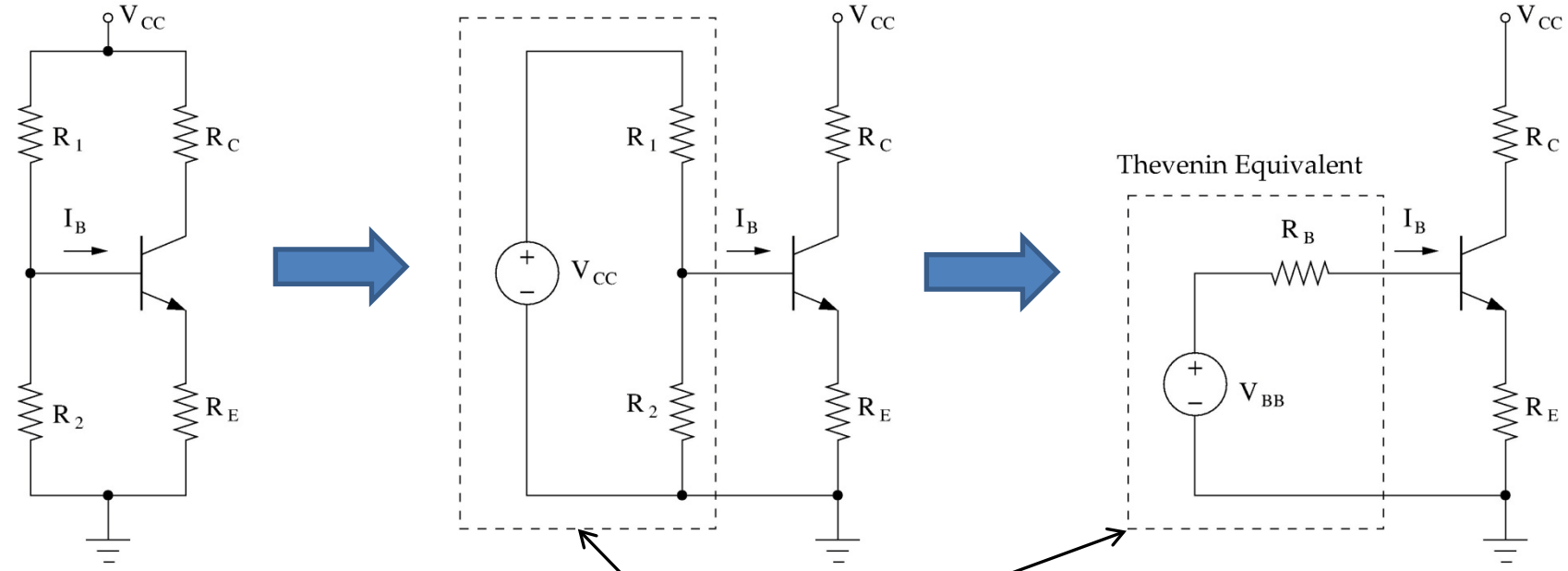
1. $I_B R_B << I_E R_E \quad \Rightarrow \quad R_B << (\beta + 1) R_E$
   - We need to set $\boxed{R_B << (\beta_{\min} + 1) R_E}$ to ensure that this condition is always satisfied!
2. $V_{BE} \approx V_{D0}$. In reality, $V_{BE} = V_{D0} \pm \Delta V_{BE}$ with $\Delta V_{BE} \approx 0.1\ \text{V}$
   - We need to set $I_E R_E >> 0.1\text{V}$ or

$$\boxed{I_E R_E \geq 1\text{V}}$$



Emitter Degeneration Bias with a voltage divider

Real Circuit



Voltage Divider

$$R_B = R_1 \| R_2$$

$$V_{BB} = \frac{R_2}{R_1 + R_2} \times V_{CC}$$

Exercise 3: Find the bias point of the BJT (Si BJT with $\beta = 200$ and $V_A = \infty$).

$$R_B = R_1 \| R_2 = 5.9\,\text{k} \| 34\,\text{k} = 5.03\,\text{k}$$

$$V_{BB} = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{5.9\,\text{k}}{5.9\,\text{k} + 34\,\text{k}} \times 15 = 2.22\ \text{V}$$

Assume BJT is in Active:

$V_{BE} = 0.7\ \text{V},\ I_C > 0$ and $V_{CE} \geq 0.7\ \text{V}$

$$\text{BE-KVL}: \quad 2.22 = I_B R_B + V_{BE} + I_E R_E$$

$$2.22 = 5.03 \times 10^3 I_E/(\beta+1) + 0.7 + 510\, I_E$$

$$I_E = 2.84\ \text{mA}$$

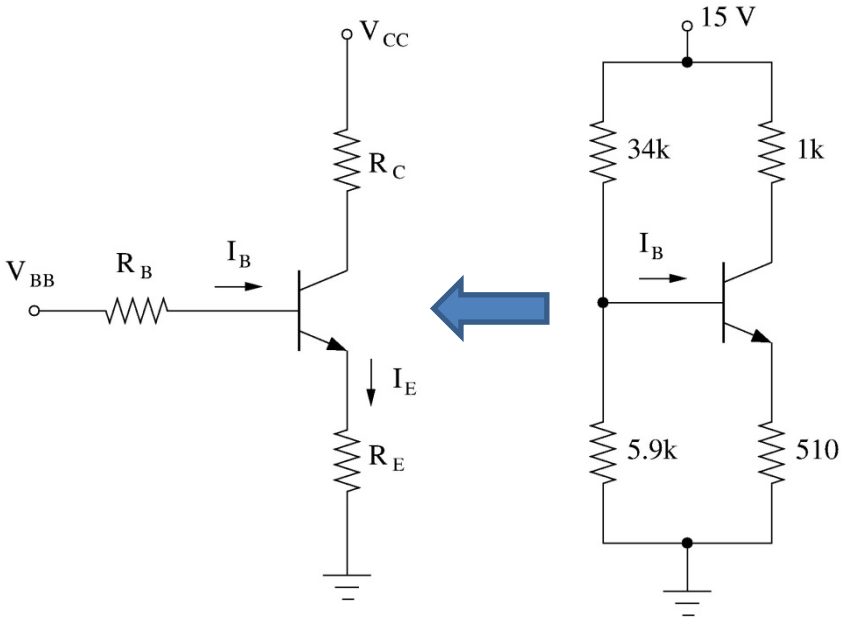
$$I_C = I_E \times \beta/(\beta+1) = 2.82\ \text{mA}$$

$$I_B = I_E/(\beta+1) = 14.1\ \mu\text{A}$$

$$\text{CE-KVL}: \quad 15 = I_C R_C + V_{CE} + I_E R_E$$

$$15 = 2.82 \times 10^{-3} \times 10^3 + V_{CE} + 2.84 \times 10^{-3} \times 510$$

$$V_{CE} = 10.7\ \text{V} > V_{D0} = 0.7\ \text{V}$$



Notes:

1. We need to solve the complete BE-KVL as we do not know if $R_B << (\beta+1)R_E$
2. $\beta >> 1$ is a good approximation that reduces the amount of work. Answers using $\beta >> 1$ approximation:

   $I_C \approx I_E \approx 2.84\ \text{mA},\quad I_B = 14.2\ \mu\text{A}$

   $V_{CE} = 10.7\ \text{V}$

Exercise 4: Design a BJT bias circuit (emitter degeneration with voltage divider) such that $I_C = 2.5$ mA and $V_{CE} = 7.5$ V. ($V_{CC} = 15$ V Si BJT with β ranging from 50 to 200 and $V_A = \infty$).

Step 1: Find R_C and R_E

$$\text{CE}-\text{KVL}: \quad 15 = I_C R_C + V_{CE} + I_E R_E$$

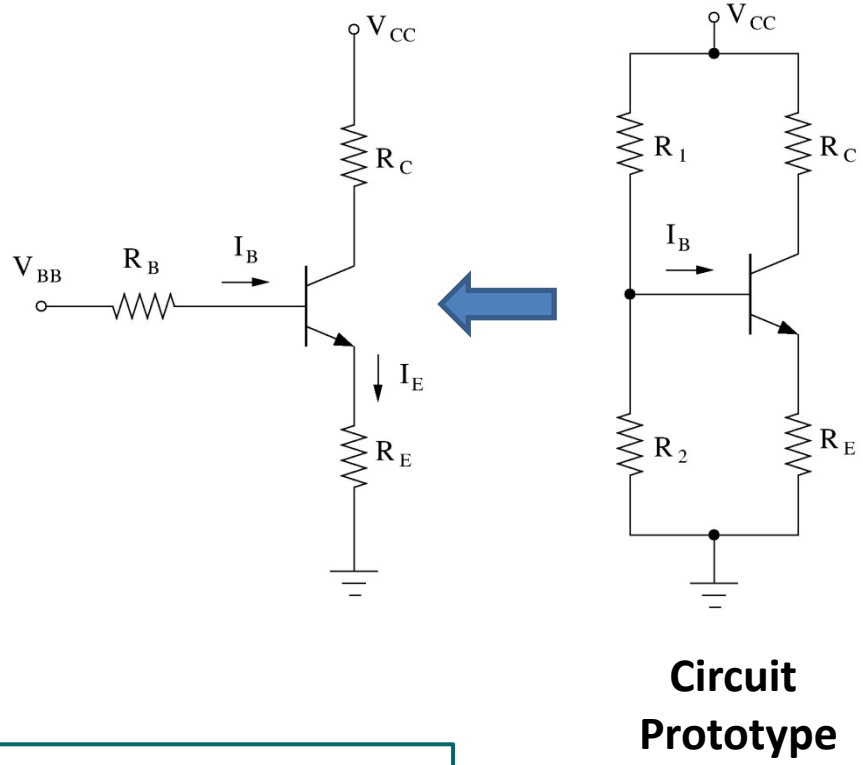
$$15 = 2.5\times10^{-3}\times(R_C + R_E) + 7.5$$

$$R_C + R_E = 3.0 \text{ k}$$

Free to choose individual values R_E & R_C (we will see later that amplifier parameters sets the individual values)

$$\text{Choose}: \quad R_E = 1.0 \text{ k}$$

$$R_C = 3.0 \text{ k} - R_E = 2.0 \text{ k}$$



Circuit Prototype

Check: $I_E R_E \geq 1\text{V}$

$$I_E R_E = 2.5\times10^{-3}\times10^{3} = 2.5 \geq 1\text{V}$$

Exercise 4 (Cont'd): Design a BJT bias circuit (emitter degeneration with voltage divider) such that $I_C = 25$ mA and $V_{CE} = 5$ V. ($V_{CC} = 15$ V Si BJT with β ranging from 50 to 200 and $V_A = \infty$).

Step 2: Find R_B and V_{BB}

$$R_B << (\beta_{\min}+1)R_E \quad \rightarrow \quad R_B \leq 0.1\,(\beta_{\min}+1)R_E = 5.1\ \text{k} \quad \rightarrow \quad R_B = 5.1\ \text{k}$$

Using relative error, ε = 10%

Use largest R_B (Will see later why)

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E$$

$$V_{BB} \approx V_{D0} + I_C R_E = 0.7 + 2.5\times10^{-3}\times10^{3} \rightarrow V_{BB} = 3.20\ \text{V}$$

Step 3: Find R_1 and R_2

$$R_B = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} = 5.10\,\text{k}$$

$$\frac{V_{BB}}{V_{CC}} = \frac{R_2}{R_1 + R_2} = \frac{3.20}{15} = 0.213$$

$$R_1 = \frac{5.10\,\text{k}}{0.213} = 23.9\,\text{k}$$

$$R_2 = 6.4\,\text{k}$$

Step 4: Find commercial R values:

$R_C = 2$ k

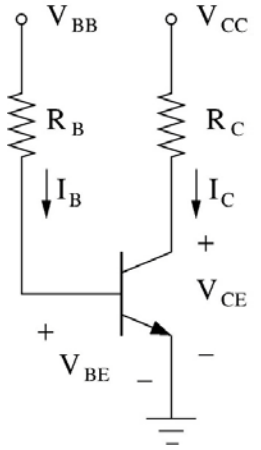
$R_E = 1$ k

$R_1 = 24$ k

$R_2 = 6.4$ k

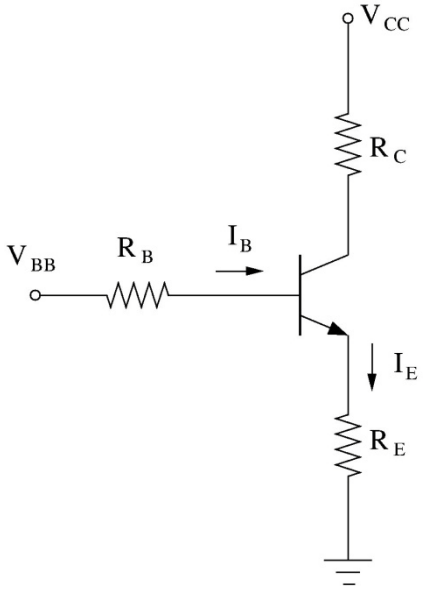
Why biasing with base voltage (fixed bias) does not work?

- Changes in BJT β changes the bias point drastically.
  - BJT can end up in saturation or in cut-off easily.
- In fixed bias, I_B is set through $I_B = \dfrac{V_{BB} - V_{D0}}{R_B}$
- BJT β then sets $I_C = \beta I_B$ (I_C changes with β).
  - CE circuit then sets V_{CE}.



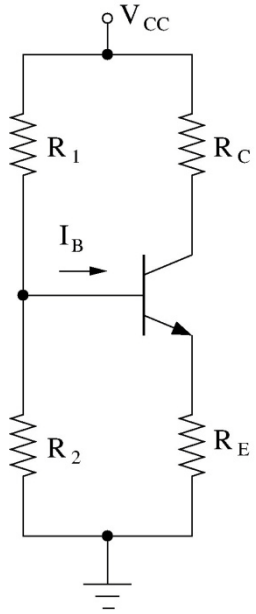
- But, requirements for BJT in active are on I_C and V_{CE} and NOT on I_B
  - $I_C > 0$, $V_{CE} > V_{D0}$
- **To make bias point independent of changes in β, the bias circuit should "set" I_C and NOT I_B!**

Emitter-degeneration bias circuits



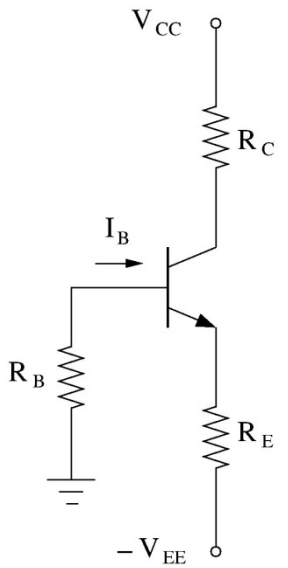
Basic Arrangement

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E$$



Bias with <u>one</u> power supply (voltage divider)

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E$$



Bias with <u>two</u> power supplies

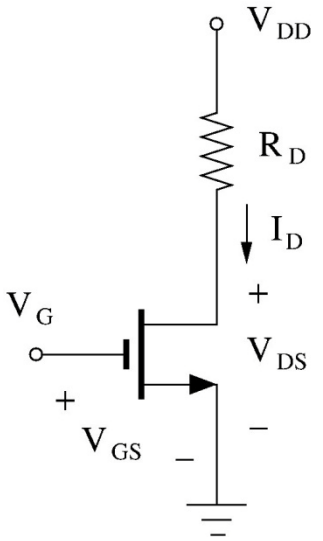
$$V_{EE} = I_B R_B + V_{BE} + I_E R_E$$

$$0 = I_B R_B + V_{BE} + I_E R_E - V_{EE}$$

MOS bias with Gate Voltage

$$I_D = 0.5\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

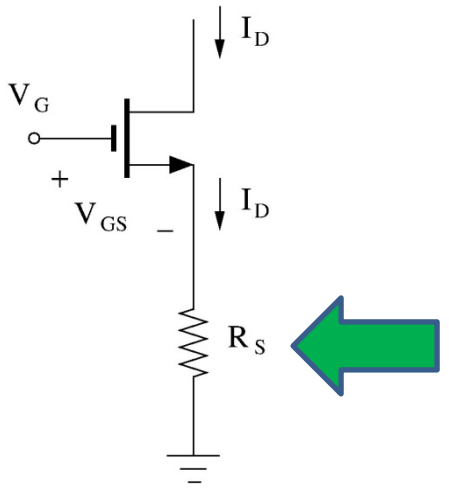
$$V_{DS} = V_{DD} - I_D R_D$$



- This method is NOT desirable as $\mu_n C_{ox}\,(W/L)$ and V_t are not "well-defined." Bias point (i.e., I_D and V_{DS}) can change drastically due to temperature and/or manufacturing variability.
  - See S&S Exercise 5.33 (S&S 5th Ed: Exercise 4.19): Changing V_t from 1 to 1.5 V leads to a 75% change in I_D.

MOS bias with Source Degeneration (Resistor R_s provides negative feedback!)

$$\begin{cases} V_{GS} = V_G - R_S I_D \\ I_D = 0.5\mu_n C_{ox} \dfrac{W}{L}(V_{GS} - V_t)^2 \end{cases}$$



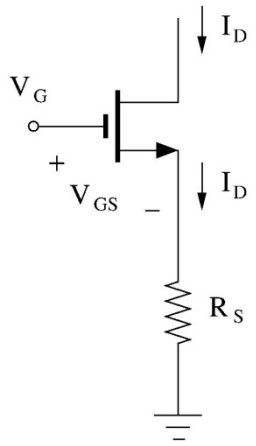
Negative Feedback:

- If $I_D \uparrow$ (because $\mu_n C_{ox}(W/L) \uparrow$ or $V_t \downarrow$) $\xrightarrow{\text{GS KVL}} V_{GS} \downarrow \xrightarrow{I_D \text{ Eq.}} I_D \downarrow$
- If $I_D \downarrow$ (because $\mu_n C_{ox}(W/L) \downarrow$ or $V_t \uparrow$) $\xrightarrow{\text{GS KVL}} V_{GS} \uparrow \xrightarrow{I_D \text{ Eq.}} I_D \uparrow$

- Feedback is most effective if $R_S I_D >> V_{GS}$

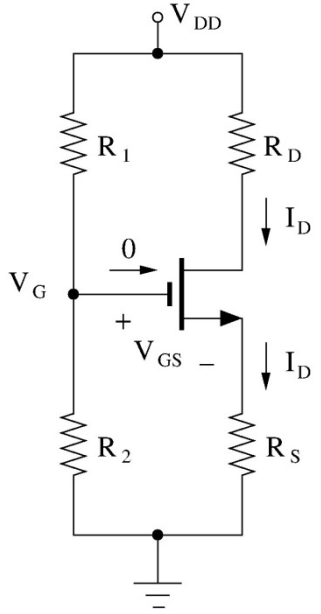
$$V_{GS} - V_G + R_S I_D = 0 \Rightarrow I_D \approx V_G / R_S$$

Source-degeneration bias circuits



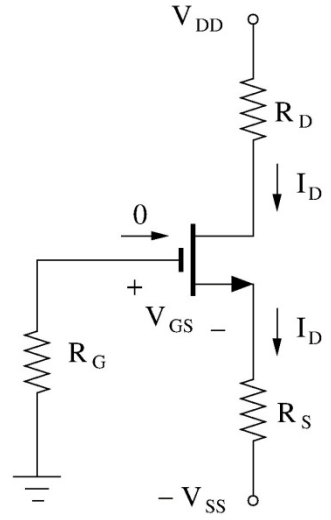
Basic Arrangement

$$V_G = V_{GS} + I_D R_S$$



Bias with <u>one</u> power supply (voltage divider)

$$V_G = V_{GS} + I_D R_S$$



Bias with <u>two</u> power supplies

$$V_{SS} = V_{GS} + I_D R_S$$

$$0 = V_{GS} + I_D R_S - V_{SS}$$

Exercise 5: Find the bias point for $V_t = 1$ V and $\mu_n C_{ox}\,(W/L) = 1.0$ mA/V^2 (Ignore channel-width modulation).

Voltage divider ($I_G = 0$)

$$V_G = (7)/(7+8)\times 15 = 7\ \text{V}$$

$$I_D = 0.5\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

$$\text{GS-KVL}: V_G = 7 = V_{GS} + R_S I_D$$

$$V_{OV} + V_t + R_S I_D = 7$$

$$V_{OV} + 1 + 10^4 \times (0.5\times 10^{-3} V_{OV}^2) = 7$$

$$5V_{OV}^2 + V_{OV} - 6 = 0 \;\rightarrow\; V_{OV} = 1\ \text{V}$$

$$V_{GS} = V_{OV} + 1 = 2\ \text{V}$$

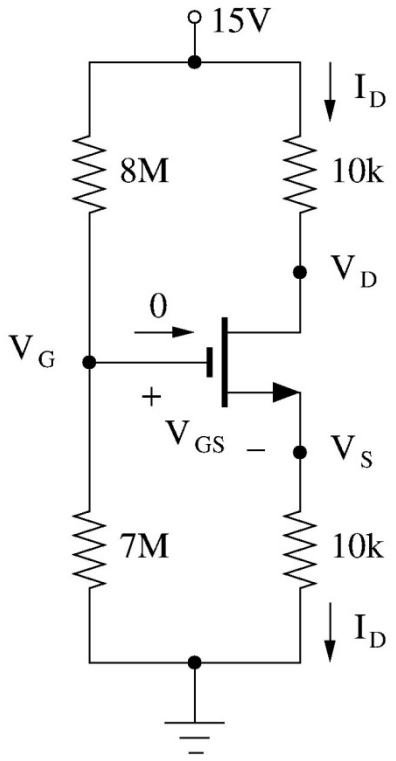
$$V_S = V_G - V_{GS} = 7 - 2 = 5\ \text{V}$$

$$I_D = V_S / R_S = 0.5\,\text{mA}$$

$$\text{DS-KVL}: 15 = R_D I_D + V_D$$

$$V_D = 15 - R_D I_D = 10\ \text{V}$$

$$V_{DS} = V_D - V_S = 5\ \text{V}$$

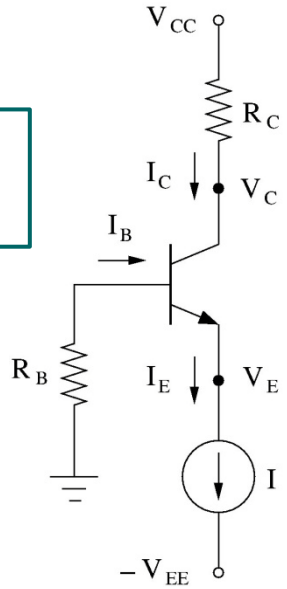


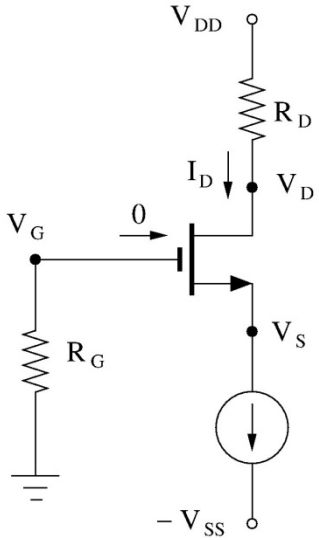
Exercise (impact of R_S): Prove that if $V_t = 1.5$ V (50% change), $I_D = 0.455$mA (9% change)

Biasing in ICs

- Resistors take too much space on the chip. So, biasing with emitter or source degeneration are NOT implemented in ICs.
- Recall that the goal of a good bias is to ensure that I_C and V_{CE} (or I_D and V_{DS} for MOS) do not change. One can <u>force</u> I_C (or I_D for MOS) to be constant using a current source.

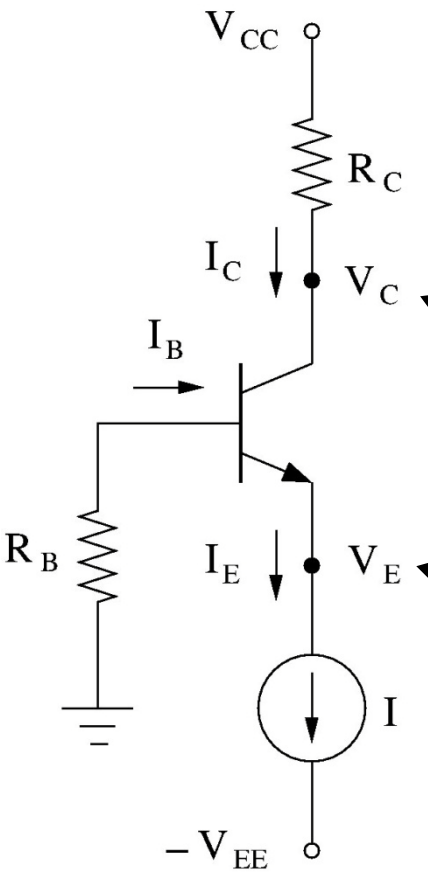
Current source forces $I_E = I$





Current source forces $I_D = I$

BJT response to a current source



1) Current source forces:
$I_C \approx I_E = I$

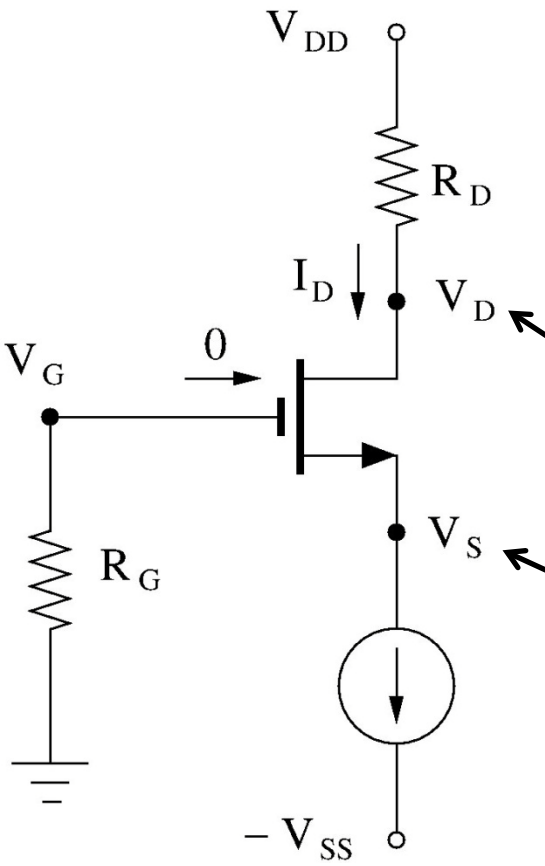
2) $I_B = I_C \,/\, \beta$

3A) $V_C = V_{CC} - R_C I_C$

3B) V_E is set by BE-KVL
$0 = R_B I_B + V_{BE} + V_E$

4) $V_{CE} = V_C - V_E$

MOS response to a current source



1) Current source forces:

$$I_D = I$$

2) V_{GS} is set by

$$I_D = 0.5\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

3A) $V_D = V_{DD} - R_D I_D$

3B) $V_S = V_G - V_{GS} = -V_{GS}$

4) $V_{DS} = V_D - V_S$

Current Mirrors (or Current Steering circuits) are used as current sources for biasing ICs

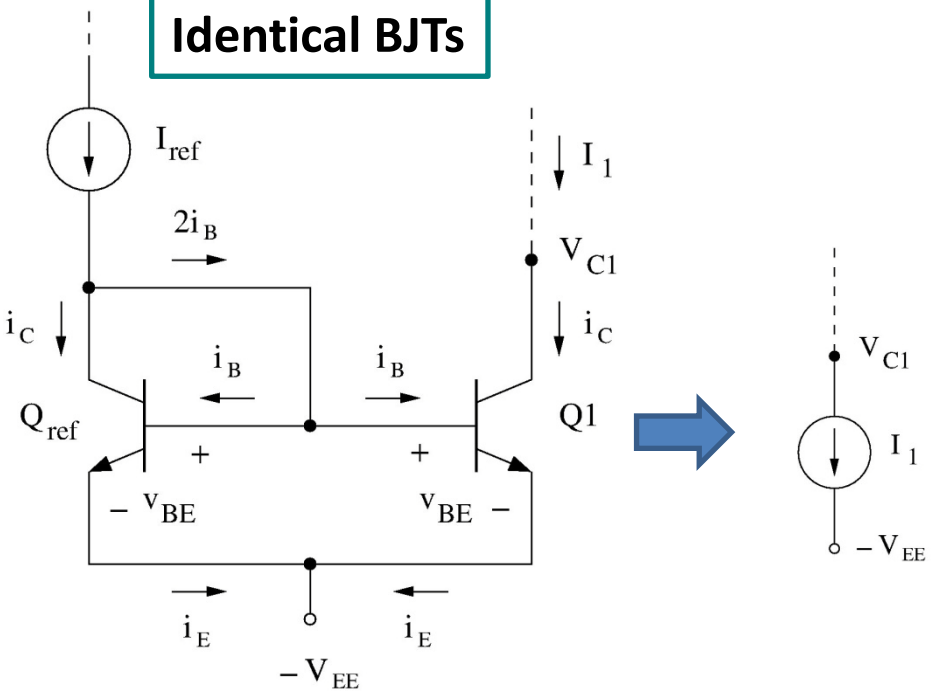
- **Q_{ref} is <u>always</u> in active since**

$$i_{C,ref} > 0$$

$$V_{CE,ref} = V_{BE,ref} = V_{D0}$$

- **Identical BJTs and $v_{BE,ref} = v_{BE1}$**
  - BJTs will have the same i_B and the same i_C (ignoring Early effect)

Identical BJTs



$$\text{KCL}: \quad I_{ref} = i_{C,ref} + 2i_B = i_C + 2\frac{i_C}{\beta}$$

$$I_1 = i_C = \frac{I_{ref}}{1 + 2/\beta} \approx I_{ref}$$

- Since $I_1 = const.$ regardless of V_{C1}, this is a current source!

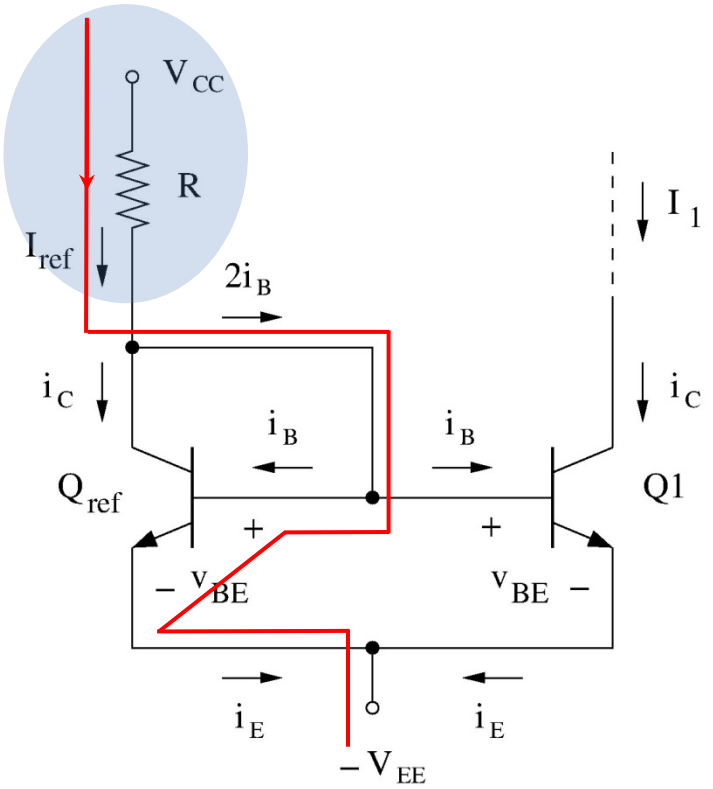
- **For the current mirror to work, Q1 should be in active:**

$$V_{CE1} = V_{C1} + V_{EE} \geq V_{D0}$$

An implementation of a BJT Current Mirror

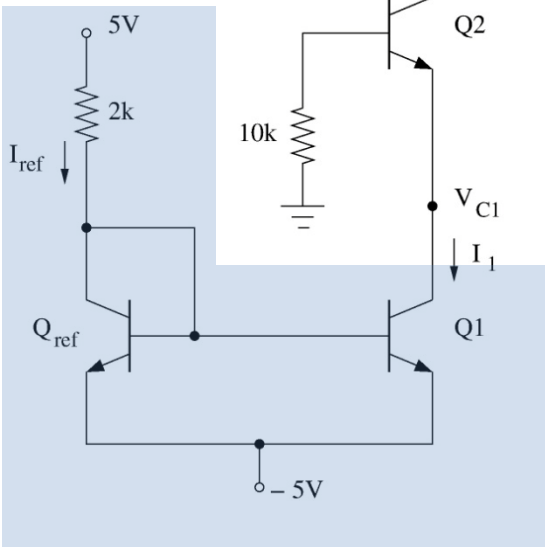
$$\text{BE-KVL}\ (Q_{ref}):\ V_{CC} = R\,I_{ref} + V_{BE} - V_{EE}$$

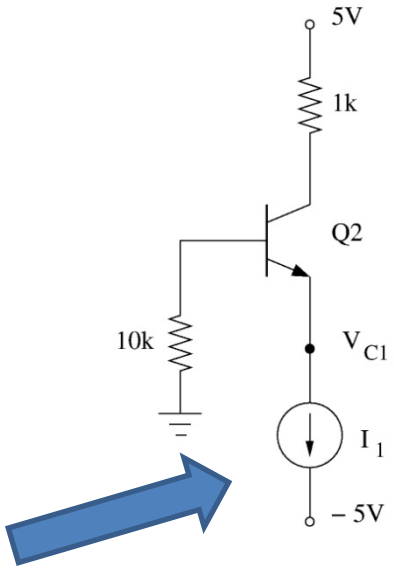
$$I_1 \approx I_{ref} = \frac{V_{CC} + V_{EE} - V_{D0}}{R}$$



Exercise 6: Find the bias point of Q2 (Si BJT with $\beta = 100$ and $V_A = \infty$).

Current Mirror





$$5 = 2\times10^3\, I_{ref} + V_{BE} - 5$$

$$I_{ref} = 4.65 \text{ mA}$$

$$I_1 \approx I_{ref} = 4.65 \text{ mA}$$

Assume Q2 in active:

$$I_{C2} \approx I_{E2} = I_1 \approx 4.65 \text{ mA}$$

$$I_{B2} = I_{C2}/\beta \approx 46.5 \ \mu\text{A}$$

$$\text{BE2-KVL}: \quad 0 = 10\times10^3 I_{B2} + V_{BE2} + V_{E2}$$

$$0 = 10\times10^3 \times 46.5\times10^{-6} + 0.7 + V_{E2}$$

$$V_{C1} = V_{E2} = -1.165 \text{ V}$$

$$\text{CE2-KVL}: \quad 5 = 10^3 I_{C2} + V_{CE2} + V_{E2}$$

$$V_{CE2} = 5 - 10^3 \times 4.65\times10^{-3} - 1.165$$

$$V_{CE2} = 1.56 \text{ V}$$

$$V_{CE2} = 1.56 > V_{D0} = 0.7 \text{ V} \quad \text{Q2 in active!}$$

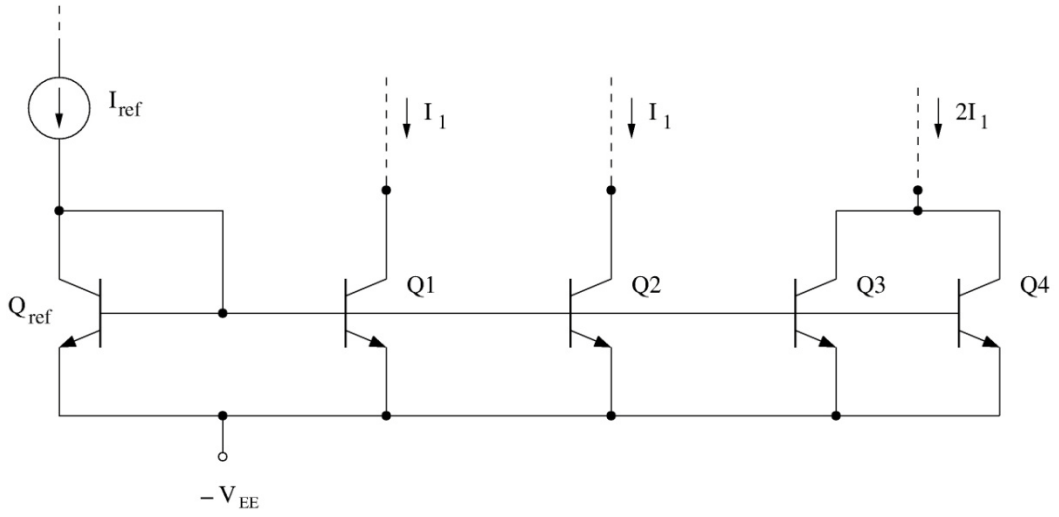
Check Q1 in active:

$$V_{CE1} = V_{C1} - (-5) = -1.165 + 5 = 3.835 \text{ V}$$

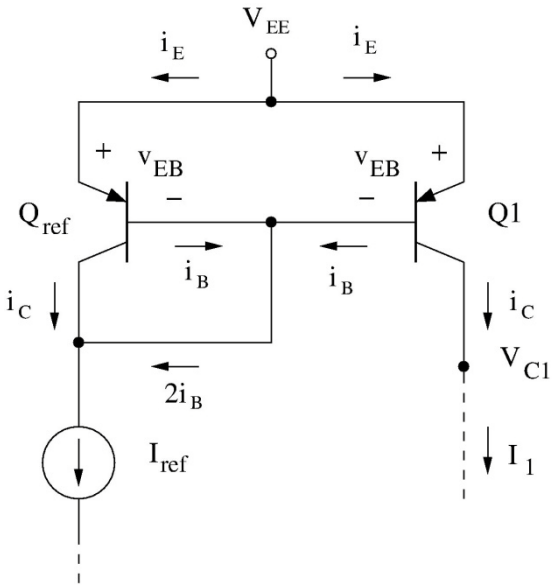
$$V_{CE1} = 3.835 > V_{D0} = 0.7 \text{ V}$$

Examples of BJT current mirrors

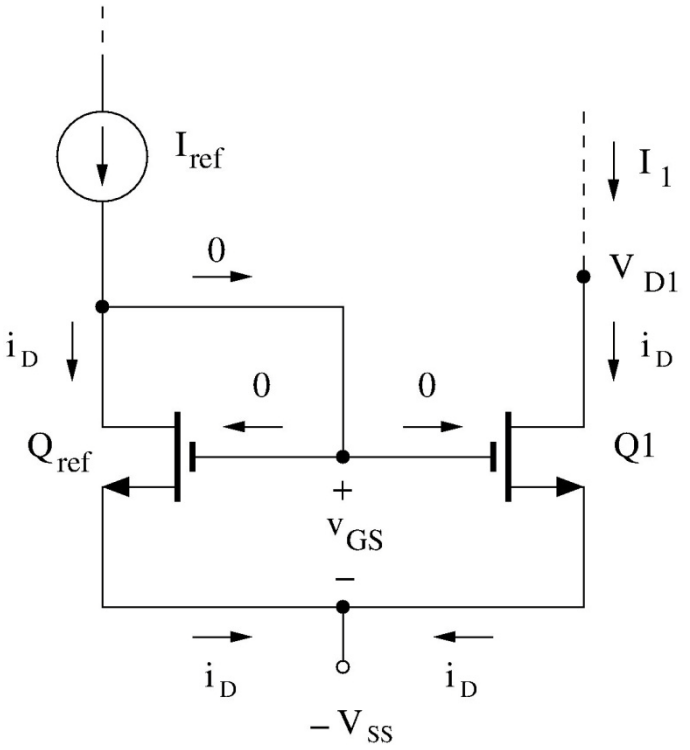
- One “reference” BJT feeds many current mirrors
- Integer multiple of I_{ref} can be made (See Q3 & Q4)

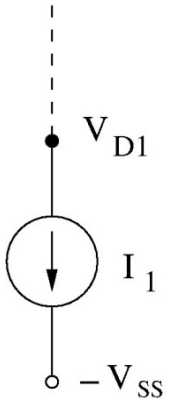


PNP current Mirror



MOS Current-Steering Circuit





An implementation of a MOS current steering circuit

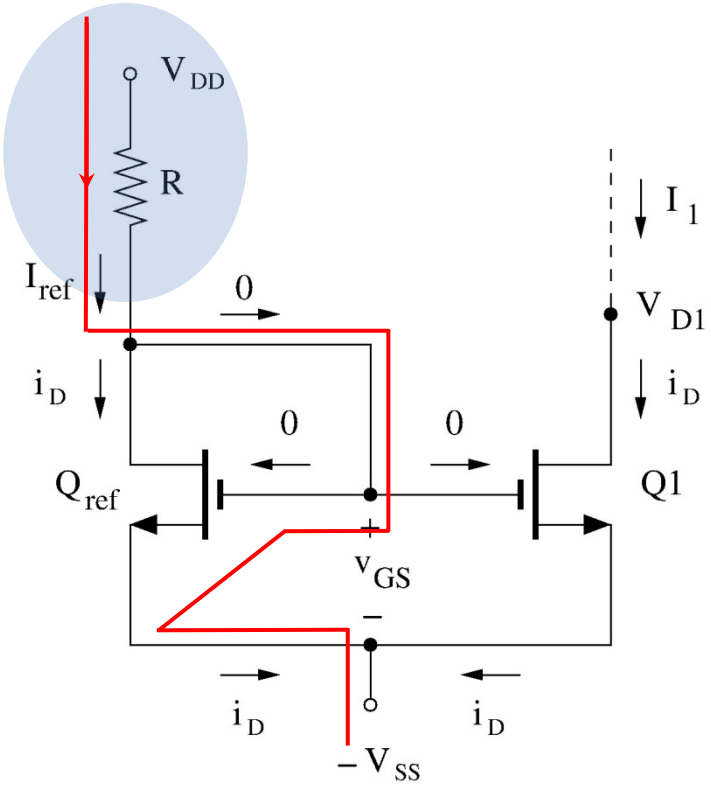
$$I_{ref} = i_D = 0.5\mu_n C_{ox}(W/L)_{ref}\, V_{OV}^2$$

$$\text{GS-KVL}\ (\text{Q}_{ref}): V_{DD} = Ri_D + v_{GS} - V_{SS}$$

$$Ri_D + V_{OV} - V_{SS} - V_{DD} + V_t = 0$$

$$[\,0.5\mu_n C_{ox}(W/L)_{ref}\ R\,]V_{OV}^2 + V_{OV} + [-V_{SS} - V_{DD} + V_t\,] = 0$$

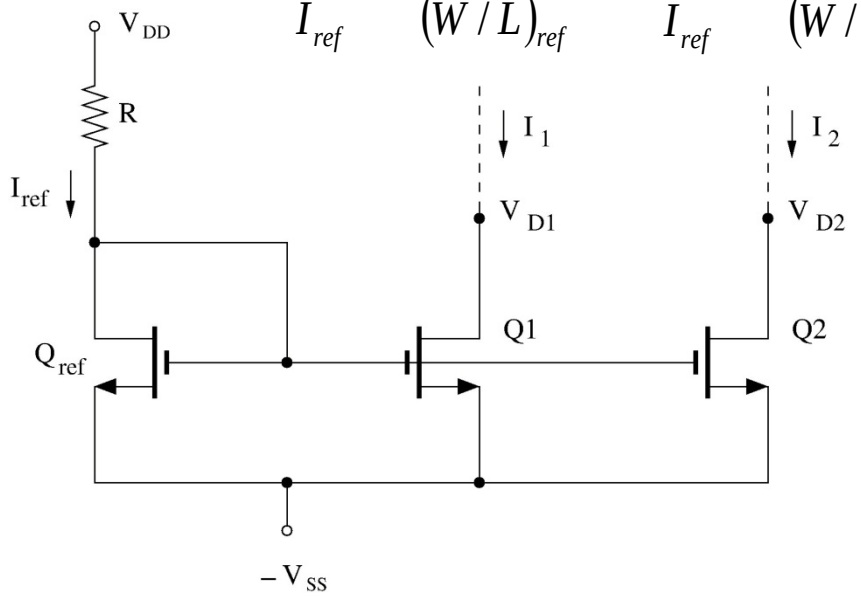
The above quadratic equation gives V_{OV}.
I_1 is then found from the MOS i_D equation.



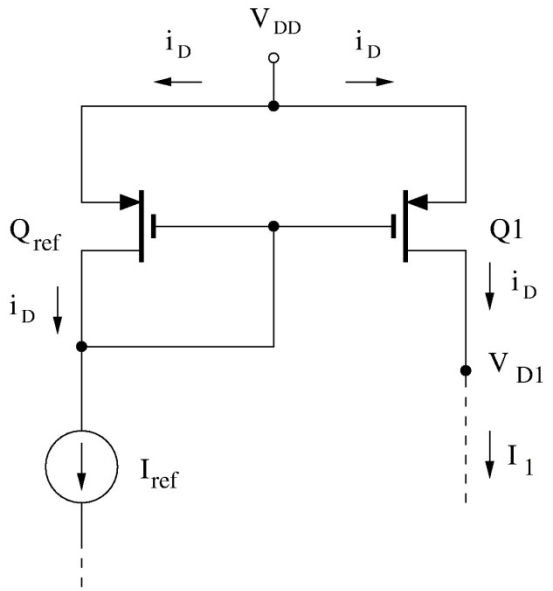
Examples of MOS current steering circuits

- One "reference" MOS feeds many current steering circuits.
- Any value of I_{ref} can be made (thus, current-steering circuit instead of current-mirror)

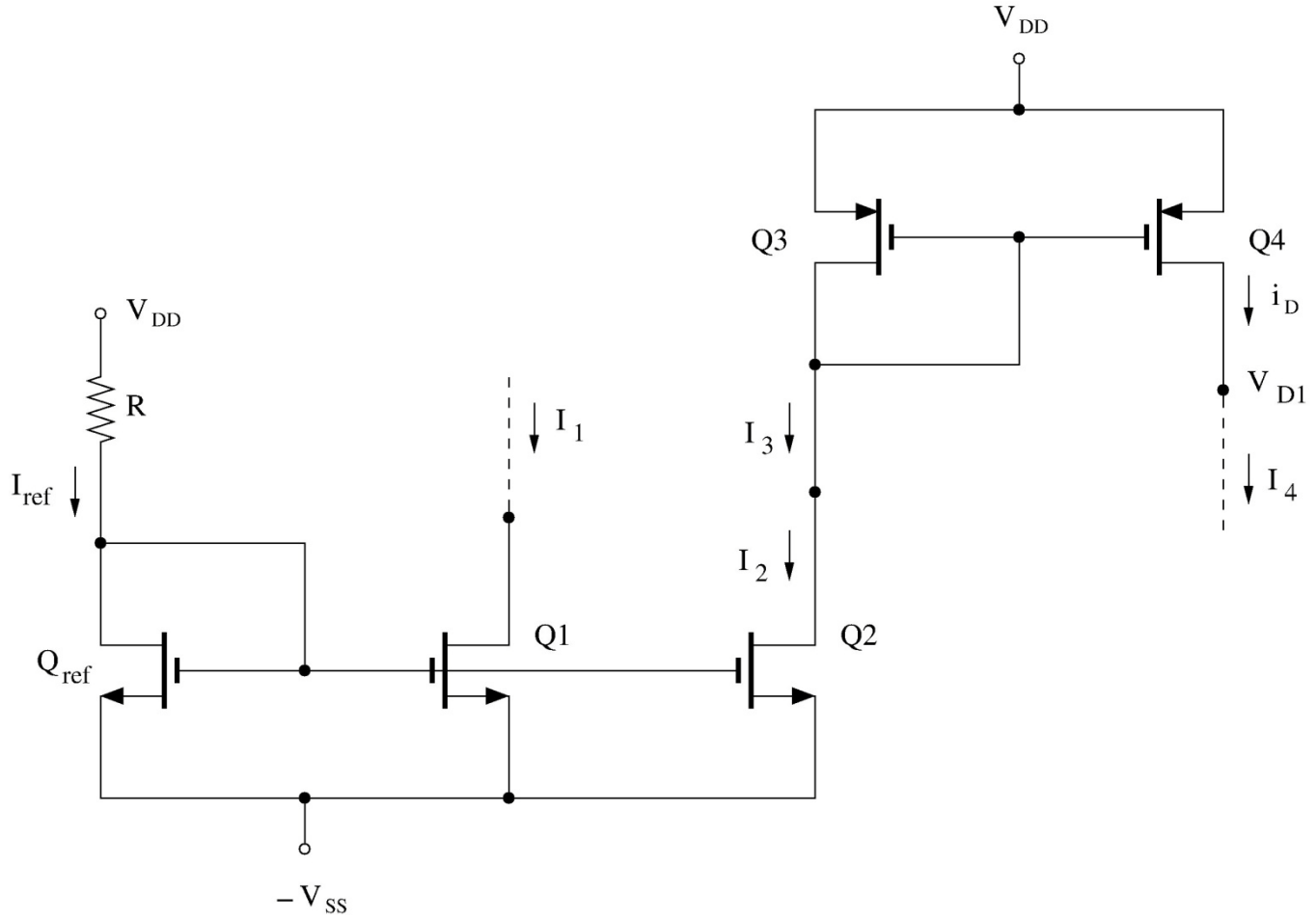
$$\frac{I_1}{I_{ref}} = \frac{(W/L)_1}{(W/L)_{ref}} \qquad \frac{I_2}{I_{ref}} = \frac{(W/L)_2}{(W/L)_{ref}}$$



PMOS current steering circuit



An implementation of current steering circuit to bias several transistors in an IC



Exercise: Compute I_4 / I_{ref}