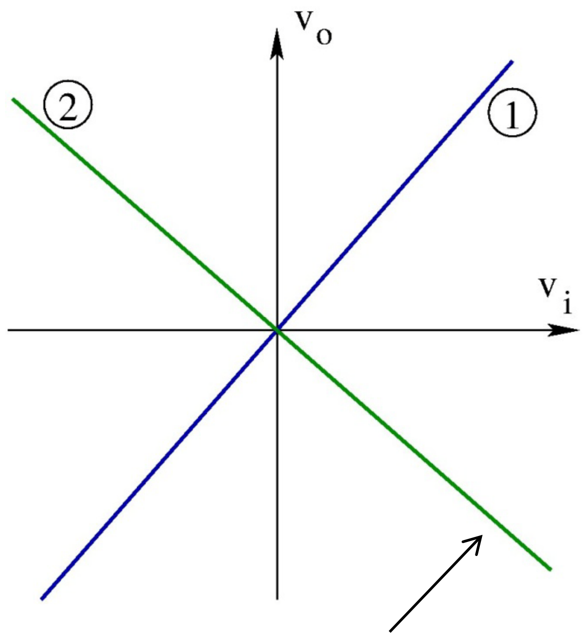
6. Introduction to Transistor Amplifiers: Concepts and Small-Signal Model

Lecture notes: Sec. 5

Sedra & Smith (6^{th} Ed): Sec. 5.4, 5.6 & 6.3-6.4
Sedra & Smith (5^{th} Ed): Sec. 4.4, 4.6 & 5.3-5.4

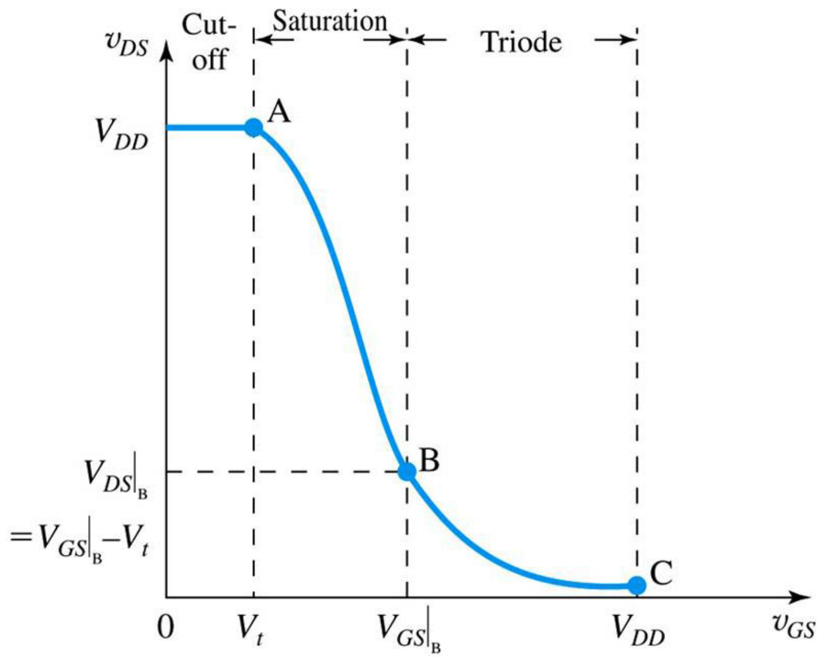
Foundation of Transistor Amplifiers (1)

- A voltage amplifier requires $v_o / v_i = \text{const.}$ (2 examples below)



- v_o / v_i can be negative (minus sign represents a 180° phase shift)

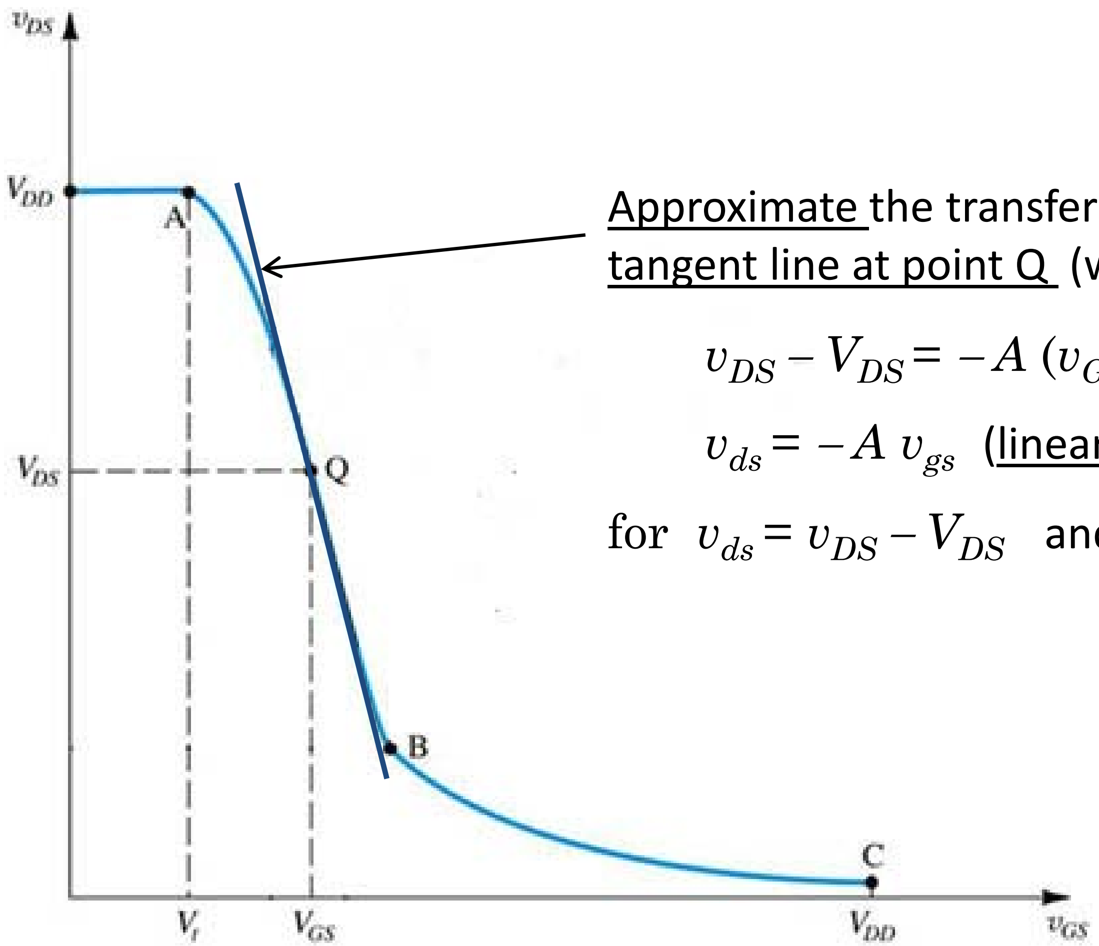
- MOS transfer function is NOT linear



- In saturation, however, transfer function looks linear (but shifted)

Foundation of Transistor Amplifiers (2)

- In saturation, transfer function appear to be linear



Approximate the transfer function with a tangent line at point Q (with a slope of $-A$):

$$v_{DS} - V_{DS} = -A\,(v_{GS} - V_{GS})$$

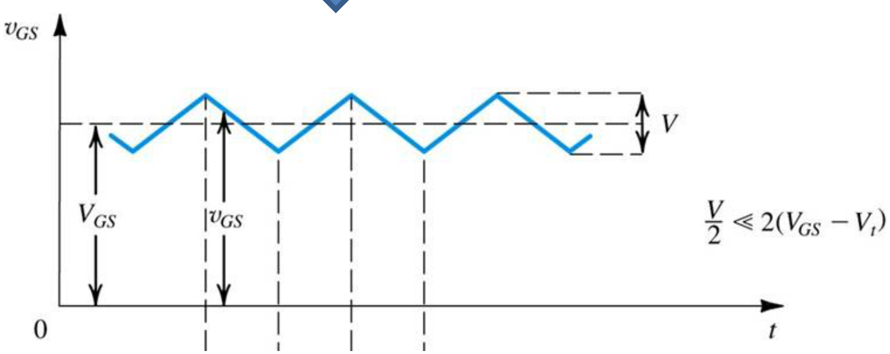
$v_{ds} = -A\, v_{gs}$ (linear relationship)

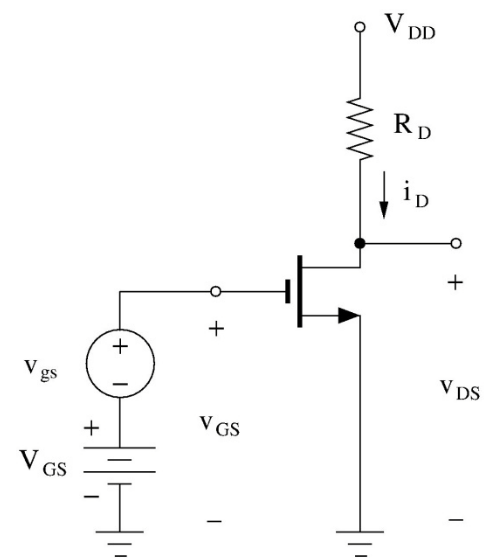
for $v_{ds} = v_{DS} - V_{DS}$ and $v_{gs} = v_{GS} - V_{GS}$

Foundation of Transistor Amplifiers (3)

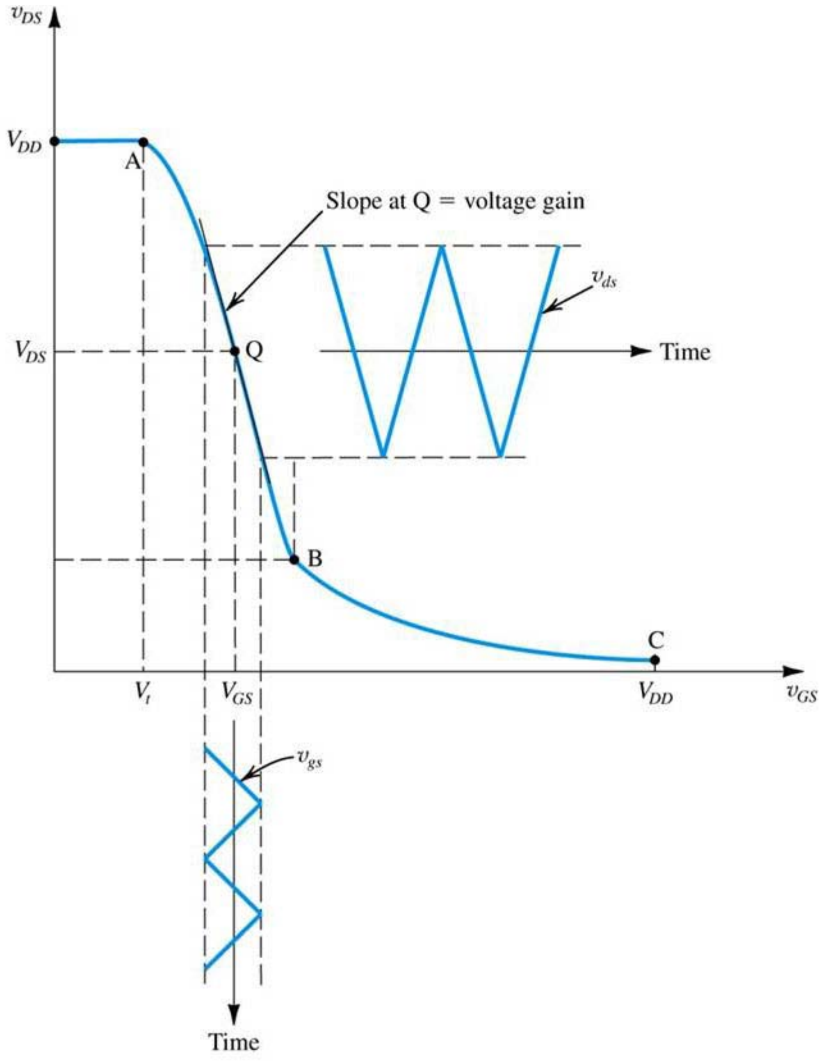
- Let us consider the response if NMOS remains in saturation at all times and v_{GS} is a combination of a **constant value** (V_{GS}) and a **<u>signal</u>** (v_{gs}):

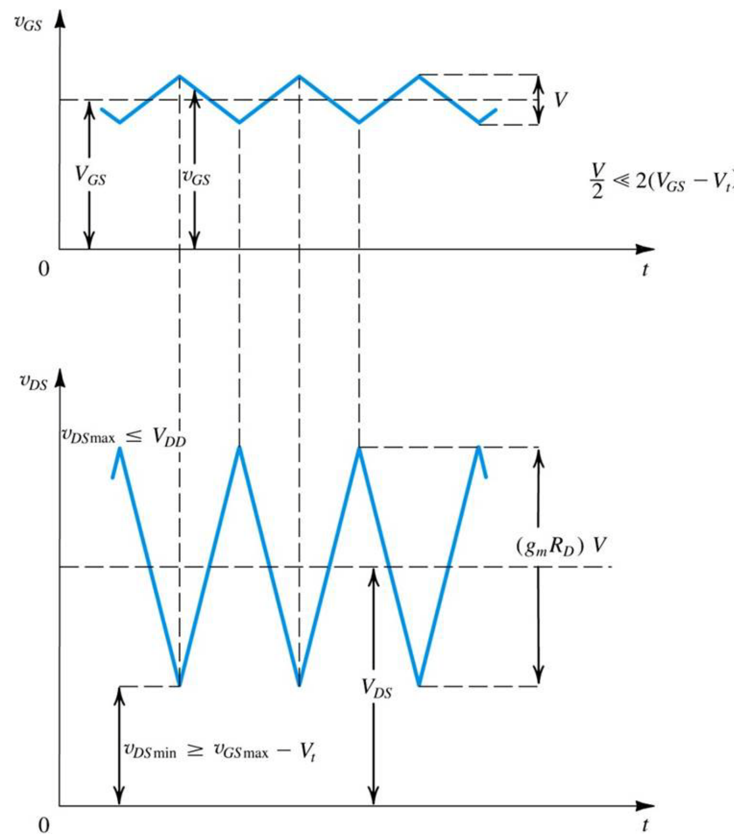
$$v_{GS} = V_{GS} + v_{gs}$$



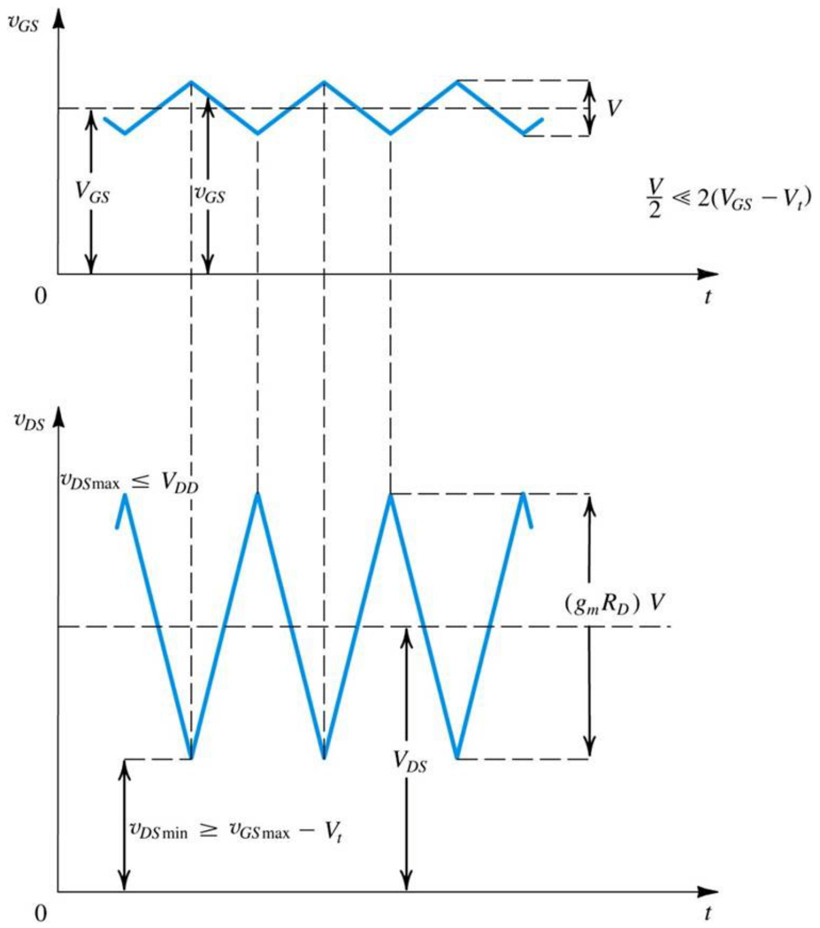


The response to a combination of $v_{GS} = V_{GS} + v_{gs}$ can be found from the transfer function





Response to the signal appears to be linear



- Response ($v_o = v_{DS}$) is also made of a constant part (V_{DS}) and a signal response part (v_{ds}).
- Constant part of the response, V_{DS}, is ONLY related to V_{GS}, the constant part of the input (Q point on the transfer function of previous slide).
  - i.e., if $v_{gs} = 0$, then $v_{ds} = 0$
- The shape of the time varying portion of the response (v_{ds}) is similar to v_{gs}.
  - i.e., v_{ds} is <u>proportional</u> to the input signal, v_{gs}

Although the overall response is non-linear, the <u>transfer function for the signal is linear</u>!

Constant: Bias

Signal and response

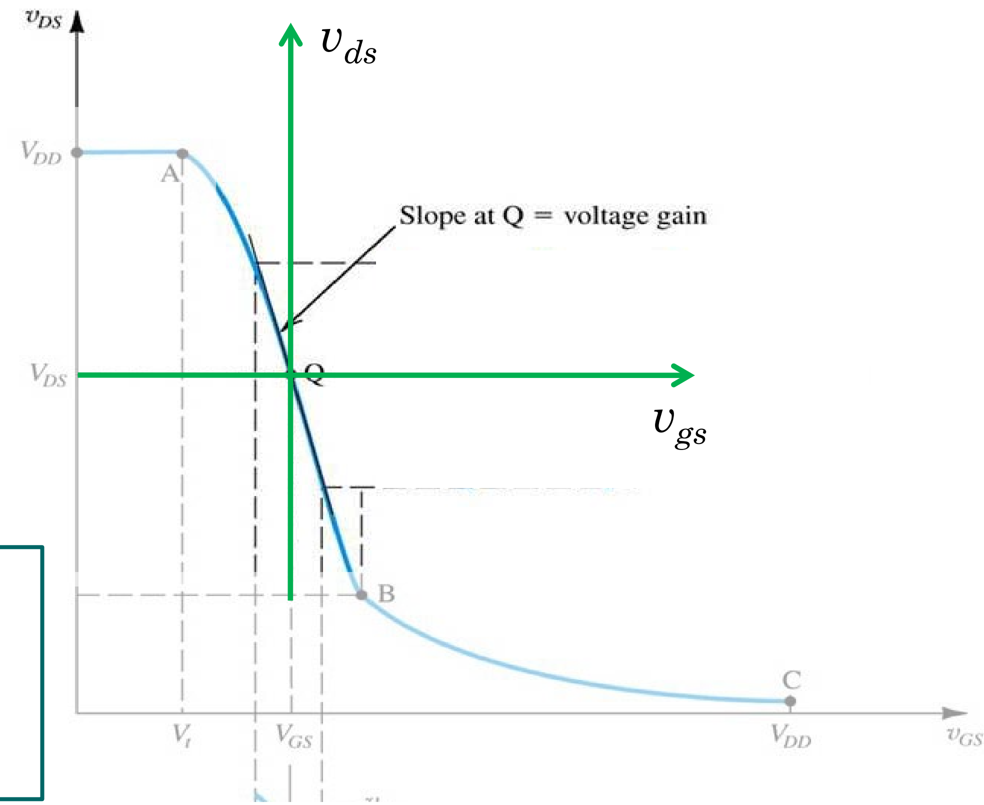
$$v_{GS} = V_{GS} + v_{gs}$$

$$v_{DS} = V_{DS} + v_{ds}$$

$$i_D = I_D + i_d$$

Non-linear relationship among these parameters

Approximately Linear relationship among these parameters



Important Points and Definitions!

- **Signal:** We want the response of the circuit to this input.

- **Bias:** State of the system when there is no signal.
  - Bias is constant in time (may vary extremely slowly compared to signal)
  - Purpose of the bias is to ensure that MOS is in saturation at all times.

- **Response** of the circuit (and its elements) to the signal is different than its response to the Bias (or to Bias + signal):
  - Signal iv characteristics of elements are different, i.e. relationships among v_{gs} , v_{ds} , i_d is different from relationships among v_{GS} , v_{DS} , i_D .
  - Signal transfer function of the circuit is different from the transfer function for total input (Bias + signal).

Above observations & conclusions equally apply to a BJT in the active mode!

Issues in developing a transistor amplifier:

1. **Find the iv characteristics of the elements for the signal** (which can be different than their characteristics equation for bias).
   - This will lead to different circuit configurations for bias versus signal
2. **Compute circuit response to the signal**
   - Focus on fundamental transistor amplifier configurations
3. **How to establish a Bias point** (bias is the state of the system when there is no signal).
   - Stable and robust bias point should be resilient to variations in $\mu_n C_{ox} (W/L), V_t$ (or β for BJT) due to temperature and/or manufacturing variability.
   - Bias point details impact small signal response (e.g., gain of the amplifier).

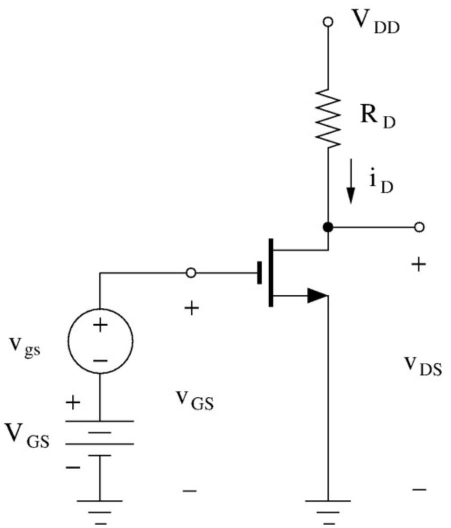
Signal Circuit

1) We will find signal iv characteristics of various elements.

2) In order to use circuit theory tools, we will use the signal iv characteristics of various elements to assign a circuit symbol. e.g.,
   - We will see that the diode signal iv characteristics is linear so for signals, diode can be modeled as a "circuit theory" resistor.
   - In this manner, we will arrive at a signal circuit.

Bias and Signal Circuits

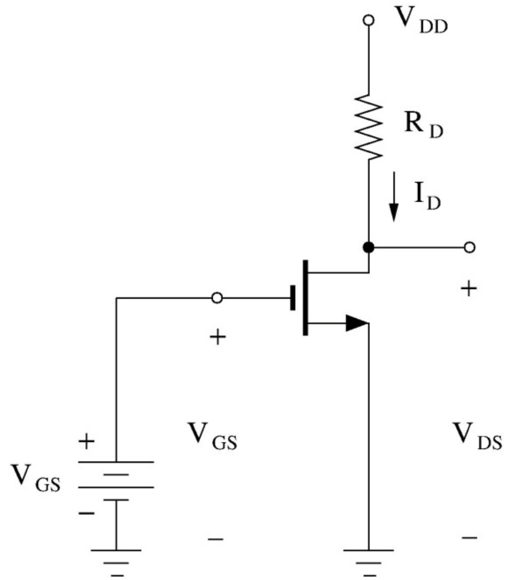
Bias & Signal



$$\text{MOS}: \; v_{GS}, v_{DS}, i_D,$$
$$(v_{GS} = V_{GS} + v_{gs}, \ldots)$$
$$R_D: \quad v_R = V_R + v_r$$
$$i_R = I_R + i_r$$

.....

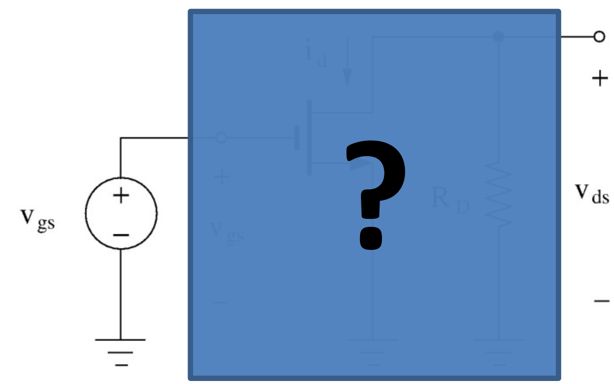
Bias



$$\text{MOS}: \; V_{GS}, V_{DS}, I_D,$$
$$R_D: \quad V_R, I_R$$

.....

Signal only
= (Bias + Signal) - Bias



$$\text{MOS}: \; v_{gs}, v_{ds}, i_d,$$
$$R_D: \quad v_r, i_r$$

.....

Finding signal circuit elements -- Resistor

Resistor	Voltage	Current	iv Equation
Bias + Signal:	v_R	i_R	$v_R = R\, i_R$
Bias:	V_R	I_R	$V_R = R\, I_R$
Signal:	$v_r = v_R - V_R$	$i_r = i_R - I_R$	**??**

$$v_r = v_R - V_R = Ri_R - RI_R = R\,(i_R - I_R) \Rightarrow v_r = Ri_r$$

- **A resistor remains as a resistor in the signal circuit.**

Finding signal circuit elements -- Capacitor

Capacitor	Voltage	Current	iv Equation
Bias + Signal:	v_C	i_C	$i_C = C\,dv_C\,/dt$
Bias:	V_C	I_C	$I_C = C\,dV_C\,/dt$
Signal:	$v_c = v_C - V_C$	$i_c = i_C - I_C$	**??**

$$i_c = i_C - I_C = C\frac{dv_C}{dt} - C\frac{dV_C}{dt} = C\frac{d(v_C - V_C)}{dt} \Rightarrow i_c = C\frac{dv_c}{dt}$$

- **A capacitor remains as a capacitor in the signal circuit.**
  - Since $V_C = const.$, $I_C = 0$,
    i.e., **A capacitor acts as an open circuit for bias circuit.**

Finding signal circuit elements – IVS & ICS

Independent voltage source	Voltage	Current	iv Equation
Bias + Signal:	v_{IVS}	i_{IVS}	$v_{IVS} = V_{DD} = const$
Bias:	V_{IVS}	I_{IVS}	$V_{IVS} = V_{DD} = const$
Signal:	$v_{ivs} = v_{IVS} - V_{IVS}$	$i_{ivs} = i_{IVS} - I_{IVS}$	**??**

$$v_{ivs} = v_{IVS} - V_{IVS} = V_{DD} - V_{DD} = 0 \quad \Rightarrow \quad v_{ivs} = 0, \quad i_{ivs} \neq 0$$

- **An independent voltage source becomes a short circuit!**

Similarly:

- **An independent current source becomes an open circuit!**

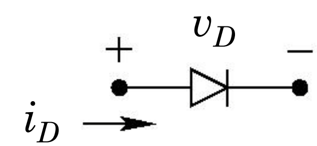
Exercise: Show that dependent sources remain as dependent sources

Summary of signal circuit elements

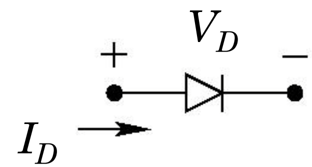
- **Resistors& capacitors:** **<u>The Same</u>**
  - Capacitor act as open circuit in the bias circuit.
- **Independent voltage source (e.g., V_{DD}) :** **<u>Effectively grounded</u>**
- **Independent current source:** **<u>Effectively open circuit</u>**
- **Dependent sources:** **<u>The Same</u>**
- **Non-linear Elements:** **<u>Different!</u>**
  - Diodes & transistors ?

Diode Signal Response

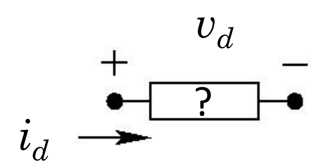
Bias + Signal: $i_D = I_s \exp\left(\dfrac{v_D}{nV_T}\right)$



Bias: $I_D = I_s \exp\left(\dfrac{V_D}{nV_T}\right)$



Signal: $i_d = i_D - I_D = I_s \exp\left(\dfrac{V_D + v_d}{nV_T}\right) - I_s \exp\left(\dfrac{V_D}{nV_T}\right)$



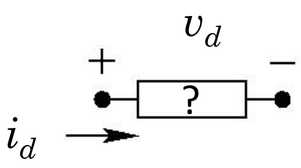
$$i_d = I_s \exp\left(\frac{V_D}{nV_T}\right) \times \left[\exp\left(\frac{v_d}{nV_T}\right) - 1\right]$$

$$\boxed{i_d = I_D \times \left[\exp\left(\frac{v_d}{nV_T}\right) - 1\right]}$$

- **A different iv equation!**
- **iv equation is non-linear!**
- **Related to bias value, I_D!**

Diode small-signal model:

$$\boxed{i_d = I_D \times \left[\exp\left(\frac{v_d}{nV_T}\right) - 1\right]}$$



Taylor Series Exapnsion : $\exp\left(\frac{v_d}{nV_T}\right) = 1 + \left(\frac{v_d}{nV_T}\right) + \frac{1}{2!}\left(\frac{v_d}{nV_T}\right)^2 + ...$

If $\frac{v_d}{nV_T} << 1$: $\exp\left(\frac{v_d}{nV_T}\right) \approx 1 + \left(\frac{v_d}{nV_T}\right)$

$$i_d \approx I_D \times \left[1 + \left(\frac{v_d}{nV_T}\right) - 1\right] = \left(\frac{I_D}{nV_T}\right) v_D$$

$$\boxed{v_d = \frac{nV_T}{I_D} i_d = r_d i_d}$$

Formal derivation of small signal model

- Signal + Bias for element A (i_A, v_A) : $i_A = \boldsymbol{f}\,(v_A)$
- Bias for element A (I_A, V_A) : $I_A = \boldsymbol{f}\,(V_A)$
- Signal for element A (i_a, v_a) : $i_a = \boldsymbol{g}\,(v_a)$

$$i_A = f(v_A)$$

$$= f(V_A) + f^{(1)}(V_A)\cdot(v_A - V_A) + \frac{f^{(2)}(V_A)}{2!}\cdot(v_A - V_A)^2 + \ldots$$

(Taylor Series Expansion)

$$= f(V_A) + f^{(1)}(V_A)\cdot v_a + \frac{f^{(2)}(V_A)}{2!}\cdot {v_a}^2 + \ldots$$

$$\approx f(V_A) + f^{(1)}(V_A)\cdot v_a$$

$$i_A = i_a + I_A = I_A + f^{(1)}(V_A)\cdot v_a$$

$$\boxed{i_a = g(v_a) = f^{(1)}(V_A)\cdot v_a}$$

Small signal means:

$$\left|f^{(1)}(V_A)\cdot v_a\right| >> \left|\frac{f^{(2)}(V_A)}{2!}\cdot {v_a}^2\right|$$

$$\left|v_a\right| << 2\cdot\left|\frac{f^{(1)}(V_A)}{f^{(2)}(V_A)}\right|$$

Derivation of diode small signal model

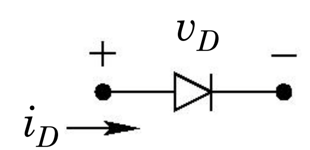
$$i_D = I_S \cdot \left(e^{\frac{v_D}{nV_T}} - 1 \right) = f(v_D) \quad \Longleftrightarrow \quad f(v) = I_S \left(e^{\frac{v}{nV_T}} - 1 \right) \qquad f^{(1)}(v) = \frac{1}{nV_T} \times I_S \, e^{\frac{v}{nV_T}}$$

$$I_D = f(V_D) = I_S \cdot \left(e^{\frac{V_D}{nV_T}} - 1 \right) = I_S \, e^{\frac{V_D}{nV_T}} - I_S$$

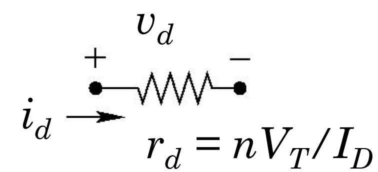
$$i_d = f^{(1)}(V_D) \times v_d = \left[\frac{I_S \cdot e^{\frac{v}{nV_T}}}{nV_T} \right]_{v=V_D} \times v_d = \left[\frac{I_S \cdot e^{\frac{V_D}{nV_T}}}{nV_T} \right] \times v_d = \left[\frac{I_D + I_S}{nV_T} \right] \times v_d$$

$$i_d = \left[\frac{I_D + I_S}{nV_T} \right] \times v_d \approx \left[\frac{I_D}{nV_T} \right] \times v_d$$

$$\boxed{ i_d = \frac{v_d}{r_d} \qquad\qquad r_d \approx \frac{nV_T}{I_D} }$$



Diode can be replaced with a resistor in the signal circuit!

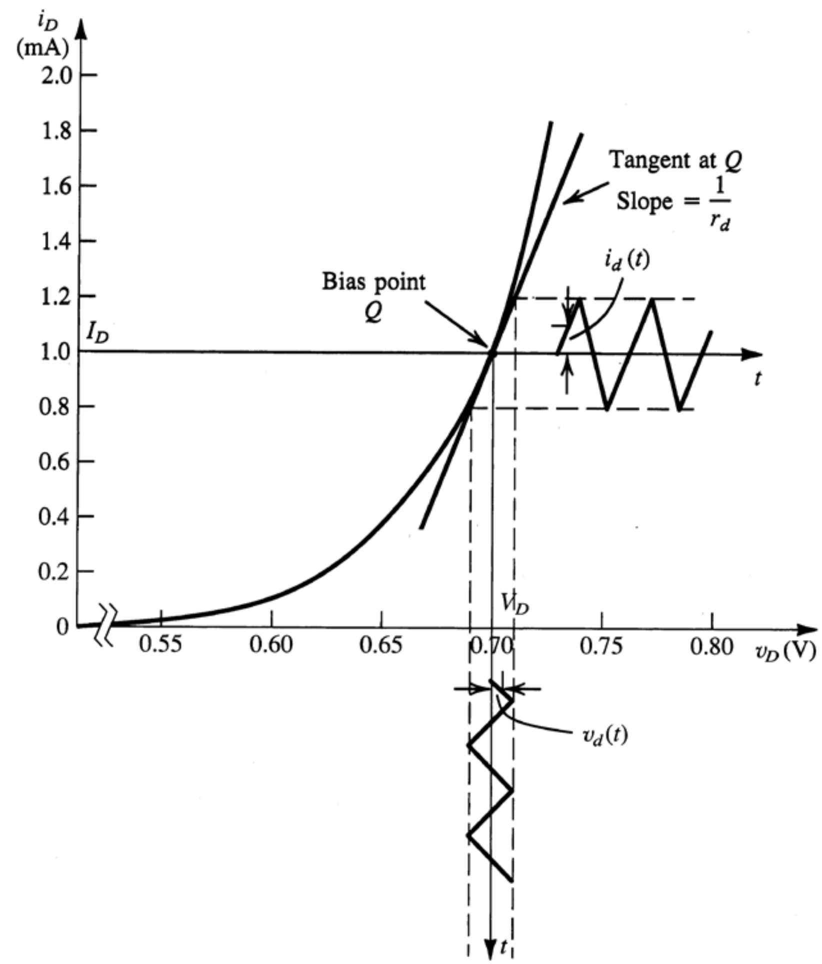


Small signal model vs iv characteristics

Small signal model is equivalent to approximating the non-liner iv characteristics curve by <u>a line tangent to the iv curve at the bias point</u>

$$i_d = f^{(1)}(V_D) \times v_d$$

$$r_d = \frac{1}{f^{(1)}(V_D)} \approx \frac{nV_T}{I_D}$$



Derivation of MOS small signal model (1)

MOS iv equations: $i_D = f\,(v_{GS}, v_{DS})$
$i_G = 0$

- Signal + Bias for MOS (i_D, v_{GS} , v_{DS}) : $i_D = \boldsymbol{f}\,(v_{GS}, v_{DS})$, $i_G = 0$
- Bias for MOS (I_D, V_{GS} , V_{DS}) : $I_D = \boldsymbol{f}\,(V_{GS}, V_{DS})$, $I_G = 0$
- Signal for MOS (i_d, v_{gs} , v_{ds}) : $i_d = \boldsymbol{g}\,(v_{gs}\,, v_{ds})$, $i_g = 0$

$I_D + i_d = i_D = f\,(v_{GS}, v_{DS})$ (Taylor Series Expansion in 2 variables)

$$= f\,(V_{GS}, V_{DS}) + \left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS}, V_{DS}} \cdot (v_{GS} - V_{GS}) + \left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS}, V_{DS}} \cdot (v_{DS} - V_{DS}) + \ldots$$

$$\approx \quad I_D \quad + \left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS}, V_{DS}} \times v_{gs} + \left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS}, V_{DS}} \times v_{ds}$$

$$\Rightarrow \quad \boxed{i_d \approx \left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS}, V_{DS}} \times v_{gs} + \left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS}, V_{DS}} \times v_{ds}}$$

Derivation of MOS small signal model (2)

$$i_D = 0.5\mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t)^2 (1 + \lambda v_{DS}) = f(v_{GS}, v_{DS})$$

$$i_d = \left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS}, V_{DS}} \cdot v_{gs} + \left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS}, V_{DS}} \cdot v_{ds}$$

$$\left.\frac{\partial f}{\partial v_{GS}}\right|_{V_{GS}, V_{DS}} = 2 \times 0.5\mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t)(1 + \lambda v_{DS}) \Big|_{V_{GS}, V_{DS}}$$

$$= 2 \times \frac{0.5\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2 (1 + \lambda V_{DS})}{(V_{GS} - V_t)} = \frac{2 I_D}{V_{OV}} \equiv g_m$$

$$\left.\frac{\partial f}{\partial v_{DS}}\right|_{V_{GS}, V_{DS}} = \lambda \times 0.5\mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t)^2 \Big|_{V_{GS}, V_{DS}}$$

$$= \lambda \times \frac{0.5\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2 (1 + \lambda V_{DS})}{(1 + \lambda V_{DS})} = \frac{\lambda I_D}{(1 + \lambda V_{DS})} \approx \lambda I_D \equiv \frac{1}{r_o}$$

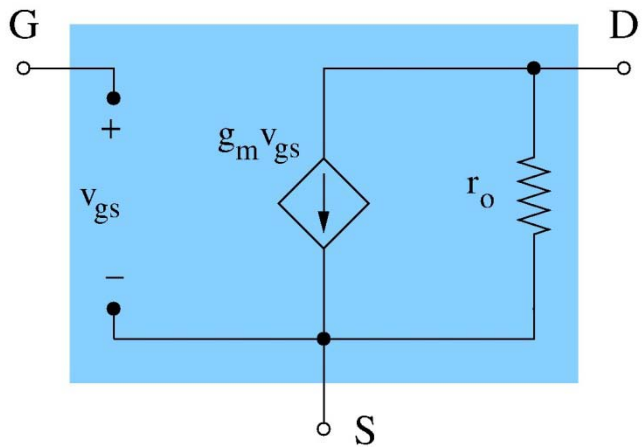
$$\boxed{i_d = g_m \cdot v_{gs} + \frac{v_{ds}}{r_o} \qquad i_g = 0}$$

MOS small signal "circuit" model

$$i_g = 0 \quad \text{and} \quad i_d = g_m \cdot v_{gs} + \frac{v_{ds}}{r_o}$$

Input open circuit

Statement of KCL
Two elements in parallel



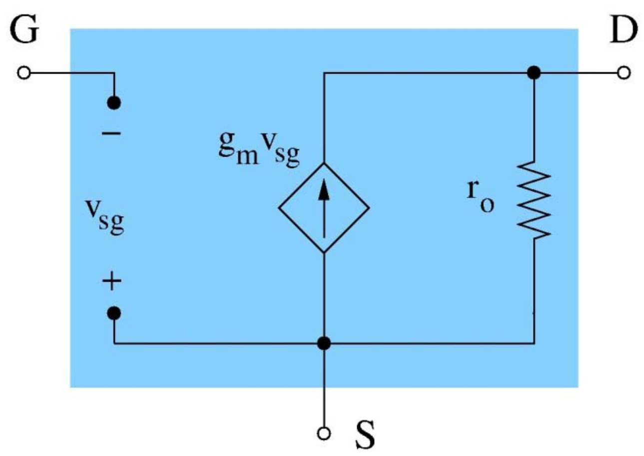
$$g_m = \frac{2 \cdot I_D}{V_{OV}}$$

$$r_o \approx \frac{1}{\lambda \cdot I_D}$$

$$g_m r_o = \frac{2}{\lambda V_{OV}} = \frac{2V_A}{V_{OV}} >> 1$$

PMOS small signal model is identical to NMOS

PMOS*



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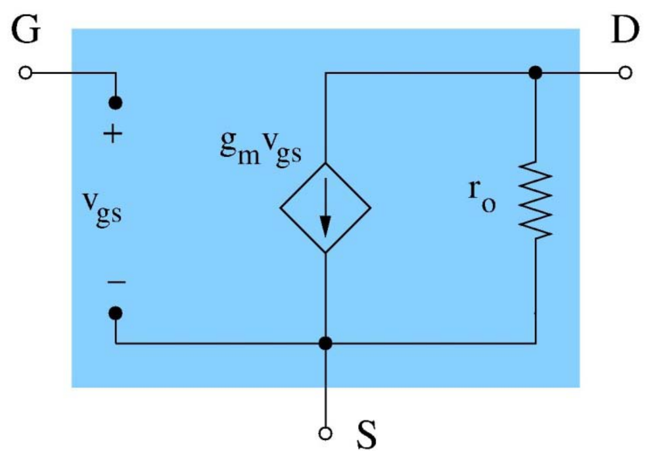
NMOS



- **PMOS small-signal circuit model is identical to NMOS**
  - We will use NMOS circuit model for both!
  - For both NMOS and PMOS, while $i_D \geq 0$ and $I_D \geq 0$, signal quantities: i_d, v_{gs}, and v_{ds} , can be negative!

Exercise: Derive PMOS small signal model (follow derivation of NMOS small-signal model)

Derivation of BJT small signal model (1)

BJT iv equations: $i_B = f_1\,(v_{BE})$
$i_C = f_2\,(v_{BE}, v_{CE})$

$$i_B = (I_s/\beta)\; e^{\frac{v_{BE}}{V_T}}$$

$$i_C = I_s\, e^{\frac{v_{BE}}{V_T}} \left(1 + \frac{v_{CE}}{V_A}\right)$$

- Signal + Bias for BJT (i_B, i_C, v_{BE} , v_{CE}) : $i_B = \boldsymbol{f_1}\,(v_{BE})$, $i_C = \boldsymbol{f_2}\,(v_{BE}, v_{CE})$
- Bias for BJT (I_B, I_C, V_{BE} , V_{CE}) : $I_B = \boldsymbol{f_1}\,(V_{BE})$, $I_C = \boldsymbol{f_2}\,(V_{BE}, V_{CE})$
- Signal for BJT (i_b, i_c, v_{be} , v_{ce}) : $i_b = \boldsymbol{g_1}\,(v_{be})$, $i_c = \boldsymbol{g_2}\,(v_{be}, v_{ce})$

We need to perform Taylor Series Expansion in 2 variables for both i_B and i_C.

$$i_b \approx \left.\frac{df_1}{dv_{BE}}\right|_{V_{BE}, V_{CE}} \times v_{be}$$

$$i_c \approx \left.\frac{\partial f_2}{\partial v_{BE}}\right|_{V_{BE}, V_{CE}} \times v_{be} + \left.\frac{\partial f_2}{\partial v_{DCE}}\right|_{V_{BE}, V_{CE}} \times v_{ce}$$

Derivation of BJT small signal model (2)

$$i_B = (I_s/\beta)\ e^{\frac{v_{BE}}{V_T}} = f_1(v_{BE})$$

$$I_B = (I_s/\beta)\ e^{\frac{V_{BE}}{V_T}}$$

$$\left.\frac{df_1}{dv_{BE}}\right|_{V_{BE},V_{CE}} = \frac{1}{V_T}(I_s/\beta)\ \left. e^{\frac{v_{BE}}{V_T}}\right|_{V_{BE}} = \frac{I_B}{V_T} \equiv \frac{1}{r_\pi}$$

$$i_b \approx \left.\frac{df_1}{dv_{BE}}\right|_{V_{BE},V_{CE}} \times v_{be} = \frac{1}{r_\pi} \times v_{be}$$

$$i_C = I_s\ e^{\frac{v_{BE}}{V_T}}\left(1+\frac{v_{CE}}{V_A}\right)$$

$$I_C = I_s\ e^{\frac{V_{BE}}{V_T}}\left(1+\frac{V_{CE}}{V_A}\right) = I_s\ e^{\frac{V_{BE}}{V_T}} \times \frac{V_A+V_{CE}}{V_A}$$

$$\left.\frac{df_2}{dv_{BE}}\right|_{V_{BE},V_{CE}} = \left.\frac{I_s}{V_T}\ e^{\frac{v_{BE}}{V_T}}\left(1+\frac{v_{CE}}{V_A}\right)\right|_{V_{BE},V_{CE}} = \frac{I_C}{V_T} \equiv g_m$$

$$\left.\frac{df_2}{dv_{CE}}\right|_{V_{BE},V_{CE}} = \left.\frac{I_s}{V_A}\ e^{\frac{v_{BE}}{V_T}}\right|_{V_{BE},V_{CE}} = \frac{I_C}{V_A + V_{CE}} \equiv \frac{1}{r_o}$$

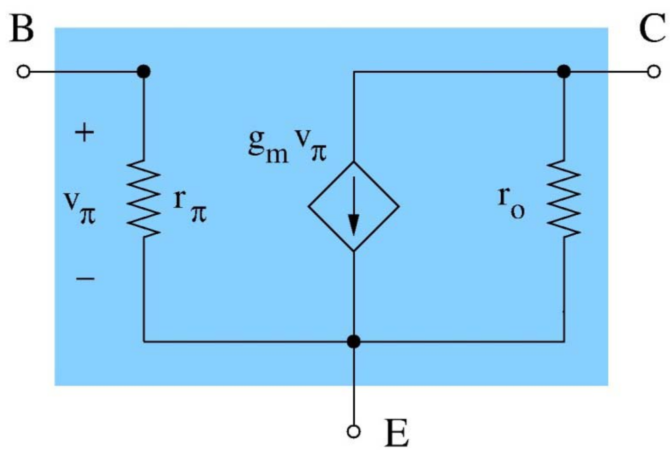
$$\boxed{i_b = \frac{v_{be}}{r_\pi} \qquad i_c = g_m v_{be} + \frac{v_{ce}}{r_o}}$$

BJT small signal "circuit" model

$$i_b = \frac{v_{be}}{r_\pi} \qquad i_c = g_m v_{be} + \frac{v_{ce}}{r_o}$$

A resistor, r_π, between B & E

Statement of KCL
Two elements in parallel



$$r_\pi = \frac{V_T}{I_B}$$

$$g_m = \frac{I_C}{V_T}$$

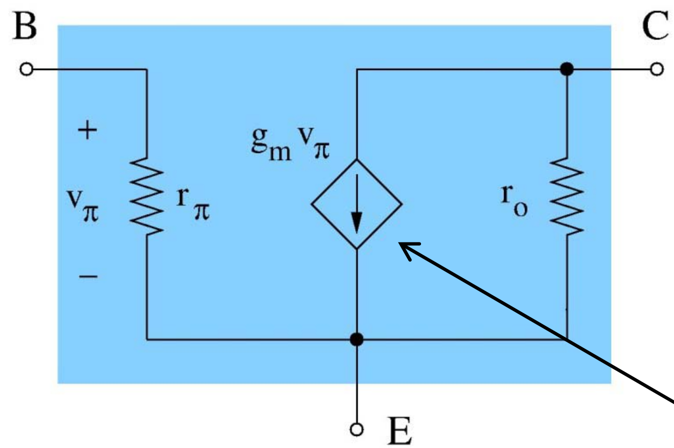
We follow S&S:
v_{be} is denoted as v_π

$$r_o = \frac{V_A + V_{CE}}{I_C} \approx \frac{V_A}{I_C}$$

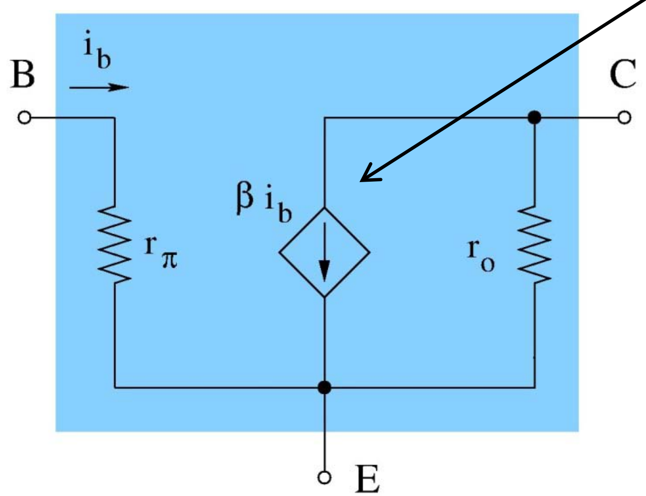
Similar to NMOS/PMOS, the small circuit model for a PNP BJT is the same as that of a NPN.

Alternative BJT small signal "circuit" model

g_m Model



$\beta\, i_b$ Model



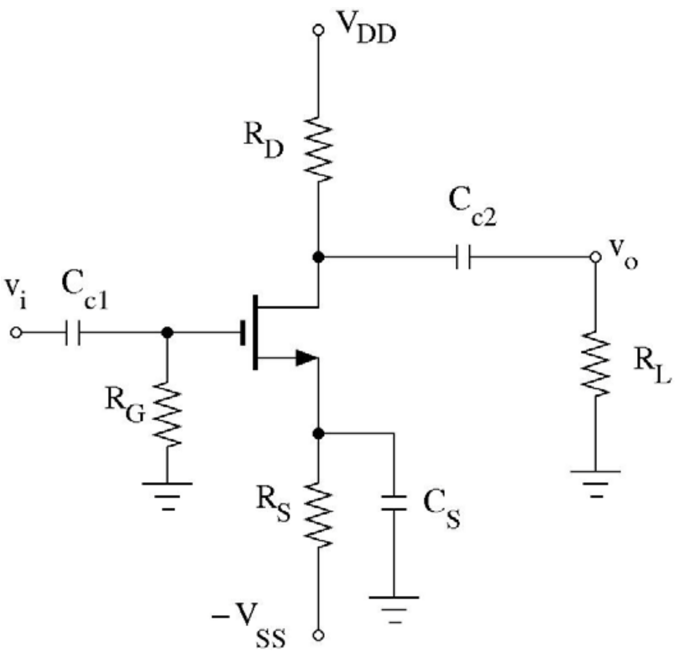
$$g_m = \frac{I_C}{V_T} = \frac{I_C}{I_B} \times \frac{I_B}{V_T} = \frac{\beta}{r_\pi}$$

$$g_m v_\pi = \frac{\beta}{r_\pi} \times v_\pi = \beta\, i_\pi$$

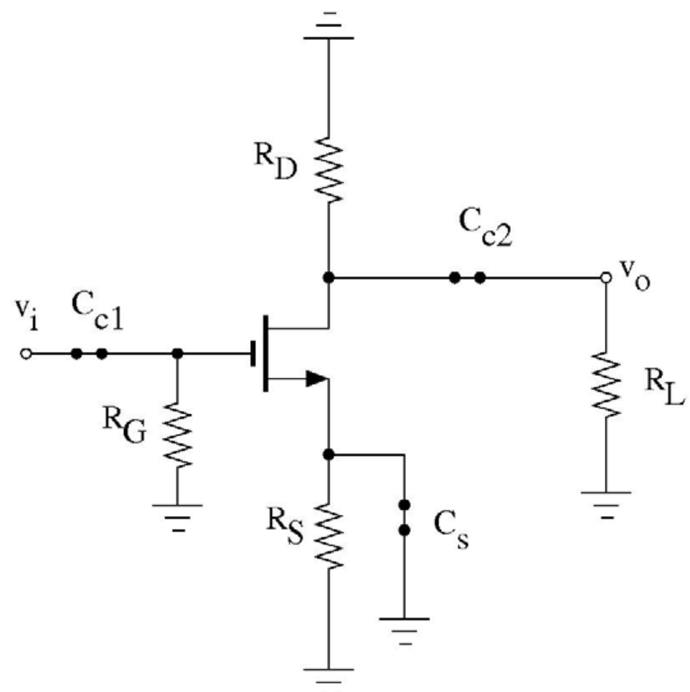
Summary of transistor small signal models

$$\boxed{g_m = \frac{2 \cdot I_D}{V_{OV}} \qquad r_o \approx \frac{1}{\lambda \cdot I_D}}$$

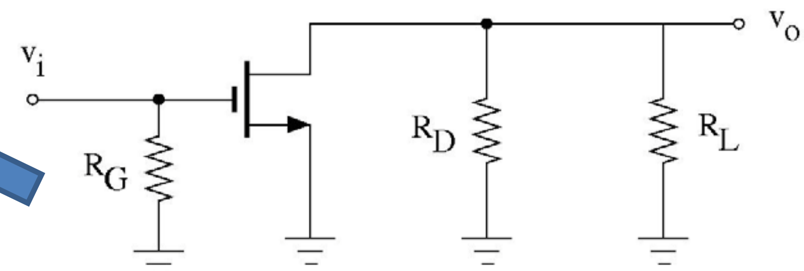
Example 1: Construct the signal circuit and replace the transistor with its small-signal model (assume capacitors are short for signal).



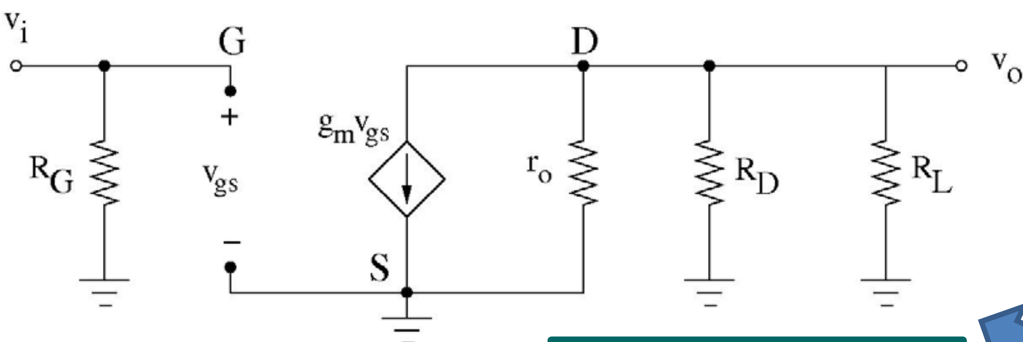
IVS → 0
R remains
Caps short



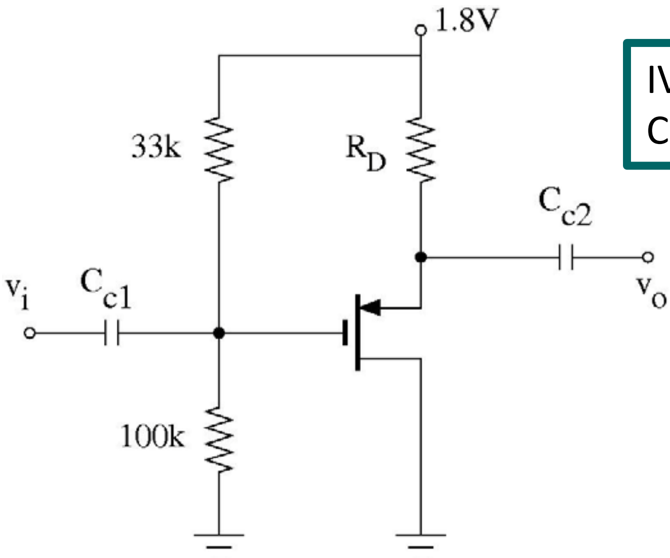
Ground at the bottom



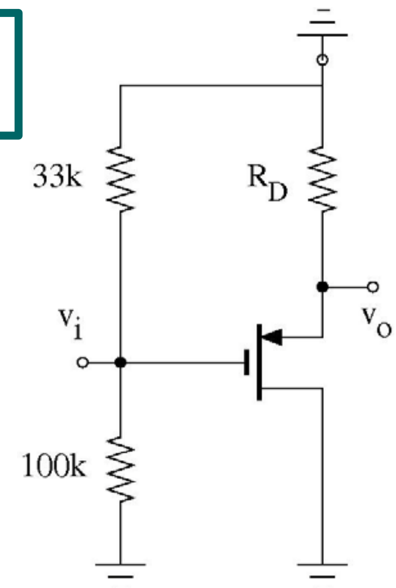
Replace MOS with its small signal model



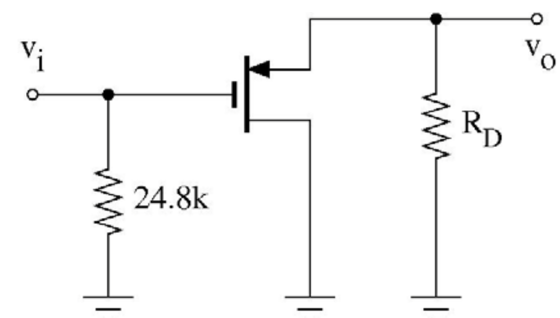
Example 2: Construct the signal circuit and replace the transistor with its small-signal model (assume capacitors are short for signal).



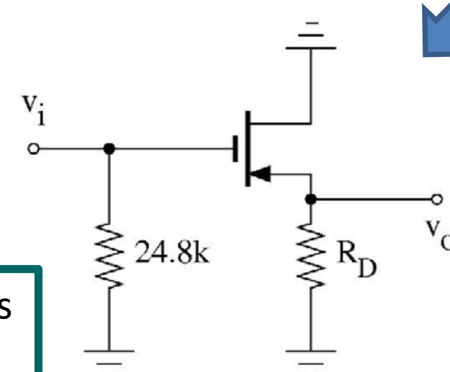
IVS $\rightarrow$ 0
Caps short



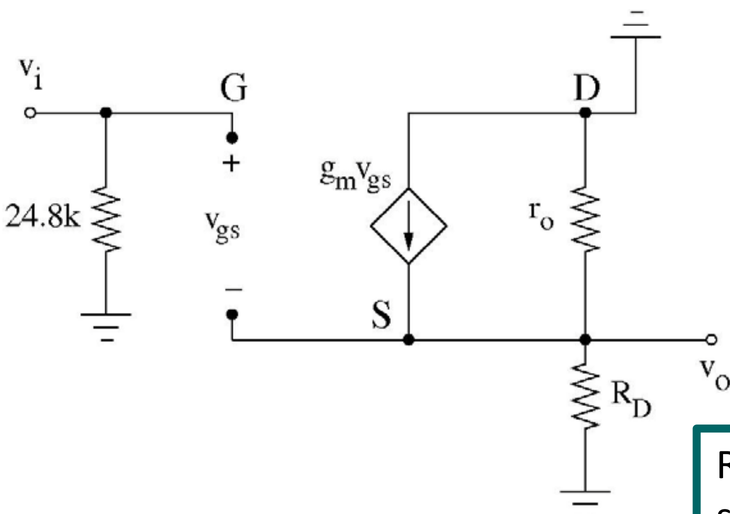
Ground at the bottom
(100k || 33k = 24.8 k)



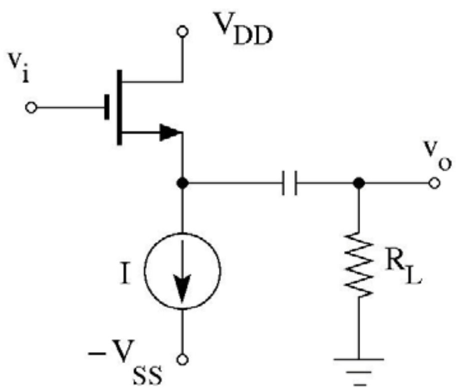
Flip PMOS



Replace MOS with its small signal model

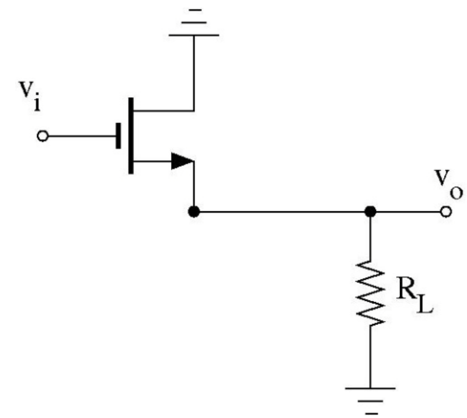


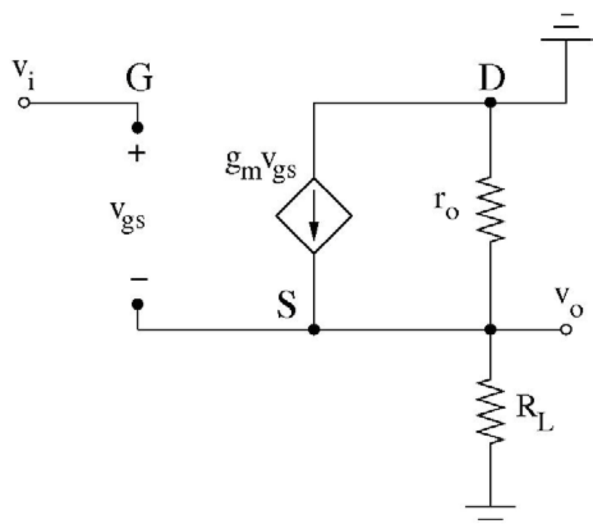
Example 3: Construct the signal circuit and replace the transistor with its small-signal model (assume capacitors are short for signal).



IVS $\rightarrow$ 0
Caps short

ICS $\rightarrow$ 0
(This makes ICS an open circuit)





Replace MOS with its small signal model