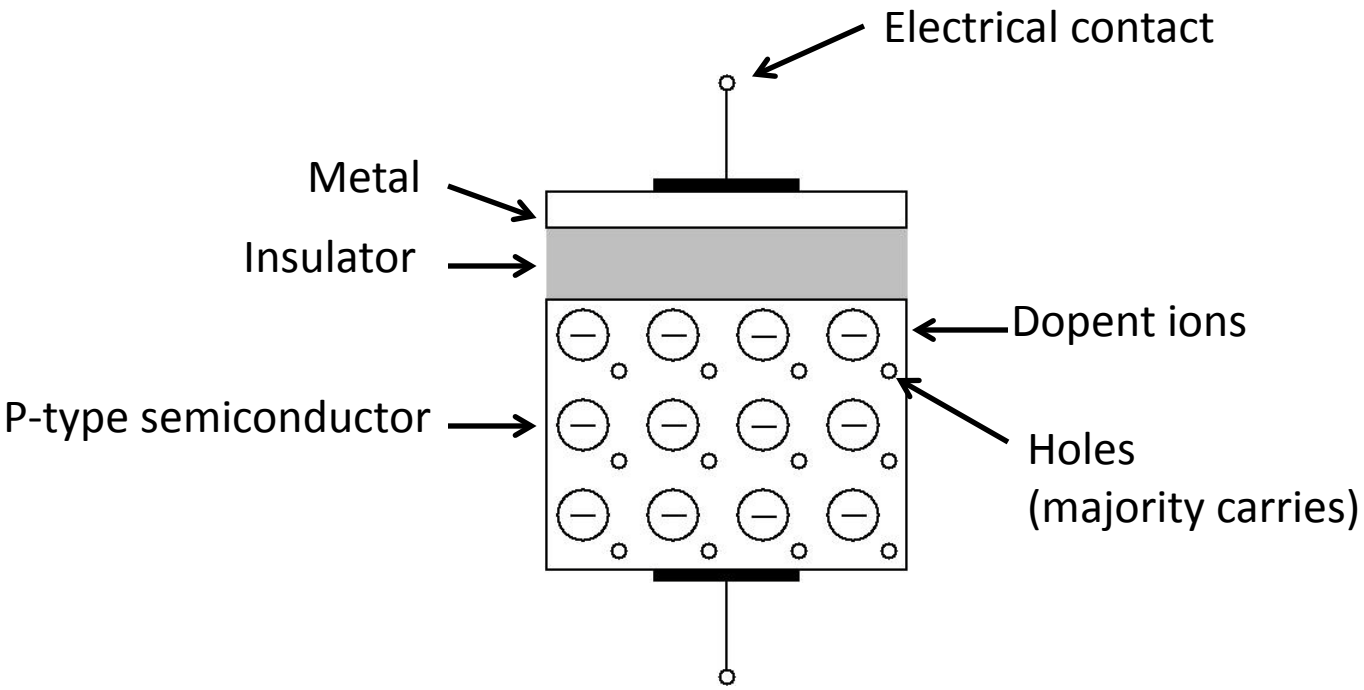
4. MOS: Device Operation and Large Signal Model

Lecture notes: Sec. 4

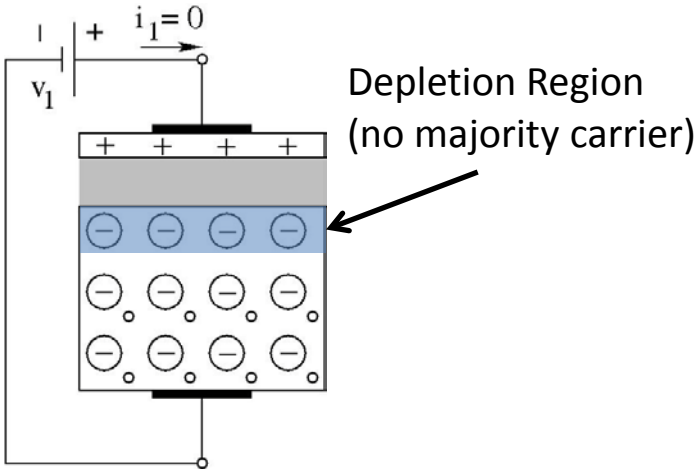
Sedra & Smith (6th Ed): Sec. 5.1-5.3
Sedra & Smith (5th Ed): Sec. 4.1-4.3

Operational Basis of a Field-Effect Transistor (1)

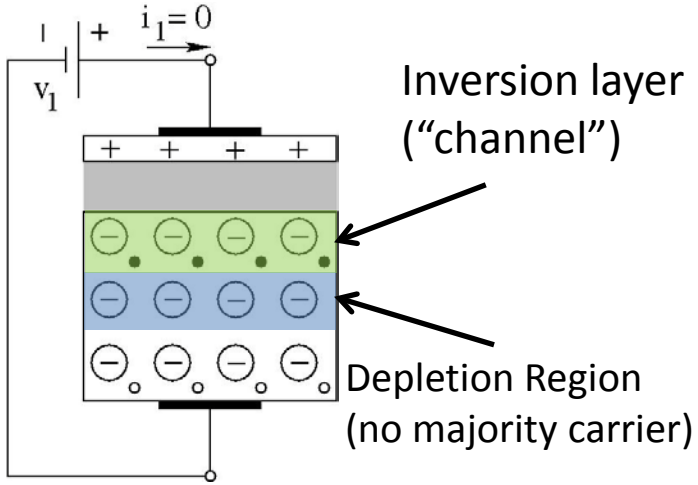
Consider the **hypothetical** semiconductor below:
(constructed similar to a parallel plate capacitor)



Operational Basis of a Field-Effect Transistor (2)



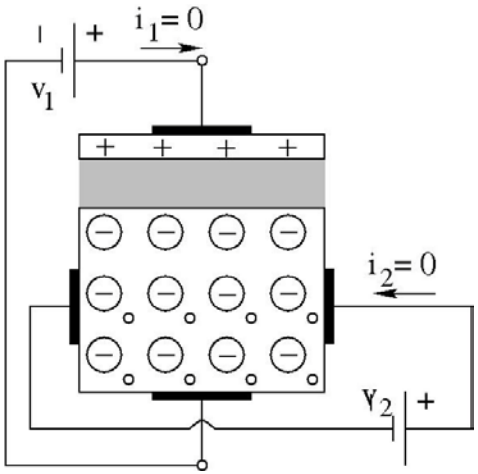
- If we apply a voltage v_1 between electrodes, a charge $Q = C\, v_1$ will appear on each capacitor plate.
  - The electric field is strongest at the interface with the insulator and charge likes to accumulate there.
- Holes are pushed away from the insulator interface forming a "depletion region".
- Depth of depletion region increases with v_1.



- If we increase v_1 above a threshold value (V_t), the electric field is strong enough to "pull" free electrons to the insulator interface. As the holes are repelled in this region, a "channel" is formed which contains electrons in the conduction band ("inversion layer").
- **Inversion layer is a "virtual" n-type material.**

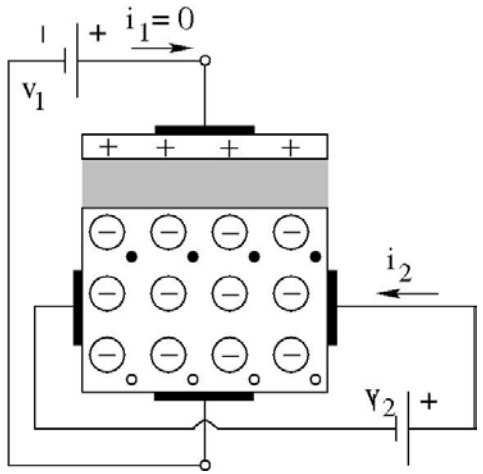
Operational Basis of a Field-Effect Transistor (3)

- We apply a voltage across the p-type semiconductor: (Assume current flows only in the n-type material, ignore current flowing in the p-type semiconductor)



No inversion layer $(v_1 < V_t)$:

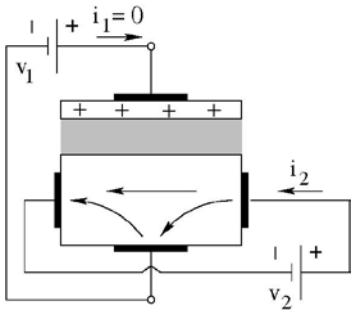
- No current will flow



With inversion layer $(v_1 > V_t)$:

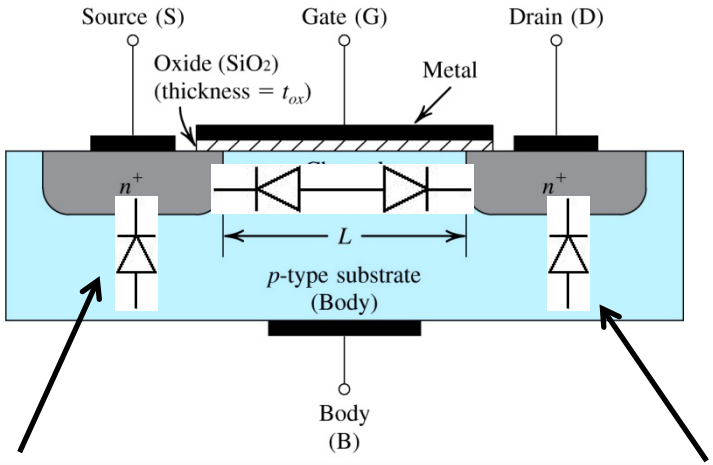
- A current will flow in the channel
- Current will be proportional to electron charge in the channel or $(v_1 - V_t)$
- **Magnitude of Current i_2 is controlled by voltage v_1 (a Transistor!)**

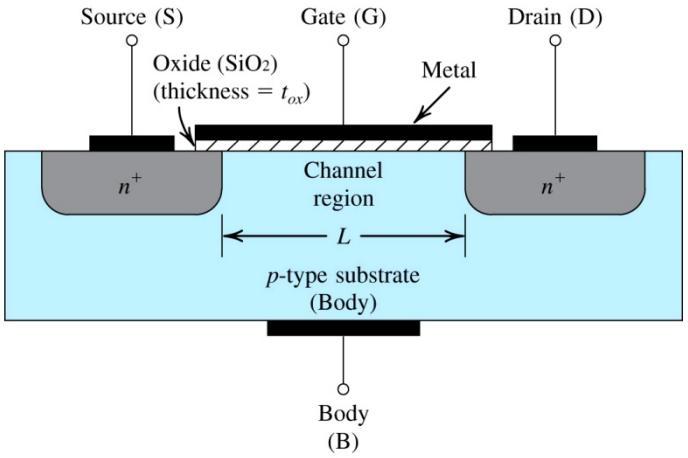
Operational Basis of a Field-Effect Transistor (4)



- We need to eliminate currents flowing in the p-type, i.e., current flows only in the "channel" which is a virtual n-type.

- Make n-type material terminals (set up diodes between terminals & p-type "body")
- Heavy doping of the n-type terminals provides a source of free electrons for the channel.
- Make insulator layer as thin as possible to increase the electric field.

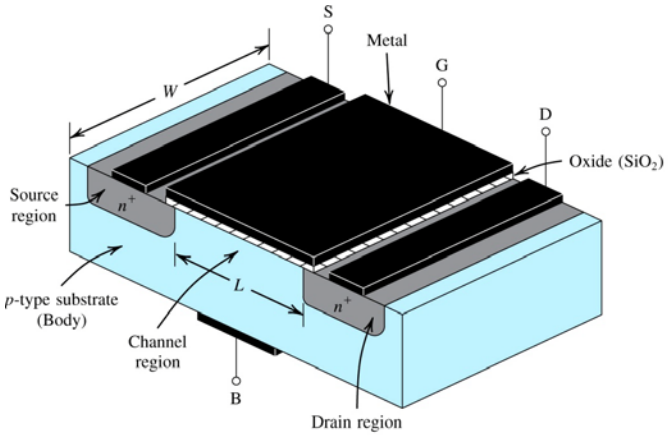




- Body-source and body-drain junctions should always be in reverse bias for FET to work!

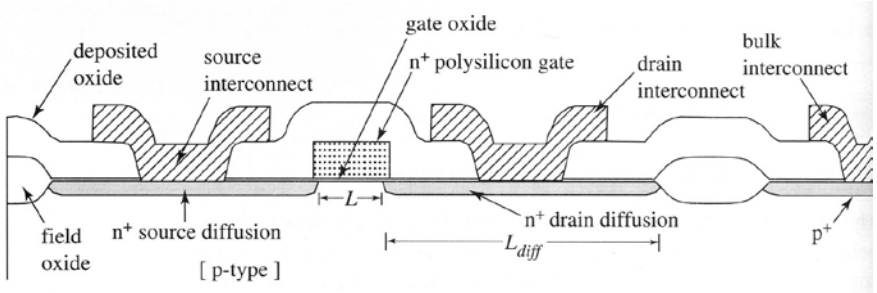
Channel width (L) is the smallest feature on the chip surface

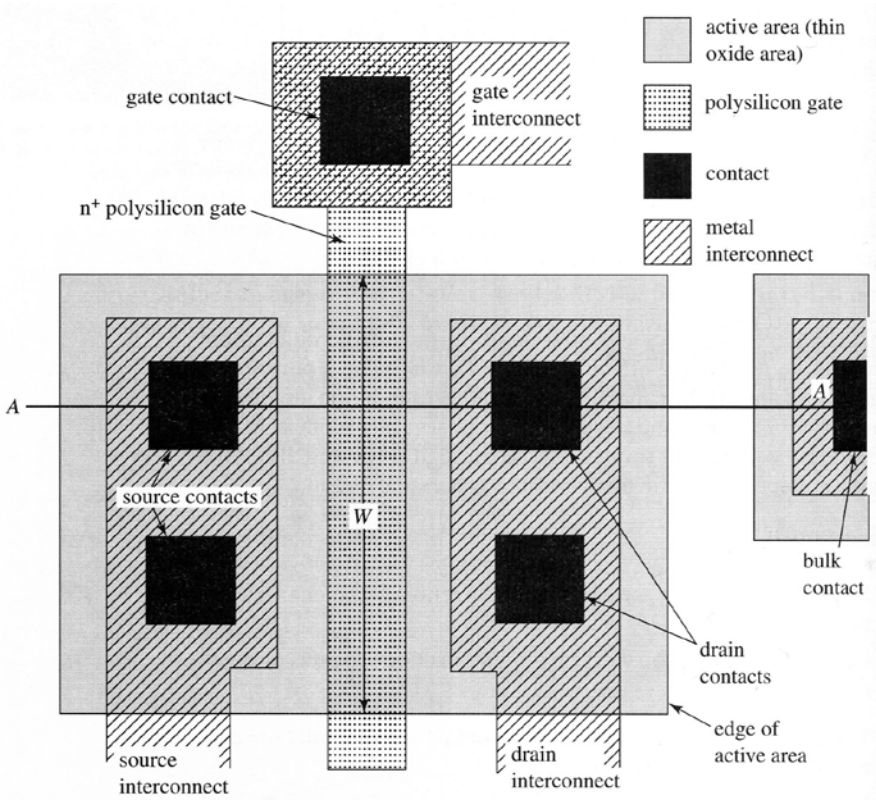
MOSFET "cartoons" for deriving MOSFET characteristics



MOSFET (or MOS): Metal-oxide field-effect transistor
NMOS: n-channel enhancement MOS

MOSFET implementation on a chip





NMOS i-v Characteristics (1)

- To ensure that body-source and body-drain junctions are reversed bias, we assume that Body and Source are connected to each other and $v_{DS} \geq 0$.
  - *We will re-examine this assumption later*

- Without a channel, no current flows ("Cut-off").
- For $v_{GS} > V_{tn}$, a channel is formed. The total charge in the channel is

$$|Q| = CV = C_{ox}WL\,(v_{GS}\text{-}V_{tn})$$

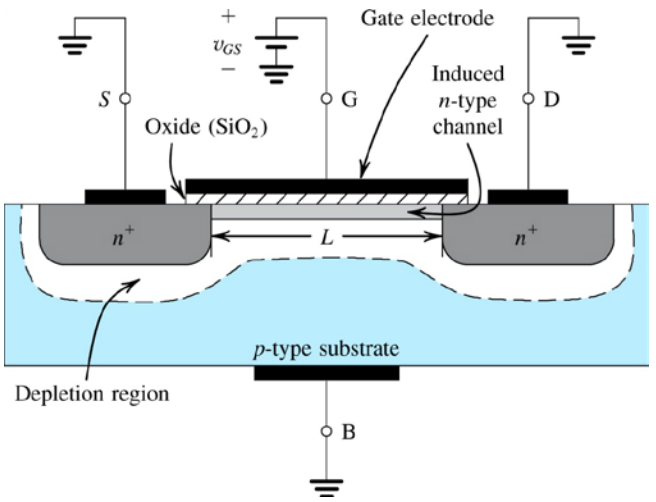
$$C = C_{ox}\,W\,L$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}: \text{ Capacitance per unit area}$$

t_{ox} : Thickness of insulator

ε_{ox} : permitivity of insulator

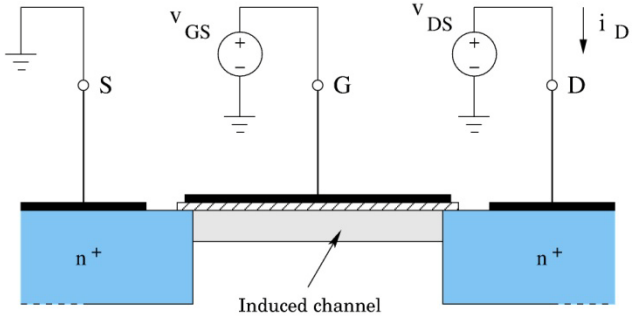
$$\varepsilon_{ox} = 3.9\varepsilon_0 = 3.45\times10^{-11}\ \text{F/m (for SiO}_2\text{)}$$



Overdrive Voltage: $V_{OV} = v_{GS} - V_{tn}$

NMOS i-v Characteristics (2)

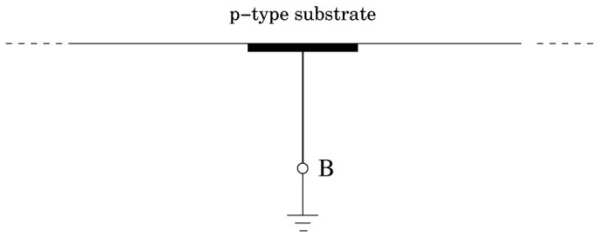
- $v_{GS} > V_{tn}$ A channel is formed
- **Apply a small v_{DS} between drain & source.**



- A current flows due to the "drift" of electrons in the n-channel:

$$i_D = \mu_n C_{ox} \frac{W}{L}(v_{GS} - V_{tn})v_{DS}$$

$$i_D = \mu_n C_{ox} \frac{W}{L} V_{OV} v_{DS}$$



For small v_{DS}, MOS acts as a resistance with its conductivity controlled by V_{OV} (or v_{GS}).

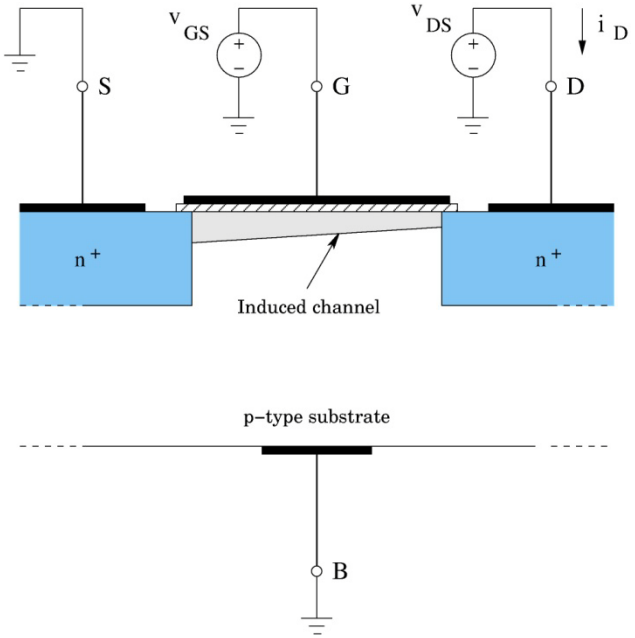
$$i_D = g_{DS} v_{DS} \quad \text{with} \quad g_{DS} = \mu_n C_{ox} \frac{W}{L} V_{OV}$$

NMOS i-v Characteristics (4)

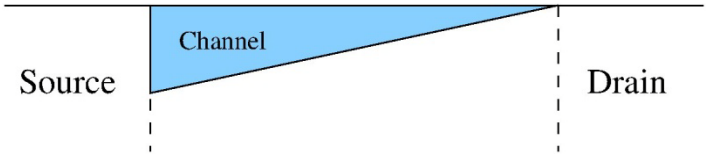
- When v_{DS} is increased the channel becomes narrower near the drain (local depth of the channel depends on the difference between V_G and local voltage).

Triode Mode

$$i_D = \mu_n C_{ox} \frac{W}{L}\left[V_{OV} v_{DS} - 0.5 v_{DS}^2\right]$$



- When v_{DS} is increased further such that $v_{DS} = V_{OV}$, the channel depth becomes zero at the drain (Channel "pinched off").
- When v_{DS} is increased further, $v_{DS} > V_{OV}$, the location of channel pinch-off remains close to the drain and i_D remains approximately constant.

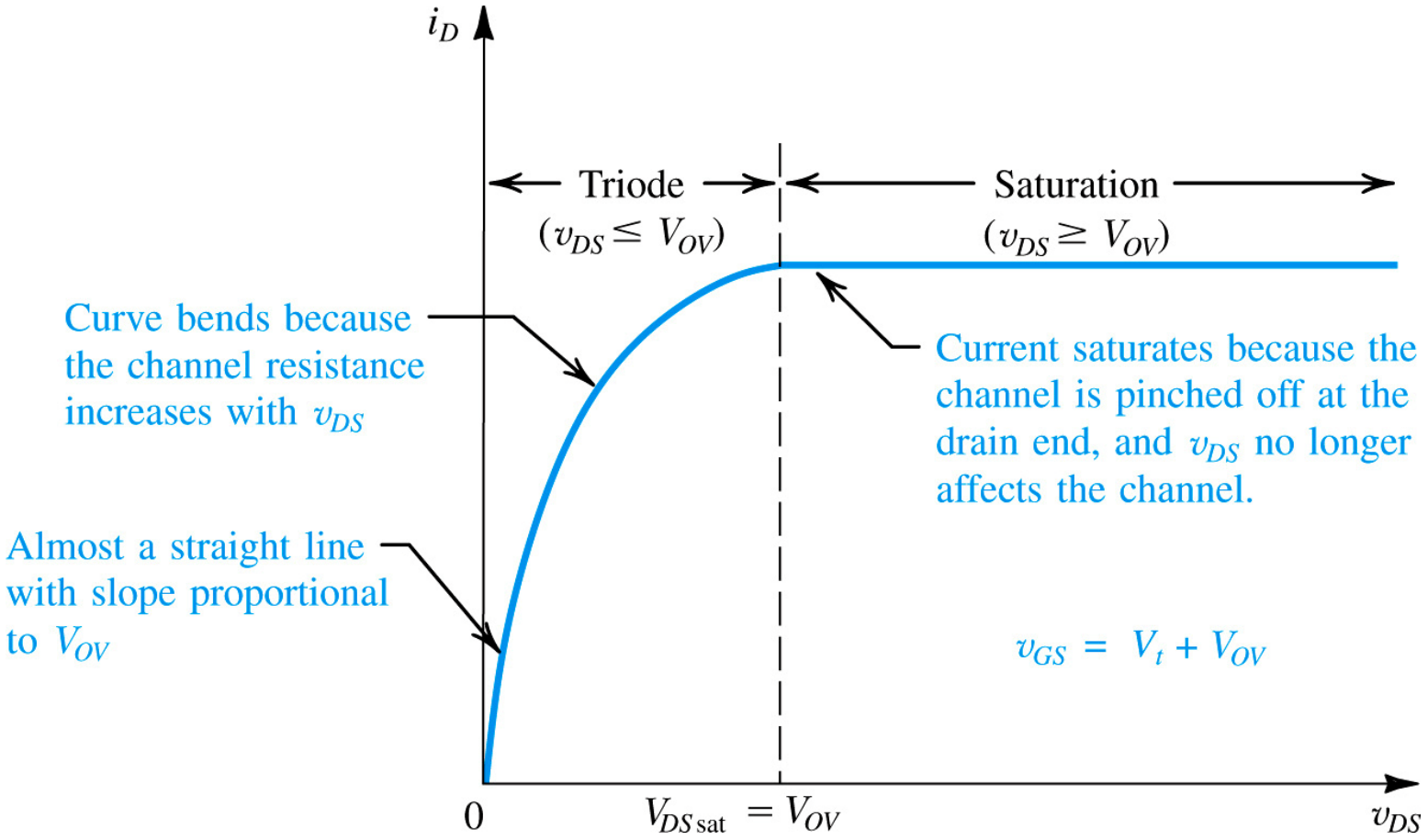


Saturation Mode

$$i_D = 0.5 \mu_n C_{ox} \frac{W}{L} V_{OV}^2$$

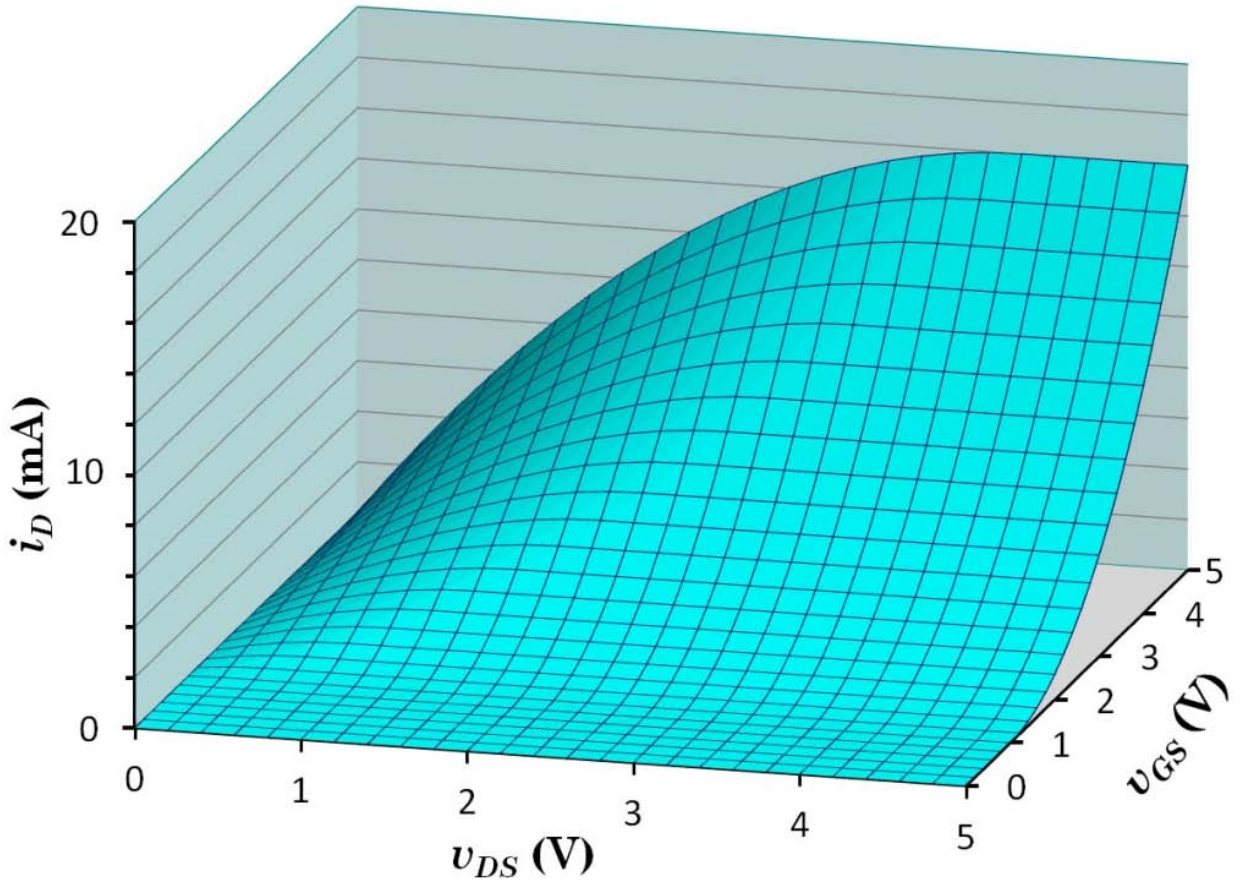
NMOS i-v Characteristics (5)

For a given v_{GS} (or V_{OV})



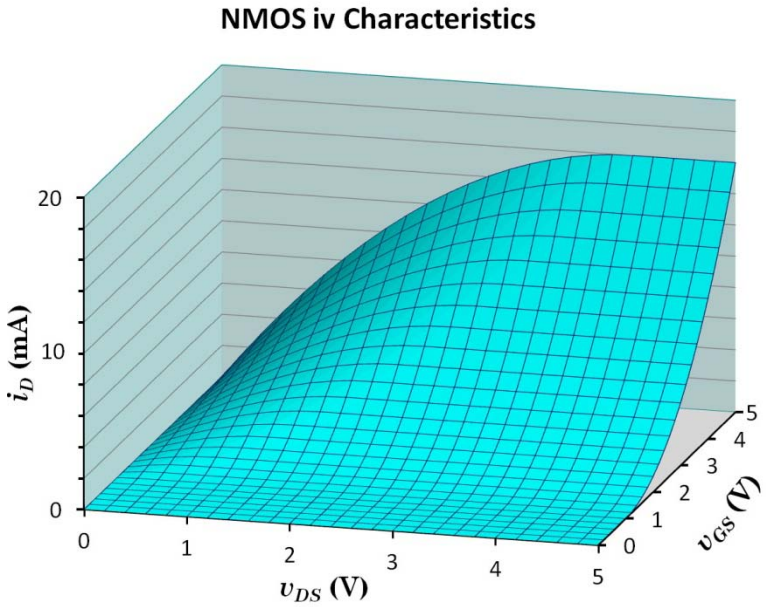
NMOS i-v Characteristics Plot (1)

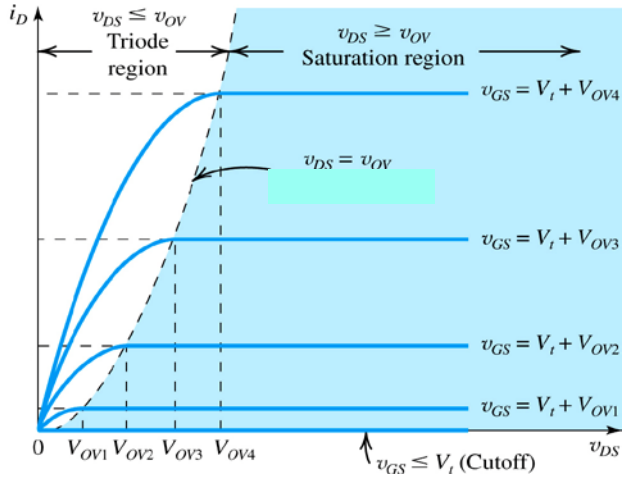
- NMOS i-v characteristics $i_D = f(v_{GS}, v_{DS})$ is a surface



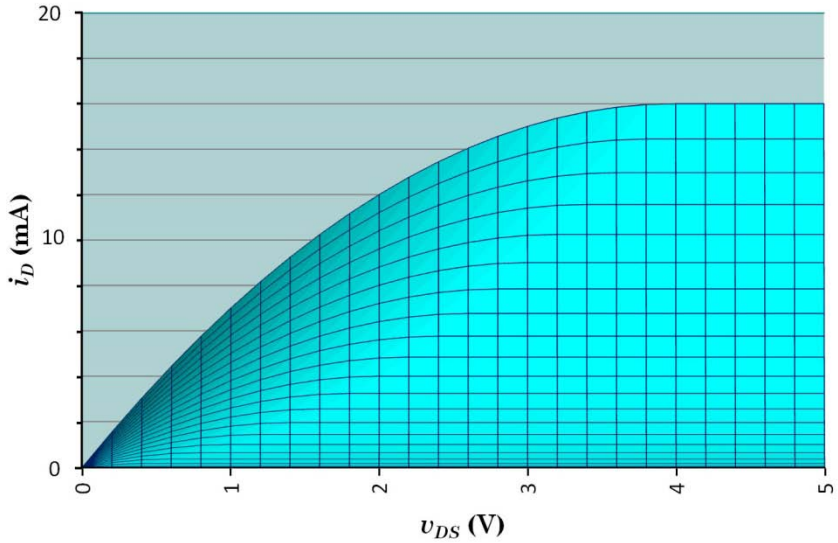
* Plot for $V_{t,n} = 1$ V and $\mu_n C_{ox}\,(W/L) = 2.0$ mA/V^2

NMOS i-v Characteristics Plot (2)



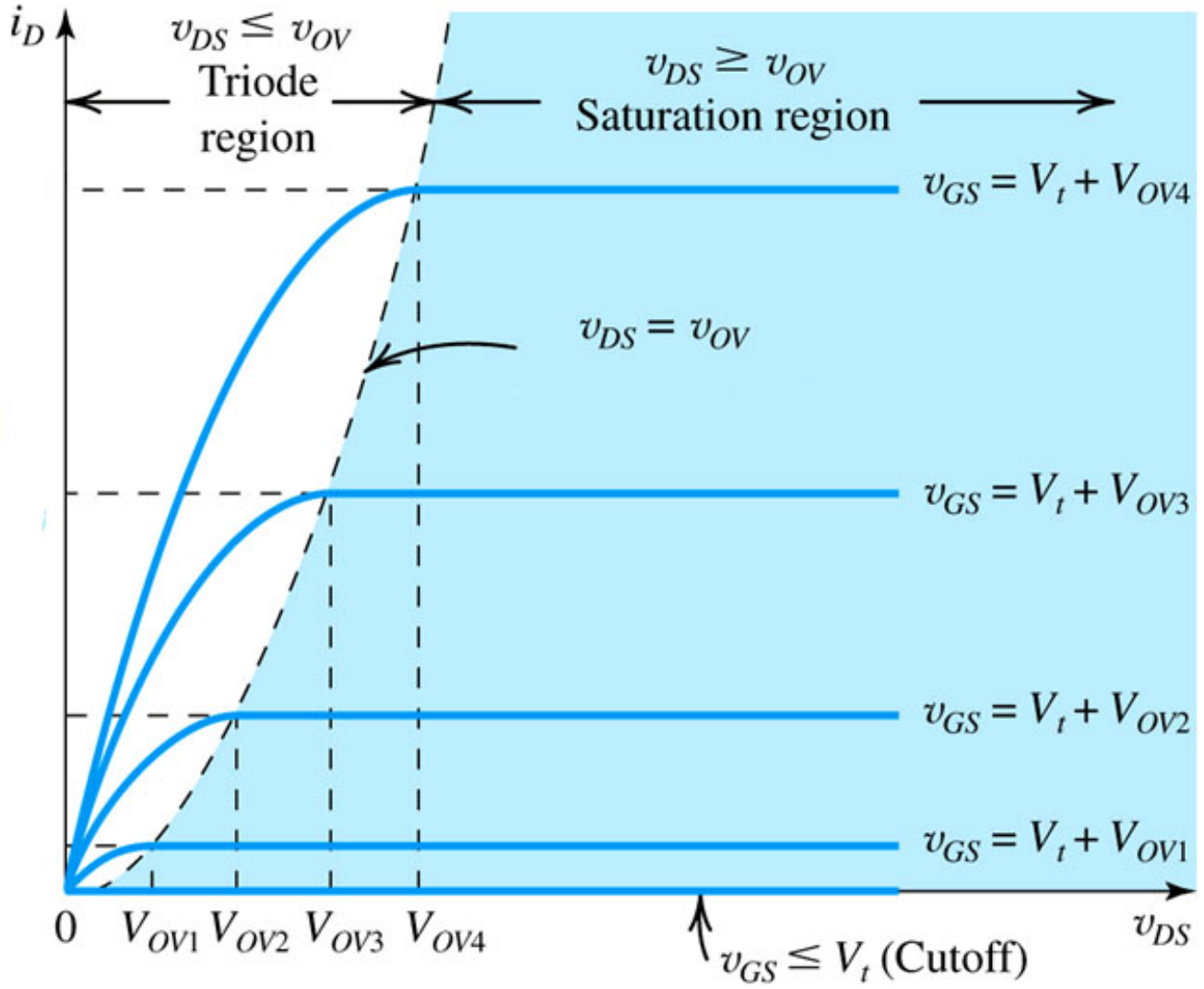


Looking at surface with v_{GS} axis pointing out of the paper*



*Note: surface was truncated (i.e., $v_{GS} < 5$ V)

NMOS i-v Characteristics Plot (3)

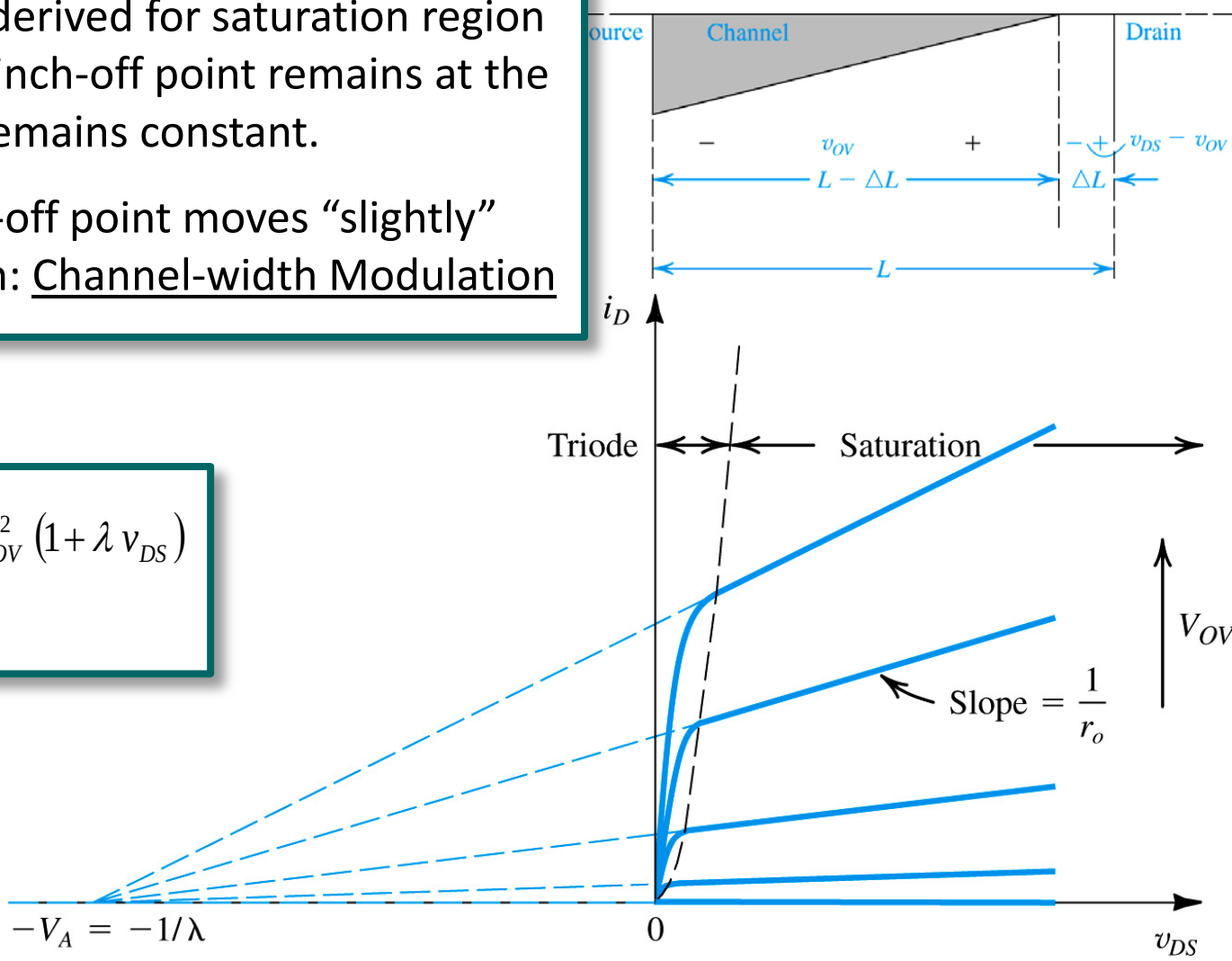


Channel-Width Modulation

- The expression we derived for saturation region assumed that the pinch-off point remains at the drain and thus i_D remains constant.
- In reality, the pinch-off point moves "slightly" away from the drain: Channel-width Modulation

$$i_D = 0.5\mu_n C_{ox}\frac{W}{L}V_{OV}^2\left(1+\lambda v_{DS}\right)$$

$$\lambda = 1/V_A$$



Body Effect

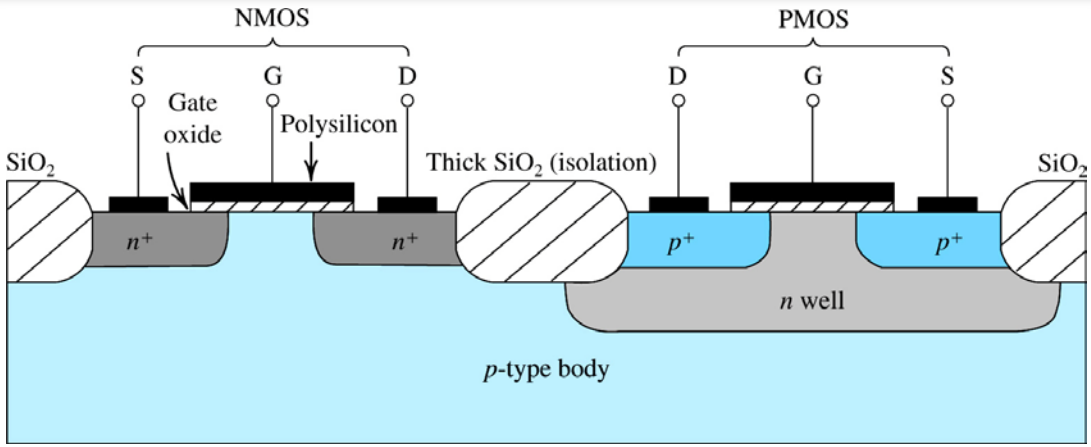
- Recall that Drain-Body and Source-Body diodes should be reversed biased.
  - We assumed that Source is connected to the body ($v_{SB} = 0$) and $v_{DS} = v_{DB} > 0$
- In a chip (same body for all NMOS), it is impossible to connect all sources to the body (all NMOS sources are connected together.
- Thus, the body (for NMOS) is connected to the largest negative voltage (negative terminal of the power supply).
- Doing so, changes the threshold voltage (called "Body Effect")

$$V_{tn} = V_{tn,0} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

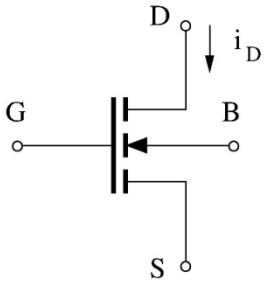
- **In this course we will ignore body effect as well as other second-order effects such as velocity saturation.**

P-channel Enhancement MOS (PMOS)

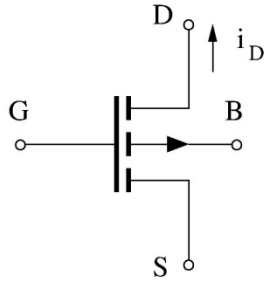
- A PMOS can be constructed analogous to an NMOS: (n-type body), heavily doped p-type source and drain.
- A virtual "p-type" channel is formed in a P-MOS (holes are carriers in the channel) by applying a negative v_{GS}.
- i-v characteristic equations of a PMOS is similar to the NMOS with the exception:
  - Voltages are negative (we switch the terminals to have positive voltages: use v_{SG} instead of v_{GS}).
  - Use mobility of holes, μ_p , instead of μ_n in the expression for i_D



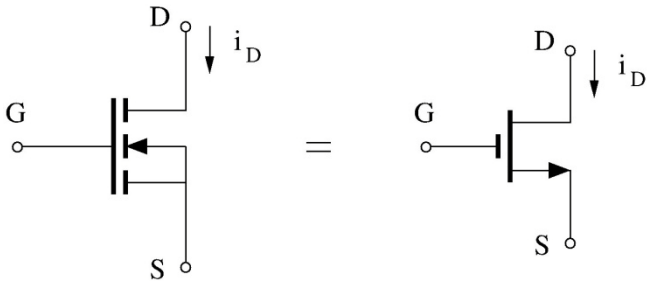
MOS Circuit symbols and conventions

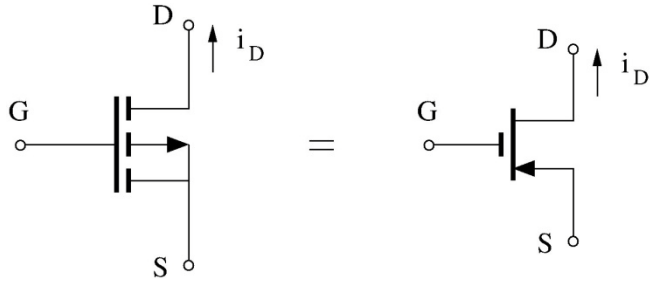


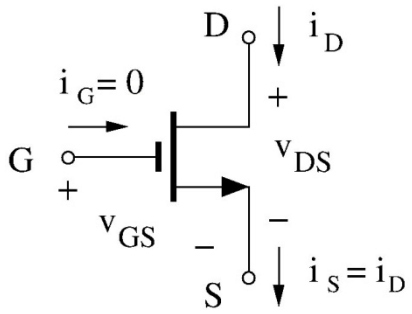
NMOS

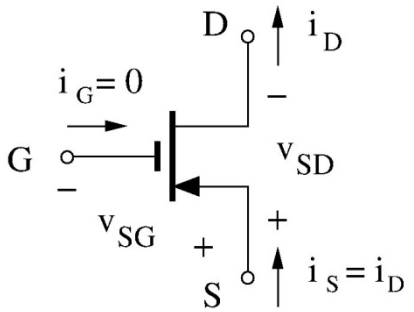


PMOS









MOS i-v Characteristics Equations

NMOS $(V_{OV} = v_{GS} - V_{tn})$

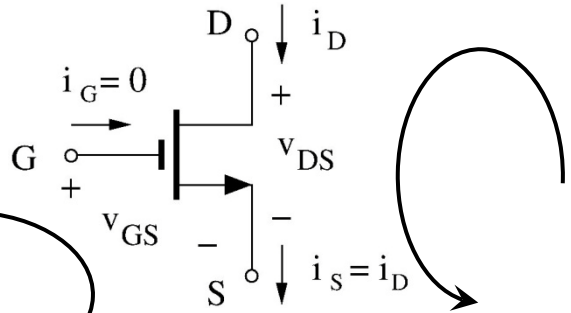
Cut-Off :	$V_{OV} \le 0$	$i_D = 0$
Triode :	$V_{OV} \ge 0$ and $v_{DS} \le V_{OV}$	$i_D = 0.5\mu_n C_{ox} \frac{W}{L}\left[2V_{OV}v_{DS} - v_{DS}^2\right]$
Saturation :	$V_{OV} \ge 0$ and $v_{DS} \ge V_{OV}$	$i_D = 0.5\mu_n C_{ox} \frac{W}{L} V_{OV}^2 \left[1 + \lambda v_{DS}\right]$

PMOS $(V_{OV} = v_{SG} - |V_{tp}|)$*

Cut-Off :	$V_{OV} \le 0$	$i_D = 0$
Triode :	$V_{OV} \ge 0$ and $v_{SD} \le V_{OV}$	$i_D = 0.5\mu_p C_{ox} \frac{W}{L}\left[2V_{OV}v_{SD} - v_{SD}^2\right]$
Saturation :	$V_{OV} \ge 0$ and $v_{SD} \ge V_{OV}$	$i_D = 0.5\mu_p C_{ox} \frac{W}{L} V_{OV}^2 \left[1 + \lambda v_{SD}\right]$

*Note: S&S defines $|V_{OV}| = v_{SG} - |V_{tp}|$ and uses $|V_{OV}|$ in the PMOS formulas.

MOS operation is "Conceptually" similar to a BJT -- i_D & v_{DS} are controlled by v_{GS}

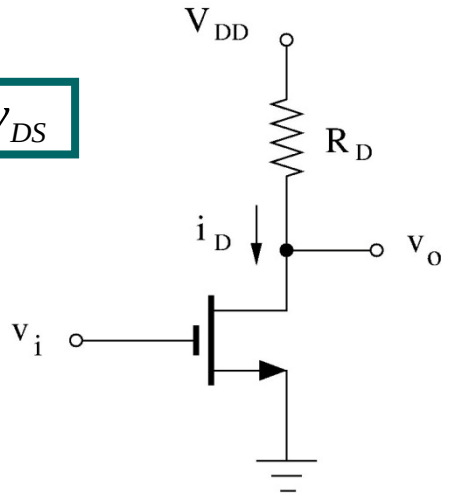


Controller part:
Circuit connected to GS sets v_{GS} (or V_{OV})

Controlled part:
i_D & v_{DS} are set by transistor state (& outside circuit)

- **A similar solution method to BJT:**
  - Write down GS-KVL and DS-KVL, assume MOS is in a particular state, solve with the corresponding MOS equation and validate the assumption.
- **MOS circuits are simpler to solve because $i_G = 0$!**
  - However, we get a quadratic equation to solve if MOS in triode (check MOS in saturation first!)

Example 1: In the circuit below, $R_D = 1$ k, and $V_{DD} = 12$ V. Compute v_o for $v_i = 0$, 6, and 12 V. ($\mu_n C_{ox}\,(W/L) = 0.5$ mA/V² , $V_t = 2$ V, and $\lambda = 0$)



$$\text{GS-KVL}: \quad v_i = v_{GS}$$

$$\text{DS-KVL}: \quad V_{DD} = 12 = R_D\, i_D + v_{DS} = 10^3\, i_D + v_{DS}$$

$v_o = v_{DS}$

Part 1: $v_i = 0$

$$\text{GS-KVL}: \; v_i = v_{GS} = 0 < V_t = 2\text{V} \;\rightarrow\; \text{Cut-off} \;\rightarrow\; i_D = 0$$

$$\text{DS-KVL}: \quad 12 = 10^3 \times 0 + v_{DS} \;\rightarrow\; v_o = v_{DS} = 12\ \text{V}$$

Part 2: $v_i = 6$ V

$$\text{GS}-\text{KVL}: \; v_i = v_{GS} = 6 > V_t = 2\text{V} \;\rightarrow\; \text{Not in Cut-off}$$

$$V_{OV} = v_{GS} - V_t = 4\text{V}$$

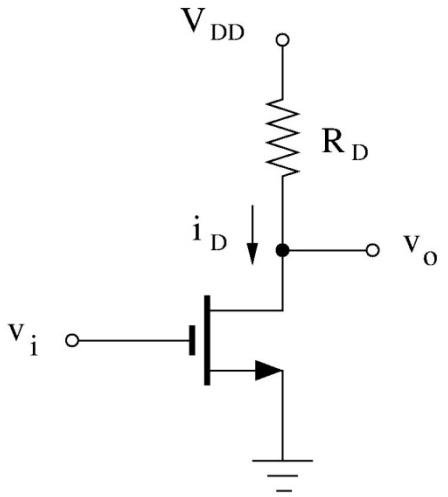
$$\text{Assume Saturation}: \; v_{DS} \geq V_{OV} = 4\ \text{V}$$

$$i_D = 0.5\mu_n C_{ox} \frac{W}{L}\, V_{OV}^2 = 0.5 \times 0.5 \times 10^{-3} \times 4^2 = 4.0\ \text{mA}$$

$$\text{DS-KVL}: \; 12 = 10^3 \times 4 \times 10^{-3} + v_{DS} \;\rightarrow\; v_o = v_{DS} = 8.0\ \text{V}$$

$$v_{DS} = 8.0\ \text{V} > V_{OV} = 4\ \text{V} \rightarrow \text{Assumption correct}$$

Example 1: In the circuit below, $R_D = 1$ k, and $V_{DD} = 12$ V. Compute v_o for $v_i = 0,\ 6,$ and 12 V. ($\mu_n C_{ox}\,(W/L) = 0.5$ mA/V² , $V_t = 2$ V, and $\lambda = 0$)



$v_o = v_{DS}$

$$\text{GS-KVL}: \quad v_i = v_{GS}$$

$$\text{DS-KVL}: \quad V_{DD} = 12 = R_D\, i_D + v_{DS} = 10^3\, i_D + v_{DS}$$

Part 3: v_i = 12 V

$$\text{GS-KVL}: \ v_i = v_{GS} = 12 > V_t = 2\text{V} \ \rightarrow \ \text{Not in Cut-off}$$

$$V_{OV} = v_{GS} - V_t = 10\text{V}$$

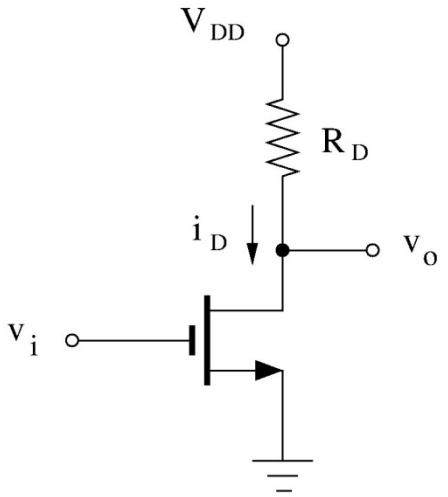
$$\text{Assume Saturation}: \ v_{DS} \geq V_{OV} = 10\ \text{V}$$

$$i_D = 0.5\mu_n C_{ox} \frac{W}{L}\, V_{OV}^2 = 0.5 \times 0.5 \times 10^{-3} \times 10^2 = 25.0\ \text{mA}$$

$$\text{DS-KVL}: \ 12 = 10^3 \times 25.0 \times 10^{-3} + v_{DS} \ \rightarrow \ v_{DS} = -13.\ \text{V}$$

$$v_{DS} = -13\ \text{V} > V_{OV} = 10\ \text{V} \rightarrow \text{Assumption incorrect}$$

Example 1: In the circuit below, $R_D = 1$ k, and $V_{DD} = 12$ V. Compute v_o for $v_i = 0,\ 6,$ and 12 V. ($\mu_n C_{ox}\,(W/L) = 0.5$ mA/V², $V_t = 2$ V, and $\lambda = 0$)



$v_o = v_{DS}$

$$\text{GS-KVL}: \quad v_i = v_{GS}$$

$$\text{DS-KVL}: \quad V_{DD} = 12 = R_D\, i_D + v_{DS} = 10^3\, i_D + v_{DS}$$

Part 3 (cont'd): v_i = 12 V

$$V_{OV} = v_{GS} - V_t = 10\text{V}$$

$$\text{Assume Triode}: \ v_{DS} < V_{OV} = 10\ \text{V}$$

$$i_D = 0.5\mu_n C_{ox} \frac{W}{L}\left[2V_{OV} v_{DS} - v_{DS}^2\right]$$

$$\text{DS-KVL}: \ 12 = 10^3 \times i_D + v_{DS}$$

$$12 = 10^3 \times 0.5 \times 0.5 \times 10^{-3} \times [20 v_{DS} - v_{DS}^2] + v_{DS}$$

$$v_{DS}^2 - 24 v_{DS} + 48 = 0$$

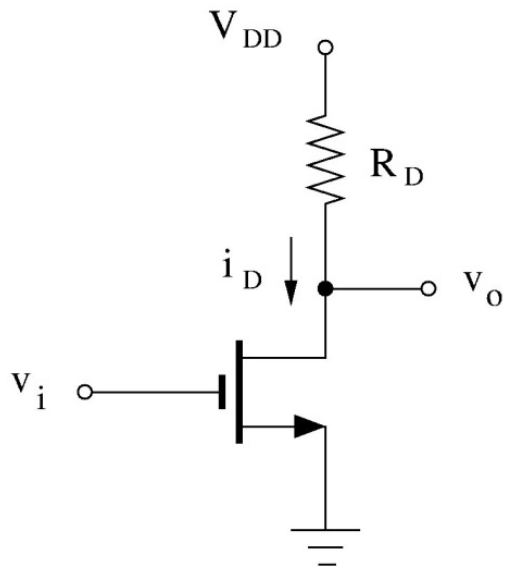
$$v_o = v_{DS} = 21.8\ \text{V} > V_{OV} = 10 \ \text{(incorrect)}$$

$$v_o = v_{DS} = 2.2\ \text{V} \quad < V_{OV} = 10\ \text{V}$$

$$12 = 10^3 \times i_D + v_{DS} \ \rightarrow \ i_D = 9.8\ \text{mA}$$

NMOS Transfer Function (1)

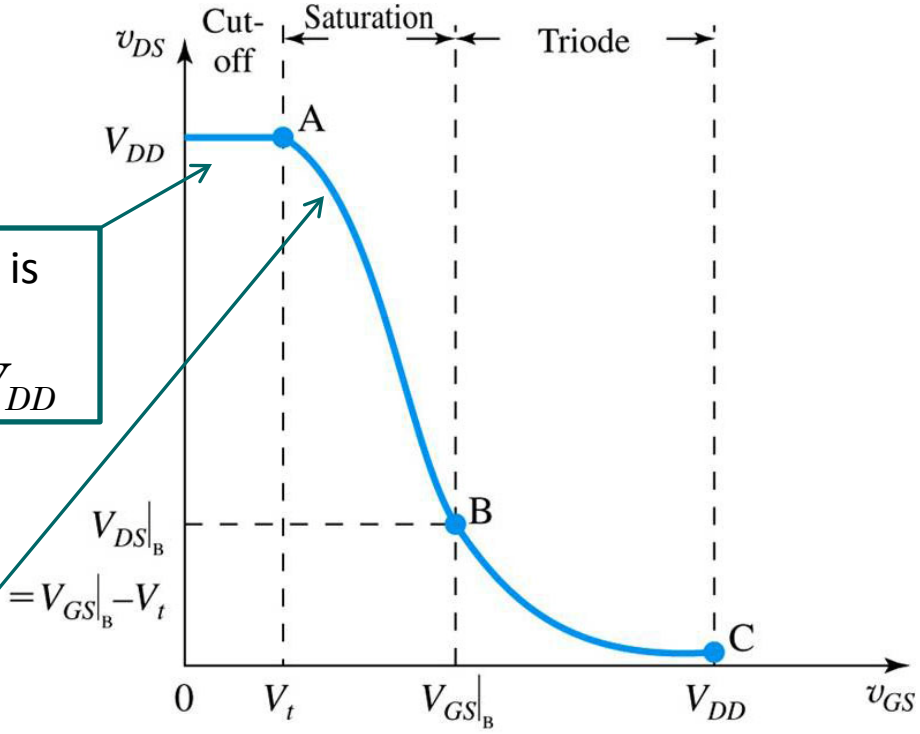
v_i can be applied directly to MOS
There is no need for a R_G .



Circuit Equations:

- $v_{GS} = v_i$
- NMOS iv characteristics: $i_D = f(v_{GS}, v_{DS})$
- KVL: $v_o = v_{DS} = V_{DD} - R_D\, i_D$

NMOS Transfer Function (2)

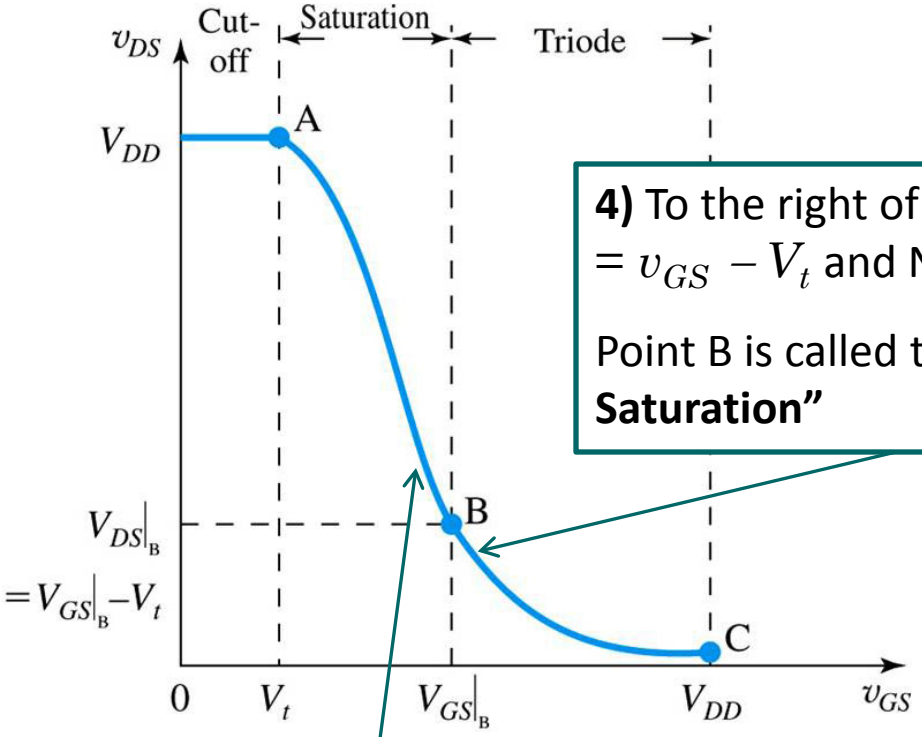


1) For $v_{GS} < V_t$, NMOS is in cutoff: $i_D = 0$ & $v_{DS} = V_{DD} - R_D\, i_D = V_{DD}$

2) Just to the right of point A:

- $V_{OV} = v_{GS} - V_t$ is small, so i_D is small.
- $v_{DS} = V_{DD} - R_D\, i_D$ is close to V_{DD}
- Thus, $v_{DS} > V_{OV}$ and NMOS is in saturation.

NMOS Transfer Function (2)



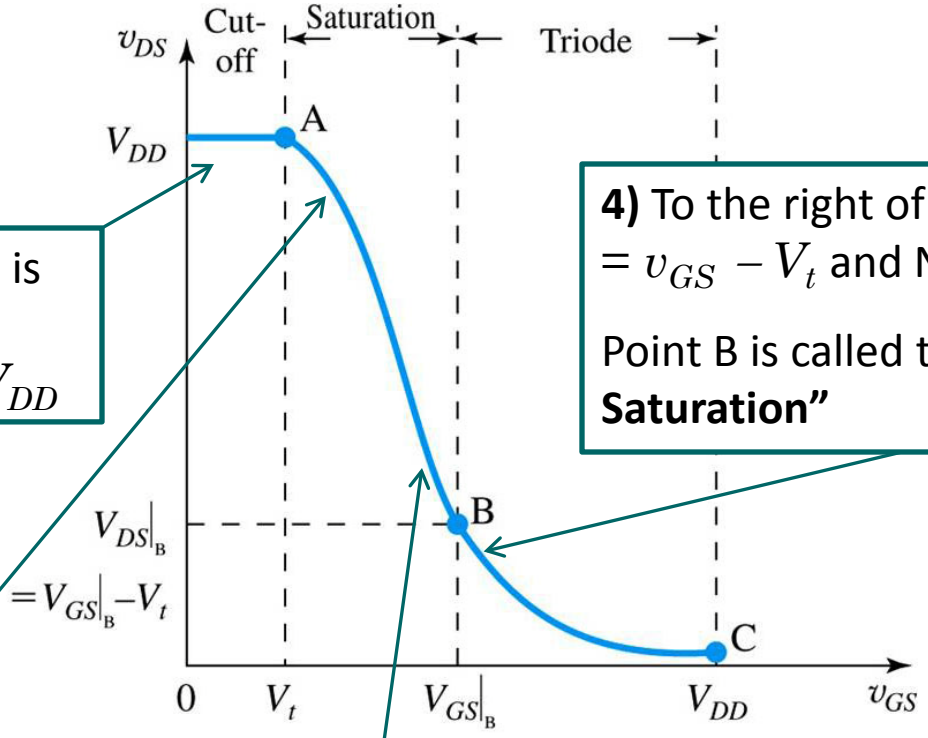
4) To the right of point B, $v_{DS} < V_{OV} = v_{GS} - V_t$ and NMOS enters triode.

Point B is called the **"Edge of Saturation"**

3) As v_{GS} increases:

- $V_{OV} = v_{GS} - V_t$ and i_D become larger;
- $v_{DS} = V_{DD} - R_D\, i_D$ becomes smaller.
- At point B, $v_{DS} = V_{OV}$

NMOS Transfer Function (2)



1) For $v_{GS} < V_t$, NMOS is in cutoff: $i_D = 0$ & $v_{DS} = V_{DD} - R_D\, i_D = V_{DD}$

2) Just to the right of point A:

- $V_{OV} = v_{GS} - V_t$ is small, so i_D is small.
- $v_{DS} = V_{DD} - R_D\, i_D$ is close to V_{DD}
- Thus, $v_{DS} > V_{OV}$ and NMOS is in saturation.

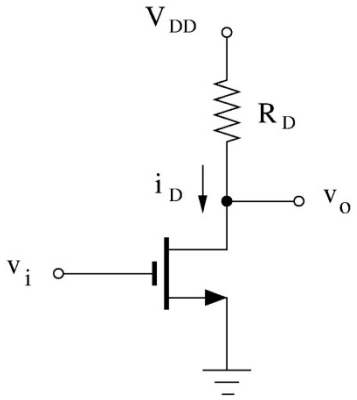
3) As v_{GS} increases:

- $V_{OV} = v_{GS} - V_t$ and i_D become larger;
- $v_{DS} = V_{DD} - R_D\, i_D$ becomes smaller.
- At point B, $v_{DS} = V_{OV}$

4) To the right of point B, $v_{DS} < V_{OV} = v_{GS} - V_t$ and NMOS enters triode.

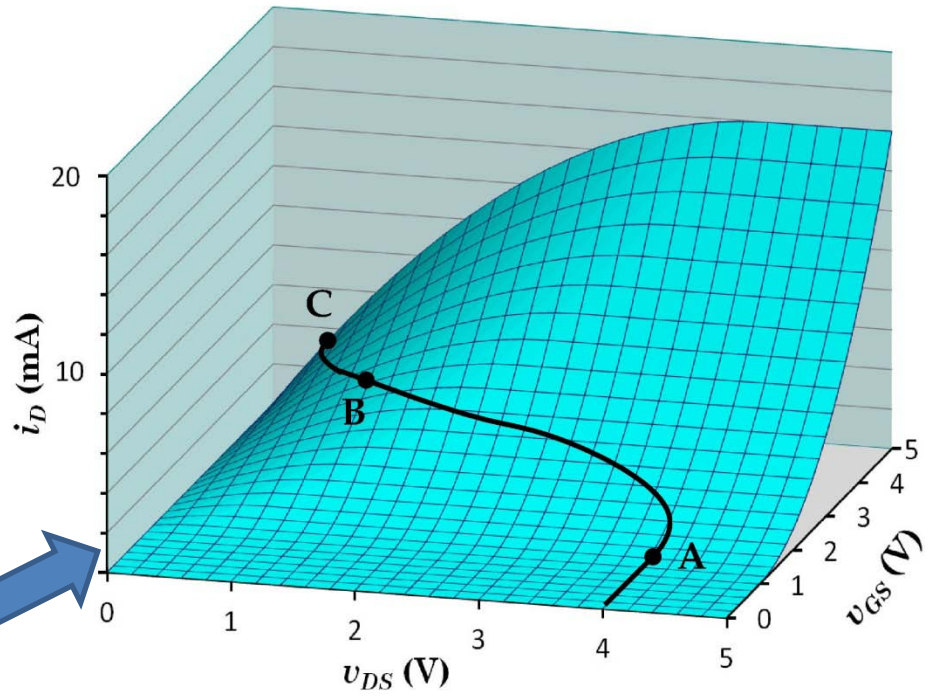
Point B is called the **"Edge of Saturation"**

Graphical analysis of NMOS Transfer Function (1)



NMOS i-v Characterisitics : $i_D = f(v_{GS}, v_{DS})$

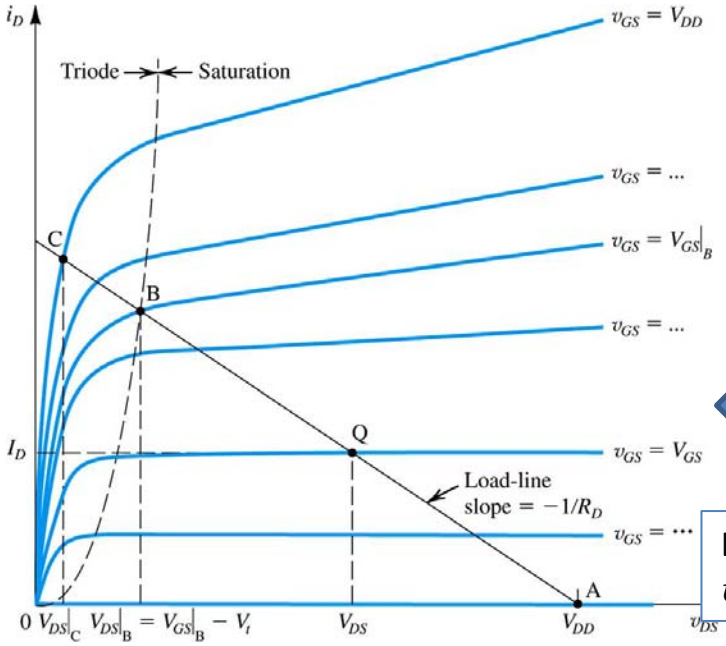
KVL : $V_{DD} = R_D i_D + v_{DS}$



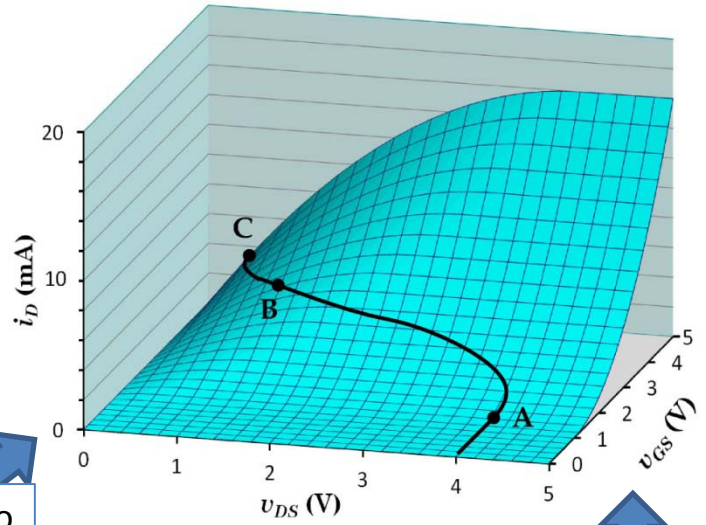
- KVL equation is a plane in this space.
- Intersection of KVL plane with the iv characteristics surface is a line.
- NMOS operating point is on this line (depending on the value of v_{GS}.)

- If we look from the bottom (i_D axis out of the paper), we can see the transfer function.

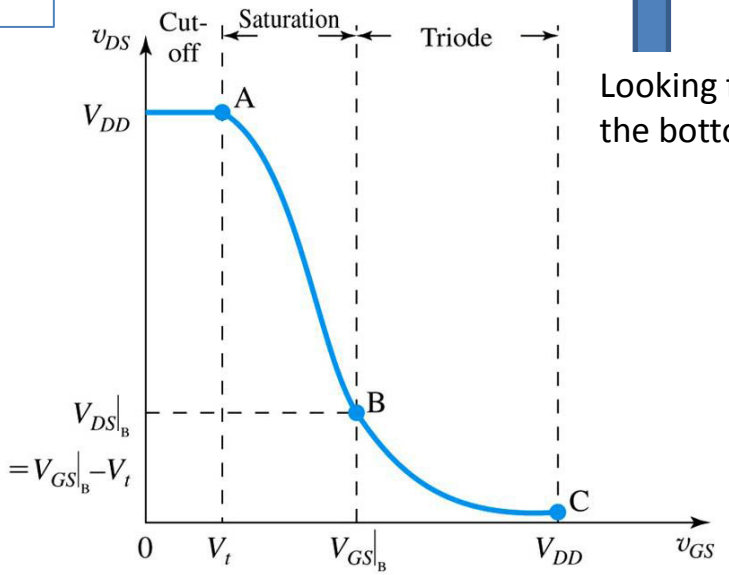
Graphical analysis of NMOS Transfer Function (2)



Looking parallel to v_{GS} axis



Looking from the bottom



- Every point on the load line corresponds to a specific v_{GS} value.
- As v_{GS} increases, NMOS moves "up" the load line.

NMOS Functional circuits

- Similar to a BJTs in the active mode, NMOS behaves rather "linearly" in the saturation region (we discuss NMOS amplifiers later)
- Transition from cut-off to triode can be used to build NMOS switch circuits.
  - Voltage at point C (see graph) depends on NMOS parameters and the circuit (in BJT $v_o = V_{sat}$)!
- We can also built NMOS logic gate similar to a RTL. But there is are much better gates based on CMOS technology!