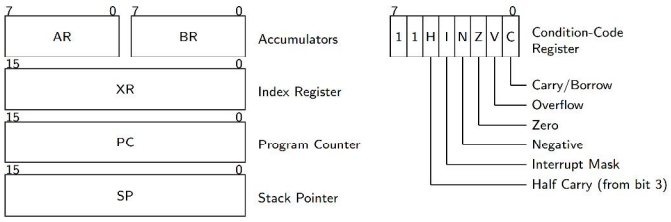
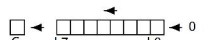
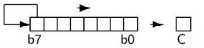
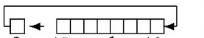
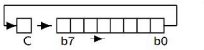



# ARIZONA STATE UNIVERSITY

## Embedded–Systems Laboratory

## Motorola M6800 Microprocessor

| ACCUMULATOR and MEMORY | | ADDRESSING MODES | | | | | | | | | | | | | | BOOL/ARITH OPERATION | CONDITION CODES[1] | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | IMMEDIATE | | | DIRECT | | | INDEXED | | | EXTENDED | | | INHERENT | | | (Each register label refers | 5 | 4 | 3 | 2 | 1 | 0 |
| OPERATIONS | MNEM. | OP | ~ | # | OP | ~ | # | OP | ~ | # | OP | ~ | # | OP | ~ | # | to contents of register) | H | I | N | Z | V | C |
| Add Accumulators | ABA | | | | | | | | | | | | | 1B | 2 | 1 | A + B → A | ↕ | • | ↕ | ↕ | ↕ | ↕ |
| Add with Carry | ADCA | 89 | 2 | 2 | 99 | 3 | 2 | A9 | 5 | 2 | B9 | 4 | 3 | | | | A + M + C → A | ↕ | • | ↕ | ↕ | ↕ | ↕ |
| | ADCB | C9 | 2 | 2 | D9 | 3 | 2 | E9 | 5 | 2 | F9 | 4 | 3 | | | | B + M + C → B | ↕ | • | ↕ | ↕ | ↕ | ↕ |
| Add | ADDA | 8B | 2 | 2 | 9B | 3 | 2 | AB | 5 | 2 | BB | 4 | 3 | | | | A + M → A | ↕ | • | ↕ | ↕ | ↕ | ↕ |
| | ADDB | CB | 2 | 2 | DB | 3 | 2 | EB | 5 | 2 | FB | 4 | 3 | | | | B + M → B | ↕ | • | ↕ | ↕ | ↕ | ↕ |
| And | ANDA | 84 | 2 | 2 | 94 | 3 | 2 | A4 | 5 | 2 | B4 | 4 | 3 | | | | A ∧ M → A | • | • | ↕ | ↕ | R | • |
| | ANDB | C4 | 2 | 2 | D4 | 3 | 2 | E4 | 5 | 2 | F4 | 4 | 3 | | | | B ∧ M → B | • | • | ↕ | ↕ | R | • |
| Arithmetic Shift Left | ASL | | | | | | | 68 | 7 | 2 | 78 | 6 | 3 | | | | | • | • | ↕ | ↕ | 2 | ↕ |
| | ASLA | | | | | | | | | | | | | 48 | 2 | 1 |  | • | • | ↕ | ↕ | 2 | ↕ |
| | ASLB | | | | | | | | | | | | | 58 | 2 | 1 | | • | • | ↕ | ↕ | 2 | ↕ |
| Arithmetic Shift Right | ASR | | | | | | | 67 | 7 | 2 | 77 | 6 | 3 | | | | | • | • | ↕ | ↕ | 2 | ↕ |
| | ASRA | | | | | | | | | | | | | 47 | 2 | 1 |  | • | • | ↕ | ↕ | 2 | ↕ |
| | ASRB | | | | | | | | | | | | | 57 | 2 | 1 | | • | • | ↕ | ↕ | 2 | ↕ |
| Bit Test | BITA | 85 | 2 | 2 | 95 | 3 | 2 | A5 | 5 | 2 | B5 | 4 | 3 | | | | A ∧ M | • | • | ↕ | ↕ | R | • |
| | BITB | C5 | 2 | 2 | D5 | 3 | 2 | E5 | 5 | 2 | F5 | 4 | 3 | | | | B ∧ M | • | • | ↕ | ↕ | R | • |
| Compare Accumulators | CBA | | | | | | | | | | | | | 11 | 2 | 1 | A – B | • | • | ↕ | ↕ | ↕ | ↕ |
| Clear | CLR | | | | | | | 6F | 7 | 2 | 7F | 6 | 3 | | | | 00 → M | • | • | R | S | R | R |
| | CLRA | | | | | | | | | | | | | 4F | 2 | 1 | 00 → A | • | • | R | S | R | R |
| | CLRB | | | | | | | | | | | | | 5F | 2 | 1 | 00 → B | • | • | R | S | R | R |
| Compare | CMPA | 81 | 2 | 2 | 91 | 3 | 2 | A1 | 5 | 2 | B1 | 4 | 3 | | | | A – M | • | • | ↕ | ↕ | ↕ | ↕ |
| | CMPB | C1 | 2 | 2 | D1 | 3 | 2 | E1 | 5 | 2 | F1 | 4 | 3 | | | | B – M | • | • | ↕ | ↕ | ↕ | ↕ |
| Complement, 1's | COM | | | | | | | 63 | 7 | 2 | 73 | 6 | 3 | | | | $\overline{M} \rightarrow M$ | • | • | ↕ | ↕ | R | S |
| | COMA | | | | | | | | | | | | | 43 | 2 | 1 | $\overline{A} \rightarrow A$ | • | • | ↕ | ↕ | R | S |
| | COMB | | | | | | | | | | | | | 53 | 2 | 1 | $\overline{B} \rightarrow B$ | • | • | ↕ | ↕ | R | S |
| Decimal Adjust, A | DAA | | | | | | | | | | | | | 19 | 2 | 1 | Convert Binary Addition of BCD | • | • | ↕ | ↕ | ↕ | 3 |
| Decrement | DEC | | | | | | | 6A | 7 | 2 | 7A | 6 | 3 | | | | M – 1 → M | • | • | ↕ | ↕ | ↕ | • |
| | DECA | | | | | | | | | | | | | 4A | 2 | 1 | A – 1 → A | • | • | ↕ | ↕ | ↕ | • |
| | DECB | | | | | | | | | | | | | 5A | 2 | 1 | B – 1 → B | • | • | ↕ | ↕ | ↕ | • |
| Exclusive Or | EORA | 88 | 2 | 2 | 98 | 3 | 2 | A8 | 5 | 2 | B8 | 4 | 3 | | | | A ⊕ M → A | • | • | ↕ | ↕ | R | • |
| | EORB | C8 | 2 | 2 | D8 | 3 | 2 | E8 | 5 | 2 | F8 | 4 | 3 | | | | B ⊕ M → B | • | • | ↕ | ↕ | R | • |
| Increment | INC | | | | | | | 6C | 7 | 2 | 7C | 6 | 3 | | | | M + 1 → M | • | • | ↕ | ↕ | ↕ | • |
| | INCA | | | | | | | | | | | | | 4C | 2 | 1 | A + 1 → A | • | • | ↕ | ↕ | ↕ | • |
| | INCB | | | | | | | | | | | | | 5C | 2 | 1 | B + 1 → B | • | • | ↕ | ↕ | ↕ | • |
| Load Accumulator | LDAA | 86 | 2 | 2 | 96 | 3 | 2 | A6 | 5 | 2 | B6 | 4 | 3 | | | | M → A | • | • | ↕ | ↕ | R | • |
| | LDAB | C6 | 2 | 2 | D6 | 3 | 2 | E6 | 5 | 2 | F6 | 4 | 3 | | | | M → B | • | • | ↕ | ↕ | R | • |
| Logical Shift Right | LSR | | | | | | | 64 | 7 | 2 | 74 | 6 | 3 | | | | | • | • | R | ↕ | 2 | ↕ |
| | LSRA | | | | | | | | | | | | | 44 | 2 | 1 |  | • | • | R | ↕ | 2 | ↕ |
| | LSRB | | | | | | | | | | | | | 54 | 2 | 1 | | • | • | R | ↕ | 2 | ↕ |
| Negate | NEG | | | | | | | 60 | 7 | 2 | 70 | 6 | 3 | | | | 00 – M → M | • | • | ↕ | ↕ | ↕ | ↕ |
| | NEGA | | | | | | | | | | | | | 40 | 2 | 1 | 00 – A → A | • | • | ↕ | ↕ | ↕ | ↕ |
| | NEGB | | | | | | | | | | | | | 50 | 2 | 1 | 00 – B → B | • | • | ↕ | ↕ | ↕ | ↕ |
| Or, Inclusive | ORAA | 8A | 2 | 2 | 9A | 3 | 2 | AA | 5 | 2 | BA | 4 | 3 | | | | A ∨ M → A | • | • | ↕ | ↕ | R | • |
| | ORAB | CA | 2 | 2 | DA | 3 | 2 | EA | 5 | 2 | FA | 4 | 3 | | | | B ∨ M → B | • | • | ↕ | ↕ | R | • |
| Push Data | PSHA | | | | | | | | | | | | | 36 | 4 | 1 | $A \rightarrow M_{SP}$, SP – 1 → SP | • | • | • | • | • | • |
| | PSHB | | | | | | | | | | | | | 37 | 4 | 1 | $B \rightarrow M_{SP}$, SP – 1 → SP | • | • | • | • | • | • |
| Pull Data | PULA | | | | | | | | | | | | | 32 | 4 | 1 | SP + 1 → SP, $M_{SP} \rightarrow A$ | • | • | • | • | • | • |
| | PULB | | | | | | | | | | | | | 33 | 4 | 1 | SP + 1 → SP, $M_{SP} \rightarrow B$ | • | • | • | • | • | • |
| Rotate Left | ROL | | | | | | | 69 | 7 | 2 | 79 | 6 | 3 | | | | | • | • | ↕ | ↕ | 2 | ↕ |
| | ROLA | | | | | | | | | | | | | 49 | 2 | 1 |  | • | • | ↕ | ↕ | 2 | ↕ |
| | ROLB | | | | | | | | | | | | | 59 | 2 | 1 | | • | • | ↕ | ↕ | 2 | ↕ |
| Rotate Right | ROR | | | | | | | 66 | 7 | 2 | 76 | 6 | 3 | | | | | • | • | ↕ | ↕ | 2 | ↕ |
| | RORA | | | | | | | | | | | | | 46 | 2 | 1 |  | • | • | ↕ | ↕ | 2 | ↕ |
| | RORB | | | | | | | | | | | | | 56 | 2 | 1 | | • | • | ↕ | ↕ | 2 | ↕ |
| Subtract Accumulators | SBA | | | | | | | | | | | | | 10 | 2 | 1 | A – B → A | • | • | ↕ | ↕ | ↕ | ↕ |
| Subtract with Carry | SBCA | 82 | 2 | 2 | 92 | 3 | 2 | A2 | 5 | 2 | B2 | 4 | 3 | | | | A – M – C → A | • | • | ↕ | ↕ | ↕ | ↕ |
| | SBCB | C2 | 2 | 2 | D2 | 3 | 2 | E2 | 5 | 2 | F2 | 4 | 3 | | | | B – M – C → B | • | • | ↕ | ↕ | ↕ | ↕ |
| Store Accumulator | STAA | | | | 97 | 4 | 2 | A7 | 6 | 2 | B7 | 5 | 3 | | | | A → M | • | • | ↕ | ↕ | R | • |
| | STAB | | | | D7 | 4 | 2 | E7 | 6 | 2 | F7 | 5 | 3 | | | | B → M | • | • | ↕ | ↕ | R | • |
| Subtract | SUBA | 80 | 2 | 2 | 90 | 3 | 2 | A0 | 5 | 2 | B0 | 4 | 3 | | | | A – M → A | • | • | ↕ | ↕ | ↕ | ↕ |
| | SUBB | C0 | 2 | 2 | D0 | 3 | 2 | E0 | 5 | 2 | F0 | 4 | 3 | | | | B – M → B | • | • | ↕ | ↕ | ↕ | ↕ |
| Transfer Accumulator | TAB | | | | | | | | | | | | | 16 | 2 | 1 | A → B | • | • | ↕ | ↕ | R | • |
| | TBA | | | | | | | | | | | | | 17 | 2 | 1 | B → A | • | • | ↕ | ↕ | R | • |
| Test Value | TST | | | | | | | 6D | 7 | 2 | 7D | 6 | 3 | | | | M – 00 | • | • | ↕ | ↕ | R | R |
| | TSTA | | | | | | | | | | | | | 4D | 2 | 1 | A – 00 | • | • | ↕ | ↕ | R | R |
| | TSTB | | | | | | | | | | | | | 5D | 2 | 1 | B – 00 | • | • | ↕ | ↕ | R | R |

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January 15, 2003

| XR and SP | | ADDRESSING MODES: IMMEDIATE | | | DIRECT | | | INDEXED | | | EXTENDED | | | INHERENT | | | BOOL/ARITH OPERATION | CONDITION CODES[1] | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPERATIONS | MNEM. | OP | ~ | # | OP | ~ | # | OP | ~ | # | OP | ~ | # | OP | ~ | # | (Each register label refers to contents of register) | 5 H | 4 I | 3 N | 2 Z | 1 V | 0 C |
| Compare XR | CPX | 8C | 3 | 3 | 9C | 4 | 2 | AC | 6 | 2 | BC | 5 | 3 | | | | $X_{MS} - M, X_{LS} - (M+1)$ | • | • | 4 | ↕ | 5 | • |
| Decrement SP | DES | | | | | | | | | | | | | 34 | 4 | 1 | SP − 1 → SP | • | • | • | • | • | • |
| Decrement XR | DEX | | | | | | | | | | | | | 09 | 4 | 1 | X − 1 → X | • | • | • | ↕ | • | • |
| Increment SP | INS | | | | | | | | | | | | | 31 | 4 | 1 | SP + 1 → SP | • | • | • | • | • | • |
| Increment XR | INX | | | | | | | | | | | | | 08 | 4 | 1 | X + 1 → X | • | • | • | ↕ | • | • |
| Load SP | LDS | 8E | 3 | 3 | 9E | 4 | 2 | AE | 6 | 2 | BE | 5 | 3 | | | | $M \rightarrow SP_{MS}, (M+1) \rightarrow SP_{LS}$ | • | • | ↕ | ↕ | R | • |
| Load XR | LDX | CE | 3 | 3 | DE | 4 | 2 | EE | 6 | 2 | FE | 5 | 3 | | | | $M \rightarrow X_{MS}, (M+1) \rightarrow X_{LS}$ | • | • | ↕ | ↕ | R | • |
| Store SP | STS | | | | 9F | 5 | 2 | AF | 7 | 2 | BF | 6 | 3 | | | | $SP_{MS} \rightarrow M, SP_{LS} \rightarrow (M+1)$ | • | • | ↕ | ↕ | R | • |
| Store XR | STX | | | | DF | 5 | 2 | EF | 7 | 2 | FF | 6 | 3 | | | | $X_{MS} \rightarrow M, X_{LS} \rightarrow (M+1)$ | • | • | ↕ | ↕ | R | • |
| SP + 1 → XR | TSX | | | | | | | | | | | | | 30 | 4 | 1 | SP + 1 → X | • | • | • | • | • | • |
| XR − 1 → SP | TXS | | | | | | | | | | | | | 35 | 4 | 1 | X − 1 → SP | • | • | • | • | • | • |

| JUMP and BRANCH | | RELATIVE | | | INDEXED | | | EXTENDED | | | INHERENT | | | | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPERATIONS | MNEM. | OP | ~ | # | OP | ~ | # | OP | ~ | # | OP | ~ | # | BRANCH TEST | H | I | N | Z | V | C |
| Branch if Carry Set | BCS | 25 | 4 | 2 | | | | | | | | | | C = 1 | • | • | • | • | • | • |
| Branch if Carry Clear | BCC | 24 | 4 | 2 | | | | | | | | | | C = 0 | • | • | • | • | • | • |
| Branch if Minus | BMI | 2B | 4 | 2 | | | | | | | | | | N = 1 | • | • | • | • | • | • |
| Branch if Plus | BPL | 2A | 4 | 2 | | | | | | | | | | N = 0 | • | • | • | • | • | • |
| Branch if Overflow Set | BVS | 29 | 4 | 2 | | | | | | | | | | V = 1 | • | • | • | • | • | • |
| Branch if Overflow Clear | BVC | 28 | 4 | 2 | | | | | | | | | | V = 0 | • | • | • | • | • | • |
| Branch if Equal | BEQ | 27 | 4 | 2 | | | | | | | | | | Z = 1 | • | • | • | • | • | • |
| Branch if Not Equal | BNE | 26 | 4 | 2 | | | | | | | | | | Z = 0 | • | • | • | • | • | • |
| Branch if < (Signed) | BLT | 2D | 4 | 2 | | | | | | | | | | N ⊕ V = 1 | • | • | • | • | • | • |
| Branch if ≤ (Signed) | BLE | 2F | 4 | 2 | | | | | | | | | | Z ∨ (N ⊕ V) = 1 | • | • | • | • | • | • |
| Branch if ≥ (Signed) | BGE | 2C | 4 | 2 | | | | | | | | | | N ⊕ V = 0 | • | • | • | • | • | • |
| Branch if > (Signed) | BGT | 2E | 4 | 2 | | | | | | | | | | Z ∨ (N ⊕ V) = 0 | • | • | • | • | • | • |
| Branch if Lower or Same (Unsigned) | BLS | 23 | 4 | 2 | | | | | | | | | | C ∨ Z = 1 | • | • | • | • | • | • |
| Branch if Higher (Unsigned) | BHI | 22 | 4 | 2 | | | | | | | | | | C ∨ Z = 0 | • | • | • | • | • | • |
| Branch Always | BRA | 20 | 4 | 2 | | | | | | | | | | Branch Relative | • | • | • | • | • | • |
| Branch to Subroutine | BSR | 8D | 8 | 2 | | | | | | | | | | Push PC; Branch Relative | • | • | • | • | • | • |
| Jump | JMP | | | | 6E | 4 | 2 | 7E | 3 | 3 | | | | Jump Absolute | • | • | • | • | • | • |
| Jump to Subroutine | JSR | | | | AD | 8 | 2 | BD | 9 | 3 | | | | Push PC; Jump Absolute | • | • | • | • | • | • |
| No Operation | NOP | | | | | | | | | | 01 | 2 | 1 | Only Advance Program Counter | • | • | • | • | • | • |
| Return From Interrupt | RTI | | | | | | | | | | 3B | 10 | 1 | Pull Interrupt Stack Frame | ↕ | ↕ | ↕ | ↕ | ↕ | ↕ |
| Return From Subroutine | RTS | | | | | | | | | | 39 | 5 | 1 | Pull PC | • | • | • | • | • | • |
| Software Interrupt | SWI | | | | | | | | | | 3F | 12 | 1 | Push Interrupt Stack Frame; Vector | • | S | • | • | • | • |
| Wait for Interrupt | WAI | | | | | | | | | | 3E | 9 | 1 | Push Interrupt Stack Frame; Wait | • | 6 | • | • | • | • |

| CONDITION-CODE | | INHERENT | | | BOOLEAN | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPERATIONS | MNEM. | OP | ~ | # | OPERATION | H | I | N | Z | V | C |
| Clear Carry | CLC | 0C | 2 | 1 | 0 → C | • | • | • | • | • | R |
| Clear Interrupt Mask | CLI | 0E | 2 | 1 | 0 → I | • | R | • | • | • | • |
| Clear Overflow | CLV | 0A | 2 | 1 | 0 → V | • | • | • | • | R | • |
| Set Carry | SEC | 0D | 2 | 1 | 1 → C | • | • | • | • | • | S |
| Set Interrupt Mask | SEI | 0F | 2 | 1 | 1 → I | • | S | • | • | • | • |
| Set Overflow | SEV | 0B | 2 | 1 | 1 → V | • | • | • | • | S | • |
| AR → CC | TAP | 06 | 2 | 1 | A → CC | ↕ | ↕ | ↕ | ↕ | ↕ | ↕ |
| CC → AR | TPA | 07 | 2 | 1 | CC → A | • | • | • | • | • | • |

**Condition-Code Notes:**

1. Bits 7 and 6 of CC are always set.
2. Sets CC.V = N ⊕ C after shift has occurred.
3. CC.C = 1 if BCD result > $99_{10}$; otherwise, CC.C = 0.
4. CC.N = Sign bit from subtraction of MS bytes.
5. CC.V = Two's-complement overflow from subtraction of MS bytes.
6. Sets CC.I when interrupt occurs. If previously set, a NonMaskable Interrupt is required to exit from the wait state.

**Interrupt Vectors**

| | | |
|---|---|---|
| FFF8 | IRQ | MS |
| FFF9 | IRQ | LS |
| FFFA | SWI | MS |
| FFFB | SWI | LS |
| FFFC | NMI | MS |
| FFFD | NMI | LS |
| FFFE | Reset | MS |
| FFFF | Reset | LS |

**Interrupt Stack**

| | |
|---|---|
| SP | |
| SP + 1 | CC |
| SP + 2 | BR |
| SP + 3 | AR |
| SP + 4 | $XR_{MS}$ |
| SP + 5 | $XR_{LS}$ |
| SP + 6 | $PC_{MS}$ |
| SP + 7 | $PC_{LS}$ |

**Legend:**

| | | | |
|---|---|---|---|
| OP | Operation Code (Hexadecimal) | $\overline{M}$ | One's Complement of M |
| ~ | Number of MPU Cycles | 0 | Bit = Zero |
| # | Number of Program Bytes | 00 | Byte = Zero |
| + | Arithmetic Plus | CC | Condition-Code register |
| − | Arithmetic Minus | ↕ | Set if true, cleared otherwise |
| × | Arithmetic Multiply | • | Not Affected |
| ∧ | Boolean AND | R | Reset Always |
| ∨ | Boolean Inclusive OR | S | Set Always |
| ⊕ | Boolean Exclusive OR | H | Half Carry from bit 3 |
| → | Transfer Into | I | Interrupt Mask |
| LS | Least Significant | N | Negative (sign bit) |
| MS | Most Significant | Z | Zero (byte) |
| M | Memory Operand | V | Overflow, Two's Complement |
| $M_{SP}$ | Mem. byte that SP addresses | C | Carry from bit 7 |

**Powers of Two**

| $n$ | $2^n$ | $\$2^n$ | $n$ | $2^n$ | $\$2^n$ | $n$ | $2^n$ | $\$2^n$ | $n$ | $2^n$ | $\$2^n$ | $n$ | $2^n$ | $\$2^n$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | $01 | 8 | 256 | $0100 | 16 | 65,536 | $01,0000 | 24 | 16,777,216 | $0100,0000 | 32 | 4,294,967,296 | $01,0000,0000 |
| 1 | 2 | $02 | 9 | 512 | $0200 | 17 | 131,072 | $02,0000 | 25 | 33,554,432 | $0200,0000 | 33 | 8,589,934,592 | $02,0000,0000 |
| 2 | 4 | $04 | 10 | 1,024 | $0400 | 18 | 262,144 | $04,0000 | 26 | 67,108,864 | $0400,0000 | 34 | 17,179,869,184 | $04,0000,0000 |
| 3 | 8 | $08 | 11 | 2,048 | $0800 | 19 | 524,288 | $08,0000 | 27 | 134,217,728 | $0800,0000 | 35 | 34,359,738,368 | $08,0000,0000 |
| 4 | 16 | $10 | 12 | 4,096 | $1000 | 20 | 1,048,576 | $10,0000 | 28 | 268,435,456 | $1000,0000 | 36 | 68,719,476,736 | $10,0000,0000 |
| 5 | 32 | $20 | 13 | 8,192 | $2000 | 21 | 2,097,152 | $20,0000 | 29 | 536,870,912 | $2000,0000 | 37 | 137,438,953,472 | $20,0000,0000 |
| 6 | 64 | $40 | 14 | 16,384 | $4000 | 22 | 4,194,304 | $40,0000 | 30 | 1,073,741,824 | $4000,0000 | 38 | 274,877,906,944 | $40,0000,0000 |
| 7 | 128 | $80 | 15 | 32,768 | $8000 | 23 | 8,388,608 | $80,0000 | 31 | 2,147,483,648 | $8000,0000 | 39 | 549,755,813,888 | $80,0000,0000 |