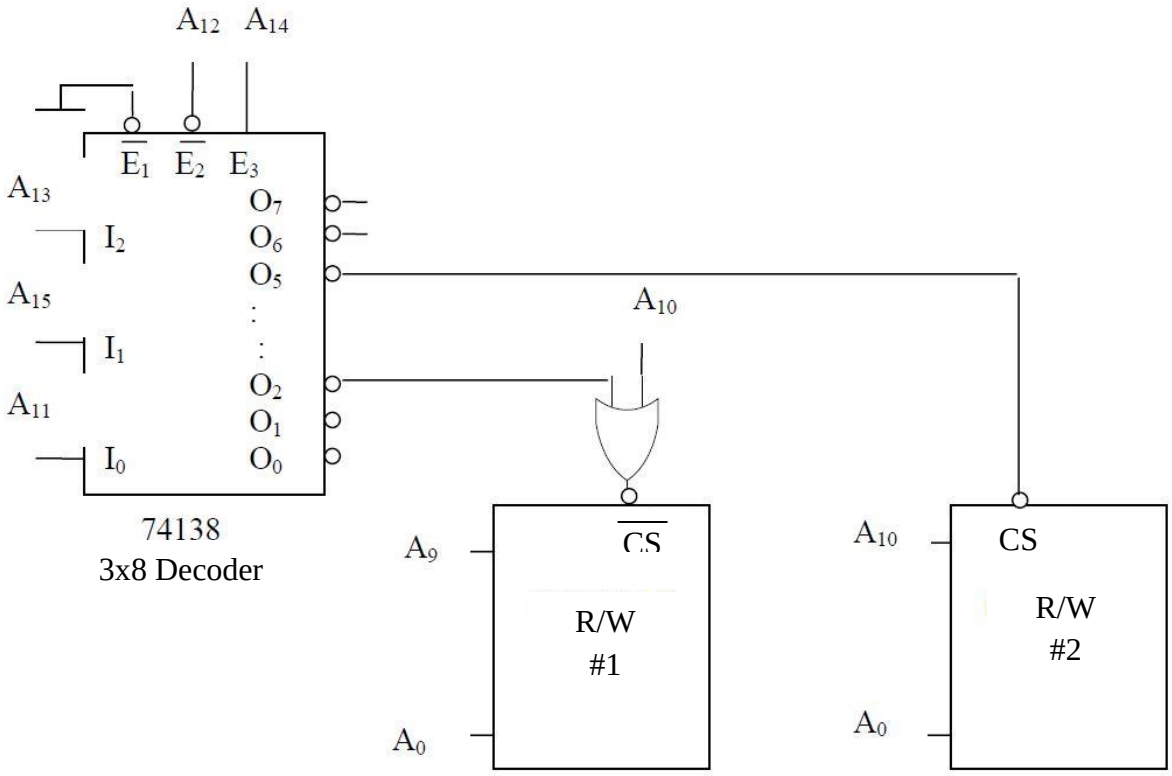
Questions from previous years' practice sessions

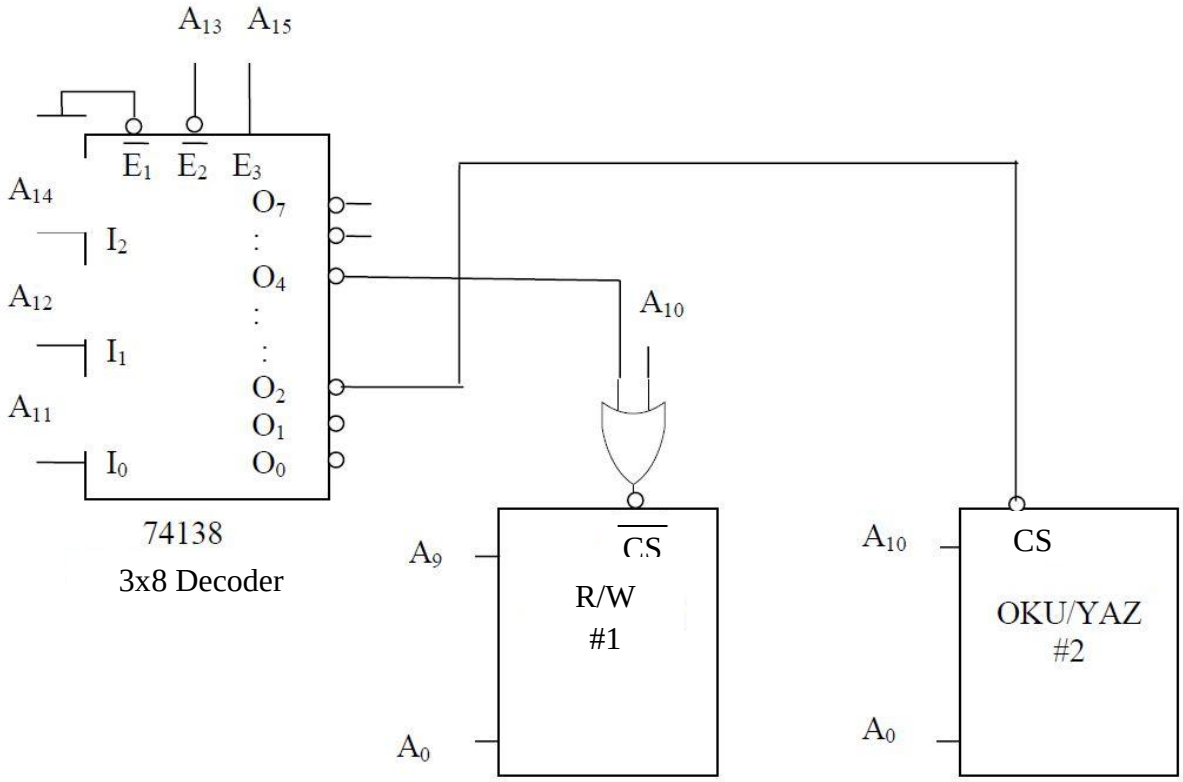
1. Address decoder circuit for two R/W memories are given below.
    a. Determine the sizes of both memories
    b. Determine the start and end addresses (span) of both memories
    c. Redesign the memory address decoder if we change only the span of second memory to $9000-$97FF. (First memory stays the same, do not use extra logic gates, you may change decoder output connections)



Solution:

a. First memory: 1K, Second memory 2K
b. First memory: $C000-$C3FF, Second memory: $6800-$6FFF

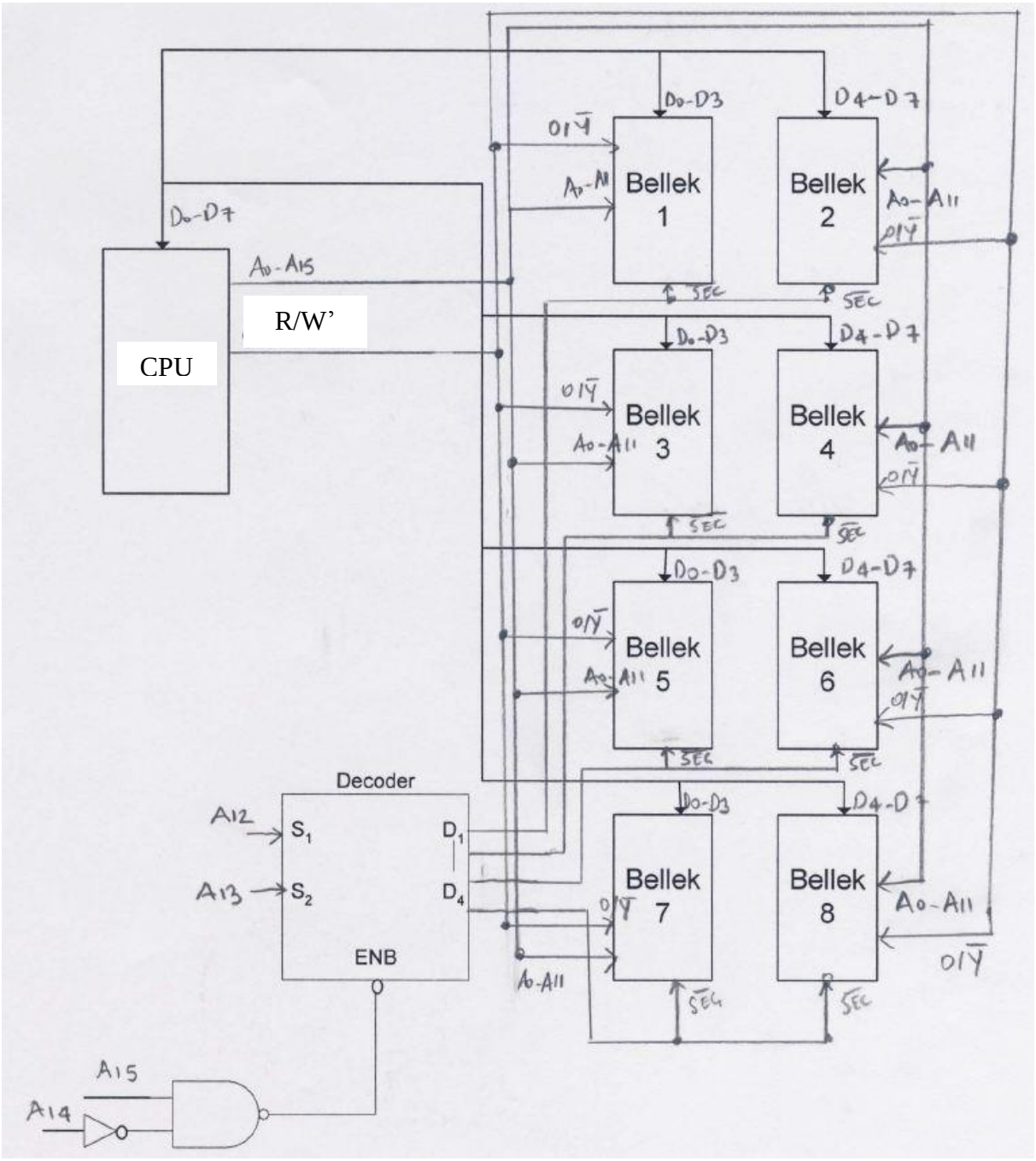
c.



2. We have 4K*4 R/W memory chips. Using these chips design a 16K*8 memory that starts from memory address $8000. Show instructional CPU connections. (Data bus is 8bits, address bus is 16bits)

Solution:

$A_{15}A_{14}A_{13}A_{12}$	$A_{11}A_{10}A_9A_8$	$A_7A_6A_5A_4$	$A_3A_2A_1A_0$	
1 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	$8000
1 0 0 0	1 1 1 1	1 1 1 1	1 1 1 1	$8FFF
1 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	$9000
1 0 0 1	1 1 1 1	1 1 1 1	1 1 1 1	$9FFF
1 0 1 0	0 0 0 0	0 0 0 0	0 0 0 0	$A000
1 0 1 0	1 1 1 1	1 1 1 1	1 1 1 1	$AFFF
1 0 1 1	0 0 0 0	0 0 0 0	0 0 0 0	$B000
1 0 1 1	1 1 1 1	1 1 1 1	1 1 1 1	$BFFF


CPU
R/W'
Bellek 1
Bellek 2
Bellek 3
Bellek 4
Bellek 5
Bellek 6
Bellek 7
Bellek 8
Decoder
ENB
A12
A13
A14
A15

O/Y = R/W

SEÇ = CS