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EHB322E Digital Electronic Circuits
MIDTERM II

Duration: 120 Minutes

Grading: 1) 40%, 2) 30%, 2) 30%

Exam is in closed-notes and closed-books format; calculators are allowed

For your answers please use the space provided in the exam sheet

GOOD LUCK!

1) Consider a Boolean function $f = x_1 + x_2 + x_3$ to be implemented by gates.
Suppose that all NMOS/PMOS transistors of gates are identical.
Equivalent resistor for an NMOS transistor: $\boldsymbol{R_N}$**= 12kΩ**
Equivalent resistor for a PMOS transistor: $\boldsymbol{R_P}$**= 24kΩ**
Suppose that each node in a gate has an internal capacitance of **0.1pF**.
Also a load capacitor of **1pF** is connected to the outputs of gates.

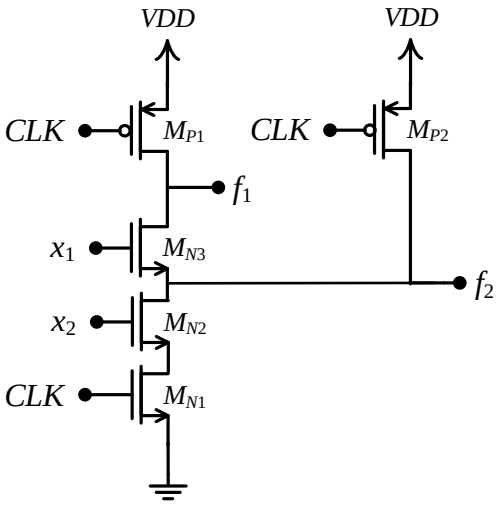
a) Implement $\boldsymbol{f}$ with "a CMOS Pass Transistor Gate". Find the **worst case (largest) and best case (smallest)** $\boldsymbol{t_{PHL}}$ **and** $\boldsymbol{t_{PLH}}$ values (total of 4 values).

b) Implement $\boldsymbol{f}$ with "a CMOS Dynamic Logic Gate". Find the **worst case (largest) and best case (smallest)** $\boldsymbol{t_{PHL}}$ **and** $\boldsymbol{t_{PLH}}$ values (total of 4 values).

- ***Hint:*** *in calculating delay values you can use Elmore delay model.*

2) Consider the CMOS dynamic circuit shown below. It has three inputs $\boldsymbol{x_1}$, $\boldsymbol{x_2}$, ***CLK*** and two outputs $\boldsymbol{f_1}$, $\boldsymbol{f_2}$.

- **a)** Derive expressions of $\boldsymbol{f_1}$ and $\boldsymbol{f_2}$ in terms of the inputs when ***CLK***=0.
- **b)** Derive expressions of $\boldsymbol{f_1}$ and $\boldsymbol{f_2}$ in terms of the inputs when ***CLK***=1.
- **c)** Does this circuit have a charge sharing problem? If yes, on which input condition?; if no, why?

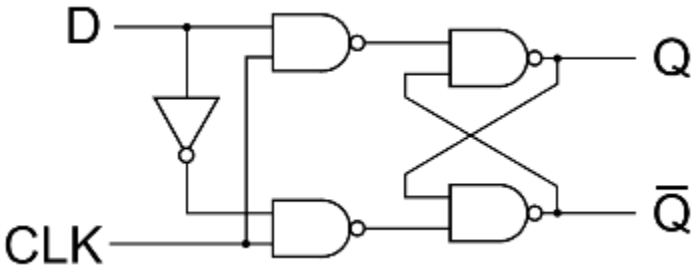


A CMOS Dynamic Circuit

3) Consider a D-flip-flop consisting of one inverter and four NAND gates, shown below.
Suppose that the inverter has t_{PHL}**=1ps** and t_{PLH} **=4ps**.
Suppose that each of the NAND gates has t_{PHL}**=1.5ps** and t_{PLH} **=1.5ps**.

a) When *CLK*=1 and the *D* input switches from 0 to 1, calculate the **total propagation delays** at the outputs Q and $\bar{Q}$.

b) When *CLK*=1 and the *D* input switches from 1 to 0, calculate the **total propagation delays** at the outputs Q and $\bar{Q}$.



A D-Flip-Flop