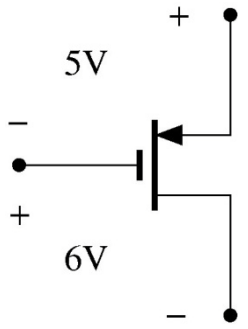
Problems for Introduction to MOS

Lecture notes: Sec. 4

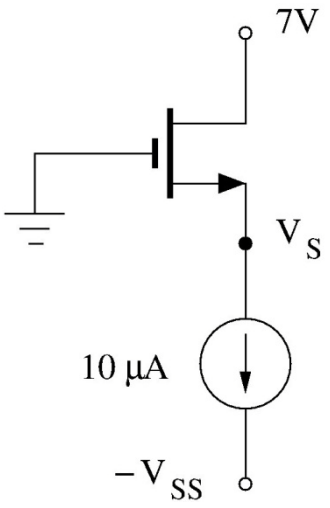
Exercise 1: Compute i_D ($\mu_p C_{ox}\,(W/L) = 0.4$ mA/V^2 , $V_{tp} = -3$ V and $\lambda = 0$).

- PMOS with $v_{SG} = 5$ V and $v_{GD} = 6$ V.
- $V_{OV} = v_{SG} - |\,V_{tp}\,| = 5 - 3 = 2$ V
  - $V_{OV} > 0 \;\rightarrow$ MOS is ON
- $v_{SD} = v_{SG} + v_{GD} = 5 + 6 = 11$ V
  - $v_{SD} = 11 > V_{OV} = 2 \;\rightarrow$ MOS in saturation
- $i_D = 0.5\mu_p C_{ox} \dfrac{W}{L} V_{OV}^2 = 0.5 \times 0.4 \times 10^{-3} (2)^2 = 0.8\,\text{mA}$



Exercise 2: Find V_S ($\mu_n C_{ox}(W/L) = 0.5$ mA/V^2 , $V_{tn} = 0.8$ V and $\lambda = 0$).

- Since $i_D = 10\ \mu\text{A}$, MOS is ON
- Assume MOS in saturation



$$i_D = 0.5\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

$$10\times10^{-6} = 0.5\times0.5\times10^{-3}\,V_{OV}^2 \rightarrow V_{OV} = 0.2\text{V}$$

$$v_{GS} = V_{OV} + V_t = 0.2 + 0.8 = 1\text{ V}$$

$$v_{GS} = V_G - V_S = 0 - V_S \rightarrow V_S = -1\text{ V}$$

$$v_{DS} = V_D - V_S = 7 - (-1) = 8\text{V}$$

$$v_{DS} = 8 > V_{OV} = 0.2\text{ V} \quad (\text{MOS in saturation})$$

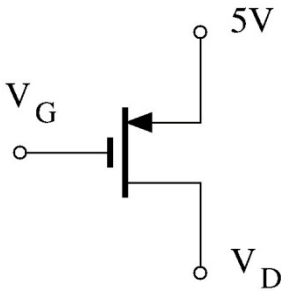
Exercise 3: Consider this PMOS with $\mu_p C_{ox}\,(W/L) = 0.6$ mA/V^2 , $V_{tp} = -1$ V and $\lambda = 0$.

A) For what values of V_G, PMOS will be ON?

B) For what values of V_D, PMOS will be in triode? (in terms of V_G)

C) For what values of V_D, PMOS will be in saturation? (in terms of V_G)

$$v_{SG} = V_S - V_G = 5 - V_G$$
$$v_{SD} = V_S - V_D = 5 - V_D$$
$$V_{OV} = v_{SG} - |V_{tp}| = 5 - V_G - |V_{tp}| = 4 - V_G$$



A) Range of V_G for MOS ON?

$$V_{OV} \geq 0 \rightarrow 4 - V_G \geq 0 \rightarrow V_G \leq 4\text{ V}$$

B) Range of V_D for MOS in triode?

$$v_{SD} \leq V_{OV} \rightarrow 5 - V_D \leq 4 - V_G \rightarrow V_D \geq V_G + 1$$

C) Range of V_D for MOS in saturation?

$$v_{SD} \geq V_{OV} \rightarrow 5 - V_D \geq 4 - V_G \rightarrow V_D \leq V_G + 1$$

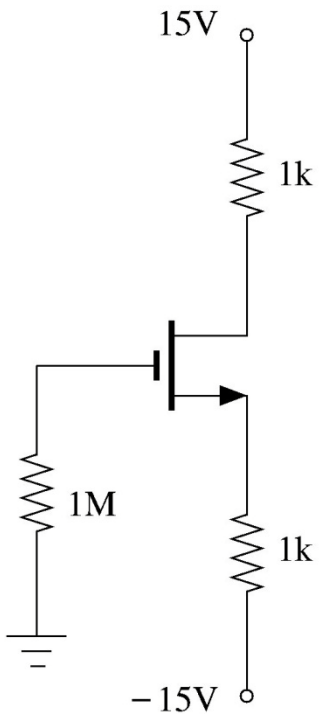
Exercise 4: Find v_{GS} , v_{DS}, and i_D ($\mu_n C_{ox}\,(W/L) = 0.4$ mA/V^2 , $V_{tn} = 3$ V and $\lambda = 0$).

$$\text{GS-KVL}: \quad 0 = 10^6\, i_G + v_{GS} + 10^3\, i_D - 15 = V_{OV} + V_t + 10^3\, i_D - 15$$

$$\rightarrow \quad 12 = V_{OV} + 10^3\, i_D$$

$$\text{DS-KVL}: \quad 15 = 10^3\, i_D + v_{DS} + 10^3\, i_D - 15$$

$$\rightarrow \quad 30 = v_{DS} + 2\times 10^3\, i_D$$



- Not in cut-off as for $i_D = 0$, GS-KVL gives $V_{OV} = 12$ V > 0.
- Assume MOS in saturation

$$i_D = 0.5\mu_n C_{ox} \frac{W}{L} V_{OV}^2$$

$$\text{GS-KVL}: \quad 12 = V_{OV} + 10^3 \times 0.5 \times 0.4 \times 10^{-3}\, V_{OV}^2$$

$$0.2\, V_{OV}^2 + V_{OV} - 12 = 0$$

$$V_{OV} = -10.64\text{V} \quad (\text{incorrect, need } V_{OV} > 0)$$

$$V_{OV} = 5.64\text{V} \quad \rightarrow \quad v_{GS} = 8.64\text{V}$$

$$\text{GS-KVL}: \quad 12 = V_{OV} + 10^3\, i_D \quad \rightarrow \quad i_D = 6.36\,\text{mA}$$

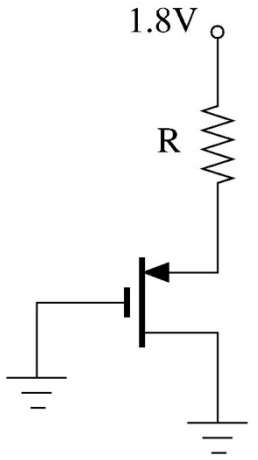
$$\text{DS-KVL}: \quad 30 = v_{DS} + 2\times 10^3\, i_D \quad \rightarrow \quad v_{DS} = 17.27\ \text{V}$$

$$v_{DS} = 17.3 > V_{OV} = 5.64\ \text{V} \quad (\text{MOS in saturation})$$

Exercise 5: Find R such that PMOS is in saturation with $V_{OV} = 0.6$ V ($\mu_p C_{ox} = 0.1$ mA/V^2, $W/L = 10/0.18$, $V_{tp} = -0.4$ V and $\lambda = 0$).

In an IC, W/L (typically specified as a fraction) is a design parameter for MOS circuits.

$$i_D = 0.5\mu_p C_{ox}\frac{W}{L}V_{OV}^2 = 0.5\times 0.1\times 10^{-3}\times(10/0.18)\times(0.6)^2 = 1\,\text{mA}$$

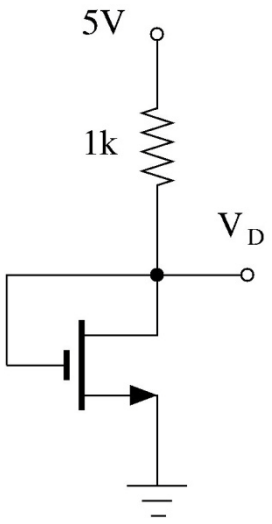


$$\text{SG-KVL}: \quad 1.8 = Ri_D + v_{SG}$$
$$= 10^{-3}R + V_{OV} + |V_{tp}|$$
$$1.8 = 10^{-3}R + 0.6 + 0.4$$
$$R = 800\,\Omega$$

$$\text{SD-KVL}: \quad 1.8 = R\,i_D + v_{SD} \rightarrow \quad v_{SD} = 1.0\text{ V}$$
$$v_{SD} = 1.0 > V_{OV} = 0.6 \rightarrow \text{ MOS in saturation}$$

Exercise 6: Find V_D ($\mu_n C_{ox}(W/L) = 0.5$ mA/V^2 , $V_{tn} = 0.8$ V and ignore channel-width modulation).

- When the gate and drain of a MOS are connected to each other, MOS becomes a 2-terminal device.
  - Called diode-connected transistor
- If MOS is ON ($v_{DS} = v_{GS} \geq V_{tn}$), MOS will always be in saturation!
  - $v_{DS} = v_{GS} \geq v_{GS} - V_{tn} = V_{OV}$



$$i_D = 0.5\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

$$\text{DS/GS - KVL}: \quad 5 = 10^3 i_D + v_{GS} = 10^3 \times 0.5 \times 0.5 \times 10^{-3} V_{OV}^2 + V_{OV} + V_{tn}$$

$$0.25\,V_{OV}^2 + V_{OV} - 4.2 = 0$$

$$V_{OV} = -6.56\text{V} \quad (\text{incorrect, need } V_{OV} > 0)$$

$$V_{OV} = 2.56\text{V}$$

$$v_{GS} = V_{OV} + V_{tn} \rightarrow V_D = v_{DS} = v_{GS} = 3.36\text{V}$$

Exercise 7: Find V_1 and V_2 ($\mu_n C_{ox}(W/L) = 5$ mA/V^2 , $V_t = 1$ V and ignore channel-width modulation).

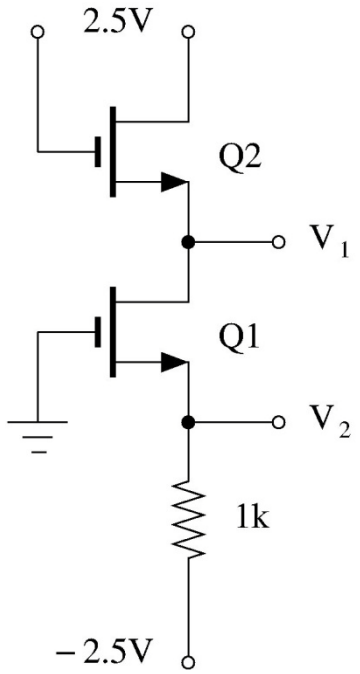
$$\text{GS1-KVL}: \quad 0 = v_{GS1} + 10^3 i_D - 2.5 = V_{OV1} + V_t + 10^3 i_D - 2.5$$

$$\rightarrow \quad V_{OV1} + 10^3 i_D = 1.5$$

$$\text{GS2-KVL}: \quad 2.5 = v_{GS2} + v_{DS1} + 10^3 i_D - 2.5$$

$$\text{DS-KVL}: \quad 2.5 = v_{DS2} + v_{DS1} + 10^3 i_D - 2.5$$

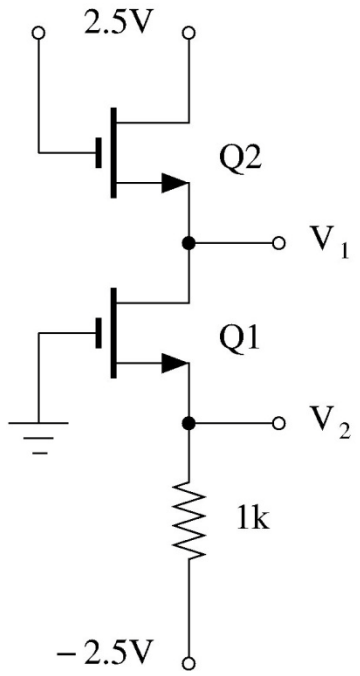
$$\text{KCL}: \quad i_{D1} = i_{D2} = i_D$$



- Q1 is not in cut-off as for $i_{D1} = 0$, GS1-KVL gives $V_{OV} = 1.5\ \text{V} > 0$.
  - Q2 is not in cut-off either as $i_{D1} = i_{D2} > 0$

Exercise 7 (cont'd) : Find V_1 and V_2 ($\mu_n C_{ox}\,(W/L) = 5$ mA/V^2 , $V_t = 1$ V and ignore channel-width modulation).

Assume both MOS in saturation



$$i_D = i_{D1} = 0.5\mu_n C_{ox}\frac{W}{L}\,V_{OV1}^2$$

GS1-KVL : $1.5 = V_{OV1} + 10^3\, i_D = V_{OV1} + 10^3 \times 0.5 \times 5 \times 10^{-3}\, V_{OV}^2$

$$2.5\,V_{OV1}^2 + V_{OV1} - 1.5 = 0$$

$$V_{OV1} = -1.0\text{V} \quad (\text{incorrect, need } V_{OV} > 0)$$

$$V_{OV1} = 0.60\text{V}$$

Both MOS in saturation, $i_{D2} = i_{D1}$ and $\lambda = 0$: $V_{OV2} = V_{OV1} = 0.60$ V

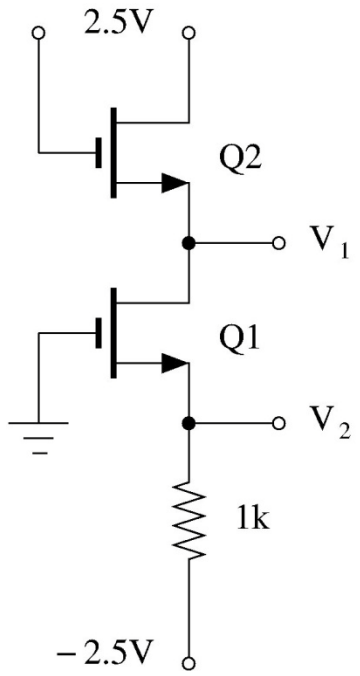
$$v_{GS1} = V_{OV1} + V_t = 0.6 + 1 = 1.6\text{ V}$$

$$v_{GS1} = V_{G1} - V_{S1} = 0 - V_2 \;\rightarrow\; V_2 = -1.6\text{ V}$$

$$v_{GS2} = V_{OV2} + V_t = 0.6 + 1 = 1.6\text{ V}$$

$$v_{GS2} = V_{G2} - V_{S2} = 2.5 - V_1 \;\rightarrow\; V_1 = 0.9\text{ V}$$

Exercise 7 (cont'd) : Find V_1 and V_2 ($\mu_n C_{ox}\,(W/L) = 5$ mA/V^2 , $V_t = 1$ V and ignore channel-width modulation).



Need to confirm our assumption of both MOS in saturation

$$v_{DS1} = V_{D1} - V_{S1} = V_1 - V_2 = 0.90 - (-1.6) = 2.5\ \text{V}$$
$$v_{DS1} = 2.5 > V_{OV1} = 0.6\ \text{V}$$

$$v_{DS2} = V_{D2} - V_{S2} = 2.5 - V_1 = 2.5 - 0.9 = 1.6\ \text{V}$$
$$v_{DS2} = 1.6 > V_{OV2} = 0.6\ \text{V}$$

For circuits with multiple transistors, it is usually advantageous to keep track of node voltages (at transistor terminals!