

ECE65 Course Summary

Devices

Diode iv characteristics equation

$$i_D = I_S \left(e^{v_D/nV_T} - 1 \right)$$

I_S : Reverse Saturation Current
(10^{-9} to 10^{-18} A)

V_T : Volt-equivalent temperature
(= 26 mV at room temperature)

n : Emission coefficient
($1 \leq n \leq 2$ for Si ICs)

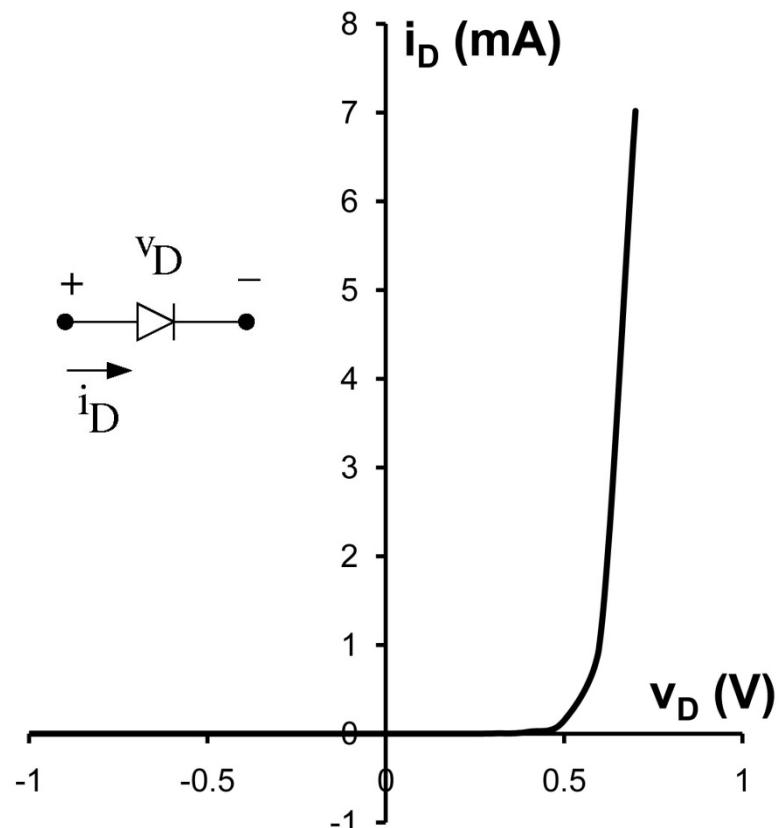
For $|v_D| \geq 3nV_T$

Forward bias: $i_D \approx I_S e^{v_D/nV_T}$

Reverse bias: $i_D \approx -I_S$

Sensitive to temperature:

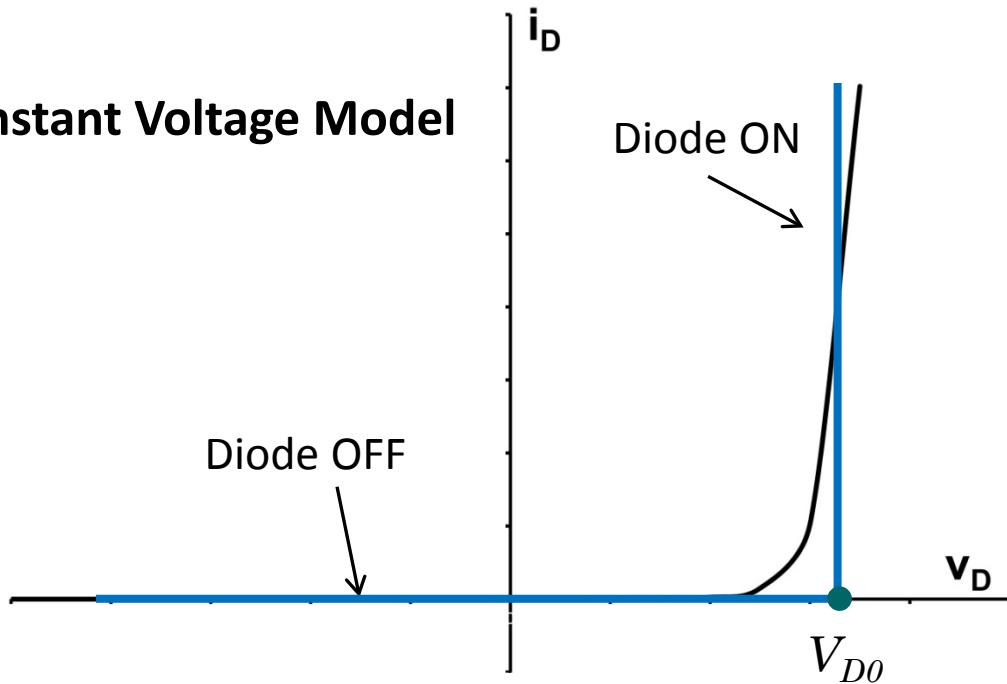
- I_S doubles for every 7°C increase
- $V_T = T(\text{k}) / 11,600$



For derivation of diode iv equation, see Sedra & Smith Sec. 3

Diode piecewise-linear model: Diode iv is approximated by two lines

Constant Voltage Model



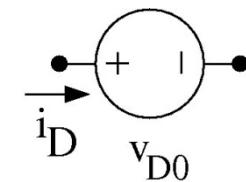
Diode ON: $v_D = V_{D0}$ and $i_D \geq 0$

Diode OFF: $i_D = 0$ and $v_D < V_{D0}$

"cut-in" voltage, $V_{D0} = 0.6 - 0.7$ V for Si

Circuit Models:

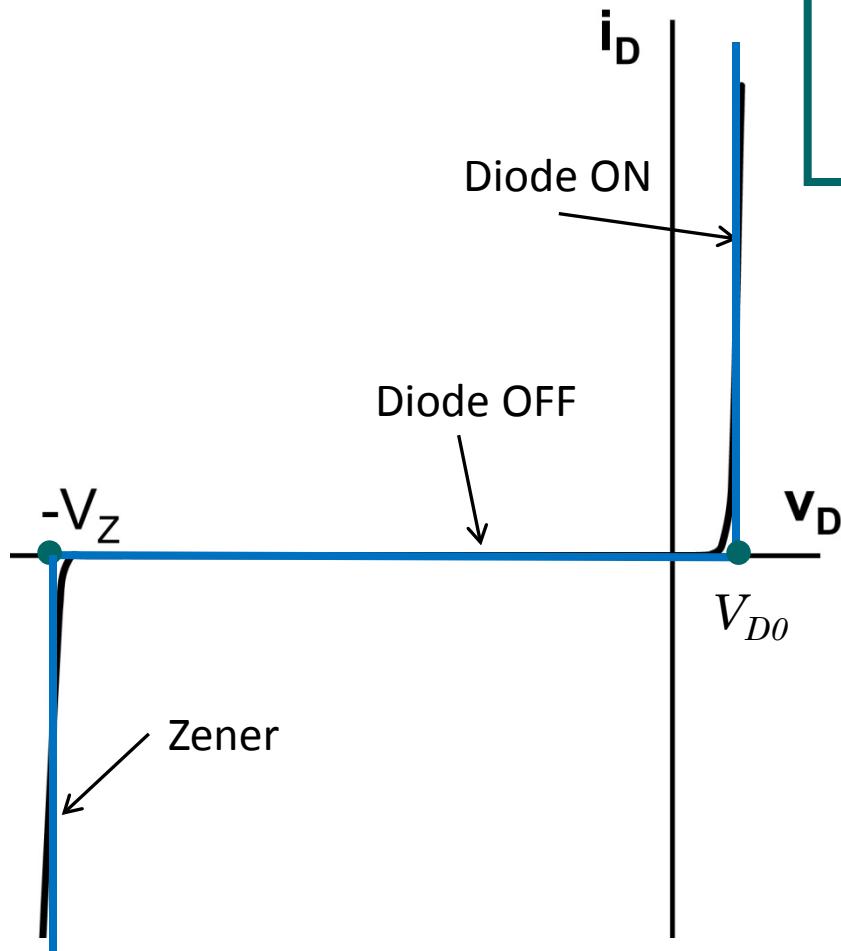
ON:



OFF:



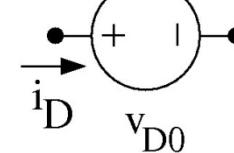
Zener Diode piecewise-linear model



Diode ON: $v_D = V_{D0}$ and $i_D \geq 0$
Diode OFF: $i_D = 0$ and $-V_Z < v_D < V_{D0}$
Zener: $v_D = -V_Z$ and $i_D \leq 0$

Circuit Models:

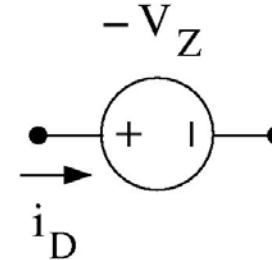
ON:



OFF:



Zener:



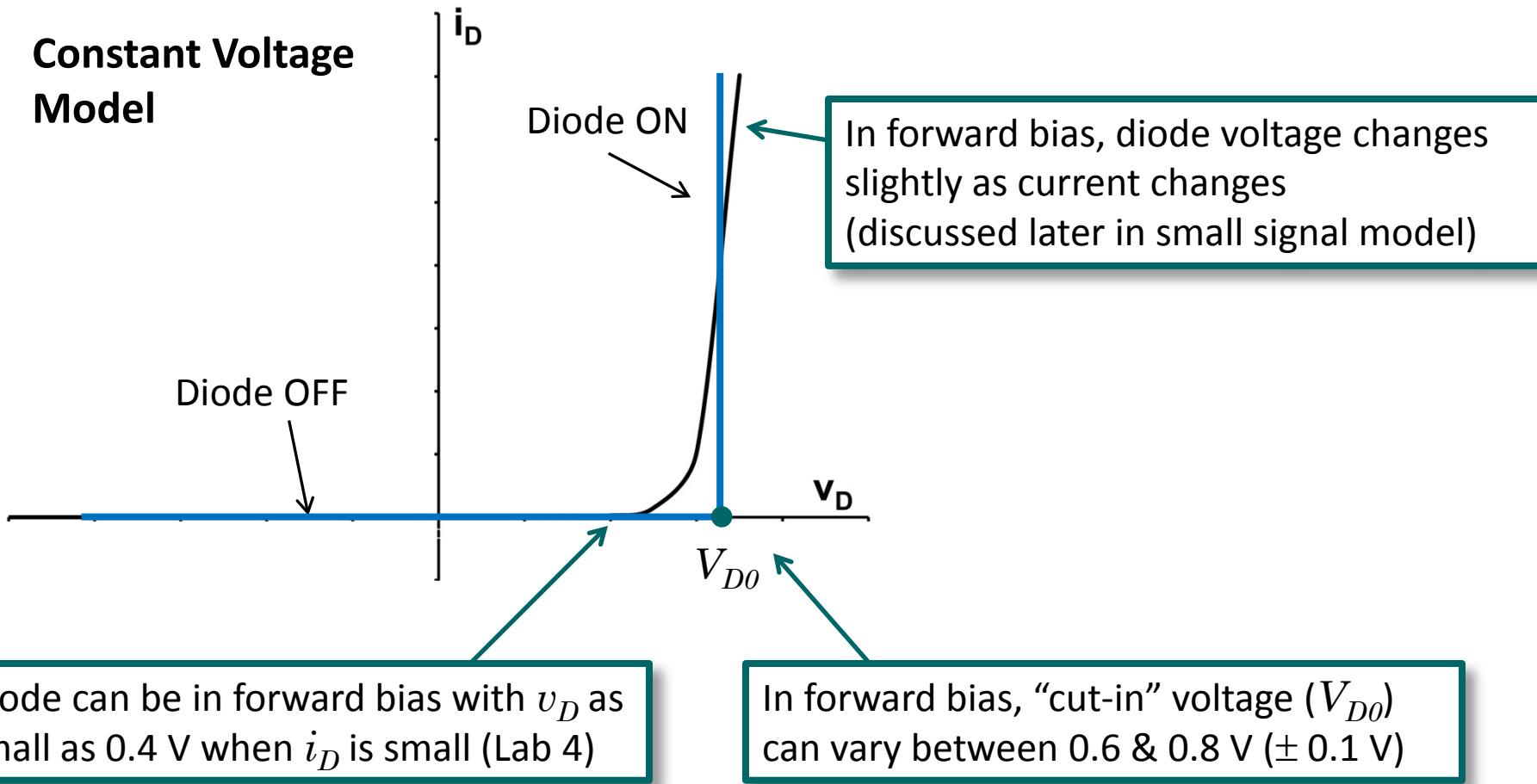
Recipe for solving diode circuits

Recipe:

1. Draw a circuit for each state of diode(s).
2. Solve each circuit with its corresponding diode equation.
3. Use the inequality for that diode state (“range of validity”) to check
 - o if the solution is valid if circuit parameters are all known.
 - o to find the range of circuit “variable” which leads to that state.

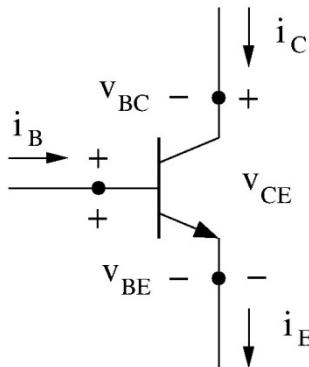
Accuracy of Constant-Voltage Model

**Constant Voltage
Model**



BJT iv characteristics includes four parameters

NPN transistor



- Two transistor parameters can be written in terms of the other four:

$$\text{KCL: } i_E = i_C + i_B$$

$$\text{KVL: } v_{BC} = v_{BE} - v_{CE}$$

- BJT iv characteristics equations are:

$$i_B = f(v_{BE})$$

$$i_C = g(i_B, v_{CE})$$

Cut-off :
BE is reverse biased

$$i_B = 0, \quad i_C = 0$$

Active:
BE is forward biased
BC is reverse biased

$$i_B = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{v_{BE}/V_T}$$

$$i_C = I_S e^{v_{BE}/V_T} \left(1 + \frac{v_{CE}}{V_A} \right)$$

(Deep) Saturation:
BE is forward biased
BC is forward biased

$$i_B = \frac{I_S}{\beta} e^{v_{BE}/V_T}$$

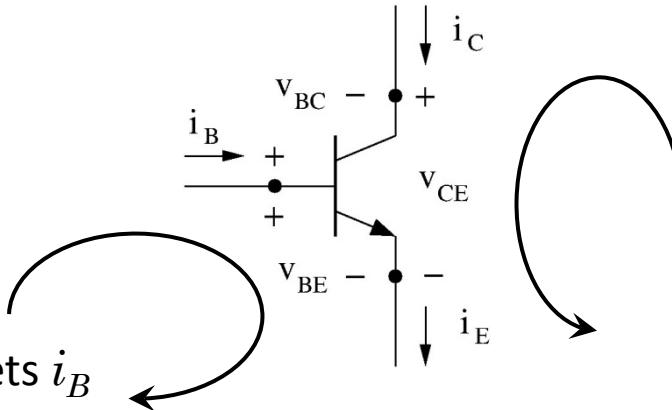
$$v_{CE} \approx V_{sat}, \quad i_C < \beta i_B$$

Transistor operates like a “valve”

i_C & v_{CE} are controlled by i_B

Controller part:

Circuit connected to BE sets i_B



Controlled part:
 i_C & v_{CE} are set by
transistor state (&
outside circuit)

BJT Linear Model

- **Cut-off** ($i_B = 0, v_{BE} < V_{D0}$): **Valve Closed** $i_C = 0,$
- **Active** ($i_B > 0, v_{BE} = V_{D0}$): **Valve partially open** $i_C = \beta i_B, v_{CE} > V_{D0}$
- **Saturation** ($i_B > 0, v_{BE} = V_{D0}$): **Valve open** $i_C < \beta i_B, v_{CE} = V_{sat}$
- For PNP transistor, replace v_{BE} with v_{EB} and replace v_{CE} with v_{EC} in the above.

For Si, $V_{D0} = 0.7$ V, $V_{sat} = 0.2$ V

* BJT Linear model is based on a diode “constant-voltage” model for the BE junction and ignores Early effect.

Recipe for solving BJT circuits

(State of BJT is unknown before solving the circuit)

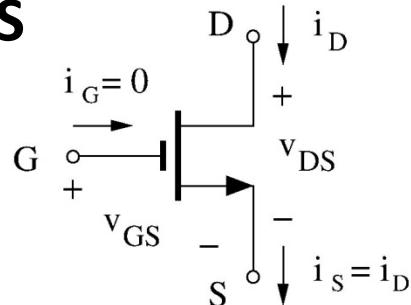
1. Write down BE-KVL and CE-KVL:
2. Assume BJT is OFF, Use BE-KVL to check:
 - a. BJT OFF: Set $i_C = 0$, use CE-KVL to find v_{CE} (Done!)
 - b. BJT ON: Compute i_B
3. Assume BJT in active. Set $i_C = \beta i_B$. Use CE-KVL to find v_{CE} .
If $v_{CE} \geq V_{D0}$, Assumption Correct, otherwise in saturation:
4. BJT in Saturation. Set $v_{CE} = V_{sat}$. Use CE-KVL to find i_C .
(Double-check $i_C < \beta i_B$)

NOTE:

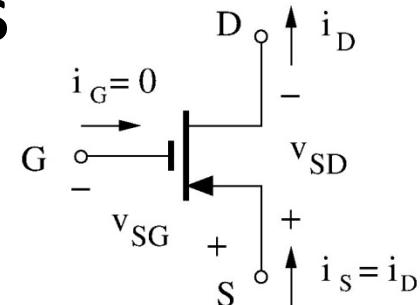
- o For circuits with R_E , both BE-KVL & CE-KVL have to be solved simultaneously.

MOS i-v Characteristics Equations

NMOS



PMOS



NMOS ($V_{OV} = v_{GS} - V_{tn}$)

Cut - Off : $V_{OV} \leq 0$

$$i_D = 0$$

Triode : $V_{OV} \geq 0$ and $v_{DS} \leq V_{OV}$

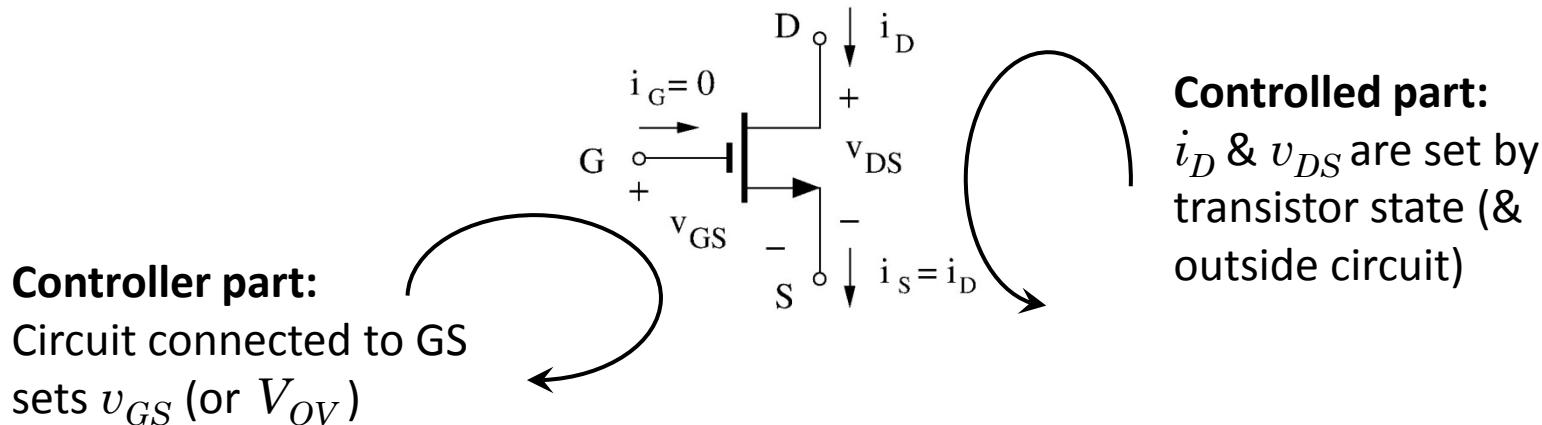
$$i_D = 0.5\mu_n C_{ox} \frac{W}{L} [2V_{OV}v_{DS} - v_{DS}^2]$$

Saturation : $V_{OV} \geq 0$ and $v_{DS} \geq V_{OV}$

$$i_D = 0.5\mu_n C_{ox} \frac{W}{L} V_{OV}^2 [1 + \lambda v_{DS}]$$

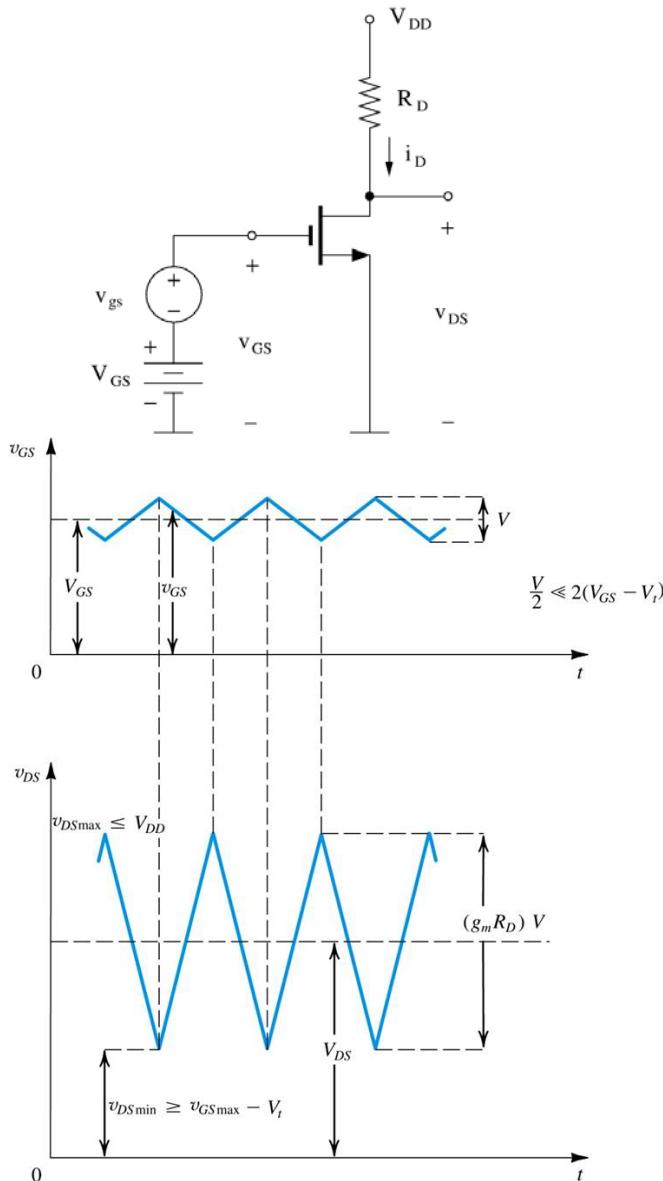
○ For PMOS set $V_{OV} = v_{SG} - |V_{tp}|$ & replace v_{DS} with v_{SD} in the above

MOS operation is “Conceptually” similar to a BJT -- i_D & v_{DS} are controlled by v_{GS}



- A similar solution method to BJT:
 - Write down GS-KVL and DS-KVL, assume MOS is in a particular state, solve with the corresponding MOS equation and validate the assumption.
- MOS circuits are simpler to solve because $i_G = 0$!
 - However, we get a quadratic equation to solve if MOS in triode (check MOS in saturation first!)

Foundation of Transistor Amplifiers



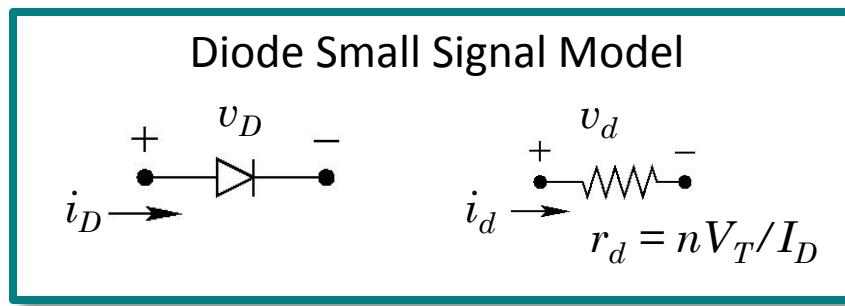
- MOS is always in saturation (BJT in active)
- Input to transistor is made of a constant bias part (V_{GS}) and a signal (v_{gs}):
 $v_{GS} = V_{GS} + v_{gs}$
- Response ($v_o = v_{DS}$) is also made of a constant part (V_{DS}) and a signal response part (v_{ds}):
 $v_{DS} = V_{DS} + v_{ds}$
- V_{DS} , is ONLY related to V_{GS} :
 - i.e., if $v_{gs} = 0$, then $v_{ds} = 0$
- The response to the signal is linear, i.e., $v_{ds} / v_{gs} = \text{const.}$ But
 - v_{GS} / v_{DS} is NOT a constant!
 - V_{GS} / V_{DS} is NOT a constant!

Issues in developing a transistor amplifier:

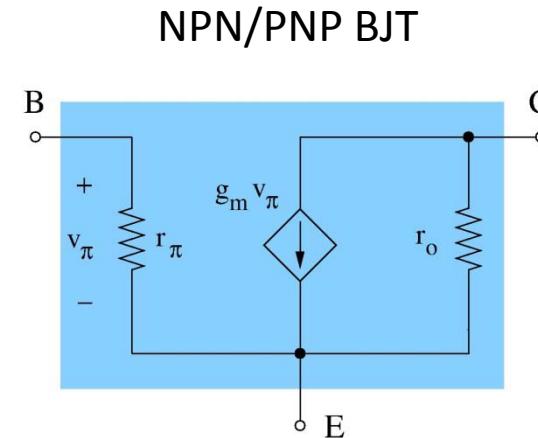
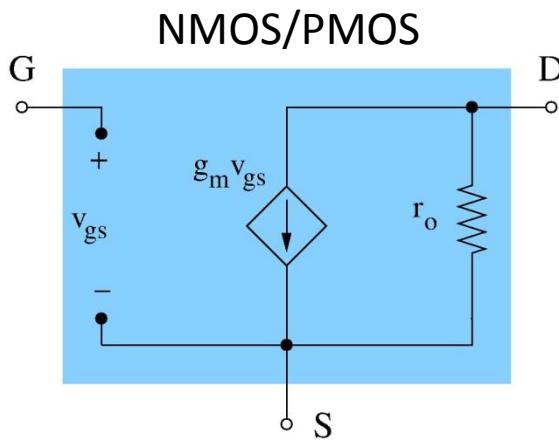
- 1. Find the iv characteristics of the elements for the signal** (which can be different than their characteristics equation for bias).
 - This will lead to different circuit configurations for bias versus signal
- 2. Compute circuit response to the signal**
 - Focus on fundamental transistor amplifier configurations
- 3. How to establish a Bias point** (bias is the state of the system when there is no signal).
 - Stable and robust bias point should be resilient to variations in $\mu_n C_{ox} (W/L)$, V_t (or β for BJT) due to temperature and/or manufacturing variability.
 - Bias point details impact small signal response (e.g., gain of the amplifier).

Summary of signal circuit elements

- Resistors & capacitors: The Same
 - Capacitor act as open circuit in the bias circuit.
- Independent voltage source (e.g., V_{DD}): Effectively grounded
- Independent current source: Effectively open circuit
- Dependent sources: The Same
- Non-linear Elements: Different!
 - Diodes & transistors ?



Transistor Small Signal Models



$$g_m = \frac{2 \cdot I_D}{V_{OV}} \quad r_o \approx \frac{1}{\lambda \cdot I_D}$$

$$r_\pi = \frac{V_T}{I_B} \quad g_m = \frac{I_C}{V_T} = \frac{\beta}{r_\pi} \quad r_o \approx \frac{V_A}{I_C}$$

➤ Comparison of MOS and BJT small-signal circuit models:

1. MOS has an infinite resistor in the input (v_{gs}) while BJT has a finite resistor, r_π (typically several kΩ).
2. BJT g_m is substantially larger than that of a MOS (BJT has a much higher gain).
3. r_o values are typically similar (10s of kΩ). $g_m r_o \gg 1$ for both.

Transistor Biasing

- To make bias point independent of changes in transistor parameters (e.g. β ,) the bias circuit should “set” I_C and NOT I_B !

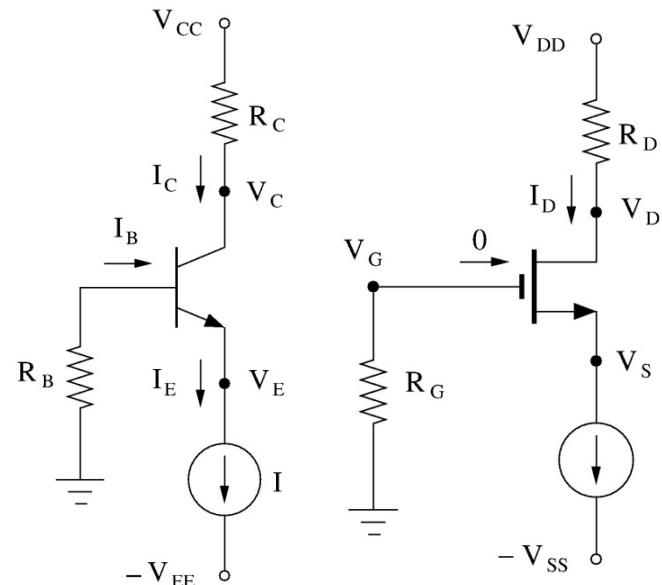
Emitter Degeneration (BJT):

- Requires a resistor in the emitter circuit.
- Requirements:
 1. $R_B \ll (\beta_{\min} + 1)R_E$
 2. $I_E R_E \geq 1\text{V}$

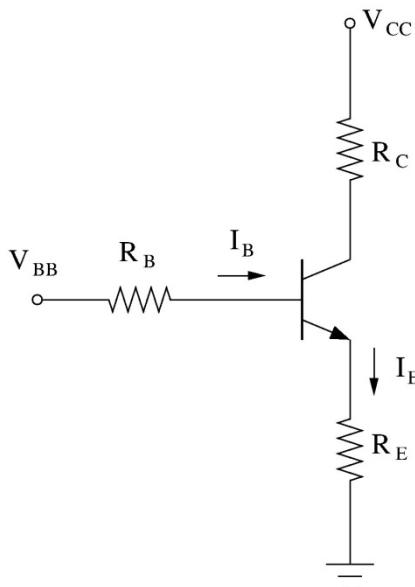
Source Degeneration (MOS):

- Requires a resistor in the source circuit.
- Requirement:
 1. $R_S I_D > V_{GS}$

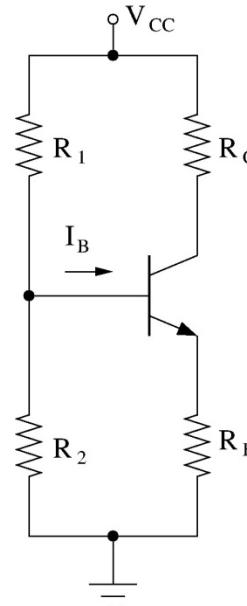
Current source:



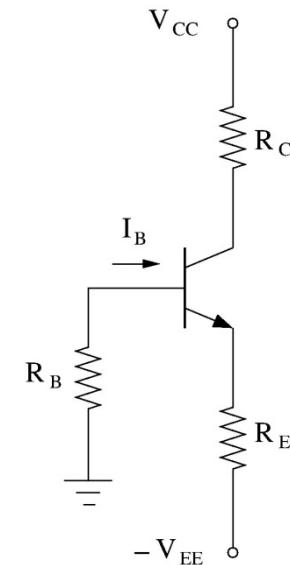
Emitter-degeneration bias circuits



Basic Arrangement



Bias with one power supply
(voltage divider)



Bias with two power supplies

- MOS source-degeneration bias circuits are identical
- To solve circuits with voltage divider bias:
 1. BJT: replace voltage divider with its Thevenin equivalent.
 2. MOS: Since $i_G = 0$, calculate V_G directly.

BJT Current Mirrors are based on two identical transistor with $v_{BE,ref} = v_{BE1}$

- Q_{ref} is always in active since

$$i_{C,ref} > 0$$

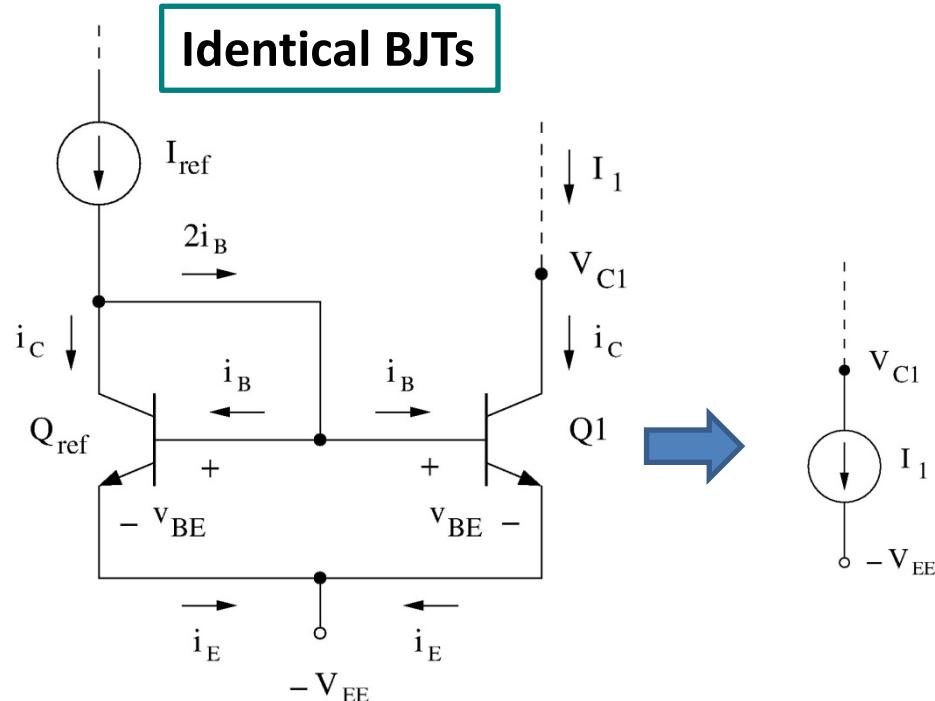
$$V_{CE,ref} = V_{BE,ref} = V_{D0}$$

- Identical BJTs and $v_{BE,ref} = v_{BE1}$
 - BJTs will have the same i_B and the same i_C (ignoring Early effect)

KCL: $I_{ref} = i_{C,ref} + 2i_B = i_C + 2\frac{i_C}{\beta}$

$$I_1 = i_C = \frac{I_{ref}}{1+2/\beta} \approx I_{ref}$$

- Since $I_1 = \text{const.}$ regardless of V_{C1} , this is a current source!



- For the current mirror to work, Q₁ should be in active:

$$V_{CE1} = V_{C1} + V_{EE} \geq V_{D0}$$

MOS Current-Steering Circuit are based on two identical transistor with $V_{ov,ref} = V_{ov1}$

- Q_{ref} is always in saturation since

$$V_{DS,ref} = V_{GS,ref} > V_{GS,ref} - V_t$$

$$\text{➤ } V_{GS,ref} = V_{GS1} = V_{GS}$$

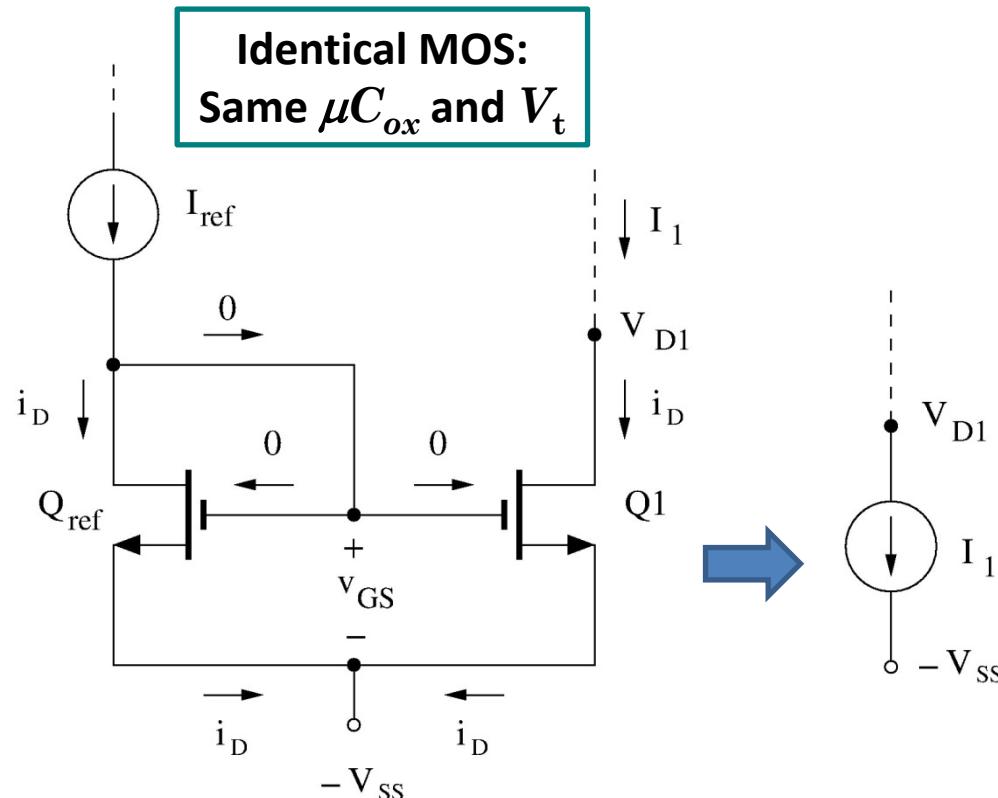
$$\text{➤ } V_{OV,ref} = V_{OV1} = V_{OV}$$

$$I_{ref} = i_{D,ref} = 0.5 \mu_n C_{ox} (W/L)_{ref} V_{OV}^2$$

$$I_1 = i_{D1} = 0.5 \mu_n C_{ox} (W/L)_1 V_{OV}^2$$

$$\frac{I_1}{I_{ref}} = \frac{(W/L)_1}{(W/L)_{ref}}$$

- Since $I_1 = \text{const.}$ regardless of V_{D1} , this is a current source!

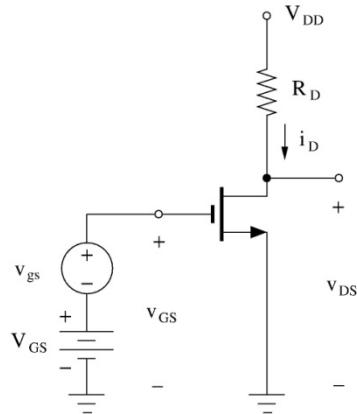


- For the current steering circuit to work, Q1 should be in saturation:

$$V_{DS1} > V_{OV} = V_{GS} - V_t$$

How to add signal to the bias

Bias & Signal
 $v_{GS} = V_{GS} + v_{gs}$



Bias & Signal
 $v_{DS} = V_{DS} + v_{ds}$

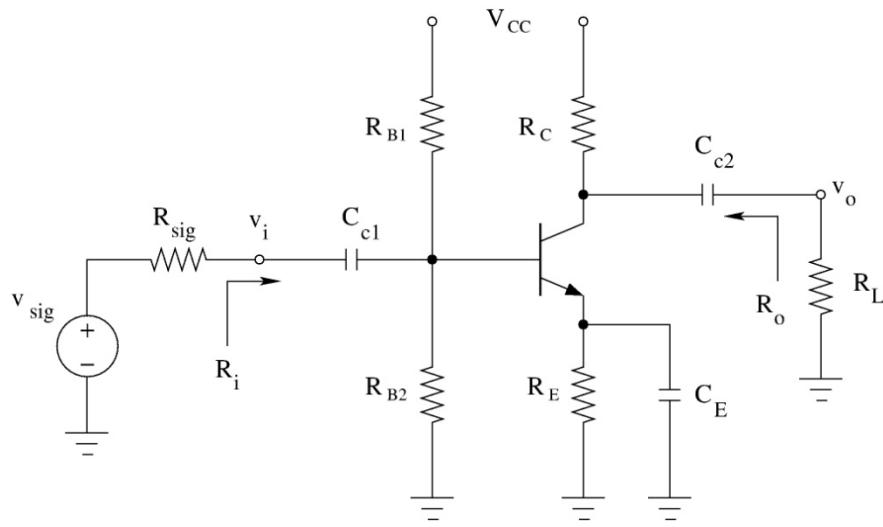
2. Capacitive Coupling

- Use a capacitor to separate bias voltage from the signal.
- Simplified biasing problem.
- Used in discrete circuits
- Only amplifies “AC” signals

1. Direct Coupling

- Use bias with 2 voltage supplies
 - For the first stage, bias such that $V_{GS} = 0$
 - For follow-up stages, match bias voltages between stages
- Difficult biasing problem
- Used in ICs
- Amplifies “DC” signals!

Discrete CE and CS Amplifiers

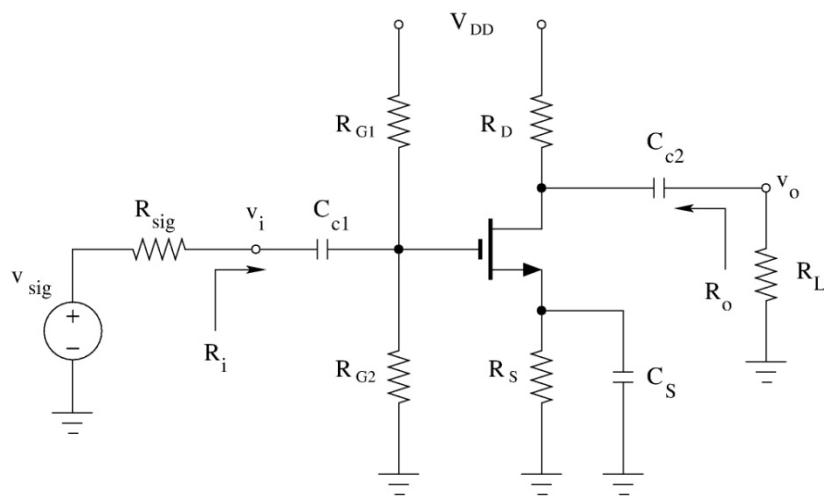


$$\frac{v_o}{v_i} = -g_m(r_o \parallel R_C \parallel R_L)$$

$$R_i = R_B \parallel r_\pi$$

$$R_o = R_C \parallel r_o$$

$r_\pi \rightarrow \infty$



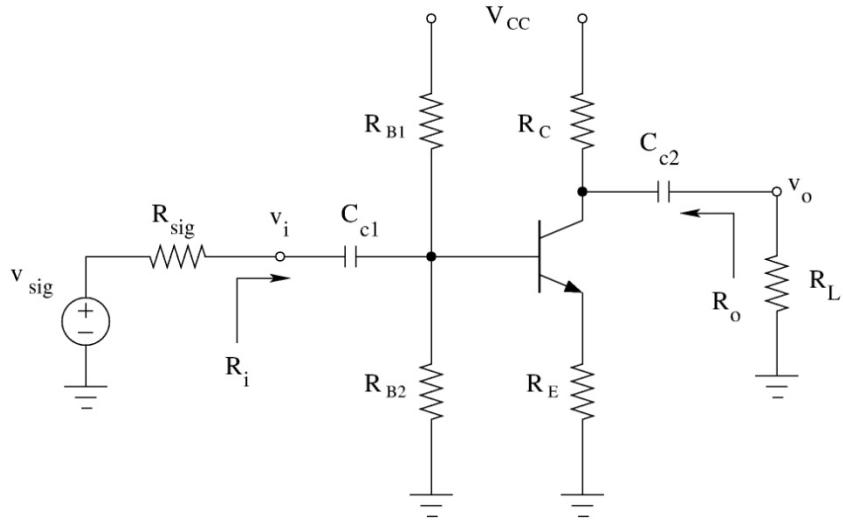
$$\frac{v_o}{v_i} = -g_m(r_o \parallel R_D \parallel R_L)$$

$$R_i = R_G$$

$$R_o = R_D \parallel r_o$$

$$\frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{v_o}{v_i}$$

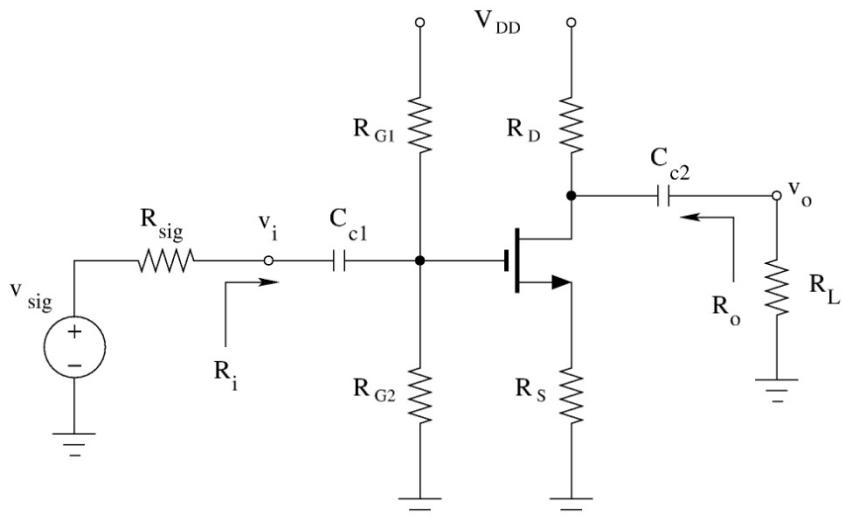
Discrete CE and CS Amplifiers with R_E / R_S



$$\frac{v_o}{v_i} = -\frac{g_m(R_C \parallel R_L)}{1 + g_m R_E + [(R_C \parallel R_L)/r_o](1 + R_E/r_\pi)}$$

$$R_i = R_B \parallel \left[r_\pi + R_E + \frac{\beta R_E}{1 + [(R_C \parallel R_L)/r_o]} \right]$$

$$R_o = R_C \parallel \left[r_o \left(1 + \frac{\beta R_E}{r_\pi + R_E + R_B \parallel R_{sig}} \right) \right]$$



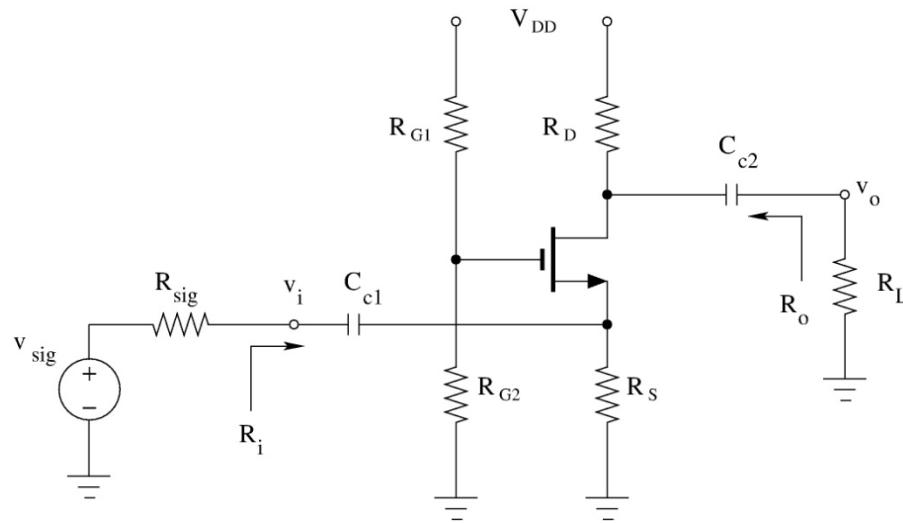
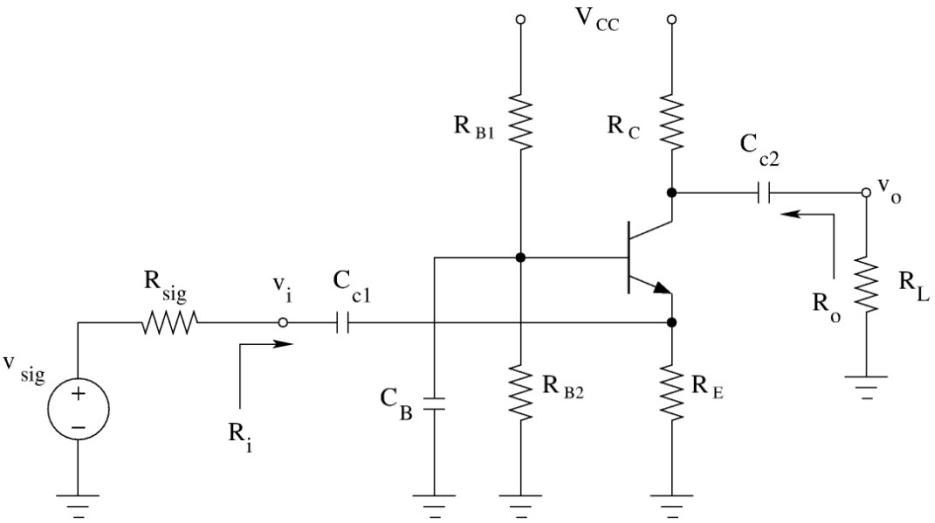
$$\frac{v_o}{v_i} = -\frac{g_m(R_D \parallel R_L)}{1 + g_m R_S + (R_D \parallel R_L)/r_o}$$

$$R_i = R_G$$

$$R_o = R_D \parallel [r_o(1 + g_m R_S)]$$

$$\frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{v_o}{v_i}$$

Discrete CB and CG Amplifiers



$$\frac{v_o}{v_i} = +g_m(r_o \parallel R_C \parallel R_L)$$

$$R_i = R_E \parallel r_\pi \parallel \left[\frac{r_o + (R_C \parallel R_L)}{1 + g_m r_o} \right]$$

$$R_o = R_C \parallel \left\{ r_o [1 + g_m (r_\pi \parallel R_E \parallel R_{sig})] \right\}$$

$r_\pi \rightarrow \infty$

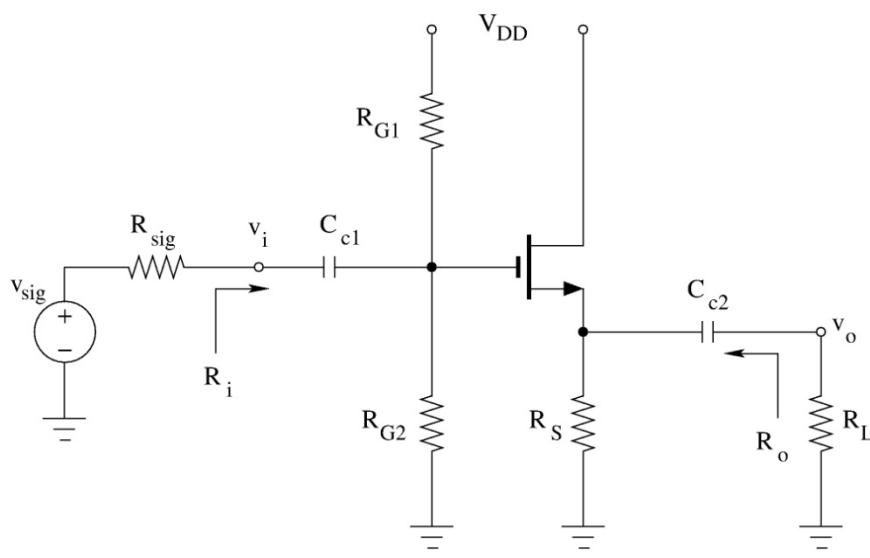
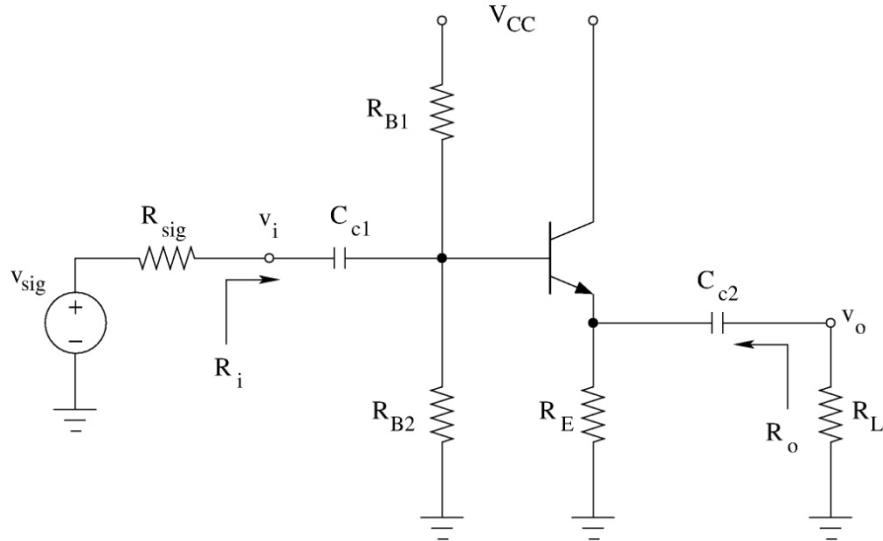
$$\frac{v_o}{v_i} = +g_m(r_o \parallel R_D \parallel R_L)$$

$$R_i = R_S \parallel \left[\frac{r_o + (R_D \parallel R_L)}{1 + g_m r_o} \right]$$

$$R_o = R_D \parallel \left\{ r_o [1 + g_m (R_S \parallel R_{sig})] \right\}$$

$$\frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{v_o}{v_i}$$

Discrete CC and CD Amplifiers



$$\frac{v_o}{v_i} = \frac{g_m(r_o \parallel R_E \parallel R_L)}{1 + g_m(r_o \parallel R_E \parallel R_L)}$$

$$R_i = R_B \parallel [r_\pi + \beta(r_o \parallel R_E \parallel R_L)]$$

$$R_o \approx R_E \parallel \frac{r_\pi + R_B \parallel R_{sig}}{\beta} \parallel r_o$$

$$\frac{v_o}{v_i} = \frac{g_m(r_o \parallel R_S \parallel R_L)}{1 + g_m(r_o \parallel R_S \parallel R_L)}$$

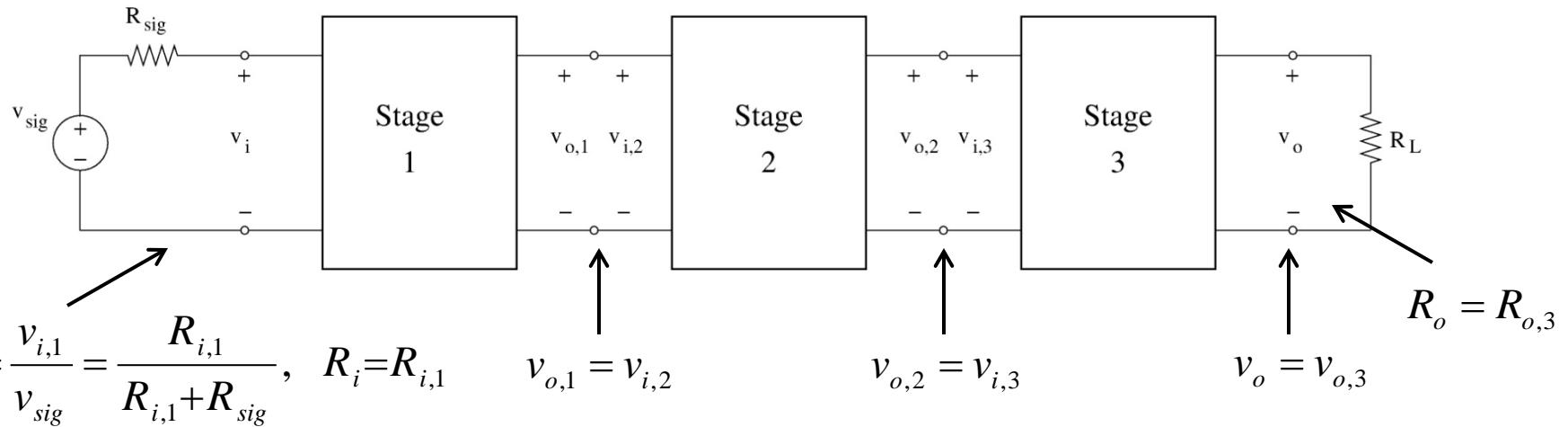
$$R_i = R_G$$

$$R_o = R_S \parallel \frac{1}{g_m}$$

$$\frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{v_o}{v_i}$$

Gain of a multi-stage amplifier

Example: A 3-stage amplifier



$$\frac{v_o}{v_{i,1}} = \frac{v_{o,3}}{v_{i,1}} = \frac{v_{o,1}}{v_{i,1}} \times \frac{v_{o,2}}{v_{i,1}} \times \frac{v_{o,3}}{v_{i,1}}$$

$$v_{o1} = v_{i2}$$

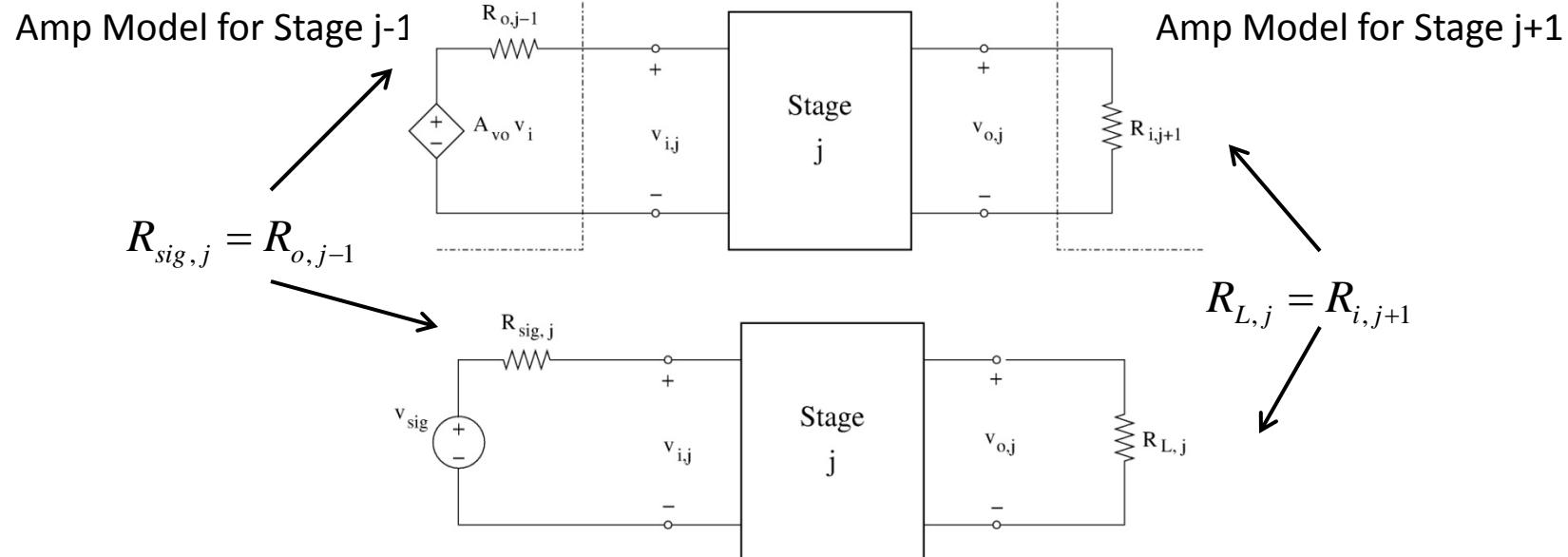
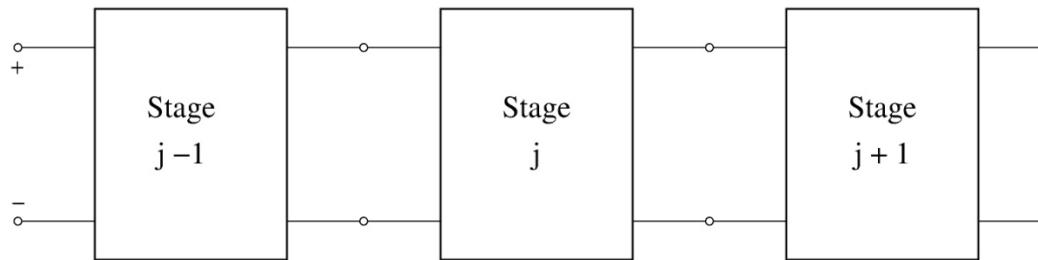
$$v_{o2} = v_{i3}$$

$$\frac{v_o}{v_{i,1}} = \frac{v_{o,1}}{v_{i,1}} \times \frac{v_{o,2}}{v_{i,2}} \times \frac{v_{o,3}}{v_{i,3}} = A_{v1} \times A_{v2} \times A_{v3}$$

$$\frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times A_{v1} \times A_{v2} \times A_{v3} \times \dots$$

But we need to know $R_{L,1}, R_{L,2}, R_{L,3}, \dots$ in order to find A_M 's.

What are R_L and R_{sig} for each stage?



- R_L for each stage is the input resistance of the following stage.
- R_{sig} for each stage is the output resistance of the previous stage.

Procedure for Solving multi-stage Amplifiers

Gain & R_i :

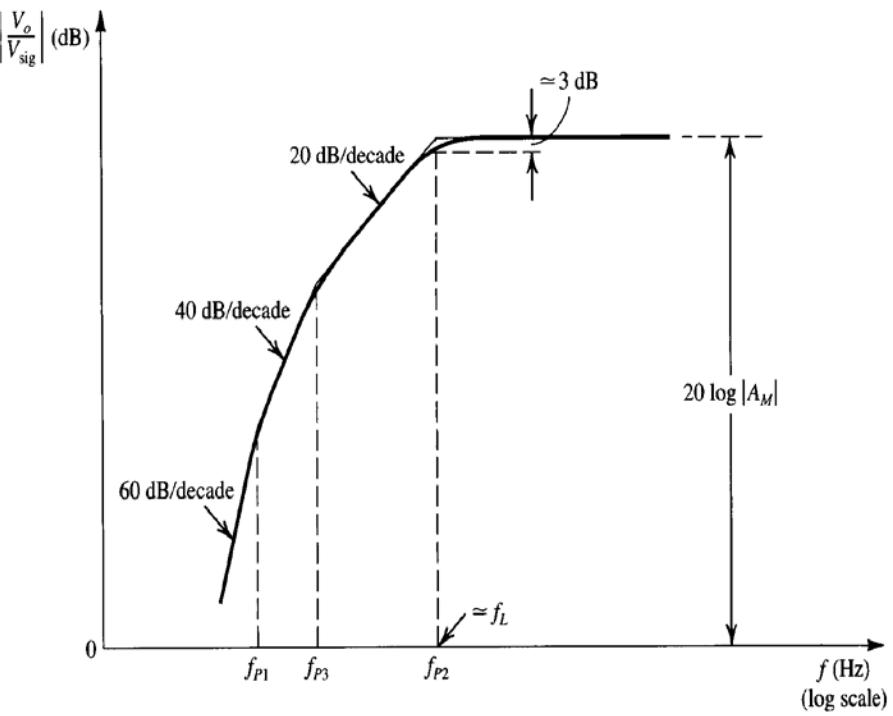
1. Start from the load side (n^{th} stage),
 - Find the gain $A_{v,n} = (v_o/v_i)_n$ and $R_{i,n}$.
2. For $(n-1)^{\text{th}}$ stage, set $R_{L,n-1} = R_{i,n}$
 - Find the gain $A_{v,n-1} = (v_o/v_i)_{n-1}$ and $R_{i,n-1}$.
3. Repeat until reaching to the first stage. Then,

$$R_i = R_{i,1} \quad \frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times A_{v1} \times A_{v2} \times A_{v3} \times \dots$$

R_o :

1. Start from the source side (1^{st} stage). Find $R_{o,1}$.
2. Go to the second stage. Set $R_{sig,2} = R_{o,1}$. Find $R_{o,2}$
3. Continue to the last stage (n^{th} stage). Then, $R_o = R_{o,n}$

Cut-off frequency of a multi-stage amplifier



Similar to a single-stage amplifier, each capacitor introduces a pole:

- 1) Coupling capacitor at the input:

$$f_{p1} = \frac{1}{2\pi(R_i + R_{sig})C_{c1}}$$

- 2) Coupling capacitor at the output:

$$f_{po} = \frac{1}{2\pi(R_o + R_L)C_{co}}$$

- 3) Coupling capacitor between stages $j-1$ and j

$$f_{pj} = \frac{1}{2\pi(R_{i,j} + R_{o,j-1})C_{cj}}$$

- 4) By-pass capacitors for stage j (if exists)

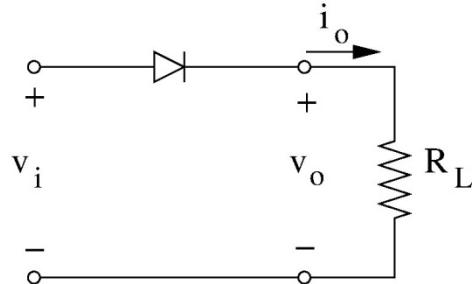
$$f_{p,bypass} = \frac{1}{2\pi R_{by-pass} C_{by-pass}}$$

- 5) Then: $f_p \approx f_{p1} + f_{p2} + \dots$

Diode Functional Circuits

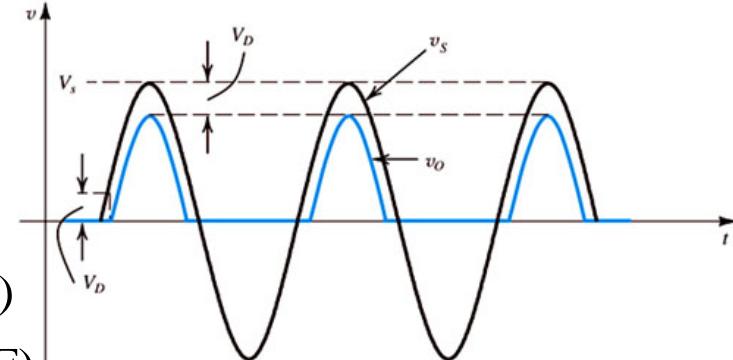
Rectifier & Clipper Circuits

Half-wave rectifier

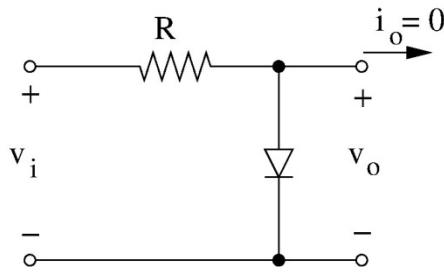


For $v_i \geq V_{D0}$, $v_o = v_i - V_{D0}$ (Diode ON)

For $v_i < V_{D0}$, $v_o = 0$ (Diode OFF)

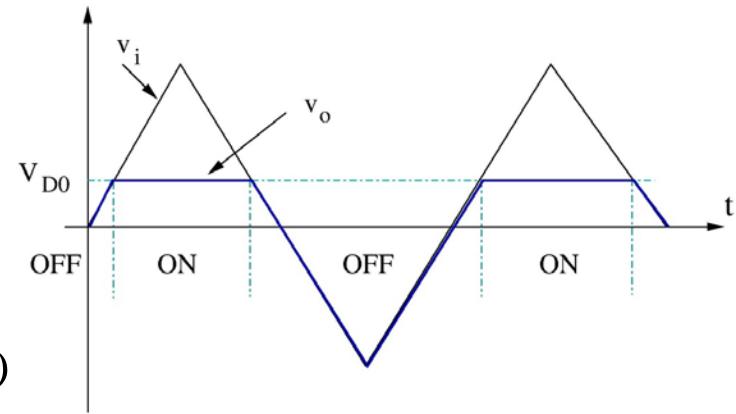


Clipper



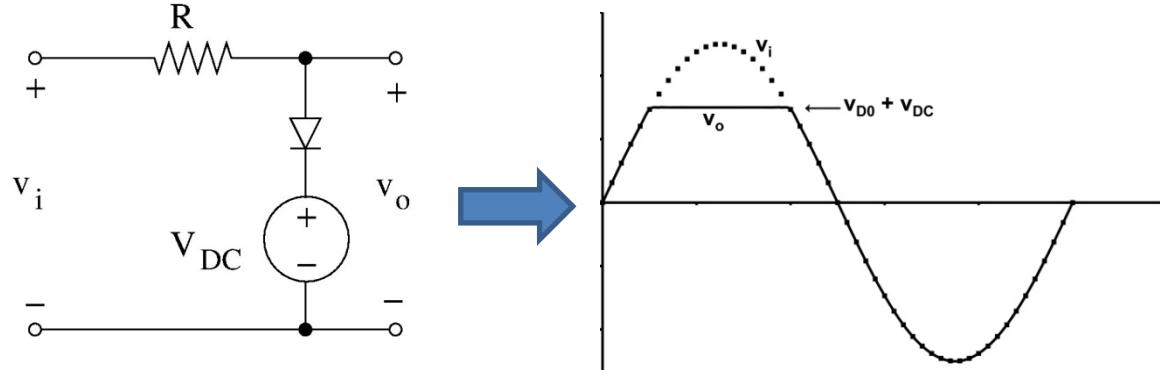
For $v_i \geq V_{D0}$, $v_o = V_{D0}$ (Diode ON)

For $v_i < V_{D0}$, $v_o = v_i$ (Diode OFF)

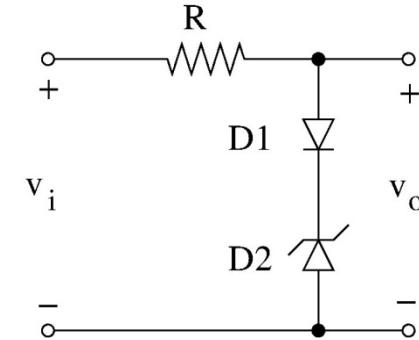


“Clipping” voltage can be adjusted

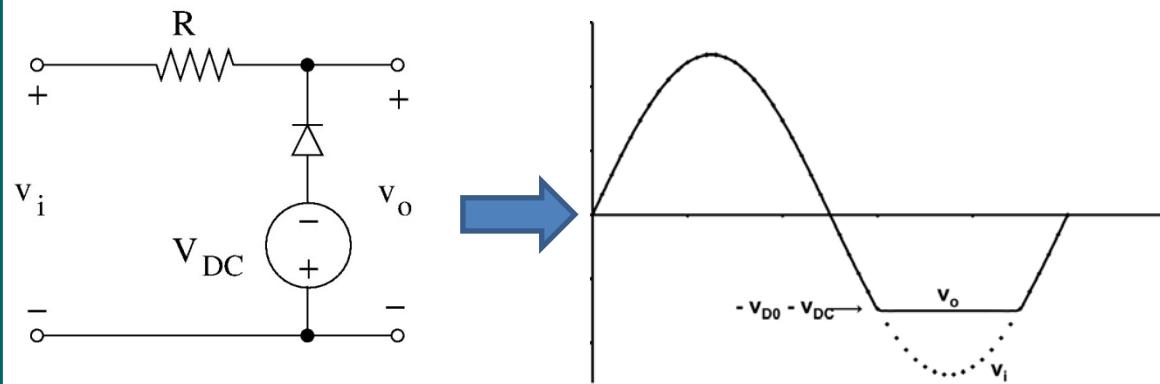
v_o limited to $\leq V_{D0} + V_{DC}$



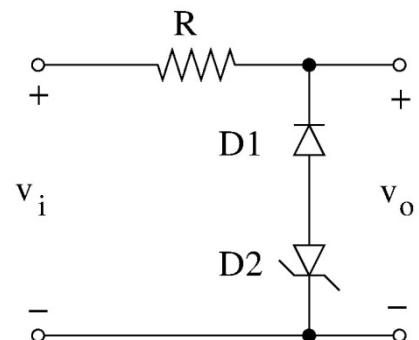
v_o limited to $\leq V_{D0} + V_Z$



v_o limited to $\geq -V_{D0} - V_{DC}$

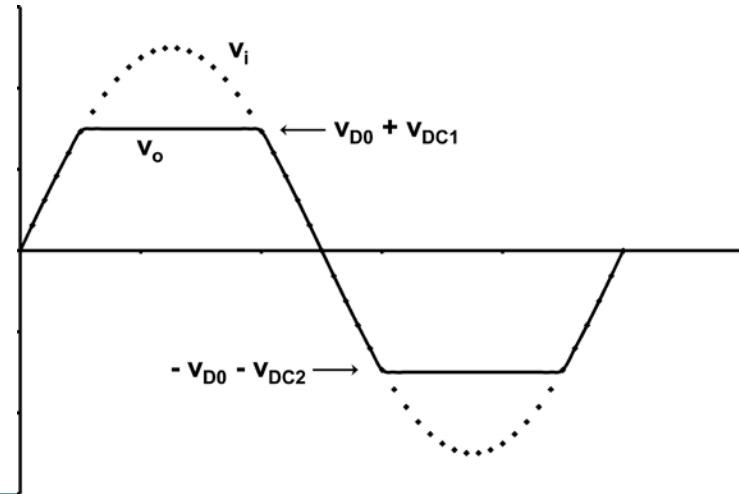
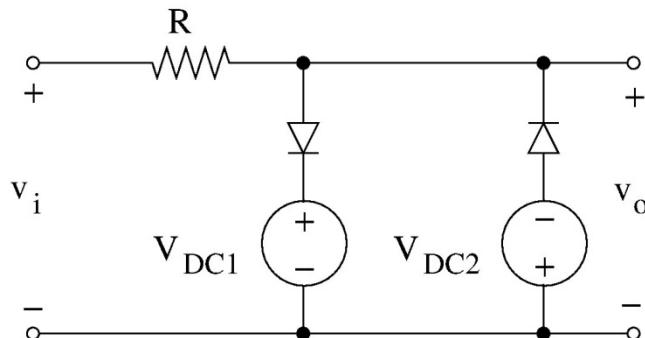


v_o limited $\geq -V_{D0} - V_Z$

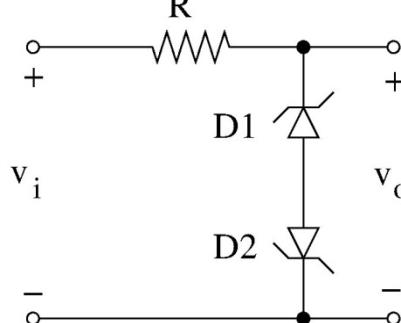


Both top & bottom portions of the signal can be clipped simultaneously

v_o limited to $\leq V_{D0} + V_{DC1}$ and $\geq -V_{D0} - V_{DC2}$

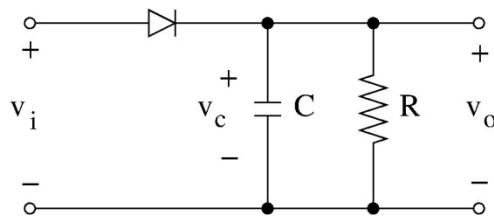


v_o limited to $\leq V_{D0} + V_{Z1}$
and $\geq -V_{D0} - V_{Z2}$

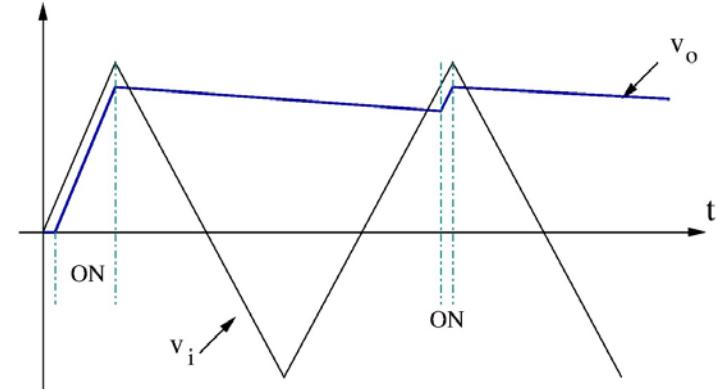


Peak Detector & Clamp Circuits

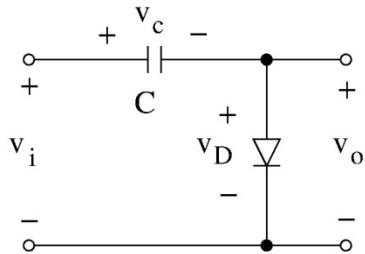
Peak Detector Circuit



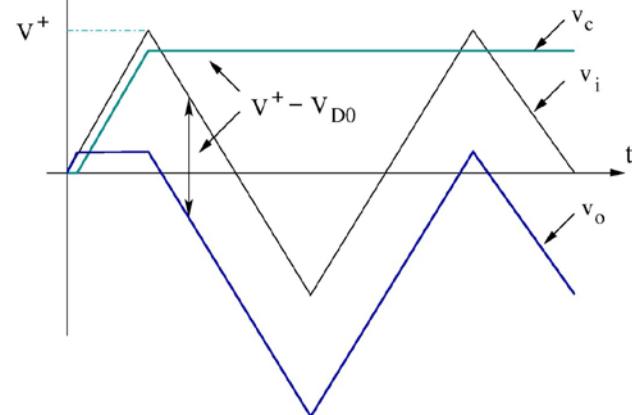
- “ideal” peak detector: $\tau/T \rightarrow \infty$
- “Good” peak detector: $\tau/T \gg 1$



Clamp Circuit

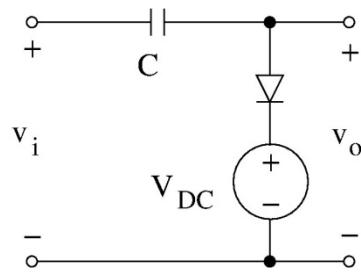


v_o is equal to v_i but shifted
“downward” by $-(V^+ - V_{D0})$

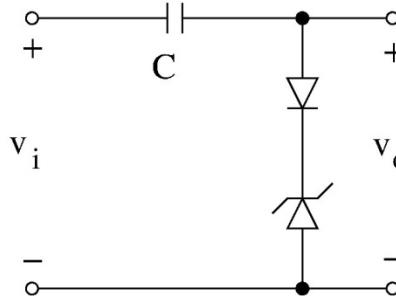


Voltage shift in a clamp circuit can be adjusted!

v_o shifted “downward”

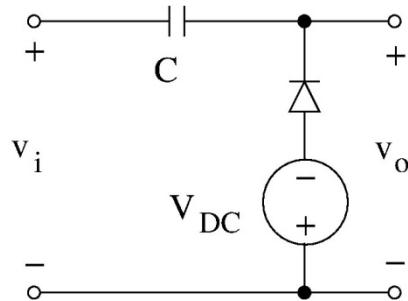


$$v_o = v_i - (V^+ - V_{DC} - V_{D0})$$

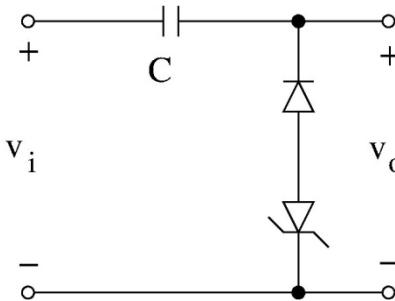


$$v_o = v_i - (V^+ - V_Z - V_{D0})$$

v_o shifted “upward”

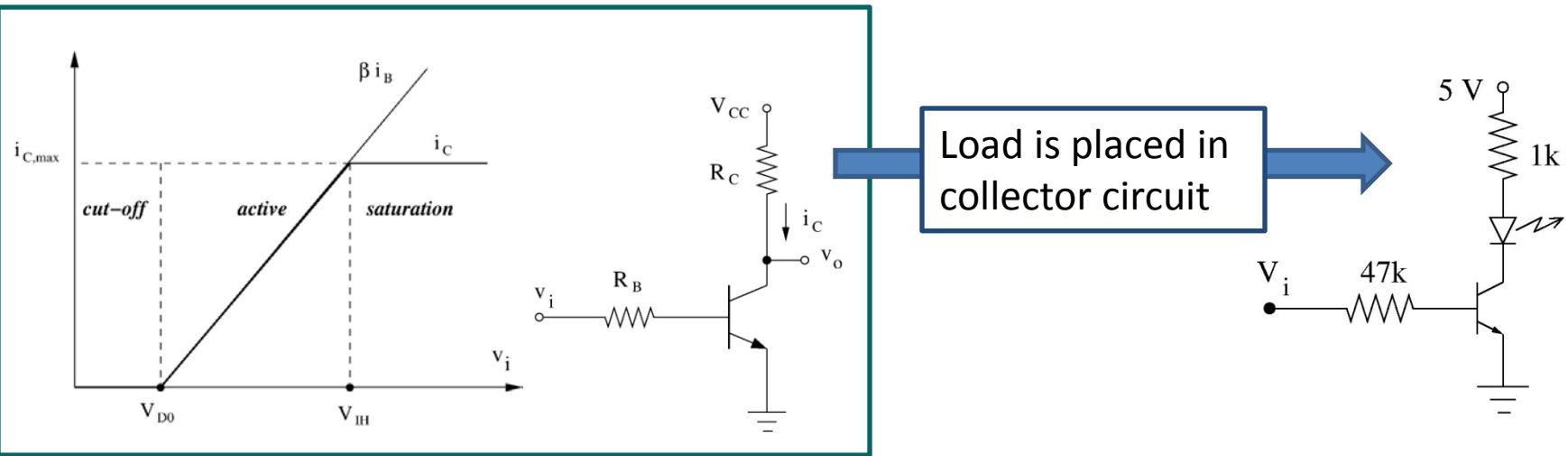


$$v_o = v_i + (V^- - V_{DC} - V_{D0})$$



$$v_o = v_i + (V^- - V_Z - V_{D0})$$

BJT as a switch



- Use: Logic gate can turn loads ON (BJT in saturation) or OFF (BJT in cut-off)
- i_c is uniquely set by CE circuit (as $v_{ce} = V_{sat}$)
- R_B is chosen such that BJT is in deep saturation with a wide margin (e.g., $i_B = 0.2 i_c / \beta$)

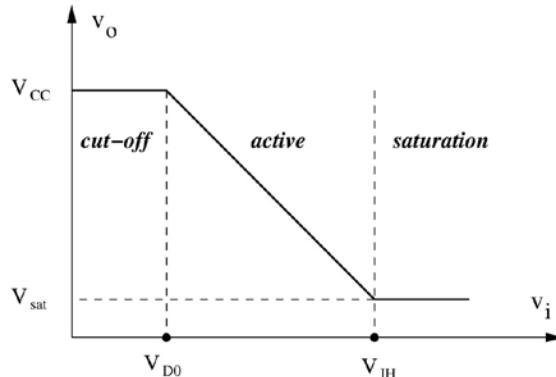
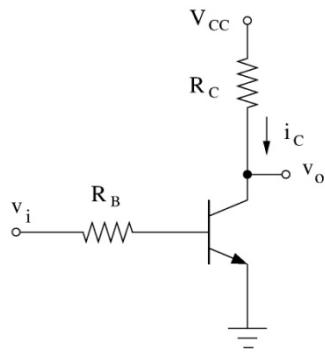
*Lab 4 circuit

Solved in Lecture notes (problems 12 & 13)

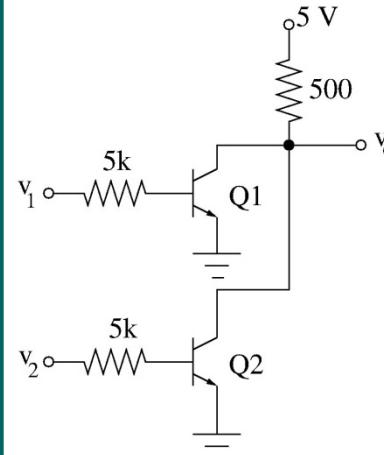
BJT as a Digital Gate

Resistor-Transistor logic (RTL)

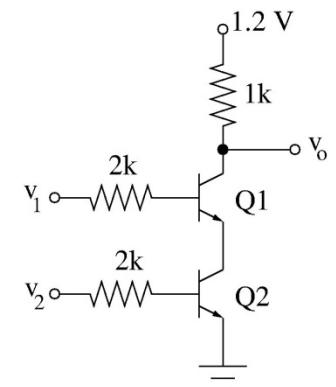
RTL NOT gate ($V_L = V_{sat}$, $V_H = V_{CC}$)



RTL NOR gate*



RTL NAND gate*

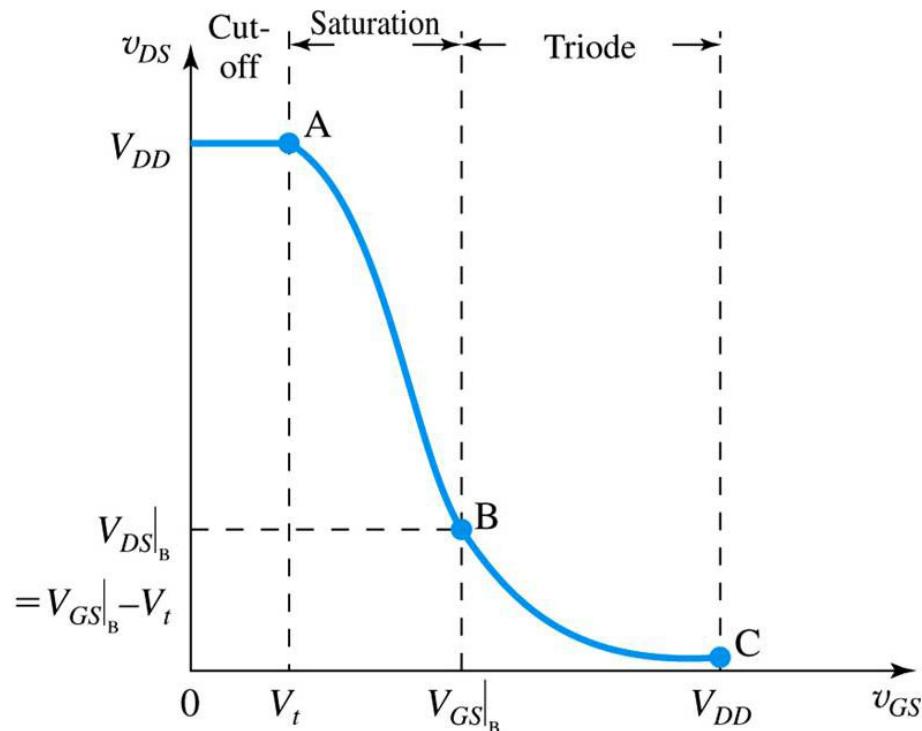


- Other variants: Diode-transistor logic (DTL) and transistor-transistor logic (TTL)
- BJT logic gates are not used anymore except for high-speed emitter-coupled logic circuits because of
 - Low speed (switching to saturation is quite slow).
 - Large space and power requirements on ICs

*Solved in Lecture notes (problems 14 & 15)

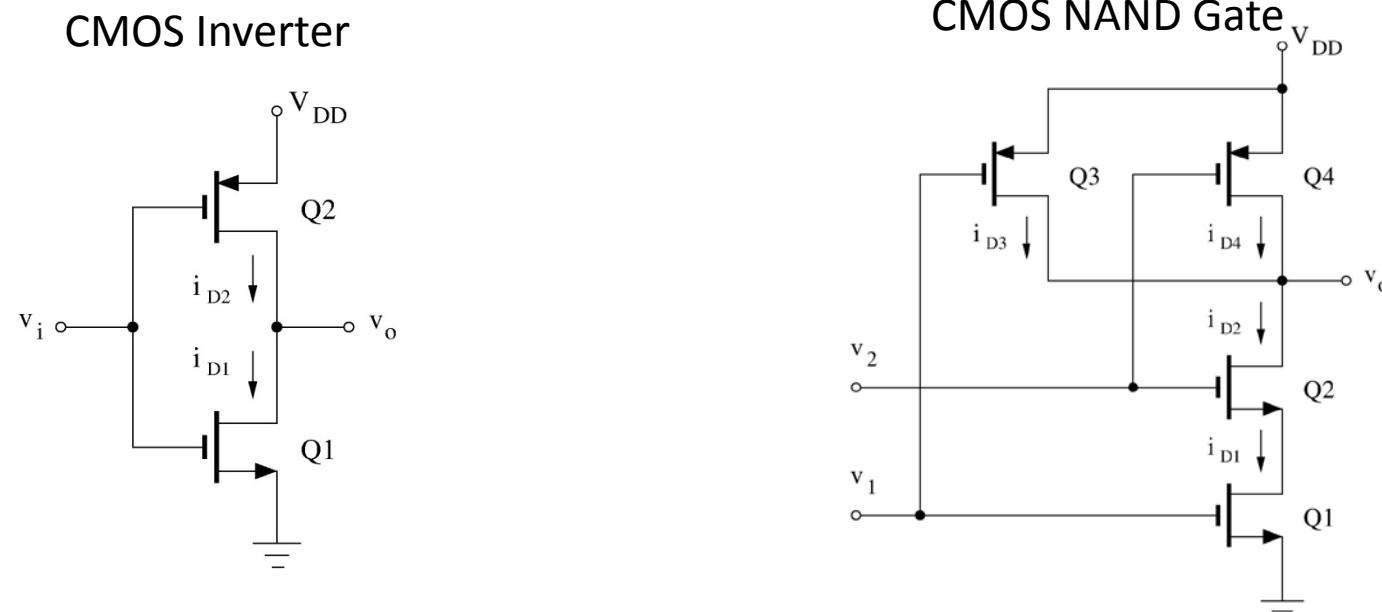
NMOS Functional circuits

- Similar to a BJTs in the active mode, NMOS behaves rather “linearly” in the saturation region (we discuss NMOS amplifiers later)
- Transition from cut-off to triode can be used to build NMOS switch circuits.
 - Voltage at point C (see graph) depends on NMOS parameters and the circuit (in BJT $v_o = V_{sat}$)!
- We can also built NMOS logic gate similar to a RTL. But there is are much better gates based on CMOS technology!



Complementary MOS (CMOS) is based on NMOS/PMOS pairs

- Maximum signal swing: Low State: 0, High State: V_{DD}
 - Independent of MOS device parameters!
- Zero “static” power dissipation ($i_D = 0$ in each state).
 - It uses the fact that if a MOS is ON and $i_D = 0$ only if MOS is in triode and $v_{DS} = 0$



How to Solve Problems

1. What is Known?
(comes from problem description.)



3. How to get there?
(use recipes!)

2. What is the aim?
(Identify circuit parameters that has to be calculated.)

- First, write down all equations that govern the circuit.
- Make sure that you have enough equations to solve for the unknowns.
- Make sure that you the solution will give you the answer to the problem.
- Only then, start solving the equations.