İTÜ Computer Engineering Department
April 9, 2015

Due: April 15, 2015, 23:00

Computer Architecture 3rd Homework

The instruction cycle of a CPU is divided into the five phases given below.

1. **Fetch Instruction**: 50ns,
2. **Decode Instruction**: 20ns,
3. **Fetch Operand**: 50ns,
4. **Execute**: 30ns,
5. **Interrupt Preparation** (*if necessary*): 150ns.

The CPU accesses the memory during the instruction and operand fetching phases, but not in the decoding and execution phases. The interrupt preparation phase is entered only in case of an interrupt request, and the preparation procedure (*saving the return address, fetching the vector address etc.*) takes a total of 150ns.

The size of the data bus is 8 bits. Memory and I/O interfaces both take 40ns to access.

The CPU will execute a program with 20 instructions. There is also a direct memory access controller (DMAC) in the system. The DMAC is conditioned to transfer 32 bytes of data from an I/O interface to the memory.

Consider we started the time as the CPU started to execute the program (T=0) and the DMAC sent a data transfer request while the CPU was fetching the first instruction (T=5ns).

1) Suppose that the controller transfers data from I/O interfaces to the memory using the **cycle stealing** method. The DMAC makes the transfer **implicitly**—the data do not pass through the DMAC itself. According to this method:

   a. When (T=?) does the DMAC finish transferring the first byte? Why?
   b. When (T=?) does the CPU finish executing the first instruction? Why?
   c. When (T=?) does the DMAC finish transferring all 32 bytes?
   d. When (T=?) does the CPU finish executing all 20 instructions?

2) Suppose that **interrupts** are used rather than the DMA method to transfer data from I/O interfaces to the memory. The corresponding interrupt service routine transfers 8 bytes of data each time it is run. This interrupt service routine has a runtime of 800ns. According to this method:

   a. When (T=?) does the DMAC finish transferring all 32 bytes?
   b. When (T=?) does the CPU finish executing all 20 instructions?