

Digital Electronic Circuits

Homework #3

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(... due April, 9th, 2009, THURSDAY)

For the problem below,

- $V_{DD}=3.3V$.
- The model parameters for the MOSFETs are,
 $\mu_n=385\text{cm}^2V^{-1}s^{-1}$, $\mu_p=130\text{cm}^2V^{-1}s^{-1}$
 $V_{T0n}=0.52V$, $V_{T0p}=-0.65V$
 $t_{ox}=7.5\text{nm}$, $\epsilon_0=8.85\times 10^{-14}\text{F/cm}$, $\epsilon_{ox,r}=3.9$
(body effect can be neglected)
- Allowed minimum device aspects are $W_{min}=0.3\mu\text{m}$, and $L_{min}=0.3\mu\text{m}$.
- Try to minimize the consumed area, while satisfying the desired performance.

Find the logic function corresponding to the **last digit of your student number** below.

$$\begin{aligned} Z_0 &= [(A+B+C)(D+E)F] ' & Z_1 &= [AB+(C+D)+EF] ' & Z_2 &= [(A+B)(C+D+EF)] ' \\ Z_3 &= [(A+BC)DE+F] ' & Z_4 &= [ABC(DE+F)] ' & Z_5 &= [(AB+C)(D+E)F] ' \\ Z_6 &= [(A+BCD)(E+F)] ' & Z_7 &= [AB+C(D+EF)] ' & Z_8 &= [A(BC+DE+F)] ' \\ & & Z_9 &= [A+BC+DEF] ' \end{aligned}$$

a) Sketch the **CMOS** complex gate realizing **your** logic function.

b) Determine the aspects W_p , W_n , L_p and L_n for the MOSFETs, if τ_{PLH} and τ_{PHL} are both aimed to be less than **0.25ns**, for an equivalent load capacitance of $C_L=0.25\text{pF}$.

Note#1: Assume that C_L remains constant (is not affected further by the device dimensions).

Note#2: All nMOSTs will have the same W_n/L_n . All nMOSTs will have the same aspect ratios W_p/L_p

c) Calculate V_{th} of the **CMOS** gate for the device aspects obtained in (b).

d) Re-determine the aspects W_p , W_n , L_p and L_n for the MOSFETs such that $V_{th}=1/2V_{DD}$. Then, calculate the worst-case values for τ_{PLH} and τ_{PHL} , for $C_L=0.25\text{pF}$.