Dr DC Hendry

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Outline I

Pass Transistor Circuits

2 The CMOS Transmission Gate

3 Design Example

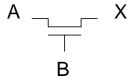
4 Transmission Gate Design Methodology

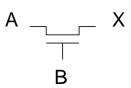
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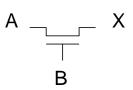
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- When used as a pass transistor the device may conduct current in either direction.

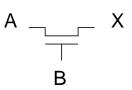




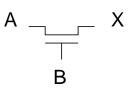
Α	В	Х
0	0	Z
		•



Α	В	X
0	0	Z
0	1	0



Α	В	Χ
0	0	Ζ
0	1	0
1	0	Z



Z
١ ۾
0
Z
1

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- This reduction in output voltage makes cascading of pass transistor circuits difficult.



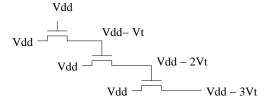


Figure: Cascaded pass transistors

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- So such circuits are normally confined to the internal circuitry of a gate.
- Full logic levels can be regenerated with an inverter at the output of the gate.

Two-to-One Mux

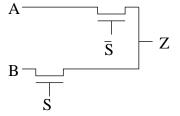


Figure: Two-to-one Mux

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- Note that the connection made is bidirectional

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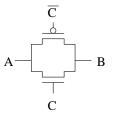


Figure: CMOS Transmission Gate Circuit

When C=1, A and B are connected, both logic zero and logic one



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• The most commonly used symbol is simply:

$$A \longrightarrow B$$

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$$f = AS_2\overline{S_1} + B\overline{S_2}.\overline{S_1} + \overline{S_2}S_1$$

This may be rewritten as (the reason will become clear later):

$$f = AS_2\overline{S_1} + B\overline{S_2}.\overline{S_1} + 1.\overline{S_2}S_1 + 0.S_2S_1$$



Transmission Gate Implementation:

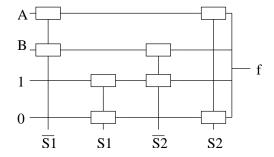


Figure: Implementation with Transmission Gates

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- Each transmission gate may now be replaced with two transistors.
- Where lines connect only to logic 1 the nMOS devices may be omitted.
- Where lines connect only to logic 0 the pMOS devices may be omitted.
- nMOS and pMOS devices may be grouped to minimise the number of wells required.



Transistor Schematic

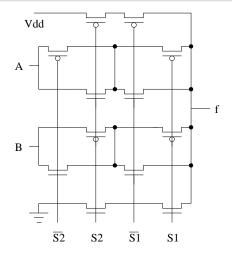


Figure: Transistor Level Schematic for Design

Design Methodology

A suitable design methodology, in addition to the correct logic output, must ensure:

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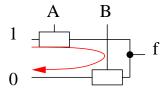
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- The output is always driven to logic 1 or logic 0.
- There are no "sneak" paths, such as:



Viable Approaches

Viable design approaches are:

 Choose a number of inputs as mux select inputs and proceed as above.

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- Plot variables on K-maps.
- Tabular methods such as modifications of Quine-McCluskey not covered here.

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$$f = \bar{a}\bar{b} + b\bar{c}\bar{d} + acd$$

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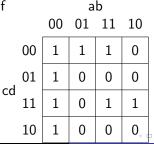
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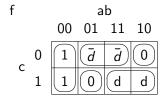


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Giving the Boolean expression for f as:

$$f = 1.\bar{a}\bar{b} + b\bar{c}\bar{d} + ac.d + a\bar{b}\bar{c}.0 + \bar{a}bc.0$$