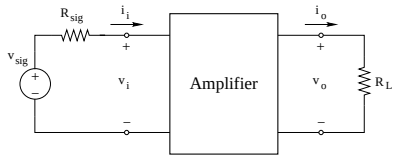
VI. Transistor Amplifiers

6.1 Introduction

In this section we will use the transistor small-signal model to analyze and design transistor amplifiers. There are two issues that we need to discuss first: 1) What are the important properties of an amplifier? and 2) How can we add a signal to the bias in a real circuit?

6.1.1 Amplifier Parameters



In Section 1, we showed that the response of a two-port network is completely determined if we solve the simple circuit shown. This solution is uniquely summarized by three parameters:

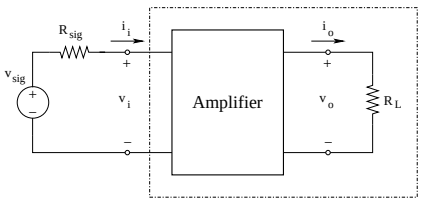
1) The ratio of v_o/v_i which is called the voltage transfer function of the circuit. For voltage amplifiers, $v_o/v_i = const$ and is called the amplifier voltage gain (or gain for short):

$$\text{Voltage Gain:} \qquad A_v = \frac{v_o}{v_i}$$

In general A_v depends on the load, R_L. A special case is the "open-loop" gain in which $R_L \to \infty$ (called open-loop gain as $i_o = 0$):

$$\text{Open-loop Gain:} \qquad A_{vo} = \frac{v_{oc}}{v_i} = \frac{v_o}{v_i}\bigg|_{R_L \to \infty}$$

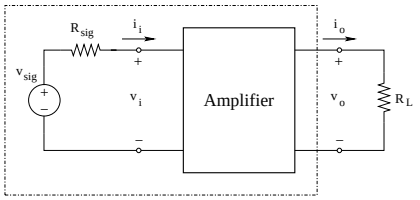
2) As the combination of the two-port network (amplifier) and the load is a two-terminal network, it can be modeled by its Thevenin equivalent. Furthermore, as this combination does not contain an independent source, it reduces to a resistor, called the input resistance:



$$\text{Input Resistance:} \qquad R_i = \frac{v_i}{i_i}$$

In general R_i depends on the load, R_L.

3) The combination of the amplifier and the input (v_{sig} and R_{sig}) is also a two-terminal network and can be modeled by its Thevenin equivalent. We denote the Thevenin resistance of this combination as R_o.



In order to calculate R_o we need to set the independent voltage source $v_{sig} = 0$ and compute the equivalent resistance seen between the output terminals, *i.e.,*

$$\text{Output Resistance:} \qquad R_o = -\left.\frac{v_o}{i_o}\right|_{v_{sig}=0} \qquad \text{(Thevenin Resistance)}$$

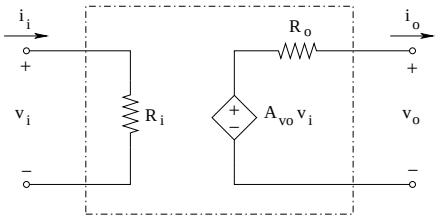
In general R_o depends on R_{sig}.

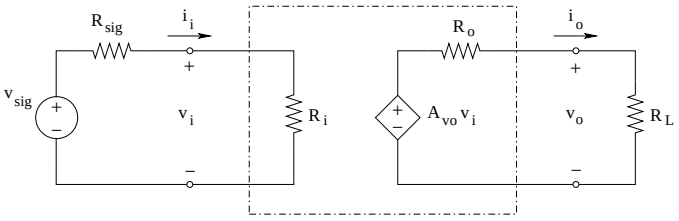
The Thevenin voltage source of the amplifier/input combination, V_T, is the open-circuit voltage, v_{oc}, and is related to the open-loop gain of the amplifier:

$$V_T = v_{oc} = v_o|_{R_L \to \infty} = A_{vo} v_i$$

Therefore, the load "sees" a Thevenin equivalent circuit with $V_T = A_{vo} v_i$ and $R_T = R_o$.

Combining models of the input and output ports, we arrive at a model for an amplifier which consists of three circuit elements as is shown below (left).





The amplifier circuit model allows us to solve any amplifier configuration if we know values of A_{vo}, R_i and R_o (similar to using Thevenin Theorem to "label" any two-terminal network with R_T and V_T). For example, we can find the overall voltage gain of the amplifier, v_o/v_{sig}, as (see figure above right):

$$\frac{v_o}{v_i} = \frac{R_L}{R_o + R_L} A_{vo} \qquad \frac{v_i}{v_{sig}} = \frac{R_i}{R_i + R_{sig}}$$

$$\frac{v_o}{v_{sig}} = \frac{v_i}{v_{sig}} \times \frac{v_o}{v_i} = \frac{R_i}{R_i + R_{sig}} \times A_v = \frac{R_i}{R_i + R_{sig}} \times A_{vo} \times \frac{R_L}{R_o + R_L}$$

We see that the open-loop gain A_{vo} is the maximum value for the amplifier gain A_v. In addition, to maximize v_o/v_{sig}, we need $R_i \to \infty$ and $R_o \to 0$. A good voltage amplifier, thus, is designed to have a "large" R_i and a "small" R_o (*i.e.,* $R_i \gg R_{sig}$ and $R_o \ll R_L$). A voltage-controlled voltage source is an ideal voltage amplifier as $R_i \to \infty$ and $R_o = 0$.

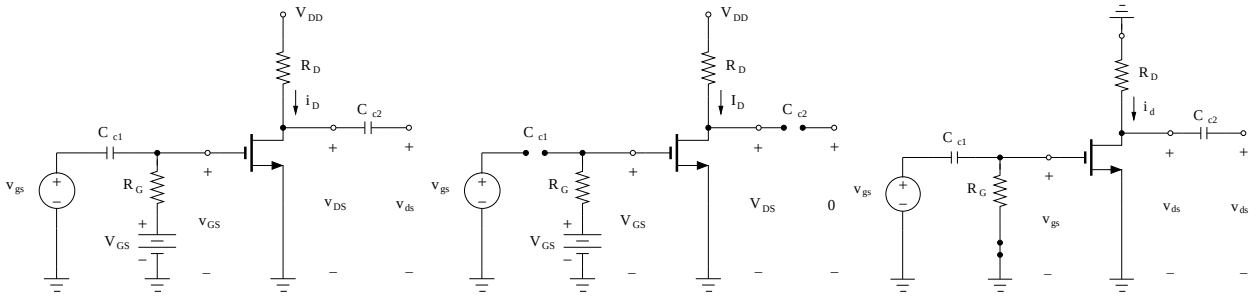
We will use this amplifier model later to find parameters of multi-stage amplifiers (Sec. 6.4)

6.1.2 Capacitor Coupling

As discussed before, a constant bias voltage should be added to the signal to ensure that the MOS is always in saturation or the BJT is in active. There are two ways to accomplish this task.

1) "Direct Coupling:" For a multi-stage amplifier, the biasing scheme can be set up such that the bias voltage of each stage matches the bias voltage of the following stage. Usually, bias with two voltage supplies is used such that for the first amplifier stage, $V_G = 0$ for MOS (or $V_B = 0$ for BJT). Integrated circuit chips use direct coupling scheme in order to avoid using capacitors which take a lot of space on the chip. Because of the need to match bias voltages between stages, biasing becomes a difficult design problem.

2) "Capacitive coupling:" Since a capacitor becomes an open circuit for bias (DC voltages & currents), it can be used to couple the signal to the circuit as is shown below for a MOS amplifier.



Real Circuit Bias Circuit Signal Circuit

The circuit to the left above shows a practical implementation of this scheme. For bias (middle circuit above), capacitors will be open circuit and, thus, the bias voltages and currents remain confined to the transistor and do not propagate to the signal or the load sides. In the signal circuit (right circuit above), if the signal is an AC signal, capacitors would act as impedances and allow the signal to enter and exist the transistor amplifier.

Impedance of a capacitor, $|Z_C| = 1/(\omega C)$, depends on the frequency. As a result v_o/v_i will also depend on frequency and, in general, the amplifier would not behave linearly for an arbitrary signal (which includes many frequencies). However, at high enough frequencies, the impedance of a capacitor becomes very small and the capacitor effectively becomes a sort circuit. For frequencies higher than this value, v_o/v_i will be independent of frequency and the linear behavior of the amplifier is recovered. The frequency at which we can ignore the impedances of the coupling capacitors is called the lower cut-off frequency of the amplifier.

In order to ensure a linear behavior for an amplifier, it is always operated above its cut-off frequency where the coupling capacitors can be ignored (*i.e.,* can be approximated as short

circuit). As such, amplifier properties (gain, R_i & R_o) are calculated assuming coupling capacitors are short. Calculation of the lower cut-off frequency is discussed in Section 6.3. You will see in ECE 102 that the gain of a transistor amplifier also drops at high frequencies and there is an upper cut-off frequency. As such, the range of frequencies that an amplifier will behave linearly is called the "mid-band."

As the capacitive coupling scheme confines bias voltages in each stage, biasing is simpler with this method. On other hand, DC signals cannot be amplified.

6.1.3 Analysis of Transistor Amplifier Circuits

Analysis of a transistor amplifier circuit follows three steps as we need to address several issues: bias, linear response (to small signals), and the impact of coupling capacitors.

Bias:
1) Zero out the signal and replace capacitors with open circuits. Compute transistor bias point parameters.
2) Compute g_m and r_o (and r_π for BJT) from bias point parameters.

Mid-band Small Signal Response:
1) Draw the signal circuit (*e.g.,* ground bias voltage sources, open bias current sources).
2) Assume capacitors are short circuit.
3) Inspect the circuit and simplify. If you identify the circuit as a prototype circuit, you can directly use the formulas for that circuit. Otherwise, replace the transistor with its small signal model and solve for A_v, R_i and R_o .

Frequency-response: Coupling and bypass capacitors introduce poles at low frequencies. In Section 6.3, we will introduce a method to estimate the lower cut-off frequency of an amplifier. ECE102 includes a more thorough review of the amplifier frequency response.

There are many practical implementation for single-transistor amplifiers due to a variety of biasing possibilities. However, the signal circuit for a signal-transistor amplifier generally reduces to one of four "fundamental amplifier configurations" (4 for BJT and 4 for MOS). As discussed in the class (see lecture slides), solution of these fundamental configurations can be used to find the gain of any transistor amplifier. You will see in ECE102 that the input and output resistances can be found using "elementary R forms." These formulas allows one to compute properties of any amplifier readily and are used extensively in ECE102.

Since we are only focusing on discrete and simple amplifier configurations in this course, amplifier parameters are computed directly from the circuit in the following sections in order to provide more examples of solving signal circuits with transistor small-signal models.

Notes:

1) Small-signal models of PNP and NPN transistors (or PMOS and NMOS transistors) are similar. Thus, the formulas derived below can be used for either case.

2) The small-signal model of a BJT is similar to that of a MOS with the exception of the additional resistor r_π (the input terminals in a MOS is open circuit). As such, we expect that formulas for MOS amplifiers would be the same as those of BJT amplifiers if we set $r_\pi \to \infty$.

3) For MOS circuits, we can use the common approximation $g_m r_o \gg 1$ as

$$g_m = \frac{2I_D}{V_{OV}}, \qquad r_o \approx \frac{V_A}{I_D} \quad \to \quad g_m r_o = \frac{2V_A}{V_{OV}} \gg 1$$

typically $g_m r_o$ is 50 or more.

4) For BJT circuits, we can also use the common approximation $g_m r_o \gg 1$ as

$$g_m = \frac{I_C}{V_T}, \qquad r_o = \frac{V_A + V_{CE}}{I_C} \approx \frac{V_A}{I_C} \quad \to \quad g_m r_o = \frac{V_A}{V_T} \gg 1$$

typically $g_m r_o$ is several thousands. In addition, $g_m r_\pi = \beta \gg 1$

5) In many text books (*e.g.,* Sedra & Smith), the formulas for BJT amplifiers are given in terms of β & r_e (instead of g_m & r_π) where

$$r_e = \frac{1}{g_m} = \frac{r_\pi}{\beta}$$

with r_e typically in 10s or 100 Ω range. Here we keep the g_m form so we that can see the comparison to MOS amplifiers.

6) Some manufacturer spec sheet for BJTs (*e.g.,* spec sheet for 3N3904) use the older notation (hybrid π model) for BJT which are $h_{fe} \equiv \beta$, $h_{re} \equiv r_\pi$, and $h_{oe} \equiv 1/r_o$

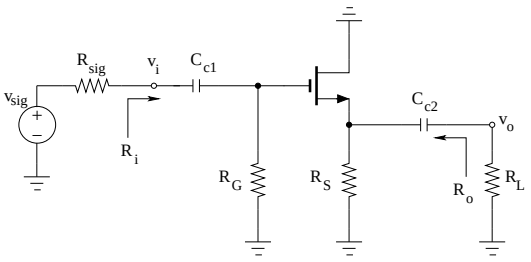
6.2 Discrete Single-transistor Amplifiers

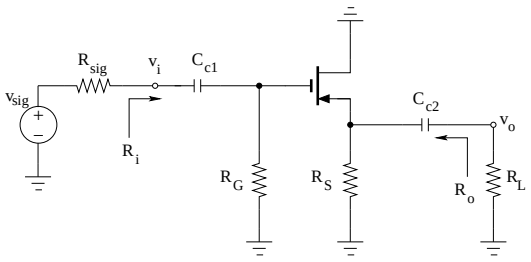
In this section, we will compute the amplifier properties of four discrete single-transistor amplifiers. Solution is done for the "most general" version of the signal circuit. As we will see in the problem section, formulas developed here can then be used to find the amplifier parameters for a variety of circuits.

6.2.1 Common-Drain and Common-Collector Amplifiers

Common-Drain or Source Follower Configuration

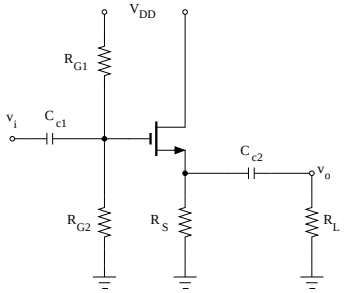
Circuits shown below are the generic signal circuits of a common-drain amplifier (*i.e.,* we have "zeroed" out all bias sources). The circuit to the left is the NMOS version and the circuit to the right is the PMOS version. Because NMOS and PMOS small-signal models are identical, both circuits will give the same signal response. As such, from now on we will only show the signal circuits for NMOS transistors.



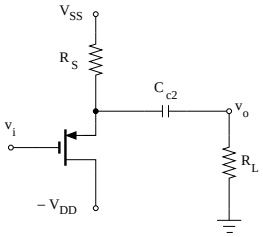


In this circuit, the input signal is applied at the gate and the output is taken at the source. As the drain is grounded (for signal), it is the common terminal of input and output. Thus, this circuit is called the common-drain amplifier.

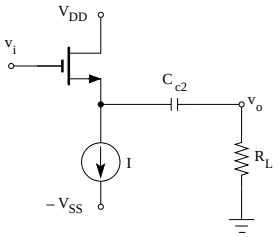
It is important to realize that as a transistor can be biased in many ways, several "complete" circuits (*i.e.,* including bias elements) will reduce to the above "signal" circuit form of a common-drain amplifier. Some examples are given below (v_{sig} and R_{sig} in the input are not shown for simplicity).



$R_G = R_{G1} \parallel R_{G2}$



$R_G \to \infty$,
$C_{c1} \to \infty$,

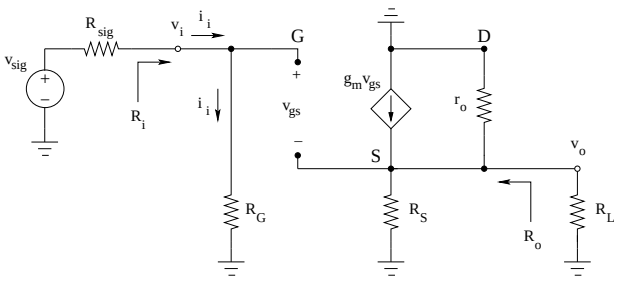


$R_G \to \infty$, $R_S \to \infty$,
$C_{c1} \to \infty$,

Exercise: Draw the signal circuit of the above three circuits and show that they reduce to the generic discrete common-drain amplifier circuit above.

We now proceed with the signal analysis by replacing the MOS with its small-signal model.

Using node-voltage method (there is one node, v_o):



$$v_{gs} = v_i - v_o$$

Node v_o $\quad \dfrac{v_o}{R_S} + \dfrac{v_o}{r_o} + \dfrac{v_o}{R_L} - g_m v_{gs} = 0$

$$\frac{v_o}{r_o \parallel R_S \parallel R_L} - g_m(v_i - v_o) = 0$$

$$\frac{v_o}{v_i} = \frac{g_m(r_o \parallel R_S \parallel R_L)}{1 + g_m(r_o \parallel R_S \parallel R_L)}$$

As can be seen, the gain of this amplifier is less than but close to 1. Because $v_s = v_o \approx v_i$, *i.e.,* signal voltage at the MOS source terminal follows the input signal v_i, this configuration is also called the Source Follower.

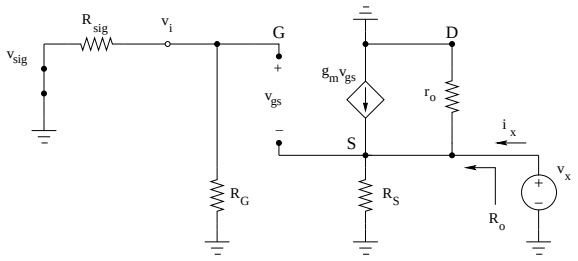
Finding R_i is easy as current i_i flows in R_G and $v_i = R_G\, i_i$ (see circuit). Therefore, $R_i = v_i/i_i = R_G$. Note that if R_G were not present (see middle and left circuits on the example complete circuits of the previous page). $R_i \to \infty$.

To find R_o we need to zero out v_{sig} and compute the Thevenin Equivalent resistance seen at the output terminals. Because of the presence of the controlled source, we need to attach a v_x voltage source to the circuit and compute i_x to get $R_o = v_x/i_x$.

We see from the circuit that $v_g = 0$ and $v_{gs} = -v_x$. Thus:

$$i_x = \frac{v_x}{r_o} + \frac{v_x}{R_S} - g_m v_{gs} = \frac{v_x}{r_o} + \frac{v_x}{R_S} + \frac{v_x}{1/g_m}$$

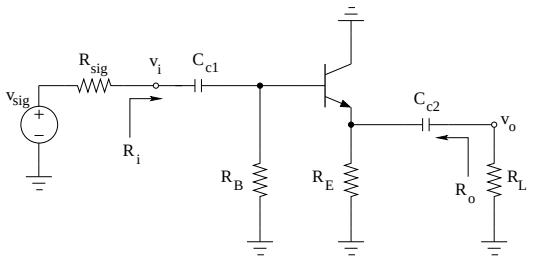
$$R_o = \frac{v_x}{i_x} = \frac{1}{g_m} \parallel R_S \parallel r_o \approx \frac{1}{g_m} \parallel R_S$$

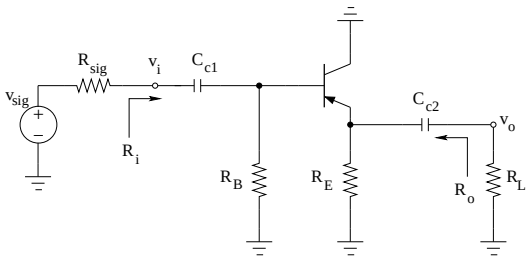


In summary, the general properties of the common-drain amplifier (source follower) include a voltage gain ≤ 1, a large input resistance (which can be made infinite in some biasing schemes) and a small output resistance. This type of circuit is called a "buffer" and is often used when there is a mismatch between input resistance of one stage and the output resistance of the previous stage (see Sec. 6.4). Additionally, $i_L = i_o \gg i_i$ as $v_o/v_i \approx 1$ while $R_i \gg R_o$. As such, this circuit can be used to amplify the signal current (and power) and drive a load (used typically as the last stage of an amplifier circuit).

Common-Collector or Emitter Follower Configuration

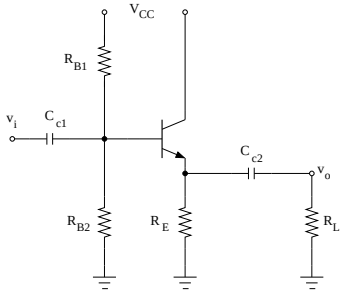
Circuits shown are the generic signal circuits of a common-collector amplifier (*i.e.,* we have "zeroed" out all bias sources). The circuit to the left is the NPN version and the circuit to the right is the PNP version. Because NPN and PNP BJT small-signal models are identical, both circuits will give the same signal response. As such, from now on we will only show the signal circuits for NPN BJT transistors.



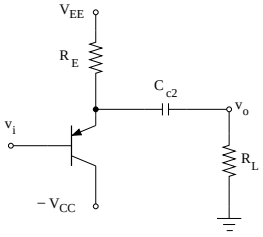


In this circuit, the input is applied at the base and the output is taken at the emitter. As the collector is grounded (for signal), it is the common terminal of input and output. Thus, this circuit is called the common-collector amplifier.

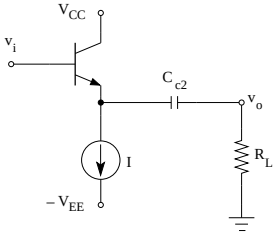
As can be seen this configuration is analogous to the MOS common-drain amplifier. Similarly to the MOS case, the BJT can be biased in many ways. Several "complete" circuits (*i.e.,* including the bias elements) will reduce to the above "signal" form of a common-collector amplifier. Some examples are given below.



$R_B = R_{B1} \parallel R_{B2}$



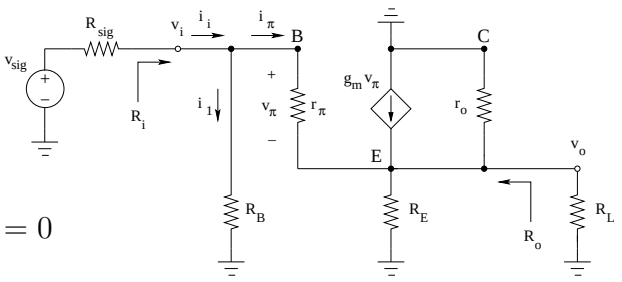
$R_B \to \infty$,
$C_{c1} \to \infty$,



$R_B \to \infty$, $R_E \to \infty$,
$C_{c1} \to \infty$,

We now proceed with the signal analysis by replacing the BJT with its small-signal model.

Using node-voltage method (there is one node, v_o):



$$v_\pi = v_i - v_o$$

$$\text{Node } v_o \qquad \frac{v_o}{R_E} + \frac{v_o}{r_o} + \frac{v_o}{R_L} + \frac{v_o - v_i}{r_\pi} - g_m v_\pi = 0$$

The last two terms in the above equation can be simplified by noting $1/r_\pi = g_m/\beta$:

$$\frac{v_o - v_i}{r_\pi} - g_m v_\pi = (v_o - v_i) \times \frac{g_m}{\beta} + g_m(v_o - v_i) = g_m(v_o - v_i)\frac{\beta + 1}{\beta} \approx g_m(v_o - v_i)$$

Substituting back in the node equation, we get:

$$\frac{v_o}{R_E} + \frac{v_o}{r_o} + \frac{v_o}{R_L} + g_m(v_o - v_i) = 0$$

$$\frac{v_o}{r_o \parallel R_E \parallel R_L} + g_m(v_o - v_i) = 0$$

$$\frac{v_o}{v_i} = \frac{g_m(r_o \parallel R_E \parallel R_L)}{1 + g_m(r_o \parallel R_E \parallel R_L)}$$

The gain of the common collector amplifier is less than 1, but usually very close to 1 because of the large BJT g_m. This configuration is also called the Emitter Follower.

To find $R_i = v_i/i_i$, we note that by KCL $i_i = i_1 + i_\pi$ and

$$i_\pi = \frac{v_i - v_o}{r_\pi} = \frac{v_i}{r_\pi} \times \left(1 - \frac{v_o}{v_i}\right)$$

$$1 - \frac{v_o}{v_i} = 1 - \frac{g_m(r_o \parallel R_E \parallel R_L)}{1 + g_m(r_o \parallel R_E \parallel R_L)} = \frac{1}{1 + g_m(r_o \parallel R_E \parallel R_L)}$$

$$i_\pi = \frac{v_i}{r_\pi + g_m r_\pi (r_o \parallel R_E \parallel R_L)}$$

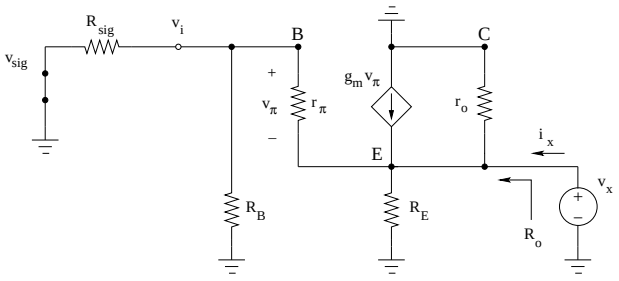
$$i_i = i_1 + i_\pi = \frac{v_i}{R_B} + \frac{v_i}{r_\pi + \beta(r_o \parallel R_E \parallel R_L)} = \frac{v_i}{R_B \parallel [r_\pi + \beta(r_o \parallel R_E \parallel R_L)]}$$

$$R_i = R_B \parallel [r_\pi + \beta(r_o \parallel R_E \parallel R_L)]$$

Note that when emitter degeneration biasing is used, we need to have $R_B \ll (1 + \beta)R_E$. In this case, $R_i \approx R_B$ (similar to the common-drain amplifier in which $R_i = R_G$). If R_B is not present, the input resistance would be very large (MΩ level).

To find R_o we need to zero out v_{sig} and compute the Thevenin Equivalent resistance seen at the output terminals.

We attach a voltage source v_x to the circuit and compute i_x to get $R_o = v_x/i_x$.



$$i_x = \frac{v_x}{r_o} + \frac{v_x}{R_E} - g_m v_\pi + \frac{v_x}{r_\pi + R_B \parallel R_{sig}}$$

v_π can be found by the voltage divider formula (below). Substituting the expression for v_π in the above expression for i_x, the last two terms of the i_x can be simplified as:

$$v_\pi = -v_x \times \frac{r_\pi}{r_\pi + R_B \parallel R_{sig}}$$

$$i_x = \frac{v_x}{r_o} + \frac{v_x}{R_E} + \frac{g_m r_\pi v_x}{r_\pi + R_B \parallel R_{sig}} + \frac{v_x}{r_\pi + R_B \parallel R_{sig}}$$

$$i_x = \frac{v_x}{r_o} + \frac{v_x}{R_E} + \frac{(\beta+1) v_x}{r_\pi + R_B \parallel R_{sig}}$$

$$i_x = \frac{v_x}{r_o \parallel R_E \parallel (r_\pi + R_B \parallel R_{sig})/(1+\beta)}$$

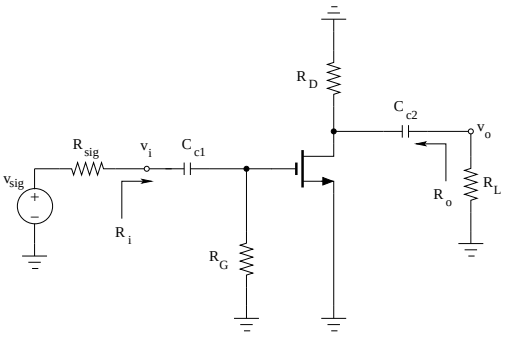
$$R_o = R_E \parallel r_o \parallel \frac{r_\pi + R_B \parallel R_{sig}}{(1+\beta)}$$

In summary, the general properties of the common-collector amplifier (emitter follower) include a voltage gain close to unity, a large input resistance and a small output resistance (similar to the common-drain amplifier). Thus, emitter follower is also used as a buffer or for amplifying the signal current (and power) and drive a load.

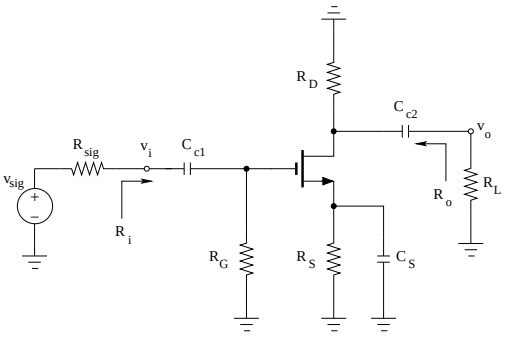
6.2.2 Common-Source and Common-Emitter Amplifiers

Common-Source Configuration

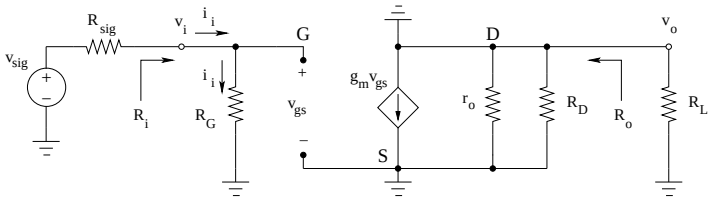
Circuit shown is the generic signal circuit of a common-source amplifier (*i.e.,* we have "zeroed" out all bias sources). In this circuit input signal is applied at the gate and the output is taken at the drain. As the source is grounded (for the signal), it is the common terminal of input and output. Thus, this circuit is called the common-source amplifier.



If source degeneration biasing is used for the common-source configuration, a resistor R_S should be present. A "by-pass" capacitor is typically used so that the signal by-passes R_S, effectively making the source grounded for the signal as is shown. For bias, this capacitor is open and R_S provides source degeneration.



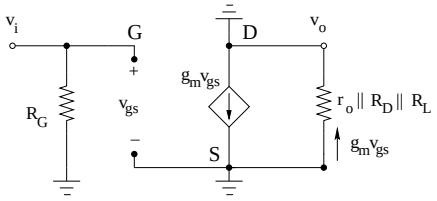
We replace the MOS with its small-signal model.



Inspecting the circuit, we find $R_i = v_i/i_i = R_G$.

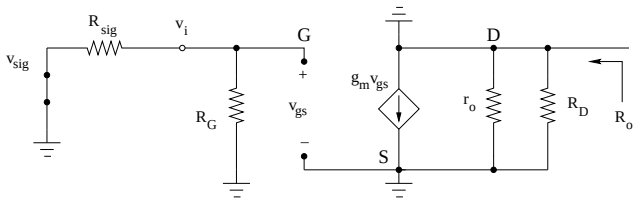
To find the gain, we note that $v_i = v_{gs}$. Furthermore, r_o, R_D, and R_L are in parallel and by KCL a current of $g_m v_{gs}$ flows in $r_o \parallel R_D \parallel R_L$ (from the ground to v_o) as is shown. Then:

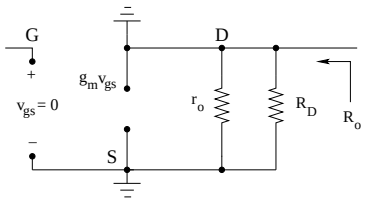
Ohm Law:
$$v_o = -g_m v_{gs}(r_o \parallel R_D \parallel R_L)$$
$$\frac{v_o}{v_i} = -g_m(r_o \parallel R_D \parallel R_L)$$



The negative sign in the gain formula is indicative of a 180° phase shift in the output signal.

To find R_o we need to zero out v_{sig} and compute the Thevenin Equivalent resistance seen at the output terminals (circuit below left). Examination of the circuit shows that $v_{gs} = v_i = 0$. Thus, the controlled source $g_m v_{gs}$ becomes an open circuit (circuit below right) and the output resistance can be found by inspection to be $R_o = R_D \parallel r_o$.

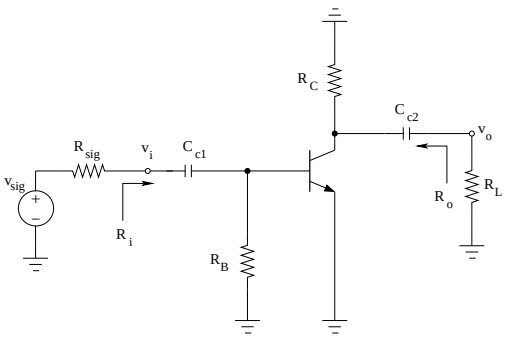




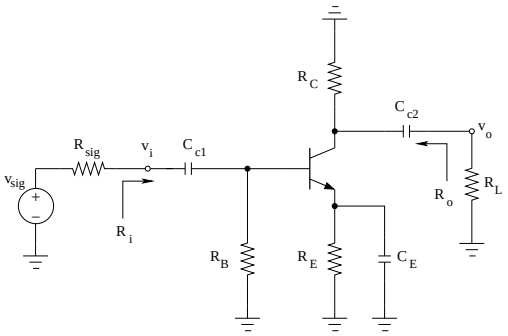
In summary, the general properties of the common-source amplifier include a large voltage gain, a large input resistance (and can be made infinite with some biasing schemes) but a medium output resistance.

Common-Emitter Configuration

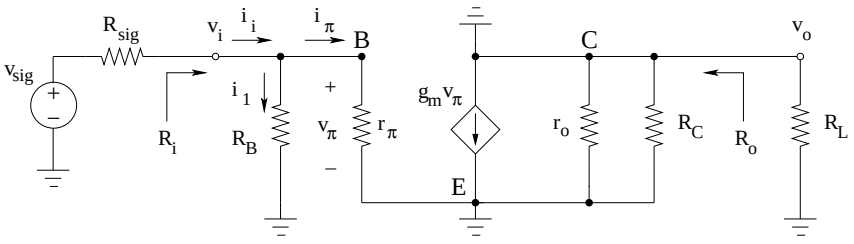
Circuit shown is the generic signal circuit of a common-emitter amplifier (*i.e.,* we have "zeroed" out all bias sources). In this circuit the input signal is applied at the base and the output is taken at the collector. As the emitter is grounded (for the signal), it is the common terminal of input and output. Thus, this circuit is called the common-emitter amplifier.



If emitter degeneration biasing is used for this configuration, a resistor R_E should be present. Similar to the MOS common-source amplifier, a "bypass" capacitor is typically used so that the signal by-passes R_E, effectively making the emitter grounded for the signal as is shown.



We replace the BJT with its small-signal model.

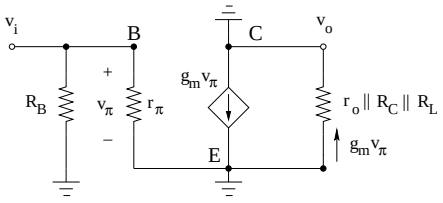


Inspecting the circuit, we find $R_i = v_i/i_i = R_B \parallel r_\pi$.

To find the gain, we note that $v_i = v_\pi$. Furthermore, r_o, R_C, and R_L are in parallel and by KCL a current of $g_m v_\pi$ flows in $r_o \parallel R_C \parallel R_L$ (from the ground to v_o) as is shown. Then:

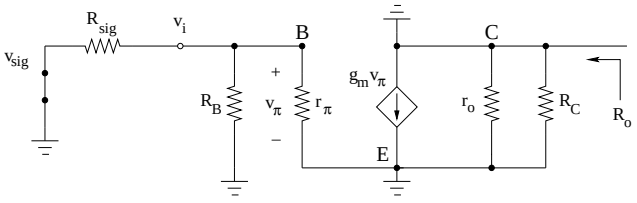
Ohm Law: $\quad v_o = -g_m v_\pi (r_o \parallel R_C \parallel R_L)$

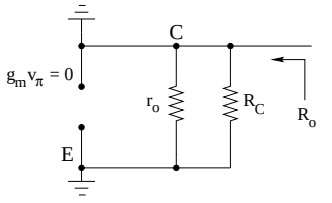
$$\frac{v_o}{v_i} = -g_m (r_o \parallel R_C \parallel R_L)$$



The negative sign in the gain is indicative of a 180° phase shift in the output signal.

To find R_o we need to zero out v_{sig} and compute the Thevenin Equivalent resistance seen at the output terminals (circuit below left). Examination of the circuit show that $v_\pi = v_i = 0$. Thus, the controlled source $g_m v_\pi$ becomes an open circuit (circuit below right) and the output resistance can be found by inspection to be $R_o = R_C \parallel r_o$.



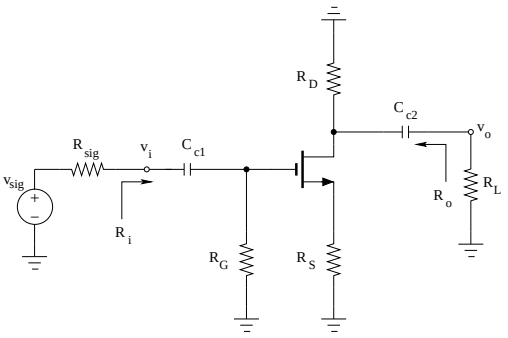


In summary, the general properties of the common-emitter amplifier include a large voltage gain, a "medium" input resistance and a "medium" output resistance.

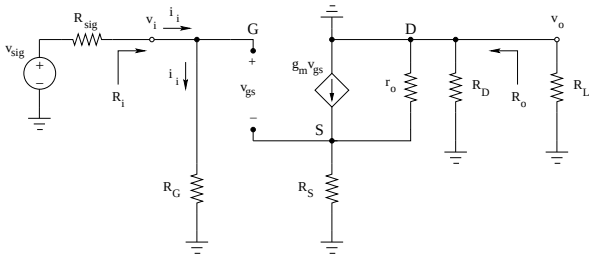
6.2.3 Common-Source and Common-Emitter Amplifiers with Degeneration

Common-Source Configuration with a Source Resistor

This circuit is the generic signal circuit of a common-source amplifier with degeneration (*i.e.,* with a source resistor). In this circuit the input signal is applied at the gate and the output is taken at the drain similar to a common-emitter amplifier.



We replace the MOS with its small-signal model.



Using node-voltage method (there are two nodes, v_o and v_s):

$$\text{Node } v_s: \quad \frac{v_s}{R_S} + \frac{v_s - v_o}{r_o} - g_m v_{gs} = 0$$

$$\text{Node } v_o: \quad \frac{v_o}{R_D \parallel R_L} + \frac{v_o - v_s}{r_o} + g_m v_{gs} = 0$$

$$\frac{v_s}{R_S} + \frac{v_o}{R_D \parallel R_L} = 0$$

where the last equation is found by summing the first two. Substituting for $v_{gs} = v_i - v_s$ in the first equation and computing v_s we get:

$$\frac{v_s}{R_S} + \frac{v_s - v_o}{r_o} - g_m(v_i - v_s) = 0$$

$$\frac{v_s}{R_S} + \frac{v_s}{r_o} - \frac{v_o}{r_o} - g_m v_i + g_m v_s = 0$$

$$v_s \times \frac{r_o + R_S + g_m r_o R_S}{R_S r_o} - \frac{v_o}{r_o} - g_m v_i = 0$$

$$[r_o + R_S(1 + g_m r_o)] \times \frac{v_s}{R_S} - v_o - g_m r_o v_i = 0$$

Substituting for v_s/R_S in terms of v_o from our node equations above, we get:

$$-[r_o + R_S(1 + g_m r_o)] \times \frac{v_o}{R_D \parallel R_L} - v_o - g_m r_o v_i = 0$$

$$\frac{v_o}{v_i} = -\frac{g_m r_o (R_D \parallel R_L)}{R_D \parallel R_L + r_o + R_S(1 + r_o g_m)}$$

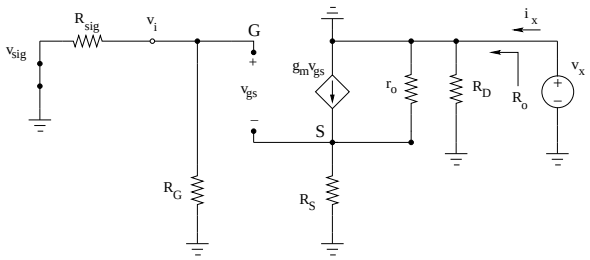
The gain equation can be simplified by dropping 1 compared to $g_m r_o$ in the denominator:

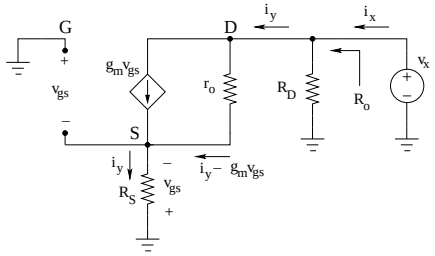
$$\frac{v_o}{v_i} \approx -\frac{g_m r_o (R_D \parallel R_L)}{R_D \parallel R_L + r_o + g_m r_o R_S} = -\frac{g_m (R_D \parallel R_L)}{1 + g_m R_S + (R_D \parallel R_L)/r_o}$$

Compared to a CS amplifier with no R_S, the amplifier gain is substantially reduced with the presence of R_S. However, the gain has become much less sensitive to changes in g_m.

Inspecting the circuit we find $R_i = v_i/i_i = R_G$, similar to a common-source amplifier.

To find R_o, we set $v_{sig} = 0$ and compute the Thevenin Equivalent resistance seen at the output terminals. We attach v_x voltage source to the circuit and compute i_x (circuit below left). Examination of the circuit shows that $v_g = v_i = 0$ (gate is grounded). As such v_{gs} is the voltage across resistor R_S (see circuit below right).





In circuits like this in which a resistor is directly attached between the terminals of v_x (R_D in this case), it is easier to compute the current i_y first:

By KCL, a current of $i_y - g_m v_{gs}$ should flow in r_o and i_y should flow in R_S. Since $v_{gs} = -R_S i_y$:

$$\text{KVL}: \quad v_x = r_o(i_y - g_m v_{gs}) + R_S i_y$$

$$v_x = r_o(i_y + g_m R_S i_y) + R_S i_y = i_y(r_o + g_m r_o R_S + R_S)$$

$$\frac{v_x}{i_y} = r_o + R_S + g_m r_o R_S = r_o + R_S(1 + g_m r_o) \approx r_o + g_m r_o R_S = r_o(1 + g_m R_S)$$

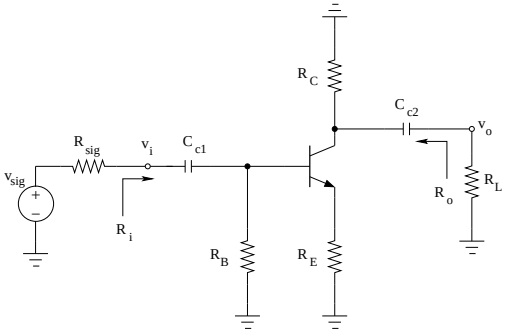
$$\text{KCL}: \quad i_x = \frac{v_x}{R_D} + \frac{v_x}{i_y} = \frac{v_x}{R_D} + \frac{v_x}{r_o(1 + g_m R_S)}$$

$$R_o = \frac{v_x}{i_x} = R_D \parallel [r_o(1 + g_m R_S)]$$

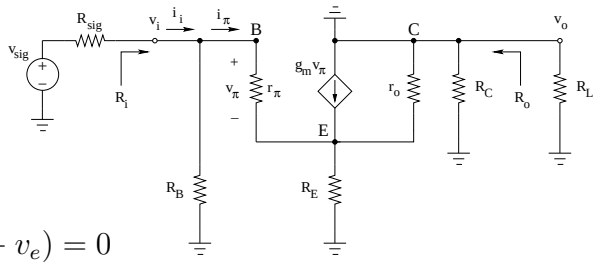
In summary, source degeneration has led to an amplifier with a lower gain which is less sensitive to transistor parameters.

Common-Emitter Configuration with an Emitter Resistor

Circuit shown is the generic signal circuit of a common-emitter amplifier with degeneration (*i.e.,* with a emitter resistor). Note that the input is applied at the base and the output is taken at the collector similar to a common-emitter amplifier.



We replace the BJT with its small-signal model.



Using node-voltage method (there are two nodes, v_o and v_e) and substituting for $v_\pi = v_i - v_e$, we get:

$$\text{Node } v_e: \quad \frac{v_e}{R_E} + \frac{v_e - v_i}{r_\pi} + \frac{v_e - v_o}{r_o} - g_m(v_i - v_e) = 0$$

$$\text{Node } v_o: \quad \frac{v_o}{R_C \parallel R_L} + \frac{v_o - v_e}{r_o} + g_m(v_i - v_e) = 0$$

Adding the two node equations gives:

$$\frac{v_e}{R_E} + \frac{v_o}{R_C \parallel R_L} + \frac{v_e - v_i}{r_\pi} = 0 \quad \rightarrow \quad \frac{v_e}{R_E \parallel r_\pi} = -\frac{v_o}{R_C \parallel R_L} + \frac{v_i}{r_\pi}$$

We now substitute for v_e in Node v_o equation. Noting that $1/r_o \ll g_m$:

$$\frac{v_o}{R_C \parallel R_L} + \frac{v_o}{r_o} - v_e\left[\frac{1}{r_o} + g_m\right] + g_m v_i \approx \frac{v_o}{R_C \parallel R_L} + \frac{v_o}{r_o} - g_m v_e + g_m v_i = 0$$

$$\frac{v_o}{R_C \parallel R_L} + \frac{v_o}{r_o} - g_m(R_E \parallel r_\pi)\left[-\frac{v_o}{R_C \parallel R_L} + \frac{v_i}{r_\pi}\right] + g_m v_i = 0$$

The above equation can be solved to find the gain as:

$$\frac{v_o}{v_i} = -\frac{g_m(R_C \parallel R_L)}{1 + (g_m + 1/r_\pi)R_E + (1 + R_E/r_\pi)(R_C \parallel R_L)/r_o}$$

$$\frac{v_o}{v_i} \approx -\frac{g_m(R_C \parallel R_L)}{1 + g_m R_E + (1 + R_E/r_\pi)(R_C \parallel R_L)/r_o}$$

Where we used $g_m \gg g_m/\beta = 1/r_\pi$ to simplify the denominator of the gain formula.

For discrete BJT amplifiers, $R_C \ll r_o$ (thus $R_C \parallel R_L \ll r_o$) and the third term in denominator can be ignored. In this case,

$$\frac{v_o}{v_i} \approx -\frac{g_m(R_C \parallel R_L)}{1+g_m R_E} = -\frac{R_C \parallel R_L}{R_E + 1/g_m}$$

which is the expression often used. Note that the amplifier gain is reduced with the presence of R_E but it has become substantially less sensitive to any change in β (only through $1/g_m$ term which is usually $\ll R_E$).

To find R_i, we define $R_1 = v_i/i_\pi$. Then, by KCL:

$$i_i = \frac{v_i}{R_B} + i_\pi = \frac{v_i}{R_B} + \frac{v_i}{R_1} = \frac{v_i}{R_B \parallel R_1}$$
$$R_i = v_i/i_i = R_B \parallel R_1$$

Since $i_\pi = v_\pi/r_\pi$, we calculate v_π in terms of v_i from our node equations. Starting from Node v_o equation:

$$\frac{v_o}{R_C \parallel R_L} + \frac{v_o - v_e}{r_o} + g_m(v_i - v_e) = 0$$
$$\frac{v_o}{R_C \parallel R_L} + \frac{v_o}{r_o} - \frac{v_e}{r_o} - g_m v_e + g_m v_i \approx \frac{v_o}{R_C \parallel R_L} + \frac{v_o}{r_o} - g_m v_e + g_m v_i = 0$$

Where we ignored v_e/r_o term compared to $g_m v_e$ term (because $g_m r_o \gg 1$). Since $v_\pi = v_i - v_e$:

$$g_m v_\pi = g_m(v_i - v_e) = -v_o\left[\frac{1}{R_C \parallel R_L} + \frac{1}{r_o}\right] = g_m v_\pi = v_i \times \left(-\frac{v_o}{v_i}\right) \times \frac{1 + (R_C \parallel R_L)/r_o}{R_C \parallel R_L}$$

Substituting for (v_o/v_i) from the gain equation of the previous page (2nd equation from the bottom, before $\beta \gg 1$ approximation), we get:

$$\frac{v_i}{v_\pi} = \frac{1 + (g_m + 1/r_\pi)R_E + (1 + R_E/r_\pi)(R_C \parallel R_L)/r_o}{1 + (R_C \parallel R_L)/r_o}$$
$$\frac{v_i}{v_\pi} = 1 + \frac{R_E}{r_\pi} + \frac{g_m R_E}{1 + (R_C \parallel R_L)/r_o}$$
$$R_1 = \frac{v_i}{i_\pi} = \frac{1}{r_\pi} \times \frac{v_i}{v_\pi} = R_1 = r_\pi + R_E + \frac{\beta R_E}{1 + (R_C \parallel R_L)/r_o}$$
$$R_i = R_B \parallel \left[r_\pi + R_E + \frac{\beta R_E}{1 + (R_C \parallel R_L)/r_o}\right]$$

For discrete BJT amplifiers, $R_C \ll r_o$ (thus $R_C \parallel R_L \ll r_o$) and $R_i \approx R_B \parallel [r_\pi + \beta R_E]$.

To find R_o, we set $v_{sig} = 0$ and compute the Thevenin Equivalent resistance seen at the output terminals. Because of the presence of the controlled source, we need to attach v_x voltage source to the circuit and compute i_x. Calculation is similar to that of the common-source amplifier with R_S. Calculations are left as an exercise (*Hint:* one should replace R_S in the common-source with R_S case with $R'_E = R_E \parallel (r_\pi + R_B \parallel R_{sig}$ and use $v_\pi = -i_y R'_E r_\pi/(r_\pi + R_B \parallel R_{sig})$. In the limit of $R_B \parallel R_{sig} \ll \beta r_o$ (a very good approximation), the output resistance is given by

$$R_o = R_C \parallel \left[r_o \left(1 + \frac{\beta R_E}{r_\pi + R_E + R_B \parallel R_{sig}} \right) \right]$$

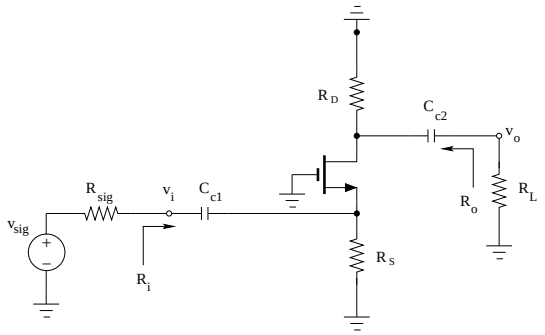
For all practical cases, the resistance in the bracket is very large and $R_o \approx R_C$.

In summary, emitter degeneration has led to an amplifier with a lower gain which is much less sensitive to transistor parameters and a substantially larger input resistance.

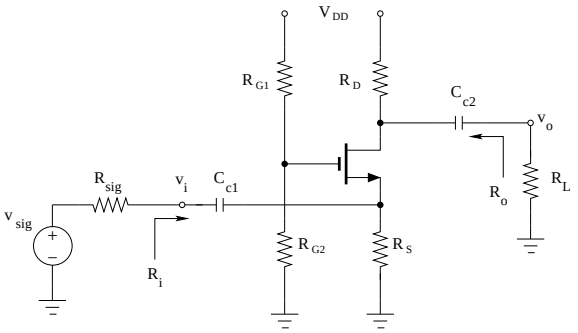
6.2.4 Common-Gate and Common-Base Amplifiers

Common-Gate Configuration

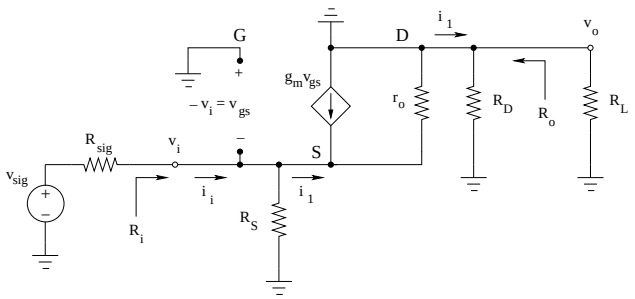
Circuit shown is the generic signal circuit of a common-gate amplifier . Note that the input is applied at the source and the output is taken at the drain. As the gate is grounded (for signal), it is the common terminal of input and output. Thus, this circuit is called the common-gate amplifier.



In some cases, the gate has to biased to a DC value (for example using voltage divider circuit shown). However, since $i_G = 0$, the gate remains grounded for the signal.



We replace the MOS with its small-signal model. Using node-voltage method (there is one node, v_o):



$$v_{gs} = 0 - v_i = -v_i$$

$$\frac{v_o}{R_L} + \frac{v_o}{R_D} + \frac{v_o - v_i}{r_o} + g_m(-v_i) = 0$$

$$\frac{v_o}{r_o \parallel R_D \parallel R_L} = v_i \times \frac{1 + g_m r_o}{r_o}$$

$$\frac{v_o}{r_o \parallel R_D \parallel R_L} \approx v_i \times \frac{g_m r_o}{r_o} \quad \rightarrow \quad \frac{v_o}{v_i} = g_m(r_o \parallel R_D \parallel R_L)$$

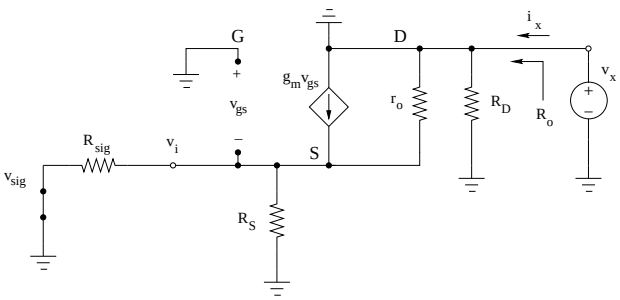
To find R_i, it is easier to compute i_Y first. By KCL at node S, current $i_y + g_m v_{gs}$ will flow in r_o and current i_y will flow in $R_D \parallel R_L$. Thus:

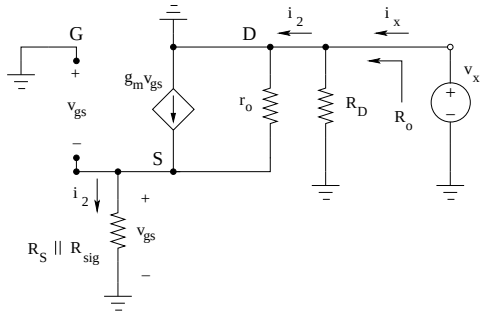
$$v_i = (i_y + g_m v_{gs}) r_o + i_y(R_D \parallel R_L) = v_i = i_y r_o - g_m r_o v_i + i_y(R_D \parallel R_L)$$

$$\frac{v_i}{i_y} = \frac{r_o + (R_D \parallel R_L)}{1 + g_m r_o} \approx \frac{1 + (R_D \parallel R_L)/r_o}{g_m}$$

$$R_i = R_S \parallel \frac{1 + (R_D \parallel R_L)/r_o}{g_m}$$

To find R_o, we set $v_{sig} = 0$ and compute the Thevenin Equivalent resistance seen at the output terminals. Because of the presence of the controlled source, we need to attach v_x voltage source to the circuit and compute i_x.





Similar to previous cases, we start by calculating i_y. By KCL, a current of $i_y - g_m v_{gs}$ should flow in r_o and i_y should flow in $R_S \parallel R_{sig}$. Then, $v_{gs} = -v_s = -(R_S \parallel R_{sig}) i_y$ and

$$\text{KVL}: \quad v_x = r_o(i_y - g_m v_{gs}) + R_S i_y = v_x = r_o i_y + g_m r_o(R_S \parallel R_{sig}) i_y + (R_S \parallel R_{sig}) i_y$$

$$\frac{v_x}{i_y} \approx r_o(1 + g_m(R_S \parallel R_{sig}))$$

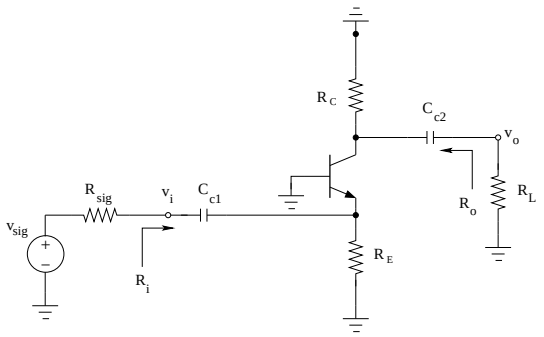
KCL: $$i_x = \frac{v_x}{R_D} + \frac{v_x}{i_y} = \frac{v_x}{R_D} + \frac{v_x}{r_o(1 + g_m(R_S \parallel R_{sig}))}$$

$$R_o = \frac{v_x}{i_X} = R_D \parallel [r_o(1 + g_m(R_S \parallel R_{sig}))]$$

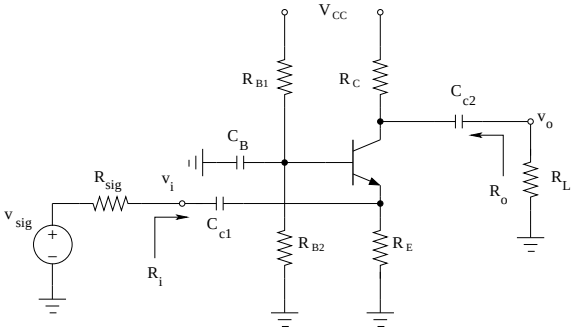
In summary, the general properties of the common-gate amplifier include a large voltage gain, a small input resistance and a medium output resistance (it has the same gain and output resistance values as that of a common-source configuration but has a much lower input resistance).

Common-Base Configuration

Circuit shown is the generic signal circuit of a common-base amplifier . Note that the input is applied at the emitter and the output is taken at the collector. As the base is grounded (for signal), it is the common terminal of input and output. Thus, this circuit is called the common-base amplifier.



In some cases, the base has to biased to a DC value (for example using voltage divider circuit shown). In this case, a bypass capacitor is needed to keep the base grounded for the signal.

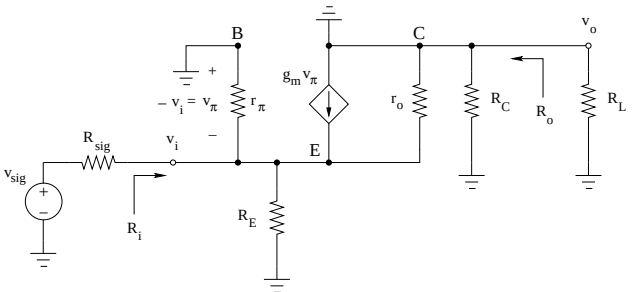


We replace the BJT with its small-signal model. Comparing the small signal circuit of the common base amplifier with that of a common-gate amplifier of the previous page, we see that the two circuits are identical if we replace R_S with $R_E \parallel r_\pi$ (and R_D with R_C). As such we can use the results from the common-gate amplifier analysis to get:

$$\frac{v_o}{v_i} = g_m(r_o \parallel R_C \parallel R_L)$$

$$R_i = R_E \parallel r_\pi \parallel \frac{1 + (R_C \parallel R_L)/r_o}{g_m}$$

$$R_o = R_C \parallel [r_o(1 + g_m(R_E \parallel r_\pi \parallel R_{sig}))]$$



In summary, the common-base configuration has a large open-loop voltage, a small input resistance and a medium output resistance (it has the same gain and output resistance values as that of a common-emitter configuration but a much lower input resistance).

6.2.5 Summary of Amplifier Configurations

- The common-source (CS) and common-emitter (CE) amplifiers have a high gain and are the main configuration in a practical amplifier. Ignoring bias resistors R_G or R_B, the CS configuration has an infinite input resistance while the CE amplifier has a modest input resistance. Both CS and CE amplifier have a rather high output resistance r_o and a limited high-frequency response (you will see this in 102).
- Addition of source or emitter resistor (degenerated CS or CE) leads to several benefits: a gain which is less sensitive to temperature, a much larger input resistance for CE configuration, a better control of amplifier saturation, and a much improved high-frequency response. However, these are realized at the expense of a lower gain.
- The common-gate (CG) and commons-base (CB) amplifiers have a high gain (similar to CS and CE) but a low input resistance. As such, they are only used for specialized applications. CG and CB amplifiers have an excellent high-frequency response. They are typically used in combination with a CS or CE stage (such as cascode amplifiers)
- The source-follower and emitter-follower configurations have a high input resistance, a gain close to unity, and a low output resistance. They are employed as a voltage buffer and/or as the output stage to increase the current and power to the load.

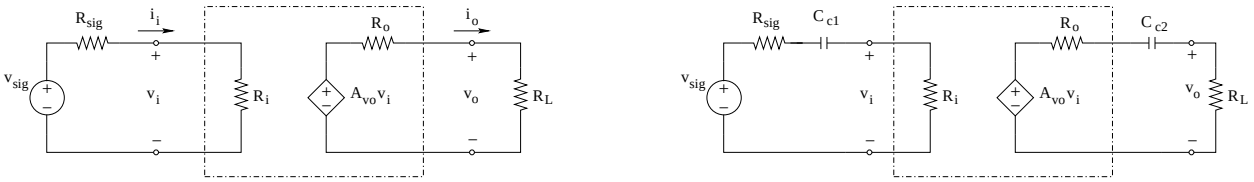
Pages 6-25 and 6-26 include a summary of formulas for discrete transistor amplifiers. These formulas are correct within approximation of $g_m r_o \gg 1$ and $\beta \gg 1$ both of which are always valid. Many of these formulas can be simplified (before plugging in numbers) as they include resistances that are in parallel and "typically" one is much smaller (at least by a factor of ten) than the others. For example, in a common emitter amplifier, we often find that $R_C \ll R_L$ and $R_C \ll r_o$. Then, $r_o \parallel R_C \parallel R_L \approx R_C$ and the gain formula can be simplified to $A_v = -R_C/r_e$.

6.3 Low Frequency Response of Transistor Amplifiers

Up to now, we have assumed that we are operating above a certain frequency such that the coupling and by-pass capacitors would have low impedances (*i.e.,* they were short circuit) leading to a linear amplifier response (*i.e.,* independent of frequency). This frequency is called the lower cut-off frequency of an amplifier – an amplifier should be operated above this frequency.

When we ignored capacitive affects, we found the amplifier parameters, v_o/v_i (or A_{vo}), R_i, and R_o which are called the mid-band parameters. These three parameters allows us to build a model for our amplifier as is shown below (left figure) with

$$\frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times A_{vo} \times \frac{R_L}{R_o + R_L}$$



To find the lower cut-off frequency, f_L, we should include impedances of coupling and by-pass capacitors and solve the circuit in the frequency domain. This is a complicated analysis and, even in simple cases, lead to large analytical expressions. Fortunately, we can get derive a simple and reasonably accurate estimate of f_L.

Let's first consider a case with no by-pass capacitor – only coupling capacitors at the input and at the output. Incorporating these capacitors in the circuit and using the amplifier parameters we had calculated before, we arrive at the circuit above right. This circuit should be solved in frequency domain (done here in phasor form). At the input:

$$\frac{V_i}{V_{sig}} = \frac{R_i}{R_i + R_{sig} + 1/(j\omega C_{c1})}$$

$$\frac{V_i}{V_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{1}{1 - j\omega_{p1}/\omega}, \qquad 2\pi f_{p1} = \omega_{p1} \equiv \frac{1}{(R_i + R_{sig})C_{c1}}$$

As can be seen, the coupling capacitor C_{c1} introduced a low-frequency pole and the amplifier gain falls at frequencies below this value. At the output:

$$\frac{V_o}{A_{vo}V_i} = \frac{R_L}{R_L + R_o + 1/(j\omega C_{c2})}$$

$$\frac{V_o}{V_i} = A_{vo} \times \frac{R_L}{R_L + R_o} \times \frac{1}{1 - j\omega_{p2}/\omega}, \qquad 2\pi f_{p2} = \omega_{p2} \equiv \frac{1}{(R_o + R_L)C_{c2}}$$

Similarly, the coupling capacitor C_{cC} introduces a low-frequency pole and the amplifier gain also falls below this frequency. Then:

$$\frac{V_o}{V_{sig}} = \frac{V_o}{V_i} \times \frac{V_i}{V_{sig}}$$

$$\frac{V_o}{V_{sig}} = \frac{R_i}{R_i + R_{sig}} \times A_{vo} \times \frac{R_L}{R_o + R_L} \times \frac{1}{1 - j\omega_{p1}/\omega} \times \frac{1}{1 - j\omega_{p2}/\omega}$$

Note the first three terms are the mid-band gain of the amplifier ,v_o/v_{sig}, when capacitors where assumed to be short circuit (see previous page). As can be seen, each capacitor has introduced a pole.

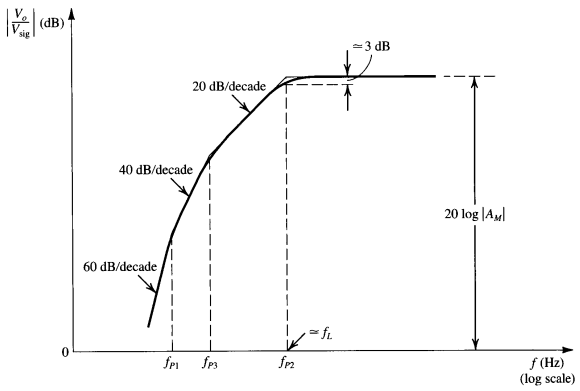
One can show that each by-pass capacitors also generates a pole and the overall overall frequency response of the amplifier is

$$\frac{V_o}{V_{sig}} = \frac{v_o}{v_{sig}} \times \frac{1}{1 - j\omega_{p1}/\omega} \times \frac{1}{1 - j\omega_{p2}/\omega} \times \frac{1}{1 - j\omega_{p3}/\omega} \times \cdot$$

Figure below shows a typical frequency response of an amplifier with 3 capacitors.

To find f_L, one should find the maximum value of the amplitude of V_o/V_{sig} (which is the mid-band gain, v_o/v_{sig}), and then find the frequency at which the gain is 3 dB below this maximum value. This requires solution of a high-order non-linear equation and is done numerically (by PSpice). However, a simple approximation for hand calculations (which is surprisingly very good) is to set

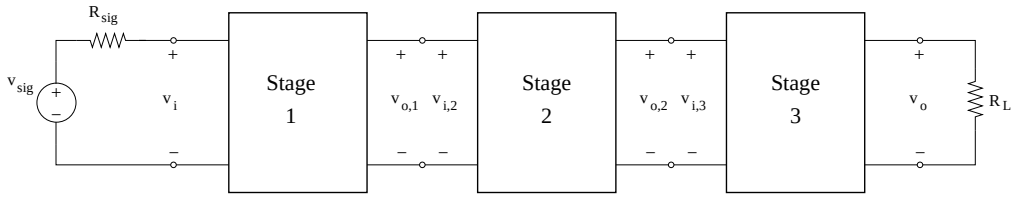
$$f_l \approx f_{p1} + f_{p2} + f_{p3} + \cdots$$



6.4 Multi-stage Amplifiers

We had argued that we only need to solve a specific amplifier circuit once. With the amplifier parameters in hand, one can then find the response of a circuit which includes many components.

To see this, let's consider a 3-stage amplifier as is shown below.



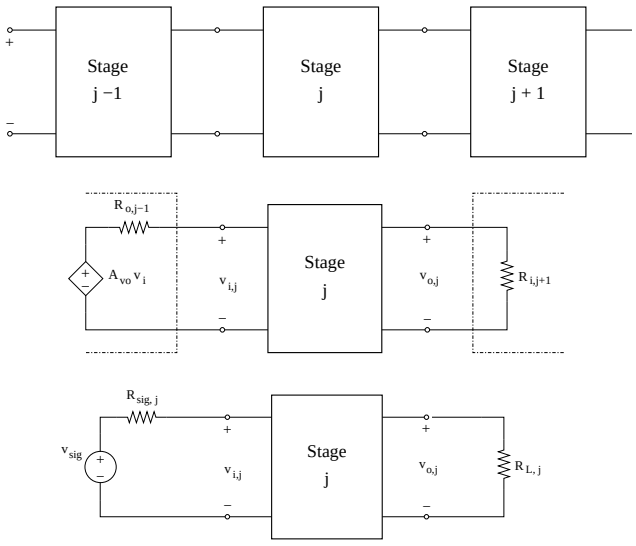
Since the output terminals of stage 1 is attached to the input terminals of stage 2, we have $v_{o,1} = v_{i,2}$. Similarly, $v_{o,2} = v_{i,}$. We also note that $v_i = v_{i,1}$ and $v_o = v_{o,3}$. Then:

$$\frac{v_o}{v_i} = \frac{v_{o,3}}{v_{i,1}} = \frac{v_{o,3}}{v_{i,3}} \times \frac{v_{i,3}}{v_{i,2}} \times \frac{v_{i,2}}{v_{i,1}} = \frac{v_o}{v_i} = \frac{v_{o,3}}{v_{i,3}} \times \frac{v_{o,2}}{v_{i,2}} \times \frac{v_{o,1}}{v_{i,1}} = A_{v3} \times A_{v2} \times A_{v1}$$

We also see that by definition, $R_i = R_{i,1}$ as $v_i = v_{i,1}$ and $i_i = i_{i,1}$. Similarly, $R_o = R_{o,3}$. We can also find the overall gain of the circuit as (generalized to a n-stage amplifier):

$$R_i = R_{i,1} \qquad\qquad R_o = R_{o,n}$$
$$\frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times A_{v1} \times A_{v2} \times A_{v3} \times \cdots$$

While the formulas above give the overall response of the multi-stage amplifier, formulas for gain, R_i, and R_o for each stage require knowledge of R_L and R_{Sig} for that particular stage. These can be found by considering the stage j and replacing stage $j-1$ and stage $j+1$ with their corresponding amplifier models as is shown below. Comparing the resulting circuit with the circuit which had solved for stage j (bottom figure), it is obvious that



$$R_{sig,j} = R_{o,j-1}$$
$$R_{L,j} = R_{i,j+1}$$

Therefore, since the gain and R_i formulas depend on R_L, solution of a multi-stage amplifier is started from the load side when R_L of the the nth stage is known: $R_{L,n} = R_L$. $(v_o/v_i)_n$ and $R_{i,n}$ is calculated. Setting $R_{L,n-1} = R_{i,n}$, one can then proceed to stage $n-1$ and compute the gain and R_i. This is continued until the first stage is reached.

Since R_o depends on R_{sig} the procedure is reversed, *i.e.,* we start from the first stage, compute $R_{o,1}$, set $R_{sig,2} = R_{o,1}$ and proceed towards the load side.

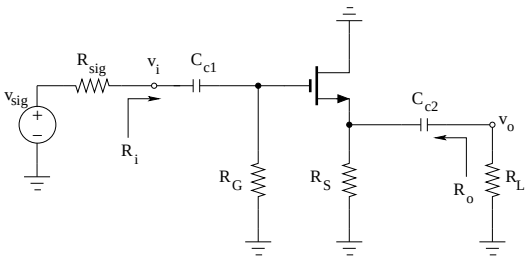
Summary of Discrete MOS Amplifiers•

Common Drain (Source Follower):

$$\frac{v_o}{v_i} = \frac{g_m(r_o \parallel R_S \parallel R_L)}{1 + g_m(r_o \parallel R_S \parallel R_L)}$$

$$R_i = R_G$$

$$R_o \approx \frac{1}{g_m} \parallel R_S$$



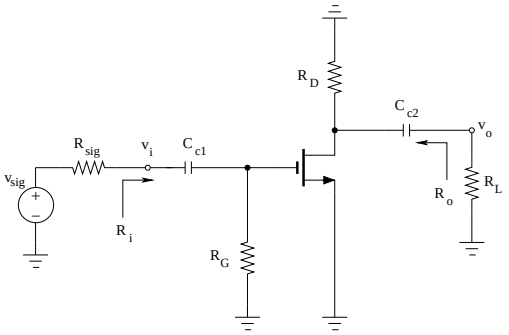
Common Source:

$$\frac{v_o}{v_i} = -g_m(r_o \parallel R_D \parallel R_L)$$

$$R_i = R_G$$

$$R_o = R_D \parallel r_o$$

$$f_{p3} = \frac{1}{2\pi C_s[R_S \parallel (r_o + R_D \parallel R_L)/(1 + g_m r_o)]}$$

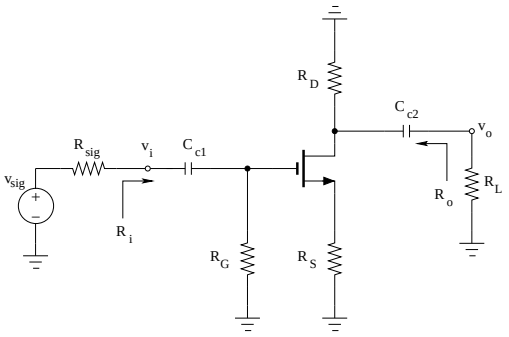


Common Source with Source Resistance:

$$\frac{v_o}{v_i} = -\frac{g_m(R_D \parallel R_L)}{1 + g_m R_S + (R_D \parallel R_L)/r_o}$$

$$R_i = R_G$$

$$R_o = R_D \parallel [r_o(1 + g_m R_S)]$$

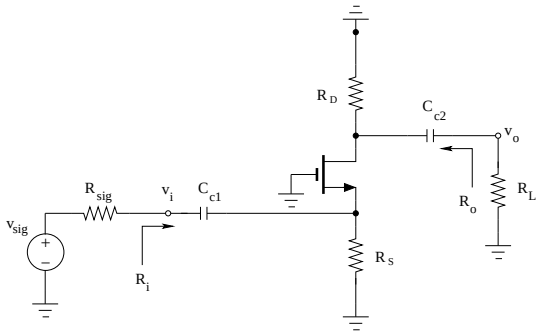


Common Gate:

$$\frac{v_o}{v_i} = g_m(r_o \parallel R_D \parallel R_L)$$

$$R_i = R_S \parallel \frac{1 + (R_D \parallel R_L)/r_o}{g_m}$$

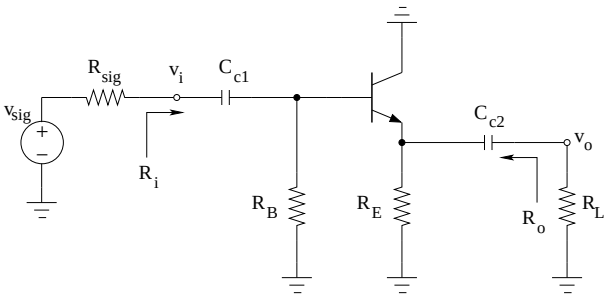
$$R_o = R_D \parallel [r_o(1 + g_m(R_S \parallel R_{sig}))]$$



• $f_l = \Sigma_j f_{pj}$ and $f_{p1} = 1/[2\pi C_{c1}(R_i + R_{sig})]$ and $f_{p2} = 1/[2\pi C_{c2}(R_L + R_o)]$

Summary of Discrete BJT Amplifiers•

Common Collector (Emitter Follower):

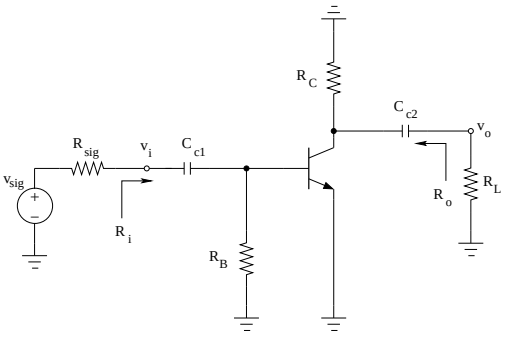


$$\frac{v_o}{v_i} = \frac{g_m(r_o \parallel R_E \parallel R_L)}{1 + g_m(r_o \parallel R_E \parallel R_L)}$$

$$R_i = R_B \parallel [r_\pi + \beta(r_o \parallel R_E \parallel R_L)]$$

$$R_o = R_E \parallel r_o \parallel \frac{r_\pi + R_B \parallel R_{sig}}{1+\beta}$$

Common Emitter:



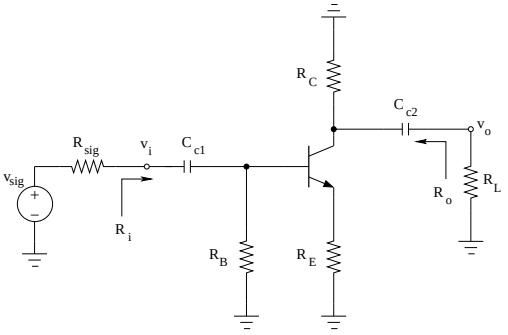
$$\frac{v_o}{v_i} = -g_m(r_o \parallel R_C \parallel R_L)$$

$$R_i = R_B \parallel r_\pi$$

$$R_o = R_C \parallel r_o$$

$$f_{p3} = \frac{1}{2\pi C_e[R_E \parallel (1/g_m + (R_B \parallel R_{sig})/\beta)]}$$

Common Emitter with Emitter Resistor:

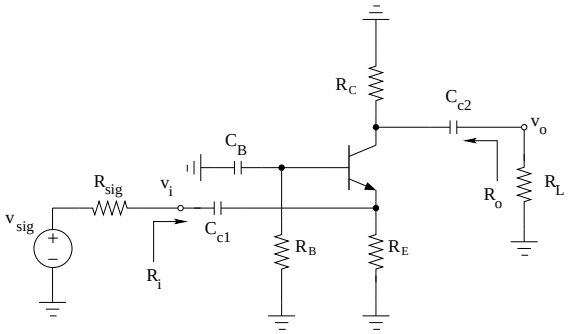


$$\frac{v_o}{v_i} \approx -\frac{g_m(R_C \parallel R_L)}{1 + g_m R_E + (1 + R_E/r_\pi)(R_C \parallel R_L)/r_o}$$

$$R_i = R_B \parallel \left[r_\pi + R_E + \frac{\beta R_E}{1 + (R_C \parallel R_L)/r_o}\right]$$

$$R_o = R_C \parallel \left[r_o\left(1 + \frac{\beta R_E}{r_\pi + R_E + R_B \parallel R_{sig}}\right)\right]$$

Common Base:



$$\frac{v_o}{v_i} = g_m(r_o \parallel R_C \parallel R_L)$$

$$R_i = R_E \parallel r_\pi \parallel \frac{1 + (R_C \parallel R_L)/r_o}{g_m}$$

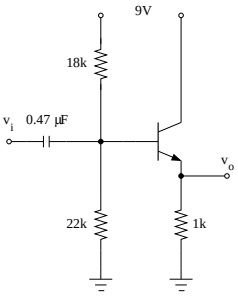
$$R_o = R_C \parallel [r_o(1 + g_m(R_E \parallel r_\pi \parallel R_{sig}))]$$

$$f_{p3} = 1/[2\pi C_b R_{CB}] \qquad R_{CB} \equiv R_B \parallel [r_\pi + (1+\beta)(R_{sig} \parallel R_E)]$$

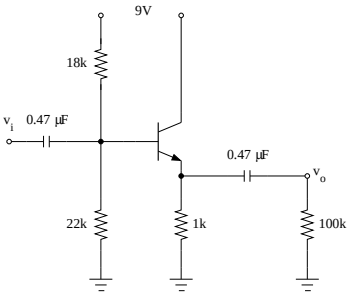
• $f_l = \Sigma_j f_{pj}$ and $f_{p1} = 1/[2\pi C_{c1}(R_i + R_{sig})]$ and $f_{p2} = 1/[2\pi C_{c2}(R_L + R_o)]$

6.5 Exercise Problems

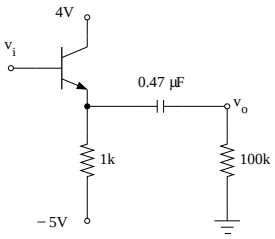
Problem 1 to 12: Find the bias point and amplifier parameters of this circuit (Si BJT with $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).



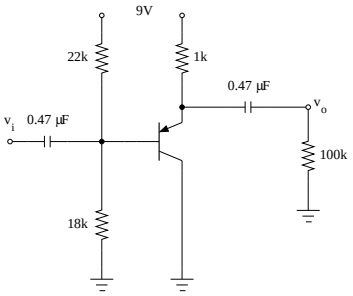
Problem 1



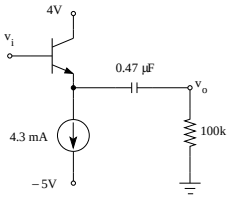
Problem 2



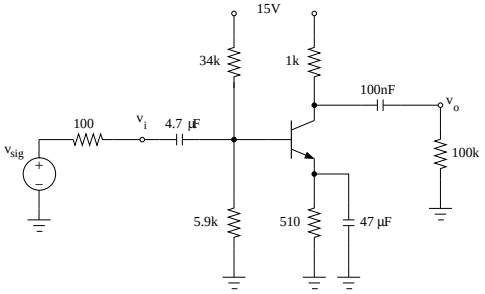
Problem 3



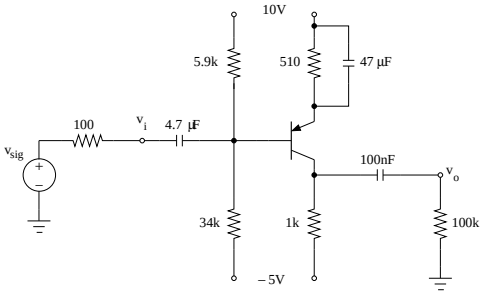
Problem 4



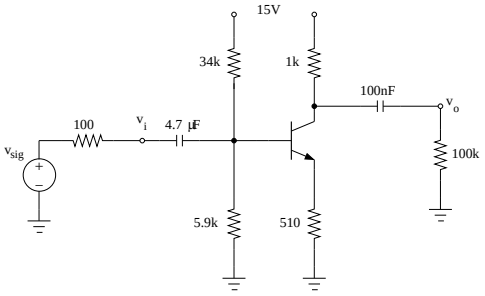
Problem 5



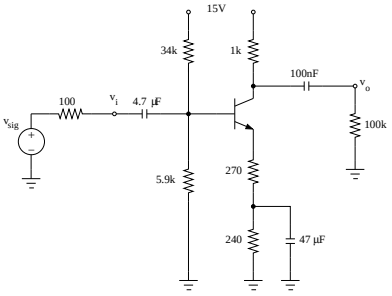
Problem 6



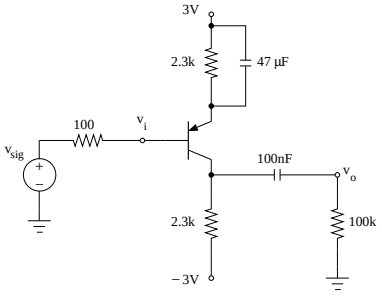
Problem 7



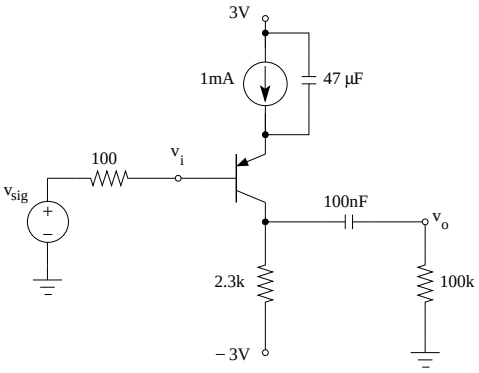
Problem 8



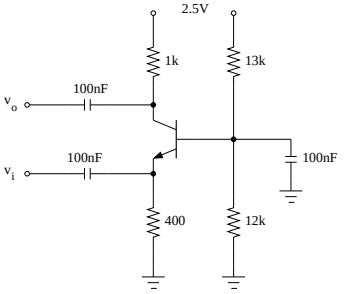
Problem 9



Problem 10

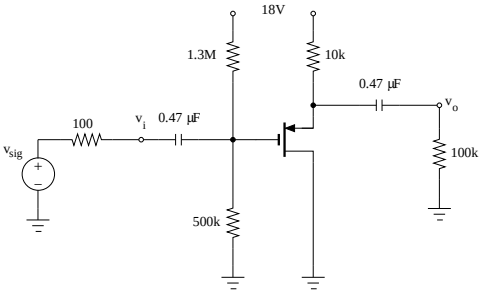


Problem 11

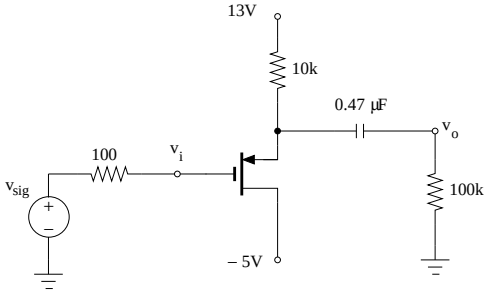


Problem 10 Problem 12

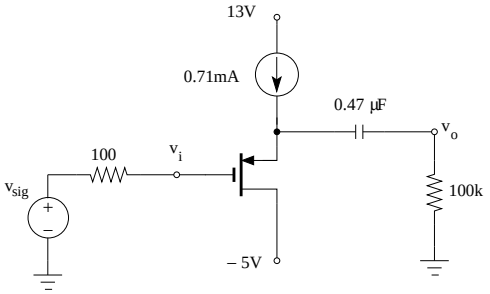
Problem 13-16. Find the bias point and amplifier parameters of this circuit ($V_{tn} = 4$ V, $V_{tp} = -4$ V, $\mu_p C_{ox}(W/L) = \mu_n C_{ox}(W/L) = 0.4$ mA/V^2, and $\lambda = 0.01$ V^{-1}. Ignore the channel-width modulation effect in biasing calculations.)



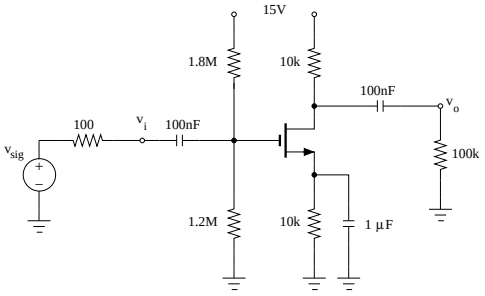
Problem 13



Problem 14

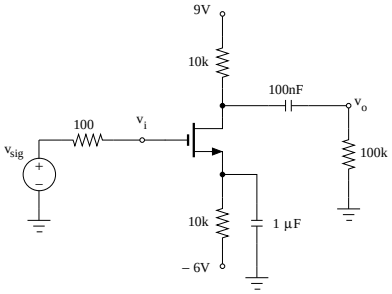


Problem 15

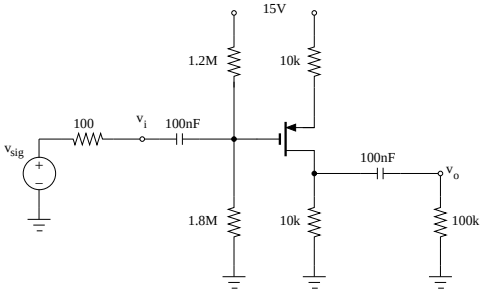


Problem 16

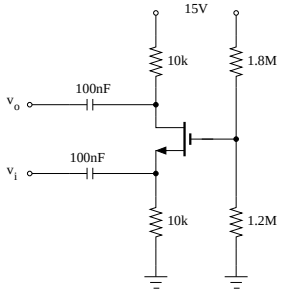
Problem 18-24. Find the bias point and amplifier parameters of this circuit ($V_{tn} = 1$ V, $V_{tp} = -1$ V, $\mu_p C_{ox}(W/L) = \mu_n C_{ox}(W/L) = 0.8$ mA/V^2, and $\lambda = 0.01$ V^{-1}. Ignore the channel-width modulation effect in biasing calculations.



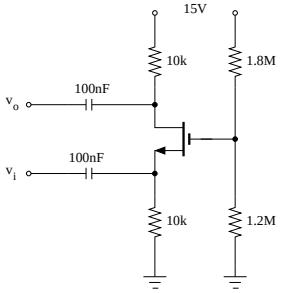
Problem 17



Problem 18



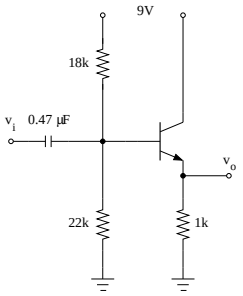
Problem 19



Problem 19

6.6 Solution to Selected Exercise Problems

Problem 1. Find the bias point and amplifier parameters of this circuit (Si BJT with $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).



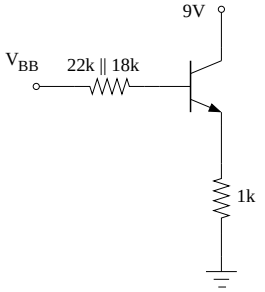
Bias: Set $v_i = 0$ and capacitors open. Set $v_i = 0$ and capacitors open. Replace R_{B1}/R_{B2} voltage divider with its Thevenin equivalent. Assuming BJT in active,

$$R_B = 18 \text{ k} \parallel 22 \text{ k} = 9.9 \text{ k}\Omega \qquad V_{BB} = \frac{22}{18+22} \times 9 = 4.95 \text{ V}$$

KVL: $V_{BB} = R_B I_B + V_{BE} + 10^3 I_E$

$$4.95 = 9.9 \times 10^3 I_E/(\beta+1) + 0.7 + 10^3 I_E$$

$$I_E = 4.05 \text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 20.3 \ \mu\text{A}$$



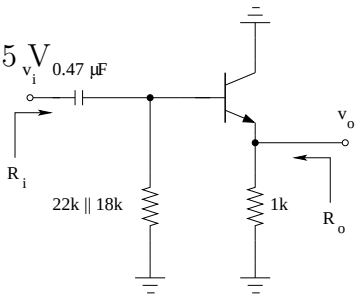
KVL: $9 = V_{CE} + 10^3 I_E$

$$V_{CE} = 9 - 10^3 \times 4 \times 10^{-3} = 5 \text{ V}$$

Since $V_{CE} > V_{D0} = 0.7$, assumption of BJT in active is correct.

Bias summary: $I_E \approx I_C = 4.05$ mA, $I_B = 20.3 \ \mu$A, $V_{CE} = 5$ V

Small-Signal: First we calculate the small-signal parameters:



$$g_m = \frac{I_C}{V_T} = \frac{4 \times 10^{-3}}{26 \times 10^{-3}} = 156 \text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = 1.28 \text{ k} \qquad r_o \approx \frac{V_A}{I_C} = \frac{150}{4 \times 10^{-3}} = 37.0 \text{ k}$$

Note that we could have ignored V_{CE} compared to V_A in the above expression for r_o. Proceeding with the small signal analysis, we zero bias sources (see circuit). As the input is at the base and output is at the emitter, this is a common-collector amplifier (emitter follower). Using formulas of page 6-21 and noting $R_L \to \infty$, $R_E \ll r_o$, and $R_E \gg r_e$:

$$\frac{v_o}{v_i} = \frac{g_m(r_o \parallel R_E \parallel R_L)}{1 + g_m(r_o \parallel R_E \parallel R_L)} = \frac{152}{153} \approx 1$$

$$R_i \approx R_B \parallel [r_\pi + \beta(r_o \parallel R_E \parallel R_L)] = (9.9 \text{ k}) \parallel (1.28 \text{ k} + 195 \text{ k}) = 9.42 \text{ k} \quad (\approx R_B)$$

$$R_o = R_E \parallel r_o \parallel \frac{r_\pi + R_B \parallel R_{Sig}}{1+\beta} = 6.4 \ \Omega \quad (\approx \frac{r_\pi}{\beta} = \frac{1}{g_m})$$

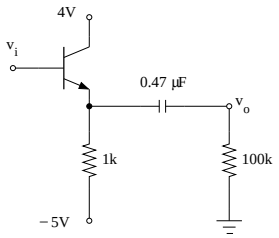
$$f_l = f_{p1} = \frac{1}{2\pi C_{c1}(R_i + R_{sig})} = \frac{1}{2\pi \times 0.47 \times 10^{-6} \times (9.9 \times 10^3 + 0)} = 34.2 \text{ Hz}$$

Problem 2. Find the bias point and amplifier parameters of this circuit (Si BJT with $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).

This is the same circuit as Problem 1 with exception of C_{c2} and R_L. The bias point is exactly the same. As $R_E \ll R_L$, the amplifier parameters would be the same except $f_l = f_{p1} + f_{p2} = 34.3 + 3.39 = 37.6$ Hz.

Problem 3. Find the bias point and amplifier parameters of this circuit (Si BJT with $n = 2$, $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).

This circuit is similar to Problem 1 expect that the transistor is biased with two voltage sources (values are chosen to give approximately the same bias point).



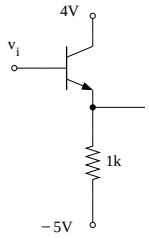
Bias: Set $v_i = 0$ and capacitors open:

BE-KVL: $0 = V_{BE} + 10^3 I_E - 5$

$$I_E = 4.3\text{mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 21.5\ \mu\text{A}$$

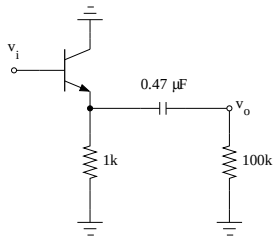
CE-KVL: $4 = V_{CE} + 10^3 I_E - 5$

$$V_{CE} = 9 - 10^3 \times 4.3 \times 10^{-3} = 4.7\ \text{V}$$



Bias summary: $I_E \approx I_C = 4.3$ mA, $I_B = 21.5\ \mu$A, $V_{CE} = 4.7$ V

Small-Signal: First we calculate the small-signal parameters:



$$g_m = \frac{I_C}{V_T} = \frac{4.3 \times 10^{-3}}{26 \times 10^{-3}} = 165.4\ \text{mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = 1.21\ \text{k} \qquad r_o \approx \frac{V_A}{I_C} = \frac{150}{4.3 \times 10^{-3}} = 34.9\ \text{k}$$

Proceeding with the signal analysis, we zero bias sources (see circuit). As the input is at the base and output is at the emitter, this is a common-collector amplifier (emitter follower). The difference with Problem 1 is that there is no R_B ($R_B = \infty$) which affects R_i only.

$$A_v = \frac{g_m(r_o \parallel R_E \parallel R_L)}{1 + g_m(r_o \parallel R_E \parallel R_L)} = \frac{161}{162} \approx 1$$

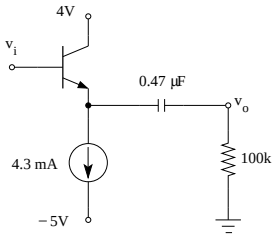
$$R_i \approx R_B \parallel [r_\pi + (1+\beta)(r_o \parallel R_E \parallel R_L)] = \infty \parallel (1.21\ \text{k} + 194\ \text{k}) = 195\ \text{k}$$

$$R_o = R_E \parallel r_o \parallel \frac{r_\pi + R_B \parallel R_{Sig}}{1+\beta} = 6.0\ \Omega \quad (\approx \frac{r_\pi}{\beta} = \frac{1}{g_m})$$

$$f_l = f_{p2} = \frac{1}{2\pi C_{c2}(R_L + R_o)} = \frac{1}{2\pi \times 0.47 \times 10^{-6} \times (100 \times 10^3 + 6)} = 3.39\ \text{Hz}$$

Problem 5. Find the bias point and amplifier parameters of this circuit (Si BJT with$\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).

This circuit is similar to the circuit of Problem 3 except that the transistor is biased with a current source.

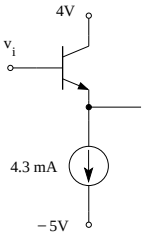


Bias: Set $v_i = 0$ and capacitors open.

$$I_E = 4.3 \text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 21.5 \ \mu\text{A}$$

BE-KVL: $0 = V_{BE} + V_E \quad \rightarrow \quad V_E = -0.7$ V

CE-KVL: $4 = V_{CE} + V_E \quad \rightarrow \quad V_{CE} = 4.7$ V

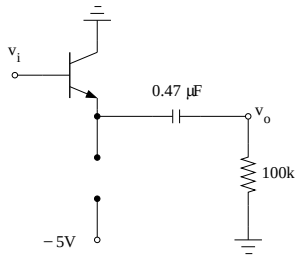


Bias summary: $I_E \approx I_C = 4.3$ mA, $I_B = 21.5\ \mu$A, $V_{CE} = 4.7$ V

Small-Signal: First we calculate the small-signal parameters:

$$g_m = \frac{I_C}{V_T} = \frac{4.3 \times 10^{-3}}{26 \times 10^{-3}} = 165.4 \text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = 1.21 \text{ k} \qquad r_o \approx \frac{V_A}{I_C} = \frac{150}{4.3 \times 10^{-3}} = 34.9 \text{ k}$$



Amplifier Response: we zero bias sources (the current source becomes an open circuit. As the input is at the base and output is at the emitter, this is a common-collector amplifier (emitter follower). The difference with problem 3 is that here $R_E \rightarrow \infty$. Using formulas of page 6-21 and noting $R_E \parallel R_L = R_L \gg r_e$

$$A_v = \frac{g_m(r_o \parallel R_E \parallel R_L)}{1 + g_m(r_o \parallel R_E \parallel R_L)} = \frac{4,279}{4,280} \approx 1$$

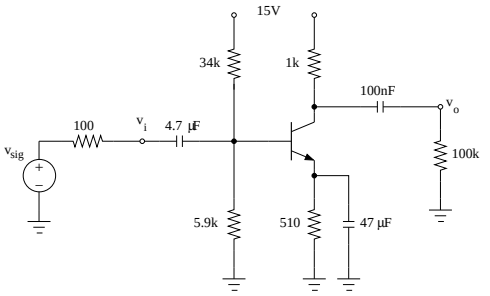
$$R_i \approx R_B \parallel [r_\pi + \beta(r_o \parallel R_E \parallel R_L)] = \infty \parallel (1.21 \text{ k} + 5.17 \text{ M}) = 5.17 \text{ M}$$

$$R_o = R_E \parallel r_o \parallel \frac{r_\pi + R_B \parallel R_{Sig}}{1 + \beta} = 6.0\ \Omega \quad (\approx \frac{r_\pi}{\beta} = \frac{1}{g_m})$$

$$f_l = f_{p2} = \frac{1}{2\pi C_{c2}(R_L + R_o)} = 3.39 \text{ Hz}$$

Comparing results from Problems 1 through 5 highlights the impact of each element on the amplifier performance as in successive problems, R_L and C_{C2} were added, and then R_B, C_{C1} and R_E were eliminated.

Problem 6. Find the bias point and amplifier parameters of this circuit (Si BJT with $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).



Bias: Set $v_i = 0$ and capacitors open. Replace R_{B1}/R_{B2} voltage divider with its Thevenin equivalent:

$$R_B = 5.9 \text{ k} \parallel 34 \text{ k} = 5.0 \text{ k},$$

$$V_{BB} = \frac{5.9}{5.9 + 34} \times 15 = 2.22 \text{ V}$$

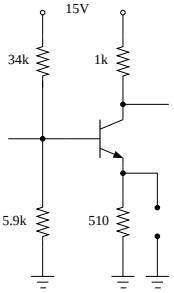
BE-KVL: $V_{BB} = R_B I_B + V_{BE} + 510 I_E$

$$2.22 = 5.0 \times 10^3 I_E / * \beta + 1) + 0.7 + 510 I_E$$

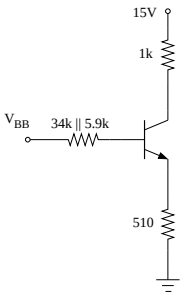
$$I_E = 2.84 \text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 14.2 \ \mu\text{A}$$

CE-KVL: $15 = 1000 I_C + V_{CE} + 510 I_E$

$$V_{CE} = 10.5 \text{ V} \qquad > V_{D0}$$



Bias summary: $I_C \approx I_E = 2.84$ mA, $I_B = 14.2 \ \mu$A, $V_{CE} = 10.5$ V



Small-Signal: First we calculate the small-signal parameters:

$$g_m = \frac{I_C}{V_T} = \frac{2.84 \times 10^{-3}}{26 \times 10^{-3}} = 109 \text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = 1.83 \text{ k} \qquad r_o \approx \frac{V_A}{I_C} = \frac{150}{2.84 \times 10^{-3}} = 52.8 \text{ k}$$

Proceeding with the small signal analysis, we zero bias sources (see circuit). As the input is at the base and output is at the collector, this is a common-emitter amplifier with NO emitter resistor as there is bypass capacitor.

$$\frac{v_o}{v_i} = -g_m (r_o \parallel R_C \parallel R_L) = -106$$

$$R_i = R_B \parallel r_\pi = 5.0 \parallel 1.83 = 1.34 \text{ k}$$

$$A_v = \frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{v_o}{v_i} = -0.93 \times 106 = -99$$

$$R_o = R_C \parallel r_o = 0.98 \text{ k} \quad (\approx R_C)$$

$$f_{p1} = \frac{1}{2\pi C_{c1}(R_i + R_{sig})} = \frac{1}{2\pi \times 4.7 \times 10^{-6} \times (1,340 + 0)} = 25.3 \text{ Hz}$$

$$f_{p2} = \frac{1}{2\pi C_{c2}(R_L + R_o)} = \frac{1}{2\pi 100 \times 10^{-9}(100 \times 10^3 + 980)} = 15.9 \text{ Hz}$$

$$f_{p3} = \frac{1}{2\pi C_e[R_E \parallel (1/g_m + (R_B \parallel R_{sig})/\beta)]}$$

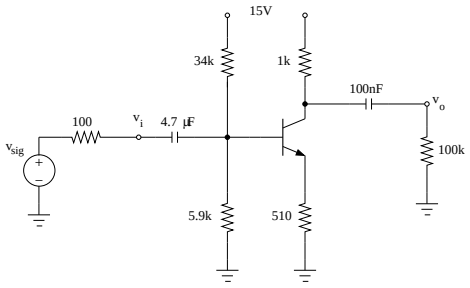
$$f_{p3} = \frac{1}{2\pi C_e[R_E \parallel 9.67]} = 356 \text{ Hz}$$

$$f_l = f_{p1} + f_{p2} + f_{pb} = 25.3 + 15.9 + 356 = 397 \text{ Hz}$$

Note that although C_b is the largest capacitor in the circuit (*e.g.,* 10 times larger than C_{c1}, f_{p3} is 10 times larger than the other poles.

Problem 8. Find the bias point and amplifier parameters of this circuit (Si BJT with $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).

Bias: Set $v_i = 0$ and capacitors open. The bias circuit is exactly that of Problem 7 with $R_B = 5.0$ k.



Bias summary:
$I_C \approx I_E = 2.84$ mA, $\quad I_B = 14.2\ \mu$A, $\quad V_{CE} = 10.5$ V

Small-Signal: The small-signal parameters are also the same as those of Problem 7: $\quad g_m = 109$ mA/V, $r_\pi =$ 1.83k, and $r_o = 52.8$ k.

Proceeding with the small signal analysis, we zero bias sources (see circuit). As the input is at the base and output is at the collector, this is a degenerated common-emitter amplifier (*i.e,* with a emitter resistor):

$$\frac{v_o}{v_i} \approx -\frac{g_m(R_C \parallel R_L)}{1 + g_m R_E} = -1.91$$

$$R_i = R_B \parallel [r_\pi + (1+\beta)R_E] = 4.8 \text{ k} \quad (\approx R_B)$$

$$A_v = \frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{v_o}{v_i} = -0.98 \times 1.91 = -1.87$$

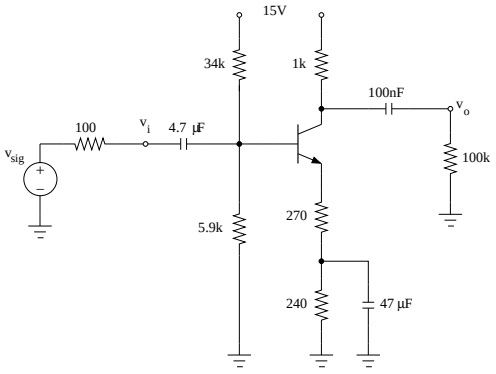
$$R_o = R_C \parallel \left[r_o \left(1 + \frac{\beta R_E}{r_\pi + R_E + R_B \parallel R_{sig}} \right) \right] \approx R_C = 1 \text{ k}$$

$$f_{p1} = \frac{1}{2\pi C_{c1}(R_i + R_{sig})} = \frac{1}{2\pi \times 4.7 \times 10^{-6} \times (4,800 + 100)} = 6.91 \text{ Hz}$$

$$f_{p2} = \frac{1}{2\pi C_{c2}(R_L + R_o)} \approx \frac{1}{2\pi C_{c2}(R_L + R_c)} \approx \frac{1}{2\pi 100 \times 10^{-9}(100 \times 10^3 + 10^3)} = 15.8 \text{ Hz}$$

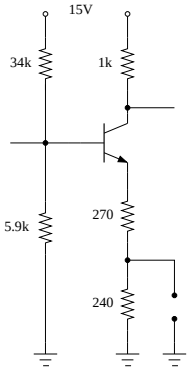
$$f_l = f_{p1} + f_{p2} = 6.9 + 15.8 = 22.7 \text{ Hz}$$

Problem 9. Find the bias point and amplifier parameters of this circuit (Si BJT with $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).



Bias:

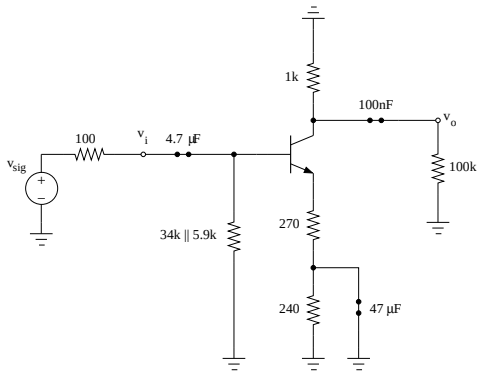
Set $v_i = 0$ and capacitors open. Because the 47 μF capacitor across the 240 Ω resistor becomes an open circuit, the total R_E for bias is $270 + 240 = 510$ Ω and the bias circuit is exactly that of Problem 7 (or Problem 9) with $R_B = 5.0$ k.



Bias summary:
$I_C \approx I_E = 2.84$ mA, $\quad I_B = 14.2$ μA, $\quad V_{CE} = 10.5$ V

Small-Signal: The small-signal parameters are also the same as those of Problem 7: $\quad g_m = 109$ mA/V, $r_\pi = 1.83$k, and $r_o = 52.8$ k.

Proceeding with the small signal analysis, we zero bias sources (see circuit). As the input is at the base and output is at the collector, this is a degenerated common-emitter amplifier (*i.e,* with a emitter resistor). For midband amplifier parameters calculations, the 47 μF capacitor across the 240 Ω resistor becomes a short circuit and the total R_E for small-signal is 270 Ω.



$$\frac{v_o}{v_i} \approx -\frac{g_m(R_C \parallel R_L)}{1 + g_m R_E} = -3.55$$

$$R_i = R_B \parallel [r_\pi + (1+\beta)R_E] = 4.6 \text{ k} \quad (\approx R_B)$$

$$A_v = \frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{v_o}{v_i} = -0.98 \times 1.91 = -3.47$$

$$R_o = R_C \parallel \left[r_o \left(1 + \frac{\beta R_E}{r_\pi + R_E + R_B \parallel R_{sig}} \right) \right] \approx R_C = 1 \text{ k}$$

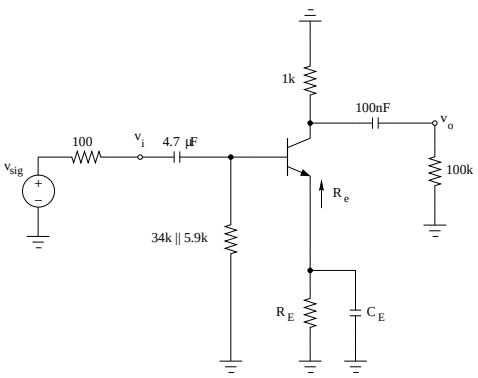
$$f_{p1} = \frac{1}{2\pi C_{c1}(R_i + R_{sig})} = \frac{1}{2\pi \times 4.7 \times 10^{-6} \times (4,600 + 100)} = 7.20 \text{ Hz}$$

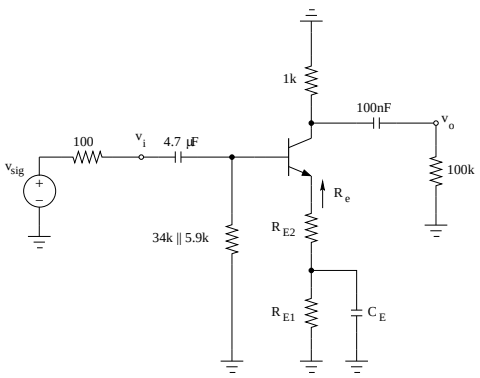
$$f_{p2} = \frac{1}{2\pi C_{c2}(R_L + R_o)} \approx \frac{1}{2\pi C_{c2}(R_L + R_c)} \approx \frac{1}{2\pi 100 \times 10^{-9}(100 \times 10^3 + 10^3)} = 15.8 \text{ Hz}$$

We need to find the pole introduced by the 47 μF by-pass capacitor, f_{pb}. Although this configuration was not included in the formulas for BJT elementary configuration of page 6-21, we can extend those formulas to cover this case.

The pole introduced by the by-pass capacitor in the common emitter case is (see figure below left)

$$f_{p3} = \frac{1}{2\pi C_e[R_E \parallel (1/g_m + (R_B \parallel R_{sig})/\beta)]}$$





Per our discussion of Section 6.7 on how to find poles introduced by each capacitor, $R_E \parallel [1/g_m + (R_B \parallel R_{sig})/\beta)]$ is the total resistance seen across the terminal of C_e. As can be seen from the circuit (above right), the resistance across C_c terminals consists of two resistors in parallel, R_E and R_e. R_e is the resistance seen between the emitter of the BJT and the ground and is: $R_e \equiv 1/g_m + (R_B \parallel R_{sig})/\beta)$ from the above formula.

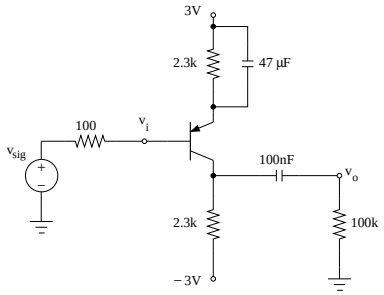
For the circuit here (defined $R_{E1} = 240\ \Omega$ and $R_{E2} = 270\ \Omega$), the resistance across C_e is made of two resistances in parallel: R_{E1} and the combination of R_{E2} and R_e, the resistance seen through the emitter of BJT in series. Thus:

$$f_{p3} = \frac{1}{2\pi C_b[R_{E1} \parallel (R_{E2} + 1/g_m + (R_B \parallel R_{sig})/\beta)]}$$

$$f_{pb} = \frac{1}{2\pi \times C_e[240 \parallel (270 + 9.17 + 0.49]} = \frac{1}{2\pi \times 47 \times 10^{-6} \times 129} = 26.2 \text{ Hz}$$

$$f_l = f_{p1} + f_{p2} = 7.20 + 15.8 + 26.2 = 49.2 \text{ Hz}$$

Problem 10. Find the bias point and amplifier parameters of this circuit (Si BJT with $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).



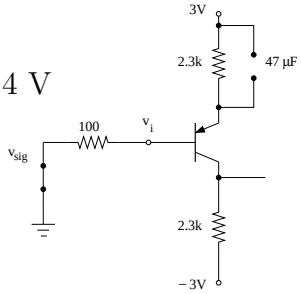
Bias: Set $v_i = 0$ and capacitors open.

BE-KVL: $3 = 2.3I_E + V_{EB}$

$I_E = 1$ mA $\approx I_C$, $\quad I_B = I_E/(1+\beta) = 5\ \mu$A

CE-KVL: $3 = 2.3 \times 10^3 I_E + V_{EC} + 2.3 \times 10^3 I_C - 3$

$V_{EC} = 6 - 4.6 \times 10^3 \times 1 \times 10^{-3} = 1.4$ V



Bias summary: $I_C \approx I_E = 1$ mA, $\quad I_B = 5.0\ \mu$A, $\quad V_{CE} = 1.4$ V

Small-Signal: First we calculate the small-signal parameters:

$$g_m = \frac{I_C}{V_T} = \frac{1 \times 10^{-3}}{26 \times 10^{-3}} = 38.5 \text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = 5.26 \text{ k} \qquad r_o \approx \frac{V_A}{I_C} = \frac{150}{1 \times 10^{-3}} = 150 \text{ k}$$

Proceeding with the small signal analysis, we zero bias sources. As the input is at the base and output is at the collector, this is a common-emitter amplifier. It does not have an emitter resistor as 47 μF capacitor shorts out R_E for signals.

$$A_v = -g_m(r_o \parallel R_C \parallel R_L) = -38.5 \times 10^{-3}(150 \text{ k} \parallel 2.3 \text{ k} \parallel 100 \text{ k}) = -85.3$$

$$R_i = R_B \parallel r_\pi = 10.4 \text{ k}$$

$$R_o = R_C \parallel r_o \approx 2.3 \text{ k}$$

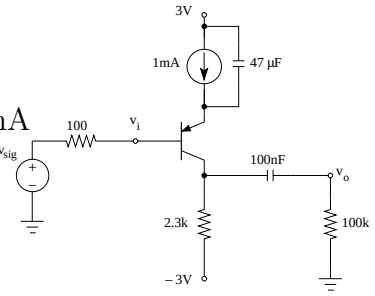
$$f_{p1} = 0$$

$$f_{p2} = \frac{1}{2\pi C_{c2}(R_L + R_o)} = \frac{1}{2\pi 100 \times 10^{-9}(10^5 + 10^3)} = 15.8 \text{ Hz}$$

$$f_{p3} = \frac{1}{2\pi C_e[R_E \parallel (1/g_m + (R_B \parallel R_{sig})/\beta)]} = \frac{1}{2\pi C_e[2,300 \parallel 26]} = 132 \text{ Hz}$$

$$f_l = f_{p1} + f_{p2} + f_{pb} = 0 + 15.8 + 132 = 148 \text{ Hz}$$

Problem 11. Find the bias point and amplifier parameters of this circuit (Si BJT with $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).



This is the same circuit as that of Problem 11 expect that the transistor is biased with a current source

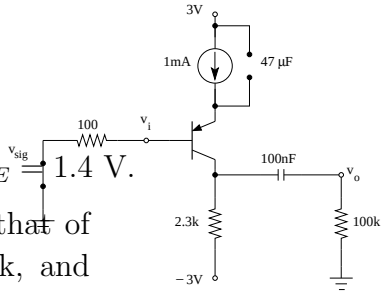
Bias: Set $v_i = 0$ and capacitors open. From the circuit $I_E = 1$ mA

$$I_E = 1 \text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 5 \ \mu\text{A}$$

BE-KVL: $V_E = V_{EB} = 0.7$ V

CE-KVL: $V_E = V_{CE} + 2.3 \times 10^3 I_C - 3 = V_{CE} - 0.7$

$V_{CE} = 1.4$ V



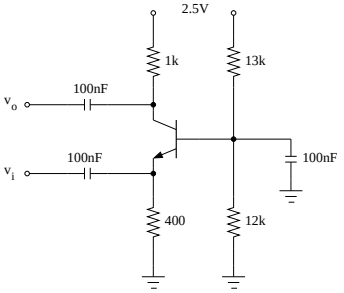
Bias summary: $I_C \approx I_E = 1$ mA, $I_B = 50 \ \mu$A, $V_{CE} = 1.4$ V.

Small-Signal: As the bias point is exactly the same as that of problem 11, we have: $g_m = 38.5$ mA/V, $r_\pi = 5.26$k, and $r_o = 150$ k.

Amplifier response: The only difference with problem 11 is that $R_E \to \infty$ in this circuit. R_E only appears in f_{p3} but $R_E = \infty$ does not change results:
$A_v = -37.9$, $R_i = 10.4$ k, $R_o = 0.99$ k, and $f_l = 0 + 15.8 + 132 = 148$ Hz.

Problem 12. Find the bias point and amplifier parameters of this circuit (Si BJT with $\beta = 200$ and $V_A = 150$ V. Ignore the Early effect in biasing calculations).

Bias: Set $v_i = 0$ and capacitors open.



$$R_B = 12 \text{ k} \parallel 13 \text{ k} = 6.24 \text{ k},$$

$$V_{BB} = \frac{12}{12+13} \times 2.5 = 1.2 \text{ V}$$

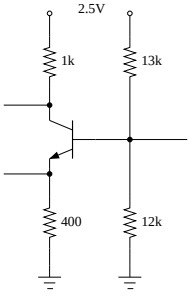
BE-KVL: $V_{BB} = R_B I_B + V_{BE} + 510 I_E$

$1.2 = 6.24 \times 10^3 I_E/(1+\beta) + 0.7 + 400 I_E$

$$I_E = 1.16 \text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 5.8 \ \mu\text{A}$$

CE-KVL: $2.5 = 1000 I_C + V_{CE} + 400 I_E$

$V_{CE} = 2.5 - 1,400 \times 1.16 \times 10^{-3} = 0.88$ V



Bias summary: $I_C \approx I_E = 1.16$ mA, $I_B = 5.8 \ \mu$A, $V_{CE} = 0.88$ V

Small-Signal: First we calculate the small-signal parameters:

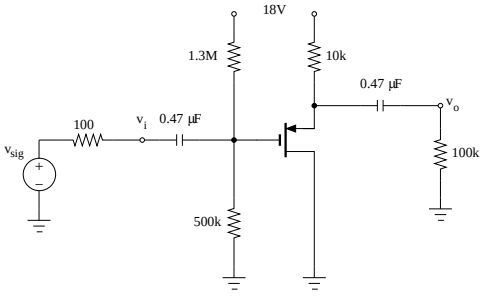
$$g_m = \frac{I_C}{V_T} = \frac{1.16 \times 10^{-3}}{26 \times 10^{-3}} = 44.6 \text{ mA/V}$$
$$r_\pi = \frac{\beta}{g_m} = 4.48 \text{ k} \qquad r_o \approx \frac{V_A}{I_C} = \frac{150}{1.16 \times 10^{-3}} = 129 \text{ k}$$

Proceeding with the small signal analysis, we zero bias sources. As the input is at the emitter and output is at the collector, this is a common-base amplifier (note $R_L = \infty$).

$$\frac{v_o}{v_i} = g_m(r_o \parallel R_C \parallel R_L) = 44.6 \times 10^{-3}(129 \text{ k} \parallel 1 \text{ k} \parallel \infty) = 44.26$$
$$R_i = R_E \parallel r_\pi \parallel \frac{1 + (R_C \parallel R_L)/r_o}{g_m} = 1 \text{ 1k} \parallel 4.48 \text{ 1k} \parallel 22.4 = 21.8 \ \Omega \quad (\approx 1/g_m)$$
$$R_o = R_C \parallel [r_o(1 + g_m(R_E \parallel r_\pi \parallel R_{sig}))] \approx R_C = 1 \text{ k}$$
$$f_{p1} = \frac{1}{2\pi C_{c1}(R_i + R_{sig})} = \frac{1}{2\pi 1000 \times 10^{-9}(21.8)} = 7.30 \text{ kHz}$$
$$f_{p2} = \frac{1}{2\pi C_{c2}(R_L + R_o)} = 0$$
$$R_{CB} \equiv R_B \parallel [r_\pi + (1 + \beta)(R_{sig} \parallel R_E)] = 6.24 \text{ k} \parallel 84.9 \text{ k} \approx 5.81 \text{ k}$$
$$f_{p3} = \frac{1}{2\pi C_b R_{CB}} == \frac{1}{2\pi \times 100 \times 10^{-9} \times 5.81 \times 10^3} = 274 \ Hz$$
$$f_l = f_{p1} + f_{p2} + f_{pb} = 7,300 + 0 + 274 = 7.57 \text{ kHz}$$

Note the small input resistance of this amplifier and corresponding large f_{p1}.

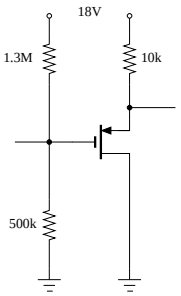
Problem 13. Find the bias point and amplifier parameters of this circuit ($V_{tn} = 4$ V, $V_{tp} = -4$ V, $\mu_p C_{ox}(W/L) = \mu_n C_{ox}(W/L) = 0.4$ mA/V^2, and $\lambda = 0.01$ V^{-1}. Ignore the channel-width modulation effect in biasing calculations.)



Bias: Since $I_G = 0$:

$$V_G = \frac{0.5 \text{ M}}{1.3 \text{ M} + 0.5 \text{ M}} \times 18 = 5 \text{ V}$$
$$R_G = 1.3 \text{ M} \parallel 500 \text{ k} = 361 \text{ k}$$

Assume PMOS is in the active state,



$$I_D = 0.5\mu_p C_{ox}(W/L)V_{OV}^2$$
$$\text{SG-KVL:} \quad 18 = 10^4 I_D + V_{SG} + V_G = 10^4 I_D + V_{OV} + |V_{tp}| + V_G$$
$$10^4 \times 0.5 \times 0.4 \times 10^{-3} V_{OV}^2 + V_{OV} - 18 + 4 + 5 = 0$$
$$2V_{OV}^2 + V_{OV} - 9 = 0$$

Negative root is unphysical, $V_{OV} = 1.89$ V and $V_{SG} = V_{OV} + |V_{tp}| = 5.89$ V.

$$I_D = 0.5 \times 0.4 \times 10^{-3} V_{OV}^2 = 0.71 \text{ mA}$$
$$\text{SD-KVL:} \quad 18 = V_{SD} + 10^4 I_D \quad \rightarrow \quad V_{SD} = 18 - 10^4 \times 0.71 \times 10^{-3} = 10.9 \text{ V}$$

Since $V_{SD} = 10.9 \geq V_{OV} = 1.89$ V, our assumption of PMOS in active is justified.

Bias summary: $I_D = 0.71$ mA, $V_{OV} = 1.89$ V, $V_{SG} = 5.89$ V, $V_{SD} = 10.9$ V.

Small-Signal: First we calculate the small-signal parameters:

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2 \times 0.71 \times 10^{-3}}{1.89} = 0.751 \text{ mA/V}$$
$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.01 \times 0.71 \times 10^{-3}} = 141 \text{ k}$$

Proceeding with the small signal analysis, we zero bias sources. As the input is at the gate and output is at the source, this is a common-drain amplifier (source follower).

$$\frac{v_o}{v_i} = \frac{g_m(r_o \parallel R_S \parallel R_L)}{1 + g_m(r_o \parallel R_S \parallel R_L)} = \frac{6.41}{7.41} = 0.866$$
$$R_i = R_G = 361 \text{ k}$$

$$A_v = \frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{v_o}{v_i} = 0.866$$

$$R_o = \frac{1}{g_m} \parallel R_S = 1.33 \text{ k} \parallel 10 \text{ k} = 1.17 \text{ k}$$

$$f_{p1} = 1/[2\pi C_{c1}(R_i + R_{sig})] = 0.94 \text{ Hz}$$

$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_o)] = 3.39 \text{ Hz}$$

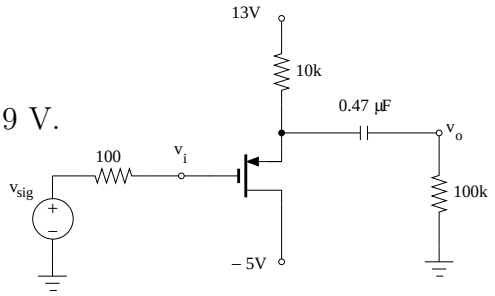
$$f_l = f_{p1} + f_{p2} = 4.33 \text{ Hz}$$

Problem 14. Find the bias point and amplifier parameters of this circuit ($V_{tn} = 4$ V, $V_{tp} = -4$ V, $\mu_p C_{ox}(W/L) = \mu_n C_{ox}(W/L) = 0.4$ mA/V^2, and $\lambda = 0.01$ V^{-1}. Ignore the channel-width modulation effect in biasing calculations.

Answer:

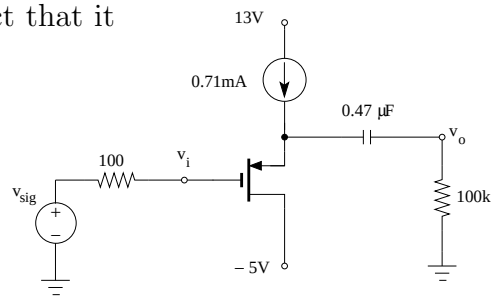
$I_D = 0.71$ mA, $V_{OV} = 1.89$ V, $V_{SG} = 5.89$ V, $V_{SD} = 10.9$ V.

$v_o/v_{sig} = 0.866$, $R_i = \infty$, $R_o = 1.17$ k,
$f_{p1} = 0$, $f_{p2} = 3.35$ Hz, $f_l = 4.3$ Hz.



Problem 15. Find the bias point and amplifier parameters of this circuit ($V_{tn} = 4$ V, $V_{tp} = -4$ V, $\mu_p C_{ox}(W/L) = \mu_n C_{ox}(W/L) = 0.4$ mA/V^2, and $\lambda = 0.01$ V^{-1}. Ignore the channel-width modulation effect in biasing calculations.)

This circuit is also similar to that of problem 14 expect that it is biased with a current source:



$$I_D = 0.71 \text{ mA}$$

$$I_D = 0.5\mu_p C_{ox}(W/L)V_{OV}^2$$

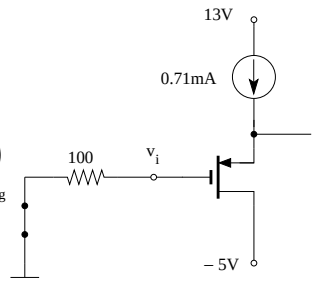
$$0.71 \times 10^{-3} = 0.5 \times 0.4 \times 10^{-3} V_{OV}^2$$

$$V_{OV} = 1.88 \text{ V}$$

$$V_{SG} = V_{OV} + |V_{tp}| = 5.88 \text{ V}$$

$$V_{SG} = V_S - V_G = 5.88 \quad \rightarrow \quad V_S = 5.88 \text{ V}$$

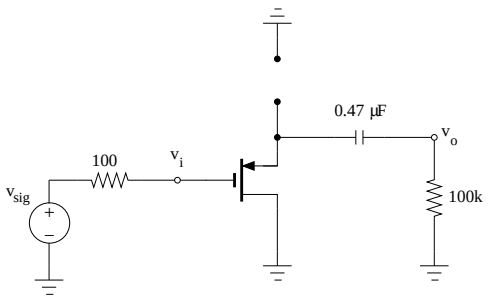
$$V_{SD} = V_S - V_D = 5.88 - (-5) = 10.9 \text{ V} \qquad (> V_{OV} = 1.89)$$



Bias summary:
$I_D = 0.71$ mA, $V_{OV} = 1.88$ V, $V_{SG} = 5.88$ V, $V_{SD} = 10.9$ V.

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2 \times 0.71 \times 10^{-3}}{1.89} = 0.751 \text{ mA/V}$$

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.01 \times 0.71 \times 10^{-3}} = 141 \text{ k}$$



This is a common-drain amplifier (source follower). Note $R_G = \infty$, $R_s = \infty$.

$$\frac{v_o}{v_i} = \frac{g_m(r_o \parallel R_S \parallel R_L)}{1 + g_m(r_o \parallel R_S \parallel R_L)} = \frac{43.9}{44.9} = 0.98$$

$$R_i = R_G = \infty$$

$$A_v = \frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{v_o}{v_i} = 0.98$$

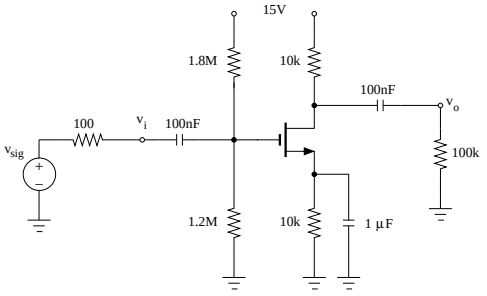
$$R_o = \frac{1}{g_m} \parallel R_S = 1.33 \text{ k} \parallel \infty = 1.33 \text{ k}$$

$$f_{p1} = 1/[2\pi C_{c1}(R_i + R_{sig})] = 0$$

$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_o)] = 3.39 \text{ Hz}$$

$$f_l = f_{p1} + f_{p2} = 3.39 \text{ Hz}$$

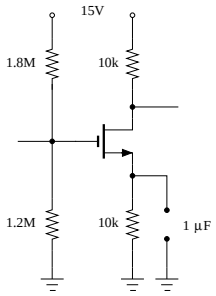
Problem 16. Find the bias point and amplifier parameters of this circuit ($V_{tn} = 1$ V, $V_{tp} = -1$ V, $\mu_p C_{ox}(W/L) = \mu_n C_{ox}(W/L) = 0.8$ mA/V^2, and $\lambda = 0.01$ V^{-1}. Ignore the channel-width modulation effect in biasing calculations.



Bias: Since $I_G = 0$:

$$V_G = \frac{1.2\text{ M}}{1.2\text{ M} + 1.8\text{ M}} \times 15 = 6\text{ V}$$
$$R_G = 1.2\text{ M} \parallel 1.8\text{ M} = 720\text{ k}$$

Assume NMOS is in the active state,



$$I_D = 0.5\mu_p C_{ox}(W/L)V_{OV}^2$$
GS-KVL: $$V_G = V_{GS} + 10^4 I_D = V_{OV} + V_t + 10^4 I_D$$
$$10^4 \times 0.5 \times 0.8 \times 10^{-3} V_{OV}^2 + V_{OV} - 6 + 1 = 0$$
$$4V_{OV}^2 + V_{OV} - 5 = 0$$

Negative root is unphysical, $V_{OV} = 1.0$ V and $V_{GS} = V_{OV} + V_t = 2.0$ V.

$$I_D = 0.5 \times 0.8 \times 10^{-3} V_{OV}^2 = 0.40\text{ mA}$$
DS-KVL: $$15 = 10^4 I_D + V_{DS} + 10^4 I_D \quad \rightarrow \quad V_{DS} = 7\text{ V} \quad (> V_{OV} = 1.0)$$

Bias summary: $I_D = 0.40$ mA, $V_{OV} = 1.0$ V, $V_{GS} = 2.0$ V, $V_{DS} = 7.0$ V.

Small-Signal:

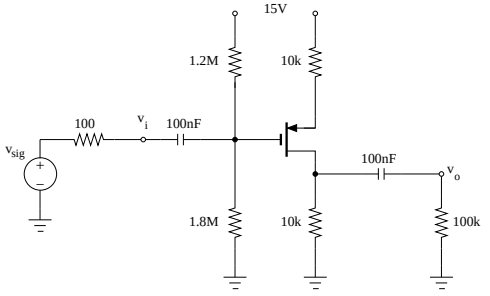
$$g_m = \frac{2I_D}{V_{OV}} = 2 \times 0.4 \times 10^{-3} = 0.8\text{ mA/V} \qquad r_o = \frac{1}{\lambda I_D} = \frac{1}{0.4 \times 10^{-3}} = 250\text{ k}$$

As the input is at the gate and output is at the collector, this is a common-source amplifier. There is no R_S because of the by-pass capacitor.

$$\frac{v_o}{v_i} = -g_m(r_o \parallel R_D \parallel R_L) = -0.8 \times 10^{-3}(250\text{ k} \parallel 10\text{ k} \parallel 100\text{ k}) = -7.02$$
$$R_i = R_G = 720\text{ k}$$
$$A_v = \frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{v_o}{v_i} = -7.02$$
$$R_o = R_D \parallel r_o = 10\text{ k} \parallel 100\text{ k} = 9.09\text{ k}$$

$$f_{p1} = 1/[2\pi C_{c1}(R_i + R_{sig})] = 2.21 \text{ Hz}$$
$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_o)] = 14.6 \text{ Hz}$$
$$f_{p3} = \frac{1}{2\pi C_s[R_S \parallel (1/g_m)]} = \frac{1}{2\pi C_s[10 \text{ k} \parallel 1.25 \text{ k}]} = \frac{1}{2\pi \times 10^{-6} \times 1.11 \times 10^3} = 143 \text{ Hz}$$
$$f_l = f_{p1} + f_{p2} + f_{pb} = 2.21 + 14.6 + 143 = 160 \text{ Hz}$$

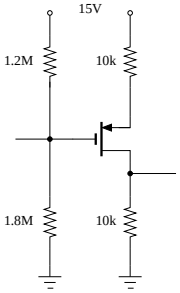
Problem 18. Find the bias point and amplifier parameters of this circuit ($V_{tn} = 1$ V, $V_{tp} = -1$ V, $\mu_p C_{ox}(W/L) = \mu_n C_{ox}(W/L) = 0.8$ mA/V^2, and $\lambda = 0.01$ V^{-1}. Ignore the channel-width modulation effect in biasing calculations.



Bias: Since $I_G = 0$:

$$V_G = \frac{1.8 \text{ M}}{1.2 \text{ M} + 1.8 \text{ M}} \times 15 = 9 \text{ V}$$
$$R_G = 1.2 \text{ M} \parallel 1.8 \text{ M} = 720 \text{ k}$$

Assume PMOS is in the active state,



$$I_D = 0.5\mu_p C_{ox}(W/L)V_{OV}^2$$
SG-KVL: $$15 = 10^4 I_D + V_{SG} + V_G = 10^4 I_D + V_{OV} + |V_{tp}| + V_G$$
$$10^4 \times 0.5 \times 0.8 \times 10^{-3} V_{OV}^2 + V_{OV} - 15 + 9 + 1 = 0$$
$$4V_{OV}^2 + V_{OV} - 5 = 0$$

Negative root is unphysical, $V_{OV} = 1.0$ V and $V_{SG} = V_{OV} + |V_{tp}| = 2.0$ V.

$$I_D = 0.5 \times 0.8 \times 10^{-3} V_{OV}^2 = 0.40 \text{ mA}$$
SD-KVL: $$15 = 10^4 I_D + V_{SD} + 10^4 I_D \quad \rightarrow \quad V_{SD} = 7 \text{ V} \quad (> V_{OV} = 1.0)$$

Bias summary: $I_D = 0.40$ mA, $V_{OV} = 1.0$ V, $V_{SG} = 2.0$ V, $V_{SD} = 7.0$ V. Small-Signal:

$$g_m = \frac{2I_D}{V_{OV}} = 2 \times 0.4 \times 10^{-3} = 0.8 \text{ mA/V} \qquad r_o = \frac{1}{\lambda I_D} = \frac{1}{0.4 \times 10^{-3}} = 250 \text{ k}$$

As the input is at the gate and output is at the collector, this is a common-source amplifier with R_S.

$$\frac{v_o}{v_i} = -\frac{g_m(R_D \parallel R_L)}{1 + g_m R_S + (R_D \parallel R_L)/r_o} = -\frac{0.8 \times 10^{-3}(10 \text{ k} \parallel 100 \text{ k})}{1 + 0.8 \times 10^{-3} \times 10^4 + (10 \text{ k} \parallel 100 \text{ k})/(250 \text{ k})}$$

$$\frac{v_o}{v_i} = -\frac{7.27}{9.04} = -0.805$$

$$R_i = R_G = 720 \text{ k}$$

$$A_v = \frac{v_o}{v_{sig}} = \frac{R_i}{R_i + R_{sig}} \times \frac{v_o}{v_i} = -0.805$$

$$R_o = R_D \parallel [r_o(1 + g_m R_S)] = 10 \text{ k} \quad (\approx R_D)$$

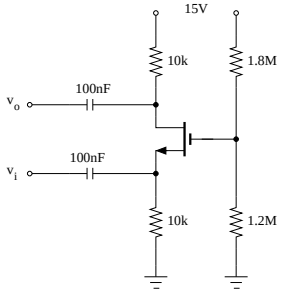
$$f_{p1} = 1/[2\pi C_{c1}(R_i + R_{sig})] = 2.21 \text{ Hz}$$

$$f_{p2} = 1/[2\pi C_{c2}(R_L + R_o)] = 14.5 \text{ Hz}$$

$$f_l = f_{p1} + f_{p2} = 16.7 \text{ Hz}$$

Note one needs to choose R_D to be several times R_S for this amplifier to have a gain larger than unity.

Problem 19. Find the bias point and amplifier parameters of this circuit ($V_{tn} = 1$ V, $V_{tp} = -1$ V, $\mu_p C_{ox}(W/L) = \mu_n C_{ox}(W/L) = 0.8$ mA/V^2, and $\lambda = 0.01$ V^{-1}. Ignore the channel-width modulation effect in biasing calculations.



Answer:

$I_D = 0.40$ mA, $V_{OV} = 1.0$ V, $V_{GS} = 2.0$ V, $V_{SD} = 7.0$ V.

$v_o/v_{sig} = 0.866$, $R_i = \infty$, $R_o = 1.17$ k,
$f_{p1} = 0$, $f_{p2} = 3.35$ Hz, $f_l = 4.3$ Hz.

Amp Response (common-gate amp):
$A_v = 7.7$, $R_i = 1.1$ k, $R_o = 10$ k, and $f_l = 1.45 \times 10^3 + 22 = 1.47$ kHz,