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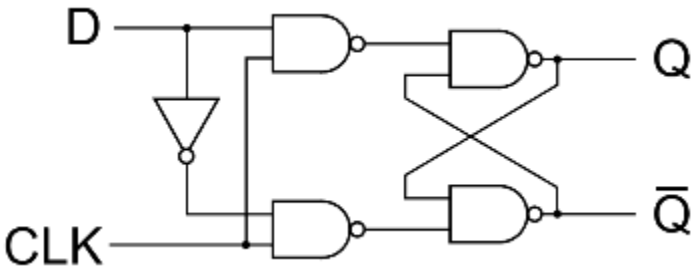
Student ID:

EHB322E Digital Electronic Circuits
Homework 3

Deadline: Wednesday 14/05/2014 (submit to Vehbi Cömert, Room:3007)

Consider a CMOS D-flip-flop shown below.



A D-Flip-Flop

1) **DESIGN:** Use the following definitions/parameters for your design.
   Equivalent resistor for an NMOS transistor: $R_N = (10k\Omega) / (W/L)_N$
   Equivalent resistor for a PMOS transistor: $R_P = (20k\Omega) / (W/L)_P$
   *Suppose that each node in the flip-flop has an internal capacitance of **10fF**.*
   *Select **L=1u** for all transistors.*
   *Suppose that all NAND gates are **identical**.*
   ***PD**: The worst case propagation delay at the output(s) when the input is switching.*
   ***A**: Total chip area represented as a sum of **W** values of all transistors (there are total of 4×4+2=18 transistors).*

   Design problem: Find ***W*** values of all transistors to minimize delay area product ***PD*×*A***.

2) **SIMULATION:** Construct the flip-flop designed in 1) using SPICE. Select V_{DD}=5V (logic 1) and ground=0V (logic 0). Connect body terminals of NMOS and PMOS transistors to their source terminals. Use T15DN and T15DP spice models for NMOS and PMOS transistors, respectively (for details refer to Homework 1). Apply square pulse waves to required inputs.

   Simulation problem: Find the worst case propagation delay ***PD*** by performing transient analysis. Sketch input and output waveforms. Compare your result with that in **1)**; justify your answer.

Grading: 1) 60%, 2) 40%

Note: *Do not forget to attach SPICE **output file** prints to your homework!*