INTRODUCTION TO ELECTRONICS (21604)
HOMEWORK #6
Assoc.Prof.Dr. İnci ÇİLESİZ
DUE DATE and TIME 11 April 2003 - 12.00

From Sedra & Smith (Examples are 10 points each, Problems are 20 points each)

1. Exercises 5.22 and 5.23.
2. Study Example 5.9 and then solve Exercise 5.24.
3. Study Example 5.10 and then solve Exercise 5.26.
4. Problems 5.1, *D5.7 and *5.26.

1a. **Exercise 5.22:** **(a)** If a signal source is capacitively coupled to the gate then $R_{in} = R_G = 1\ M\Omega$.

(b) Provided the MOSFET operates in the saturation region, $I_D = 0{,}25mA/V\left(V_{GS} - 2V\right)^2 = 1mA$. Thus V_{GS} = 4 V. Also V_G = 0 V becase no current flows into the gate. Thus V_S = -4 V and $R_S = \dfrac{V_S - V_{SS}}{I_D} = 6k$.

(c) Allowed swing at the drain is ±2V. Since the MOSFET operates in the saturation region, $V_{GS} - 2V \le V_{DS} \Leftrightarrow V_G - 2V \le V_D \Rightarrow V_D \ge 2V$. Since $R_D = \dfrac{V_{DD} - V_D}{I_D}$, and $v_{Dmin} = V_D - 2V = 0V$, $R_D = 10k$.

1b. **Exercise 5.23:** Using the R_S value we found above,

$I_D = 0{,}25mA/V(V_{GS} - 3V)^2 = 0{,}25mA/V(V_G - V_S - 3V)^2$

V_G = 0 V and $V_S = -V_{SS} + I_D R_D$ yields $I_D = 0{,}25mA/V\left(0 - I_D R_S + V_{SS} - 3V\right)^2$, i.e., we obtain a second order equation, the solution of which gives $I_{D_{1/2}} = \dfrac{88 \pm 26{,}2}{72} mA$, with I_{D1} = 0,86 mA, I_{D2} = 1,59 mA. If we take the lower value for drain current we see that $\Delta I_D = \dfrac{I_D - 1mA}{1mA} = -0{,}14 = -14\%$. With the higher value that change would have been +59%.

2. **Exercise 5.24:** For double the current by changing the width only, by definition, W2 = 2*W_1 = 200 µm. Since $r_o = \dfrac{V_A}{I_D}$, r_{o2} is decreased by half, i.e., r_{o2} = 500k. Since $\Delta I_o = \dfrac{5V - V_{GS}}{r_{o2}} = \dfrac{5V - 2V}{5k} = 6\mu A$, I_o = 206 µA.

3. **Exercise 5.26:** Using $g_m = \sqrt{2k_n' \frac{W}{L} I_{REF}} = 1{,}06 mA/V$, $r_{o,n} = \frac{|V_{An}|}{I_{REF}} = 128k$ and $r_{o,p} = \frac{|V_{Ap}|}{I_{REF}} = 192k$, $A_v = -g_m(r_{o,n} \| r_{o,p}) = -81{,}4 V/V$.

4a. **Problem 5.1:** Using values given in Table 5.1 on p. 364 and $C_{ox} = \frac{3{,}97\varepsilon_o}{t_{ox}}$

20 nm oxide → Cox = 1,75 fF/μm², 100 nm oxide → Cox = 0,35 fF/μm² as also given on Table 5.1. WE know that $A_{ox} = \frac{C}{C_{ox}}$. Thus for 1 pF capacitance:

20 nm oxide → Cox = 1,75 fF/μm², Aox = 0,28 mm² and 100 nm oxide → Cox = 0,35 fF/μm², Aox = 0,06 mm².
On the other hand for 10 pF capacitance:
Assuming W = L for simplicity, maximum dimensions, i.e., maximum A, would be for minimum oxide thickness, that is 20 nm. Aox = 2,8 mm² → W = L = 169 μm.

4b. **Problem D5.7:** From $C_{ox} = \frac{3{,}97\varepsilon_o}{t_{ox}}$, for 50 nm oxide thickness, C_{ox} = 0,70 fF/μm², with help from Table 5.1 on p. 364, $k_n' = \mu_n C_{ox}$ = 40,7 μA/V². For operation in the saturation region the minimum requirement is $V_{DS} = V_{GS} - V_{th} = 2{,}5V$. Using this value in $I_D = \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_{th})^2 = 1A$, W/L = 7862 μm/μm is obtained. If L = 2 μm,
P = W = 15725 μm = 15,725 mm, a very large value!!!!
Total device area is $A_{total} = [L(drain) + L(channel) + L(source)]P = 94350 \mu m^2$
The last part of this problem requires a quick look at page 436 for a simple reminder of Eq. (5.13) according to which $r_{DS} = \frac{1}{\frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_{th})} = 0{,}762\Omega$, and $V_{DS} = r_{DS} I_D = 0{,}762V$.

4c. **Problem *5.26:**

Case	T	V_S(V)	V_G(V)	V_D(V)	I_D(μA)	Type	Mode	$\mu C_{ox}W/L$(μA/V²)	V_t(V)
a	1	0	2	5	100	NMOS	saturation	200	1
	1	0	3	5	400	NMOS	saturation	200	1
b	2	5	3	-4,5	50	PMOS	saturation	400	-1,5
	2	5	2	-0,5	450	PMOS	saturation	400	-1,5
c	3	5	3	4	200	PMOS	triode	400	-1
	3	5	2	0	800	PMOS	saturation	400	-1
d	4	-2	0	0	72	NMOS	saturation	100	0,8
	4	-4	0	-3	270	NMOS	triode	100	0,8