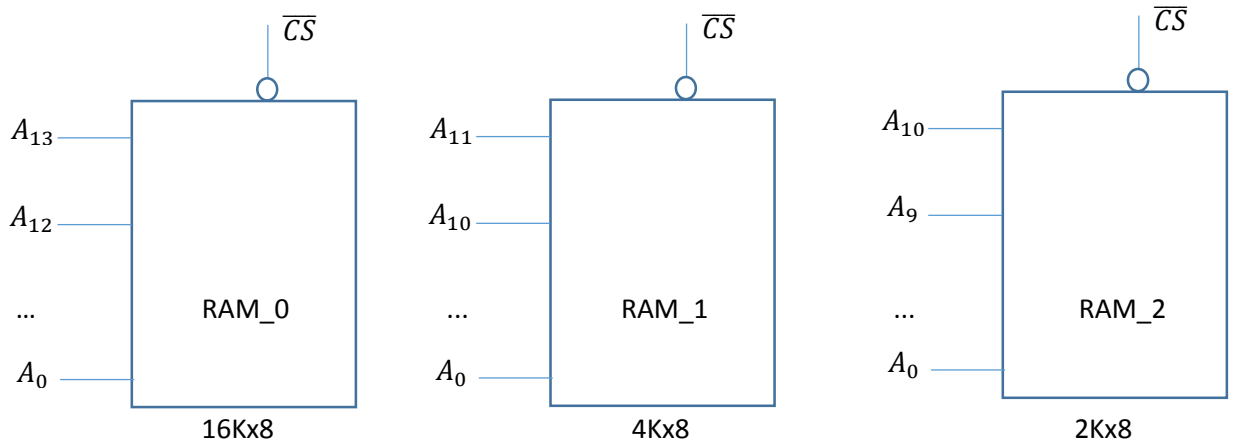
# BLG212E-HW1

Please connect following memory components to CPU which has 16-bit address bus and 8 bit data bus.




(8bit data line of RAMs are not shown.)

RAM_0 address range should be $8000-$BFFF

RAM_1 address range should be $D000-$DFFF

RAM_2 address range should be $E800-$EFFF

You can use logic gates (EXOR, AND, OR, NOR, NOT …) and decoders (1x2, 2x4, 3x8, 4x16 …).

Put your all drawings on the paper.

You can find reference documentation on the following link.

http://ninova.itu.edu.tr/tr/dersler/bilgisayar-bilisim-fakultesi/2123/blg-212e/ekkaynaklar?g216633