

EHB322E Digital Electronic Circuits

Quiz 1

Duration: 30 Minutes

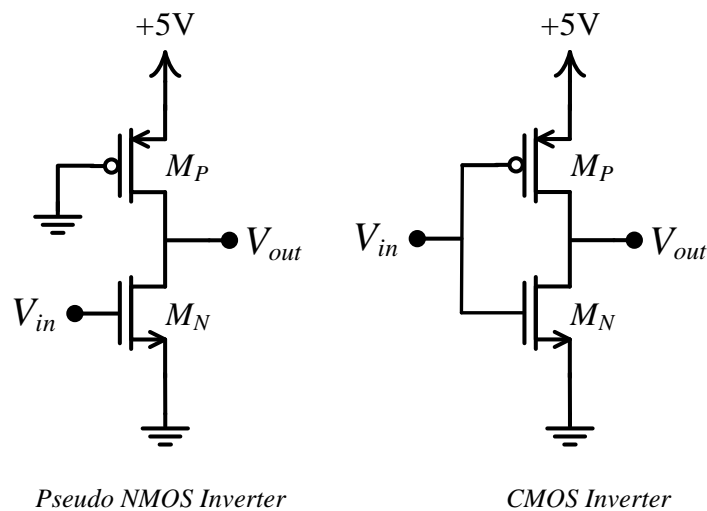
Grading: 1) 20%, 2) 80%,

Quiz is in closed-notes and closed-books format

For your answers please use the space provided in the exam sheet

GOOD LUCK!

- 1) Please circle TRUE if you think that the statement is true; FALSE otherwise.



- a. Consider the pseudo NMOS inverter shown above.

Statement: Increasing W value of M_N makes the value of V_{OH} increase.

TRUE / FALSE

- b. Consider the pseudo NMOS inverter shown above.

Statement: Increasing W value of M_N makes the value of t_{PLH} decrease.

TRUE / FALSE

- c. Consider the CMOS inverter shown above.

Statement: If (W/L) ratios and absolute threshold voltage values of PMOS/NMOS transistors are same then the switching threshold value of V_M is $5/2V$.

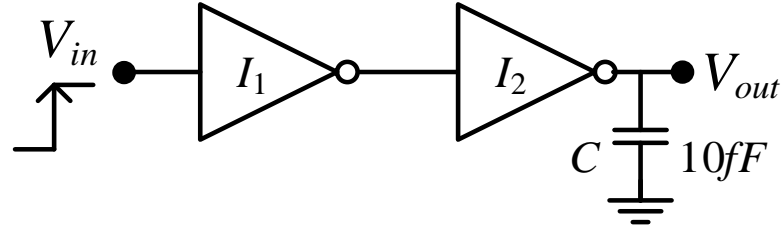
TRUE / FALSE

- d. Consider the CMOS inverter shown above.

Statement: The output (load) capacitor is a sum of C_{GS} and C_{GD} capacitors of the transistors.

TRUE / FALSE

- 2) Consider the buffer of two CMOS inverters shown below. A capacitor of 10fF is connected to the output. A signal switching from low to high is applied to the input.
Transistor parameters: $c_{ox}=1 \text{ fF}/\mu\text{m}^2$, $\tau_n = \tau_p=1\text{ps}$, $W_{P1}=2\mu$, $W_{N1}=1\mu$, $W_{P2}=4\mu$, $W_{N2}=2\mu$, $L_{N1}=L_{P1}=L_{N2}=L_{P2}=1\mu$.



A buffer of two CMOS inverters.

Propagation delays of an inverter is formulized as follows. C_L represents the load capacitor of the inverter.

$$t_{PHL} = (C_L/C_N) \tau_n \quad C_N = c_{ox} W_N L_N$$

$$t_{PLH} = (C_L/C_P) \tau_p \quad C_P = c_{ox} W_P L_P$$

Determine **the total propagation delay** at the output. Neglect C_{GD} capacitors.