
İTÜ Computer Engineering Department
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**Due:** April 8, 2015, 23:00

# Computer Architecture 2nd Homework

A CPU supporting both vectored and autovectored interrupts has an *Autovector* (**VA**) input, a *Data Acknowledge* (**DACK**) input, an *Interrupt Request* (**IRQ**) input, an *Interrupt Acknowledge* (**INTACK**) output and an 8-bit data bus.

Interrupt requests are sent to the CPU through the **IRQ** input and the CPU activates its **INTACK** output when it is ready for the interrupt routine. If the **VA** input is inactive, the CPU operates in vectored mode and reads the vector number from the data bus as its **DACK** input is activated. If the **VA** input is active, the CPU does not read the vector number and operates in autovectored mode.

Four interrupt sources (*A1, A2, B1, B2*) of two different types (*A, B*) will be used in combination with the described CPU. Type *A* devices have vectored interrupts, while type *B* devices have autovectored interrupts. Each device has an *Interrupt Request* (**IRQ**) output and an *Interrupt Acknowledge* (**INTACK**) input. Type *A* devices withdraw their interrupt requests within 20ns of the activation of their **INTACK** input and place their vector addresses on the data bus through their additional 8-bit *Vector Number* (**VN**) output.

The interrupt request priority order for the devices is $A_1 > B_1 > A_2 > B_2$.

All signals on the CPU and the devices operate in positive logic (activated with a logic 1).

**1)** A system using the described CPU, the four devices (*A1, A2, B1, B2*), and an interrupt priority circuit is to be designed.

   **a.** Draw a representation of this system, indicating the interrupt priority circuit **as a block** without showing the internal structure.

   **b.** Design and draw a **serial** priority circuit using logic gates that would comply with the connections you indicated on the system.

   **c.** Design and draw a **parallel** priority circuit using logic gates that would comply with the connections you indicated on the system.

**2)** For each device type you used (*A, B*), briefly describe how the CPU determines the start address of the interrupt service routine.