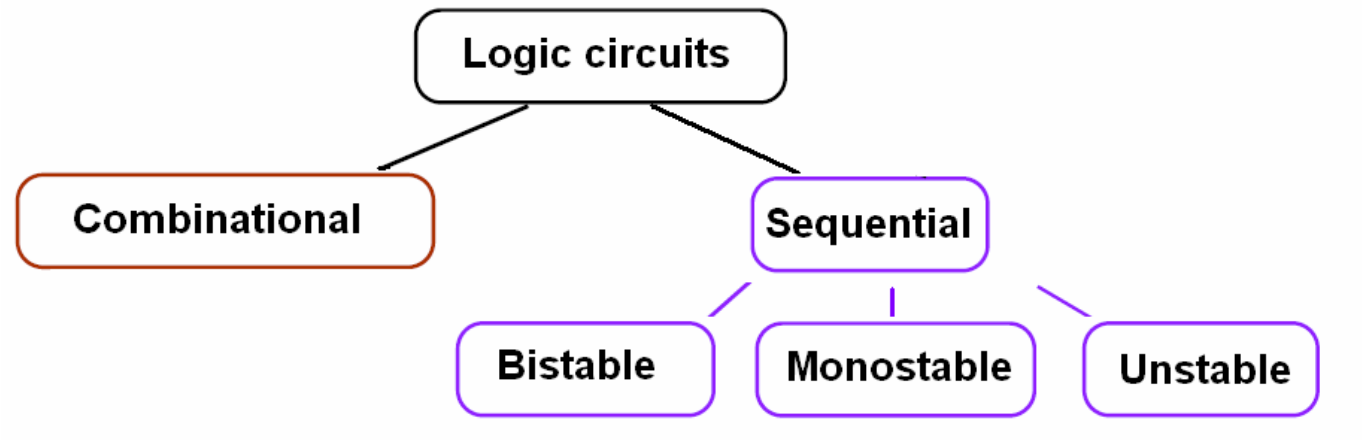
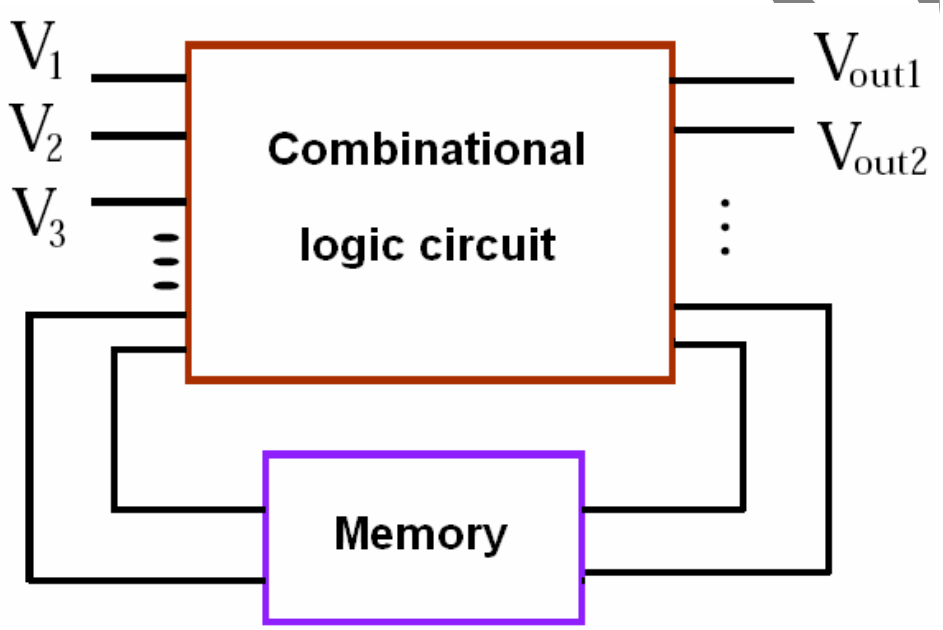
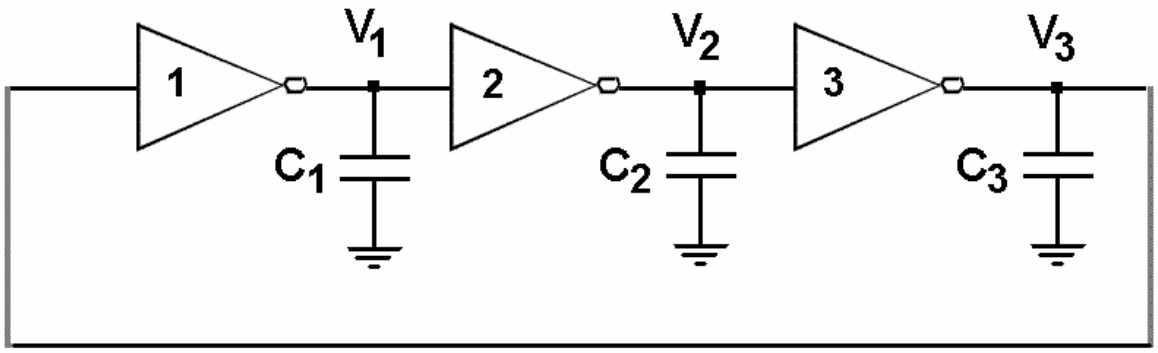
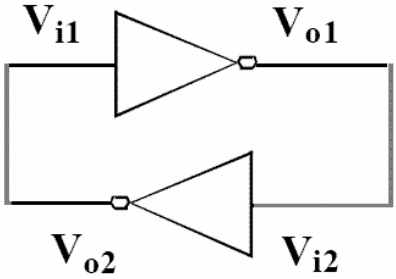

Logic circuits
Combinational
Sequential
Bistable
Monostable
Unstable

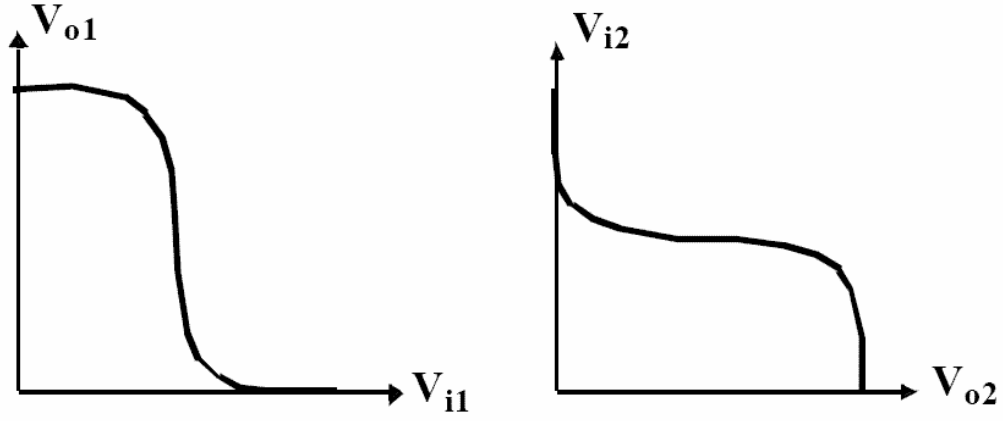

V1
V2
V3
Combinational
logic circuit
Vout1
Vout2
Memory

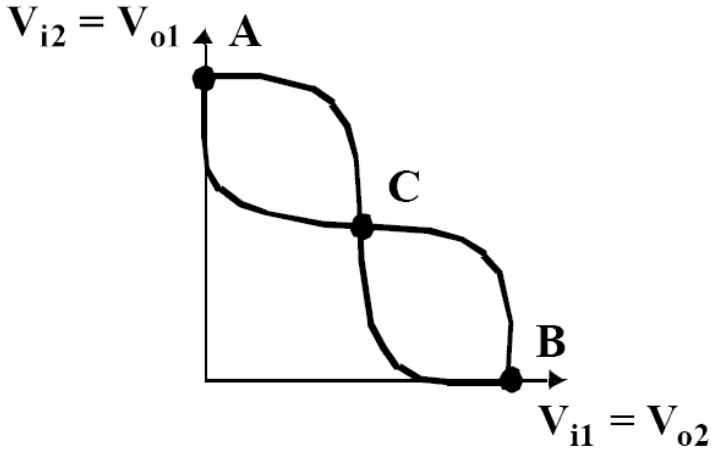
# Unstable circuit – Ring oscillator



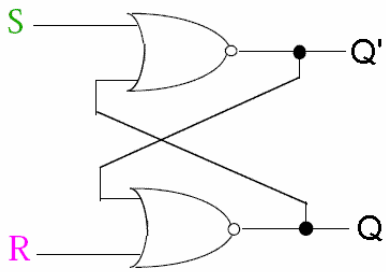

# Bistable circuit



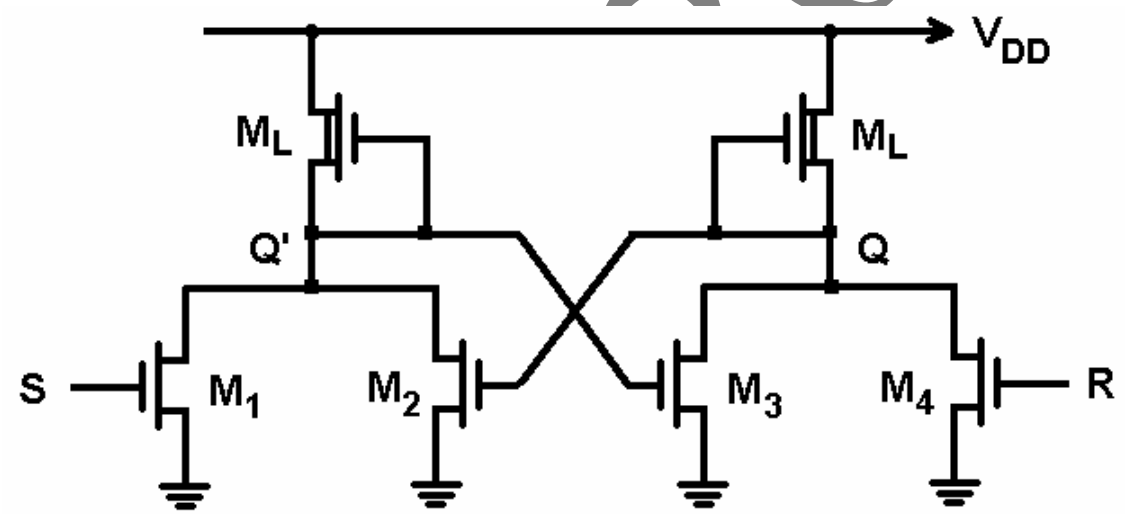



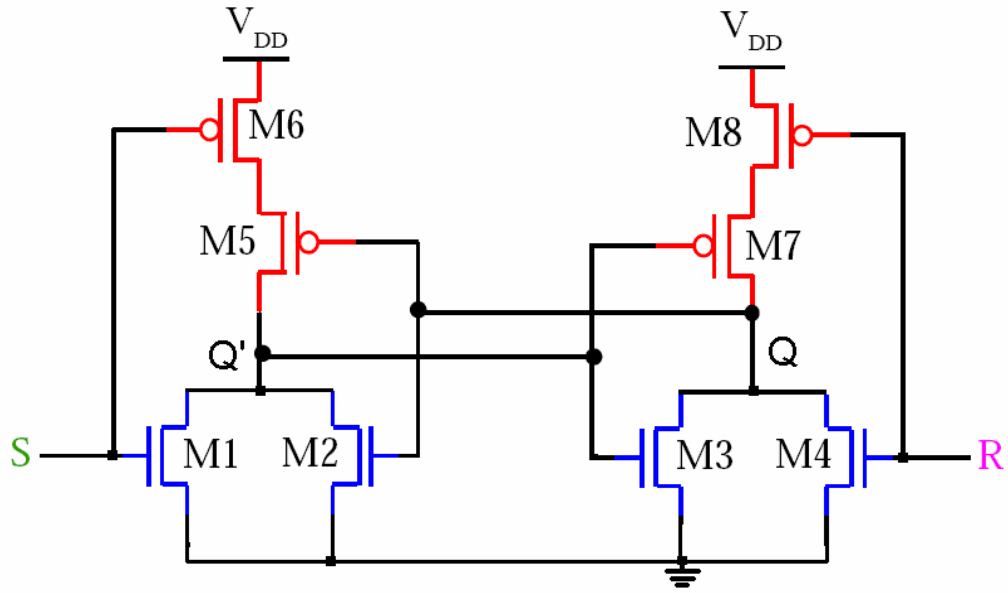
# NOR-based SR flipflop



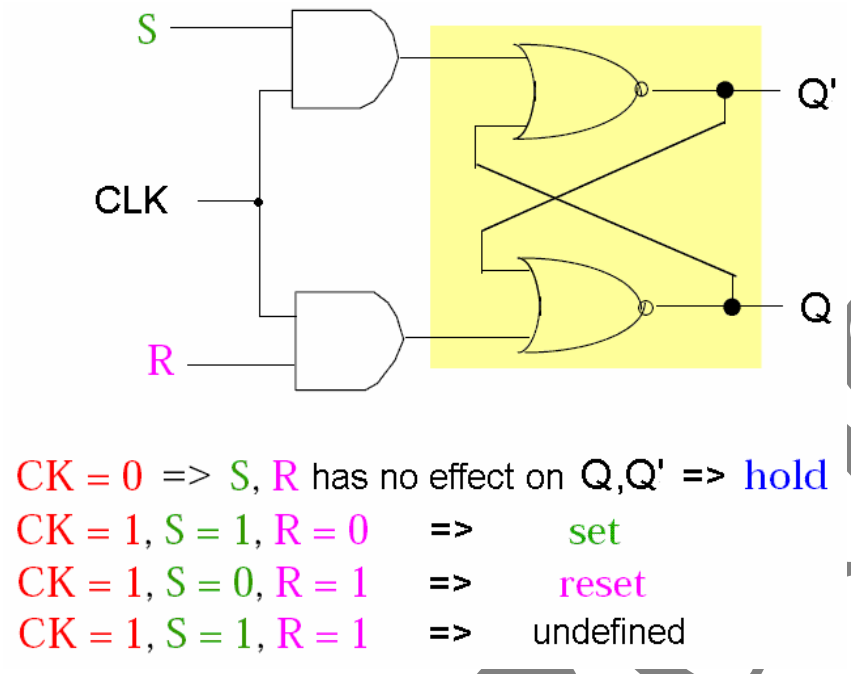


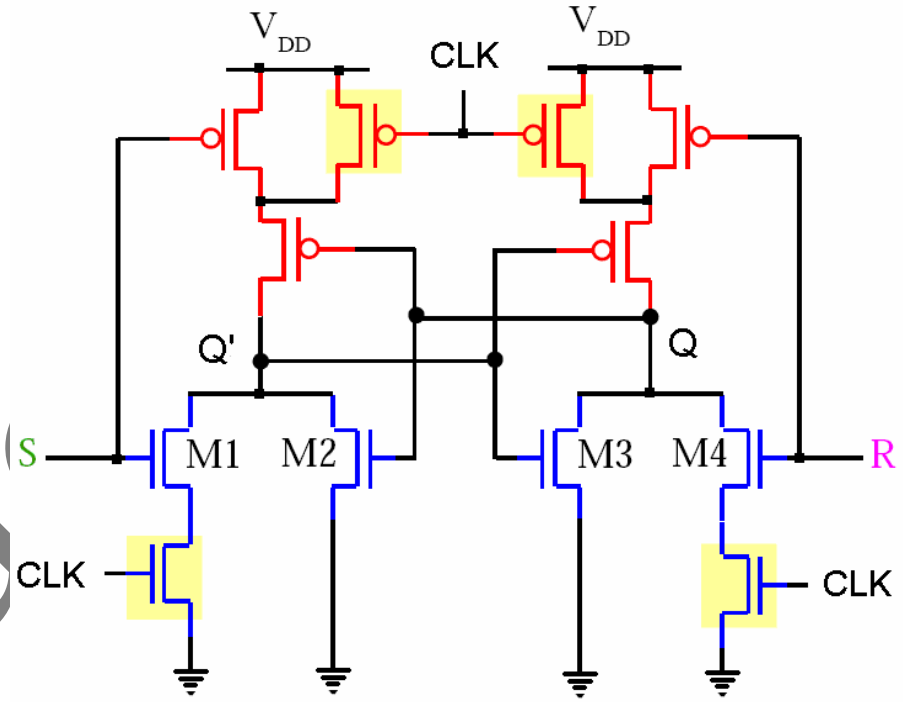
| S | R | $Q_{n+1}$ | $Q'_{n+1}$ | Operation |
|---|---|---|---|---|
| 0 | 0 | $Q_n$ | $Q'_n$ | hold |
| 1 | 0 | 1 | 0 | set |
| 0 | 1 | 0 | 1 | reset |
| 1 | 1 | 0 | 0 | undefined |



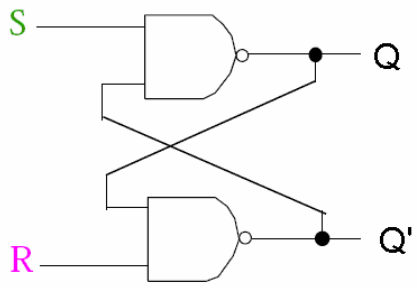



# Clock-triggered SR flipflop



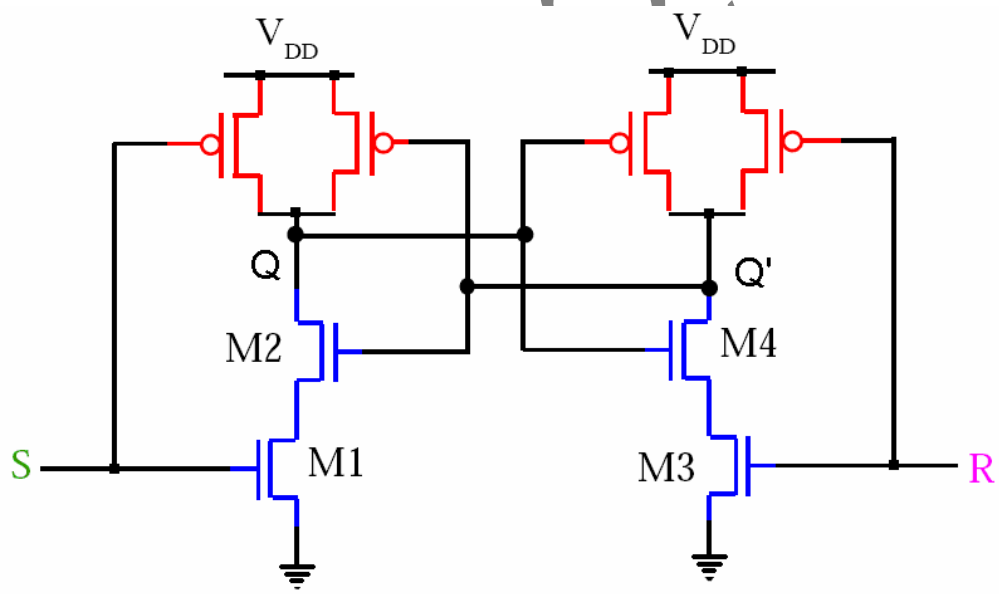



# NAND-based SR flipflop





| S | R | $Q_{n+1}$ | $Q'_{n+1}$ | Operation |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | undefined |
| 0 | 1 | 1 | 0 | set |
| 1 | 0 | 0 | 1 | reset |
| 1 | 1 | $Q_n$ | $Q'_n$ | hold |



# D flip-flop