Digital Electronic Circuits

Homework #4

(…to be returned due **30th April 2009, THURSDAY**)

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Find the logic function corresponding to the **last digit of your student number** below.
☺ (*Happily, it is the same circuit you had designed as **Homework #3**. Isn't it?*) ☺

$\mathbf{Z_0} = [\ (A+B+C)(D+E)F\ ]'$ $\mathbf{Z_1} = [\ AB+(C+D)+EF\ ]'$ $\mathbf{Z_2} = [\ (A+B)(C+D+EF)\ ]'$
$\mathbf{Z_3} = [\ (A+BC)DE+F\ ]'$ $\mathbf{Z_4} = [\ ABC(DE+F)\ ]'$ $\mathbf{Z_5} = [\ (AB+C)(D+E)F\ ]'$
$\mathbf{Z_6} = [\ (A+BCD)(E+F)\ ]'$ $\mathbf{Z_7} = [\ AB+C(D+EF)\ ]'$ $\mathbf{Z_8} = [\ A(BC+DE+F)\ ]'$
$\mathbf{Z_9} = [\ A+BC+DEF\ ]'$

- $\mathbf{V_{DD}=3.3V}$.
- The model parameters for the **MOSFET**s are,

$\mu_n=\mathbf{385}\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, $\mu_p=\mathbf{130}\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ **,** $\mathbf{V_{T0n}=0.52V}$, $\mathbf{V_{T0p}=-0.65V}$
$\mathbf{t_{ox}=7.5}\text{nm}$, $\varepsilon_0=\mathbf{8.85}\text{x}\mathbf{10^{-14}}\text{F/cm}$, $\varepsilon_{ox,r}=\mathbf{3.9}$
(body effect can be neglected)

By taking $\mathbf{W_n=W_p=5\mu m}$ and $\mathbf{L_n=L_p=0.3\mu m}$,

a) Calculate $\mathbf{V_{th}}$ of the **CMOS** gate.

b) Determine the worst-case τ_{PLH} and τ_{PHL} for an equivalent load capacitance of $\mathbf{C_L=0.25pF}$ (*you can neglect the parasitic capacitances of the MOSFETs*).

c) By simulating the circuit (*loaded by $\boldsymbol{C_L=0.25pF}$*) with SPICE, determine $\mathbf{V_{th}}$ and the worst-case τ_{PLH} and τ_{PHL} delays.

SPICE model parameters for the MOSFETs (**GAMMA** is taken **zero** for avoiding body effect)
In the future, normally you should not !..

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.MODEL NM NMOS LEVEL=1 VTO=.7 TOX=7.5E-9 KP=177E-6 UO=385 GAMMA=0
+ PHI=0.7 CGSO=87P CGDO=87P CGBO=27.9P PB=.6 CJ=1.78E-4 MJ=.481
+ CJSW=358P MJSW=.218 LAMBDA=.02

.MODEL PM PMOS LEVEL=1 VTO=-.7 TOX=7.5E-9 KP=59.8E-6 UO=130 GAMMA=0
+ PHI=0.7 CGSO=124P CGDO=.124N CGBO=40.3P PB=.6 CJ=1.83E-4 MJ=.526
+ CJSW=229P MJSW=.172 LAMBDA=.01
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