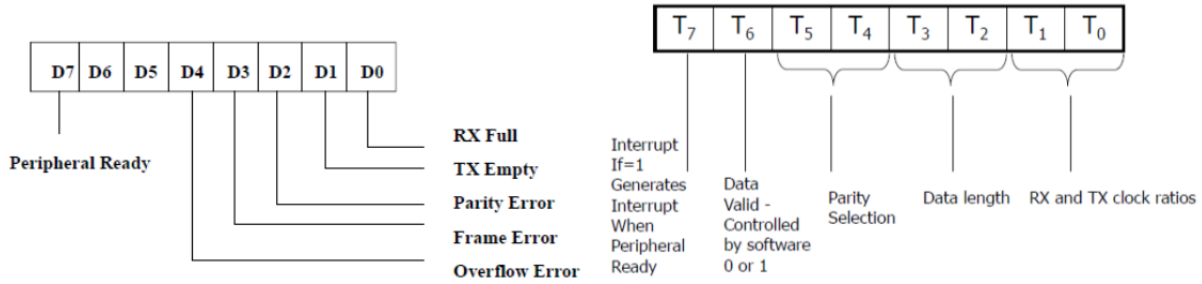
Peripheral Interface Adapter (EDU-PIA) Status/Control Register

D_1D_0	Ready (RDY) Input	Interrupt Output
0 0	1 → 0 => D_7=1	High, No interrupt
0 1	0 → 1 => D_7=1	High, No interrupt
1 0	1 → 0 => D_7=1	Hi->Low->Hi, Interrupt
1 1	0 → 1 => D_7=1	Hi->Low->Hi, Interrupt

D_3D_2	Acknowledge (ACK) Input	Interrupt Output
0 0	1 → 0 => D_6=1	High, No interrupt
0 1	0 → 1 => D_6=1	High, No interrupt
1 0	1 → 0 => D_6=1	Hi->Low->Hi, Interrupt
1 1	0 → 1 => D_6=1	Hi->Low->Hi, Interrupt

D_5 D_4	DATA VALID (DV)
0 0	DV is reset (low)
0 1	DV is set (high)
1 0	1→0→1 after the data is loaded on the port
1 1	0→1→0 after the data is loaded on the port

Asynchronous Communication Interface Adapter (ACIA) Status and Control Registers



T1	T0	Receive and Transmit Clock Ratios
0	0	1/1
0	1	1/2
1	0	1/4
1	1	1/8

T3	T2	Data Length and the Number of Stop Bits
0	0	7 bit data + 1 stop bit
0	1	7 bit data + 2 stop bit
1	0	8 bit data + 1 stop bit
1	1	8 bit data + 2 stop bit

T5	T4	Parity Bit Settings
0	0	No Parity Check
0	1	Odd Parity
1	0	Even Parity
1	1	Invalid