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Computer Engineering Department
Assist. Prof. Feza BUZLUCA
Asist.Prof. Mustafa Ersel KAMAŞAK
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DIGITAL CIRCUITS 2nd MIDTERM SOLUTIONS

SOLUTION 1 (30 Points):

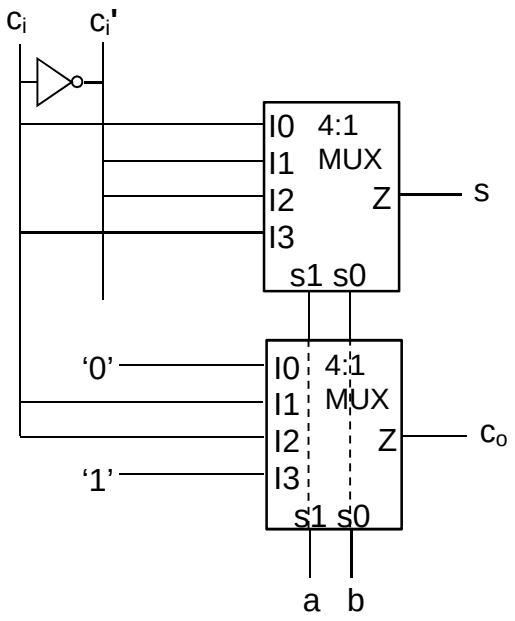
a. (15 Points)

A full adder has two outputs (sum and carry output); therefore we need two multiplexers.

Truth tables of the full adder:

a	b	c_i	s	to MUX
0	0	0	0	c_i
0	0	1	1	
0	1	0	1	c_i'
0	1	1	0	
1	0	0	1	c_i'
1	0	1	0	
1	1	0	0	c_i
1	1	1	1	

a	b	c_i	c_o	to MUX
0	0	0	0	0
0	0	1	0	
0	1	0	0	c_i
0	1	1	1	
1	0	0	0	c_i
1	0	1	1	
1	1	0	1	1
1	1	1	1	

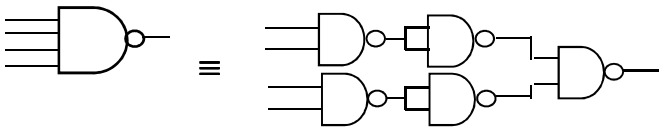


b. A full adder has three inputs; therefore we need a 3:8 decoder.

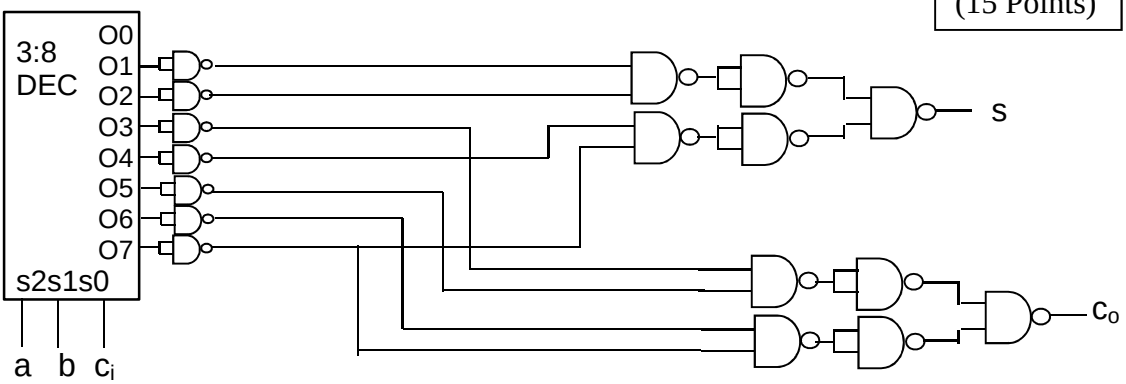
If we had OR gates, we could connect the outputs of the decoder, which correspond to the minterms (1 points) of the function to an OR gate.

Remember: If invert input of an OR gate we obtain a NAND gate.

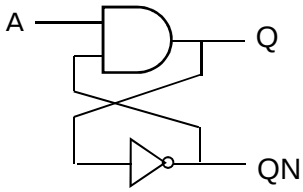
We have only 2-input NAND gates. $\overline{a \cdot b \cdot c \cdot d} = \overline{\overline{(a \cdot b)} \cdot \overline{(c \cdot d)}}$



(15 Points)



SOLUTION 2 (30 Points):



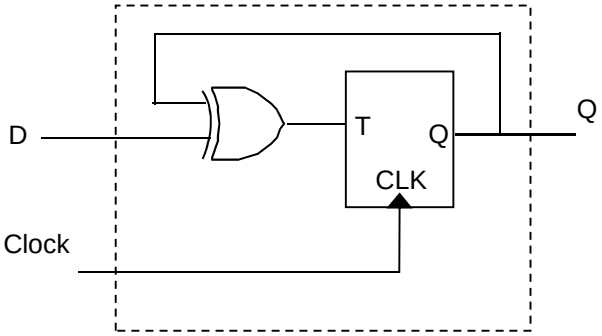
a. (10 Points)
If A=0 then Q=0 (because of AND gate), QN=1 circuit is in a **stable** state.
If becomes 1 (A=1) while QN=1 then Q=1. It makes QN=0 and Q becomes 0 (Q=0), which makes QN=1agin. Now the circuit is in an **unstable** state.
The circuit is not bistable, it is unstable; therefore it **cannot** be used as a memory unit.

b.

i) (10 Points)
We need a D flip-flop

D	Q(t)	Q(t+1)	T must be (To provide the necessary Q(t)→Q(t+1) transition.)
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

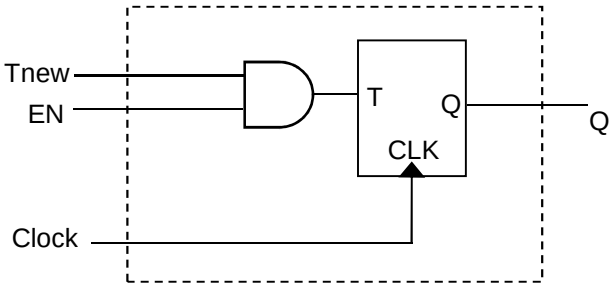
According to the table T=D⊕Q(t)



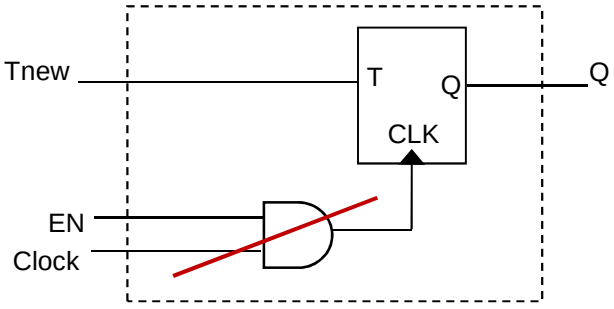
The same result can be obtained by using the equations of the flip-flops.
Q(t+1) = T⊕Q(t)
Q(t+1) = D
T⊕Q(t) = D (apply to both sides: ⊕Q(t))
T = D⊕Q(t)

ii) (10 Points)
A T flip-flop preserves its previous value if T is zero (T=0). So we have to design a new T flip-flop with inputs EN and Tnew, such as
if EN=0 then T=0 and
if EN=1 then T=Tnew.

Only one AND gate is sufficient.



The following circuit has a problem. If clock=1 and EN=0 then CLK=0 and the flip-flop is disabled (it's OK). But if EN becomes 1 while clock=1, flip-flop will get a rising edge on the CLK input and it will process its input Tnew. However the real clock signal is 1. There is not a 0-1 transition on the clock input.



BLG 231E
Question 3

expression: 3pt
minimization: 2pt

a) $J = O_0 + O_2$

$K = O_4 + O_5$

$D = B O_7 + O_6$

$J = \bar{A}\bar{Q}_1\bar{Q}_0 + \bar{A}Q_1\bar{Q}_0 = \bar{A}\bar{Q}_0$ 5pt

$K = A\bar{Q}_1\bar{Q}_0 + A\bar{Q}_1Q_0 = A\bar{Q}_1$ 5pt

$D = BAQ_1Q_0 + AQ_1\bar{Q}_0$

$= AQ_1(B+\bar{Q}_0)$ 5 pt

$Q_0^+ = J\bar{Q}_0 + \bar{K}Q_0$

$= \bar{A}\bar{Q}_0\bar{Q}_0 + (\overline{A\bar{Q}_1})Q_0$

$= \bar{A}\bar{Q}_0 + \bar{A}Q_0 + Q_1Q_0$

$= \bar{A} + Q_1Q_0$ 5pt

$Q_1^+ = D$

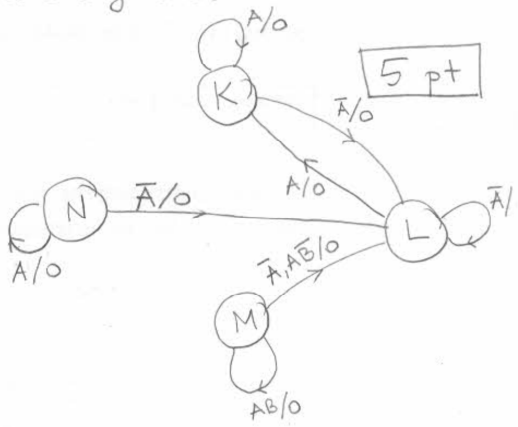
$= AQ_1(B+\bar{Q}_0)$

$Z = JK = \bar{A}\bar{Q}_0 A\bar{Q}_1 = 0$ ← Output is always zero.
5pt

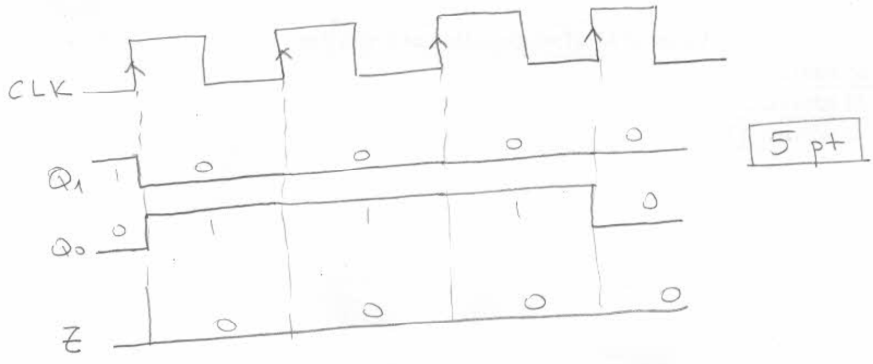
$Q_1^+ Q_0^+ / Z$

Q_1Q_0 \ AB	00	01	11	10
K 00	01/0	01/0	00/0	00/0
L 01	01/0	01/0	00/0	00/0
M 11	01/0	01/0	11/0	01/0
N 10	01/0	01/0	10/0	10/0

5 pt



b) $10 \xrightarrow{01} 01 \xrightarrow{00} 01 \xrightarrow{00} 01 \xrightarrow{11} 00$



5 pt