IMPORTANT: Besides your calculator and the sheets you use for calculations you are only allowed to have an A4 sized "copy sheet" during this exam. Notes, problems and alike are not permitted. Please submit your "copy sheet" along with your solutions. You may get your "copy sheet" back after your solutions have been graded. **Do not forget to write down units!**

ELE222E INTRODUCTION TO ELECTRONICS (20748)
Final Examination 29 May 2008 9.30-11.30
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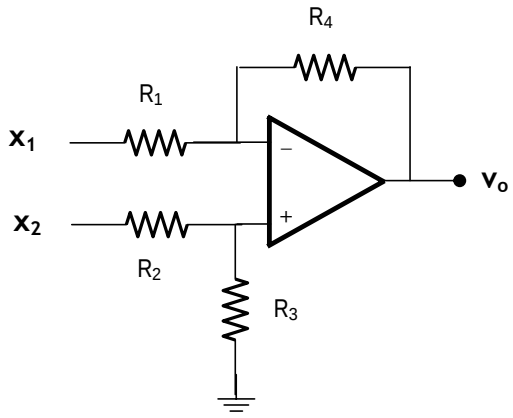
1. Why is a semiconductor diode a one-way conducting device? Explain. (5 points)

2. On a table compare and contrast BJT and MOSFET structures. Compare and contrast at least two properties or characteristics in each category, i.e., similarities and differences between BJT and MOSFET. (10 points)

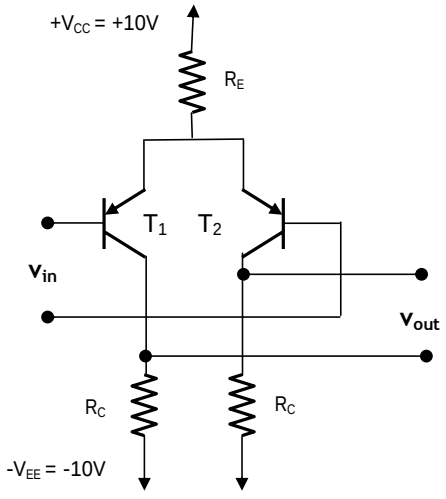
3. Analysis/synthesis:

   a. Analyze the OPAMP circuit shown on the right and express $\mathbf{v_o}$ in terms of the resistors R_1, …, R_4, and inputs x_1 and x_2. (10 points)

   b. Taking advantage of the analysis above, design an OPAMP circuit that will realize the function $v_o = 3x_3 - 2x_2 - 5x_1$. Please use meaningful resistor values. (20 points)



4. Design a differential amplifier stage like the one shown on the right. Select the resistors such that, $I_{C1} = I_{C2} \leq 0{,}5mA$ and $150 \leq |A_d| = \left|\frac{v_{out}}{v_{in}}\right| \leq 200$. Make sure both transistors are in active area using the selected collector resistor values. Calculate the CMRR. (30 points)
   $h_{FE} = h_{fe}$ =100, V_T = 25 mV, $|V_{BE}|$ = 0,6 V, $h_{oe} = h_{re}$ = 0.



5. Using NMOS transistors design a basic current mirror with V_{DD}= 0 V and $-V_{SS}$ = –5 V and I_{REF} = 0,4 mA. Let the two MOS transistors be identical with V_T = 1 V, $\mu_n C_{ox}$ = 20 μA/V^2, V_A = 20 V, W = 40 μm, and L = 10 μm. Find the output resistance and V_{GS}. (25 points)

GOOD LUCK!

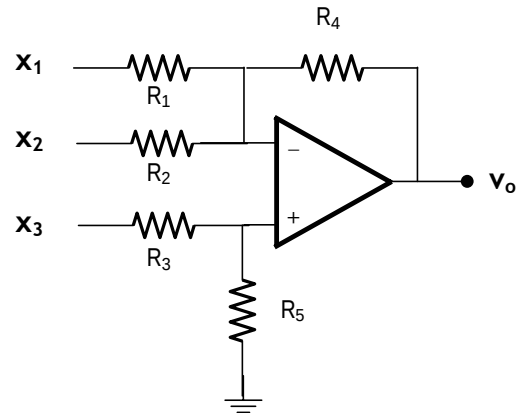
SOLUTIONS:

1. The answer can be found in books.
2. The answer can be found in books.
3. The function realized by the given circuit is found from solving

$\frac{x_1 - v_-}{R_1} = \frac{v_- - v_o}{R_4}$ where $v_- = v_+ = \frac{R_3}{R_2 + R_3} x_2 \rightarrow v_o = -\frac{R_4}{R_1} x_1 + \frac{R_3}{R_2 + R_3} \cdot \left(1 + \frac{R_4}{R_1}\right) x_2$

For example, if $\frac{R_4}{R_1} = \frac{4k}{1k} = 4; \frac{R_3}{R_2 + R_3} = \frac{2k}{2k + 3k} = \frac{2}{5}$ then the circuit realizes the function $v_o = 2x_2 - 4x_1$

In a similar way $v_o = 3x_3 - 2x_2 - 5x_1$ can be realized by the OPAMP circuit below:



Now we have to find the R values:

$\frac{R_4}{R_1} = 5 \Rightarrow \underline{\underline{R_4 = 10k}}, \underline{\underline{R_1 = 2k}}; \frac{R_4}{R_2} = 2 \Rightarrow \underline{\underline{R_2 = 5k}}$

$\frac{R_5}{R_3 + R_5}\left(1 + \frac{R_4}{R_1} + \frac{R_4}{R_2}\right) = \frac{R_5}{R_3 + R_5}(1 + 5 + 2) = 3 \Rightarrow \frac{R_5}{R_3 + R_5} = \frac{3}{8} \Rightarrow \underline{\underline{R_5 = 3k}}, \underline{\underline{R_3 = 5k}}$

4. <u>First DC analysis:</u>

$I_{C1} = I_{C2} = \frac{h_{FE}}{h_{FE} + 1}\left[\frac{V_{CC} - V_{EB1}}{2R_E}\right] = \frac{100}{101} \cdot \frac{10V - 0{,}6V}{2R_E} \le 0{,}5mA$

Let's take $I_{C1} = I_{C2} = \frac{100}{101} \cdot \frac{10V - 0{,}6V}{2R_E} = 0{,}5mA \Rightarrow \underline{\underline{R_E = 9k3}} \rightarrow r_{e1} = r_{e2} = \frac{25mV}{0{,}5mA} = \underline{\underline{50\Omega}}$

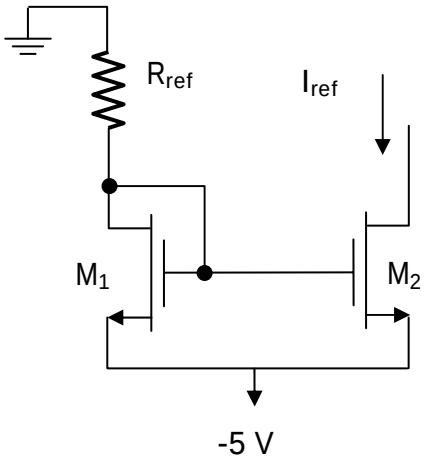
Let's take $|A_d| = \left|\frac{v_{out}}{v_{in}}\right| = 200 \Rightarrow \frac{v_{out}}{v_{in}} = -\frac{R_C}{r_e} = -200 \Rightarrow R_C = 200 * r_e = \underline{\underline{10k}}$.

Let's see whether both T_1 and T_2 will be in the active area at DC:

$V_{BC1} = V_{BC2} = -10V + R_C I_C = -10V + 10k * 0{,}5mA = -5V$. Since the bases are at ground, there is large enough voltage difference between B and C of both transistors. Both BC junctions are reverse biased. T_1 and T_2 are both active.

$$CMRR = 20 \cdot \log\left|\frac{2R_E + r_e}{r_e}\right| = 20 \cdot \log\left|\frac{2*9k3 + 50}{50}\right| = \underline{\underline{51{,}4[dB]}}$$

5. My design looks like this:



We know for sure M_1 is in saturation because its Gate and Drain are shorted. For M_1:

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[V_{GS} - V_{th}\right]^2 \Rightarrow V_{GS} = V_{th} \pm \sqrt{\frac{I_D}{\frac{\mu_n C_{ox}}{2}\frac{W}{L}}} = 1V \pm \sqrt{\frac{0{,}4mA}{40\mu A/V^2}} = \begin{cases} 1 + 3{,}16V \\ 1 - 3{,}16V \end{cases}.$$

Since for channel creation in NMOS $V_{GS} \geq V_T \Rightarrow V_{GS} = \underline{\underline{4{,}16V}}$. As both M_1 and M_2 are identical and they have the same V_{GS}, they are both in saturation. To find the resistor value,

$$I_D = I_{ref} = \frac{V_{DD} - V_{SS} - V_{GS}}{R_{ref}} \Rightarrow R_{ref} = \frac{V_{DD} - V_{SS} - V_{GS}}{I_D} = \frac{0 - (-5V) - 4{,}16V}{0{,}4mA} = \underline{\underline{2k1}}$$

Finally the output resistance is

$$r_o = \frac{V_A}{I_D} = \frac{20V}{0{,}4mA} = \underline{\underline{50k}}$$