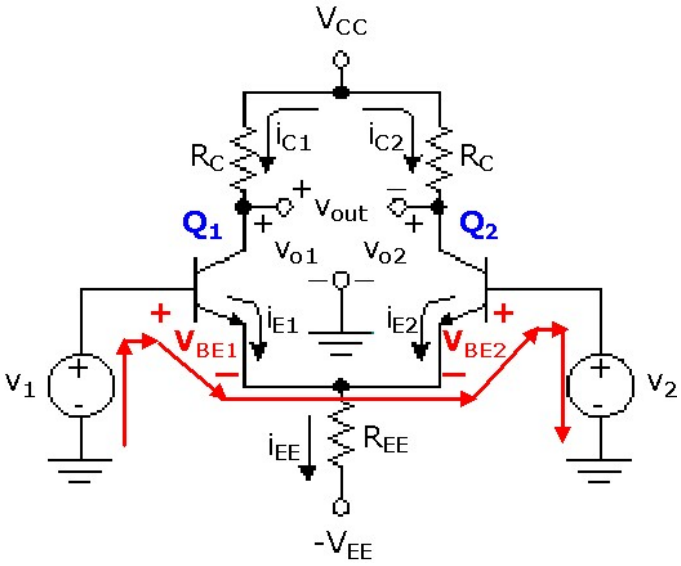
Section G3: Differential Amplifiers

The differential amplifier may be implemented using BJTs or FETs and is a commonly used building block in analog IC design. We are going to be concentrating on the BJT implementation of the **differential pair** as emitter-coupled, common-emitter (or emitter-resistor) amplifiers. In addition to providing the input stage of the operational amplifier, this configuration is the foundation for emitter-coupled logic (ECL), a very high speed, universally employed family of logic circuits.

The simplest form of the differential amplifier is shown to the right (a modified version of Figure 9.1 in your text). This circuit is formed using two matched transistors (Q_1 and Q_2), in the CE configuration whose emitters have been tied together. The differential pair has two inputs (v_1 and v_2), and three possible outputs (v_{o1}, v_{o2}, and v_{out}).



A couple of notes about this circuit:

- The output voltage, v_{out}, is the difference between v_{o1} and v_{o2}, or $v_{out} = v_{o1} - v_{o2}$.
- The notation of the emitter resistor R_E has been changed to R_{EE} since is common to both amplifiers. As we will see shortly, this resistor may be the equivalent resistance of a current source as discussed in the previous section, both to save chip space and reduce fabrication complexity (transistors are smaller than resistors and it's easier to make a whole bunch of the same thing). However it is created, it is necessary that R_{EE} have a large value to keep the voltage drop across it nearly constant with reasonable changes in current.
- The resistors R_C in the circuit above may be replaced with other transistors in some applications (once again, to remove the requirement of resistive components). It is absolutely imperative however, that whatever is in the collector circuit ensures that Q_1 and Q_2 never enter saturation.

To solve for the dc transfer characteristics of the differential amplifier, we begin by using the expression for base-emitter voltage derived from

Equation 4.10. In terms of total instantaneous voltage and collector current, v_{BE} and i_C, we now have

$$v_{BE} = V_T \ln\left(\frac{i_C}{I_O}\right),$$

where I_o is the reverse saturation current and we have once again assumed that n=1. Using this relationship, and **neglecting base currents** so that $i_E \approx i_C$, we can express v_{BE1} and v_{BE2} as

$$v_{BE1} = V_T \ln\left(\frac{i_{E1}}{I_O}\right); \quad v_{BE2} = V_T \ln\left(\frac{i_{E2}}{I_O}\right). \qquad \text{(Equation 9.2, Corrected)}$$

Now, writing the KVL equation about the base junction loop as indicated by the red path in the figure above, we have

$$v_1 - v_{BE1} + v_{BE2} - v_2 = 0. \qquad \text{(Equation 9.1, Modified)}$$

Assuming we have **matched devices**, V_T and I_O are the same for Q_1 and Q_2. Substituting the information of Equation 9.2 into Equation 9.1, rearranging and employing the property of logarithms [ln(A)-ln(B)=ln(A/B)],

$$v_1 - V_T \ln\left(\frac{i_{E1}}{I_O}\right) + V_T \ln\left(\frac{i_{E2}}{I_O}\right) - v_2 = 0;$$

$$\frac{v_1 - v_2}{V_T} = \ln\left(\frac{i_{E1}}{I_O}\right) - \ln\left(\frac{i_{E2}}{I_O}\right) = \ln\left(\frac{i_{E1}/I_O}{i_{E2}/I_O}\right). \qquad \text{(Equation 9.3, Modified)}$$

$$\frac{v_1 - v_2}{V_T} = \ln\left(\frac{i_{E1}}{i_{E2}}\right)$$

Taking the exponential of both sides of the last equation above, we can solve for the current ratio, i_{E1}/i_{E2}:

$$\frac{i_{E1}}{i_{E2}} = e^{\left(\frac{v_1 - v_2}{V_T}\right)}; \text{ or}$$

$$i_{E1} = i_{E2} e^{\left(\frac{v_1 - v_2}{V_T}\right)} \text{ and } i_{E2} = i_{E1} e^{\left(\frac{-(v_1 - v_2)}{V_T}\right)}. \qquad \text{(Equation 9.4, Modified)}$$

A KCL at the coupled emitters of Q_1 and Q_2 yields

$$i_{EE} = i_{E1} + i_{E2}. \qquad \text{(Equation 9.5)}$$

Substituting the information from the modified version of Equation 9.4 into Equation 9.5, we can find final expressions for i_{E1} and i_{E2} in terms of circuit and physical parameters. Note that in the equations below, $i_{E1} \approx i_{C1}$ and $i_{E2} \approx i_{C2}$. Recall however that the emitter and collector currents are actually related by $i_C = \alpha i_E$, where $\alpha = \beta/(\beta+1) \approx 1$ for $\beta >> 1$.

$$\begin{aligned} i_{E1} \cong i_{C1} &= \frac{i_{EE}}{1 + \exp\left[-(v_1 - v_2)/V_T\right]} \\ i_{E2} \cong i_{C2} &= \frac{i_{EE}}{1 + \exp\left[(v_1 - v_2)/V_T\right]} \end{aligned}. \qquad \text{(Equation 9.6)}$$

Let's look at what the results of Equation 9.6 tell us.

- For a given current i_{EE}, the amplifier responds only to the difference between the voltages applied to the bases of Q_1 and Q_2 (i.e., v_1 and v_2 in Figure 9.1 and in the equations above). This is the foundation of differential amplifier operation (and is where the name comes from).
- If $v_1 = v_2 = v_{ci}$ (we'll talk about the v_{ci} and v_{di} notation in a couple of minutes), $i_{E1} = i_{E2} = i_{EE}/2$ and the current is split evenly between the two transistors for any value of common-mode voltage, v_{Ci}.
- If the differential voltage, $v_{di} = v_1 - v_2$, becomes greater than about $4V_T$ ($\approx$100mV), the current i_{EE} will flow almost entirely in one of the two transistors. Specifically,
  - if v_{di} >100mV, approximately 98% of i_{EE} will flow through Q_1 and Q_2 will be essentially cut off, or
  - if v_{di} <-100mV, approximately 98% of i_{EE} will flow through Q_2 and Q_1 will be essentially cut off.

  NOTE: The $4V_T$ figure comes from the intersection of plots of the emitter currents of the two transistors or by solving the expressions of Equation 9.6.

Linear amplification using the differential pair is only possible for small differential voltages. Generally, inputs of on the order of V_T (approximately 20mV) are used as a guideline to ensure linear behaviors, but your author states that a difference of less than 100mV is an adequate restriction. Note that, for the simple common-emitter configurations, 100mV may be too large (other sources cite a limit in the range of $V_T/2$). However, to increase the range of linear operation, small emitter resistors may be added – this is probably where your author gets his limit.

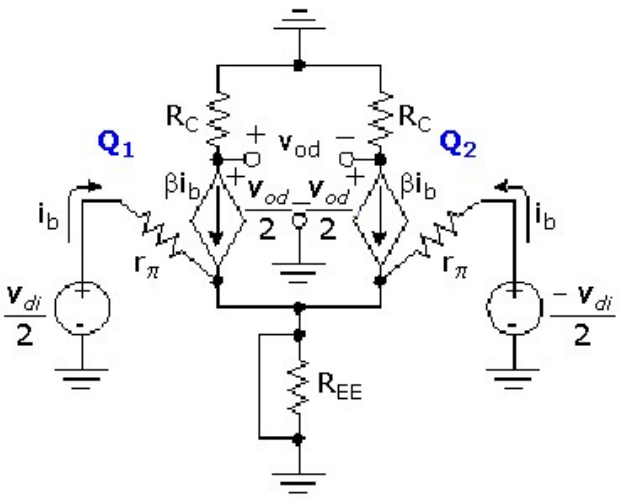
I am going to take a slightly different approach that your author in the next segment of this discussion, but I will attempt to keep all notations the same. Note that in all of the following analyses we will assume that r_o is very large so that it may be neglected unless specifically stated otherwise.

Differential Mode Gain

For differential-mode operation, we apply an ac differential voltage, v_{di}, between the bases of Q_1 and Q_2, in addition to a dc common mode voltage v_{Ci}. From the symmetry of the differential pair, this differential input signal should divide evenly between the base emitter junctions of the two transistors. In terms of the differential and common-mode voltages, the original input voltages of Figure 9.1 may be expressed as

$$v_1 = v_{Ci} + \frac{v_{di}}{2} \text{ and } v_2 = v_{Ci} - \frac{v_{di}}{2}. \qquad \text{(Equation 9.9, Modified)}$$

Note that v_1-v_2=v_{di}, which is what we want. This is true since the input to Q_2 is equal in magnitude to that of Q_1, but 180° out of phase (indicated by the negative sign). The small signal model of the differential amplifier in differential mode is illustrated in Figure 9.2a and is reproduced to the right. Using the symmetry of the differential pair and comparing the notation of this circuit with Figure 9.1, we have v_{out}=v_{od} and $|v_{o1}|=|v_{o2}|=v_{od}/2$. Note that although v_{o1} and v_{o2} are of equal magnitude, they are 180° out of phase (i.e., $v_{o1}=-v_{o2}$).



Modifying Equation 9.6 to reflect the differential input voltage v_{di},

$$i_{E1} \cong i_{C1} = \frac{i_{EE}}{1 + \exp[-v_{di}/V_T]}$$

$$i_{E2} \cong i_{C2} = \frac{i_{EE}}{1 + \exp[v_{di}/V_T]}$$

Analyzing the above relationships, we can see that as the current one transistor increases, the current through the other transistor decreases at the same rate. Therefore, since the total current through R_{EE} never changes,

the voltage change across R_{EE} is zero. This means that the ac signal voltage across R_{EE} is zero and the resistor may be replaced with a short circuit in the ac equivalent, as shown in the above figure.

If the transistors are biased at an emitter current of $i_{EE}/2$, and with R_{EE} effectively shorted for ac operation, another way of looking at the current increase/decrease may be developed in terms of r_π, where $r_\pi=\beta r_e$, assuming $\beta>>1$. A KVL in either base loop yields

$$\frac{v_{di}}{2} = i_b r_\pi = i_b \beta r_e = i_e r_e .$$

Solving for i_e, we get an expression for the current increase/decrease to be $i_e = \frac{v_{di}}{2r_e}$. Assuming $i_C \approx i_E$, the output at each collector terminal will be 180^o out of phase with a magnitude of

$$| v_{o1} | = | v_{o2} | = \frac{v_{od}}{2} = \frac{v_{di} R_C}{2r_e} = \frac{g_m R_C v_{di}}{2},$$

or, the voltage measured between the two collector terminals will be

$$v_{od} = \frac{v_{di} R_C}{r_e} = g_m R_C v_{di} .$$

As indicated above, the output of the differential amplifier may be taken either **differentially (or double-ended)**, where the output is taken between the two collectors, or **single-ended**, where the output is taken from either collector to ground.

If the output is taken between the collector terminals, the **differential gain (differential, or double-ended output)** of the amplifier will be equal to

$$A_d = -g_m R_C = \frac{-R_C}{r_e} . \qquad \text{(Equation 9.12)}$$

As stated earlier, the single-ended output voltages at v_{o1} and v_{o2} are of equal magnitude, and are each one-half the magnitude of the double-ended output voltage, v_{od}. If the output is taken between either collector terminal and ground, the **differential gain (single-ended output)** of the amplifier will be equal to one-half of the gain calculated for the double-ended output, or

$$A_d = \frac{-R_C}{2r_e}. \qquad \text{(Equation 9.11)}$$

If the differential amplifier has resistors in the individual emitter legs, the **double-ended differential gain** is

$$A_d = \frac{-R_C}{r_e + R_E},$$

which should be expected, because we now have coupled emitter-resistor (ER) amplifiers.

The **input resistance** in differential mode is the equivalent resistance seen between the two bases. If there is no resistor in the emitter legs of the circuits, and R_{EE} is effectively shorted, we can see from Figure 9.2a that the input resistance will be

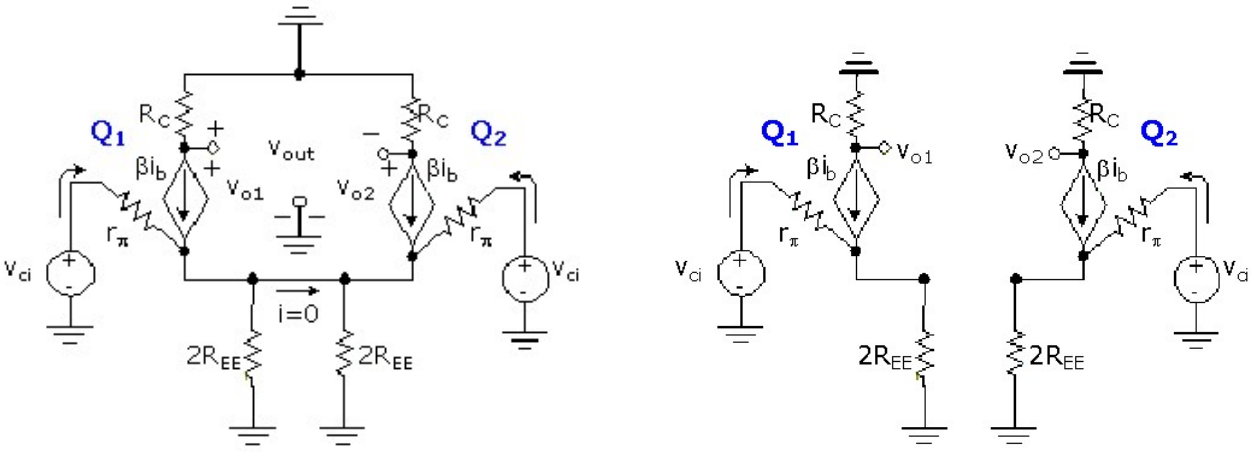
$$R_{in}(\textit{differential mode}) = 2r_\pi. \qquad \text{(Equation 9.16)}$$

For the coupled ER configuration (i.e., with R_Es in the emitter leads), we can employ the impedance reflection rule to express the input resistance as

$$R_{in}(\textit{differential mode}) = 2r_\pi + 2(\beta + 1)R_E = 2(\beta + 1)(r_e + R_E).$$

Common Mode Gain

The mid-frequency ac small signal model for common mode operation is given in Figure 9.2b and is reproduced below and to the left. A simplified version of this small signal model is given below and to the right. Note that the common mode circuit may be split into a pair of parallel circuits, called the **common-mode half-circuit**, with $i_E = i_{EE}/2$ and with an emitter resistor of $2R_{EE}$ (recall that $2R_{EE} || 2R_{EE} = R_{EE}$, so we haven't changed the original circuit of Figure 9.1).



The input to each half circuit is of the same magnitude and phase. If the transistors are matched, the circuit is perfectly symmetric, and we assume that $2R_{EE} >> r_e$, we may derive the **single-ended common-mode gain**, using either half circuit, to be

$$A_C = \frac{-R_C}{2R_{EE}}. \qquad \text{(Equation 9.13)}$$

Ideally, the **differential (double-ended) common-mode gain** is zero since $v_1 - v_2 = v_{ci} - v_{ci} = 0$ (and the circuit is perfectly symmetric). Practically, however, circuits are not perfectly symmetric and devices cannot be perfectly matched. This means that the common-mode gain will not be zero for a differential output. The double-ended output voltage may then be expressed in terms of the common-mode and differential-mode gains as follows:

$$v_{out} = A_d v_{di} + A_c v_{ci} = A_d (v_1 - v_2) + A_c \left(\frac{v_1 + v_2}{2} \right). \qquad \text{(Equation 9.14)}$$

Even if some discrepancy from ideal exists in the differential amplifier circuit, the double-ended common-mode gain is much smaller than that for the single-ended output. Therefore, the input stage of a multistage amplifier (an op-amp for example) is usually a balanced differential pair with the output taken differentially (double-ended). This means that the differential amplifier stage will have a low common-mode gain, which we will see below is a desirable quality in terms of the common-mode rejection ratio (the next part talks about the CMRR, hold on).

The common-mode input resistance is found using the amplifier of Figure 9.2b (the complete small signal model to the left above). The equivalent resistance seen by the common-mode sources is calculated by reflecting R_{EE} ($=2R_{EE}||2R_{EE}$) up into the base circuit, and is given by

$$R_{in}(common\ \ mode) = 2r_{\pi} + 2(\beta + 1)R_{EE} \cong 2\beta R_{EE}\ ,\text{(Equation 9.17, Modified)}$$

where the final simplification is made by assuming $\beta >> 1$ and $R_{EE} >> r_e$. Note that the term βR_{EE} may become very large. If this occurs, the transistor output resistance may no longer be neglected in a parallel relationship (i.e., r_o is not much larger than βR_{EE}) and the common mode input resistance becomes

$$R_{in}(common\ \ mode) = \beta\left(R_{EE}\ ||\ \frac{r_o}{2}\right).$$

As usual, if the assumption $\beta >> 1$ does not hold, all β terms become $\beta+1$. Note that the input resistance for common-mode operation is much larger than that for differential-mode operation.

Common-Mode Rejection Ratio (CMRR)

An effective differential pair will react primarily to the difference between the input voltages and the differential-mode gain will be much larger than the common-mode gain. A figure of merit for the differential amplifier is called the **common-mode rejection ratio**, or **CMRR**. The CMRR is defined as the ratio of the differential-mode gain to the common-mode gain. Using the expressions defined for single-ended outputs, the CMRR is given by

$$CMRR = \left|\frac{A_d}{A_c}\right| = \left|\frac{-R_C\ /\ 2r_e}{-R_C\ /\ 2R_{EE}}\right| = \frac{R_{EE}}{r_e} = g_m R_{EE}\,.$$

Normally, the CMRR is expressed in dB as

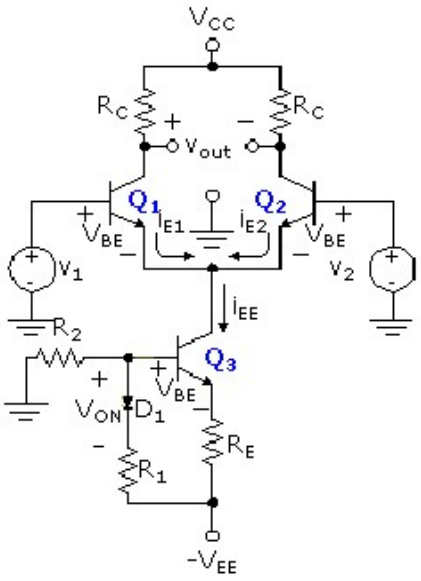
$$CMRR = 20\log\left(\frac{R_{EE}}{r_e}\right) = 20\log(g_m R_{EE})\,. \qquad \text{(Equation 9.15)}$$

Differential Amplifier with Constant Current Source

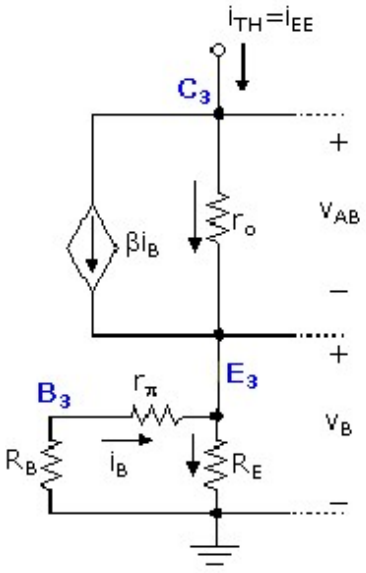
For an ideal differential amplifier, the differential common-mode gain would be zero and the CMRR would be infinite. Since this is not practical, one way

to increase the CMRR is to make R_{EE} as large as possible. The fabrication of large resistances on an IC is not practical, so an alternate approach involves replacing R_{EE} with a transistor configured as a dc current source. The closer the current source behaves to an ideal current source, the higher the common-mode rejection ratio (recall that an ideal current source has infinite impedance).

The circuit of Figure 9.3a (reproduced to the right) is an example of a **differential amplifier with a diode-compensated fixed-bias current source**. The diode compensation makes the circuit operation less dependent on temperature variations (see Section D10 for a discussion of diode compensation in BJT circuits). The diode D_1 and transistor Q_3 are selected so that they have nearly identical characteristics over the range of operating temperatures. *Just for fun – realize that D_1 may be another BJT that is matched to Q_3 and is diode-connected (its collector is tied to its base). Also, any of the current sources we discussed in the previous section may be used to create the constant current source used for biasing purposes.*



To analyze the circuit of Figure 9.3a and determine the CMRR, we need to calculate the equivalent resistance of the constant current source circuit (called R_{TH} by your author). A modified version of Figure 9.3b is presented to the right and will be used for this analysis. ***Note that I have changed the designations of the nodes and voltages across r_o and R_E since the v_1 and v_2 in Figure 9.3b of your text are not the same as indicated in Figure 9.3a. Also, the i_{TH} of Figure 9.3b is the same current as i_{EE} in Figure 9.3a (i.e., the collector current of Q_3).*** With all this in mind, the circuit to the right is the small signal equivalent of the current source (with the base, collector and emitter of Q_3 noted by B_3, C_3 and E_3, respectively) if the diode is assumed to be ideal and $\beta>>1$. Since it is expected that the equivalent resistance of this current source will be large, we must also include the output resistance, r_o, in our analysis. Finally, by assuming an ideal diode, R_B is our old friend $R_1||R_2$.



The equivalent resistance of the constant current source circuit is given by

$$R_{TH} = \frac{v_{AB} + v_B}{i_{TH}}. \qquad \text{(Equation 9.18, Modified)}$$

Writing a KCL equation at node **C_3**, we have

$$i_{TH} = \beta i_b + \frac{v_{AB}}{r_o}, \qquad \text{(Equation 9.20, Modified)}$$

while a KCL equation at node **E_3** yields

$$\beta i_B + \frac{v_{AB}}{r_o} + i_B - \frac{v_B}{R_E} = 0. \qquad \text{(Equation 9.21, Modified)}$$

Expressing the voltages in terms of the currents i_B and i_{TH}, we have

$$\begin{aligned} v_{AB} &= (i_{TH} - \beta i_B) r_o \\ v_B &= -i_B (r_\pi + R_B) \end{aligned}. \qquad \text{(Equation 9.22, Modified)}$$

I'm not going to go through all the algebra here, but if you substitute Equation 9.22 into 9.21, and solve for i_{TH}, then substitute this result (along with Equation 9.22) into Equation 9.18, you get an expression for R_{TH} to be

$$R_{TH} = \frac{r_\pi + R_B + r_o\left[1 + (r_\pi + R_B)/R_E\right] + \beta r_o}{1 + (r_\pi + R_B)/R_E}. \qquad \text{(Equation 9.24)}$$

To simplify this nasty looking expression, your author makes a series of assumptions:

- To maintain bias stability, we use $R_B = 0.1\beta R_E$.
- $\beta >> 1$, so that $1 >> 1/\beta$
- $r_o >> R_E$
- $0.1R_E >> r_e$

Putting all this into Equation 9.24 yields the incredibly simple result

$$R_{TH} \approx 11 r_o, \qquad \text{(Equation 9.31)}$$

where $r_o = V_A/I_C$. Note that ***all*** of the above approximations must be valid for Equation 9.31 to be used. If it can be, life is good, R_{TH} is independent of β and is huge!

Differential Amplifier with Single-Ended Input and Output

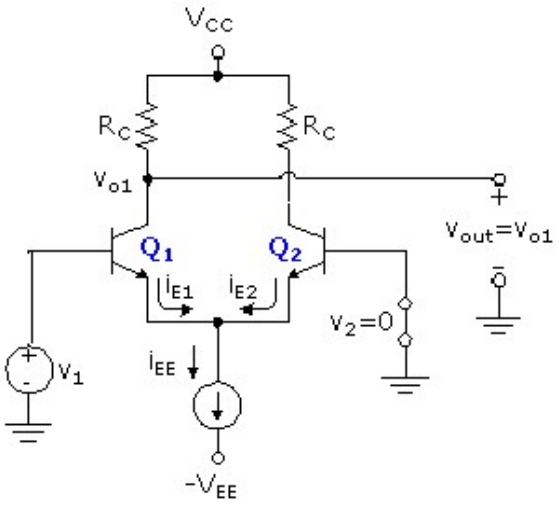


Figure 9.4 (given to the right) illustrates a differential amplifier where the input to Q_2 is grounded and the output is taken as v_{o1}. As discussed in the previous section, a constant current source is used in place of R_{EE}. This configuration is known as a **single-ended input and output amplifier with phase reversal**. To analyze this amplifier, all we have to do is set v_2=0 in the earlier equations. If we assume that the equivalent resistance of the current source is very large, the common-mode gain is approximately equal to zero. This means the single-ended differential-mode gain of the amplifier will determine the output, which will be

$$v_{out} = A_d v_{di} = \frac{-R_C v_1}{2r_e}. \qquad \text{(Equation 9.33)}$$

The negative sign indicates that there is a 180° phase shift between the input (v_1) and the output (v_{o1}), as expected for a common emitter amplifier. If a phase reversal is not desired for a single-ended output that is referenced to ground, the output can be taken from Q_2.