3. Consider the circuit of Figure 6.1.

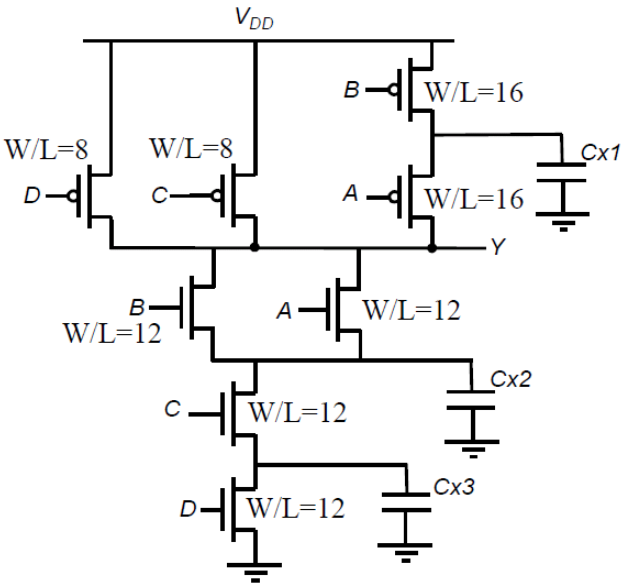

Figure 6.1 CMOS combinational logic gate.

a. What is the logic function implemented by the CMOS transistor network? Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS $W/L = 4$ and PMOS $W/L = 8$.

Solution

The logic function is : $Y = \overline{(A + B)CD}$. The transistor sizes are given in the figure above.

b. What are the input patterns that give the worst case t_{pHL} and t_{pLH}. State clearly what are the initial input patterns and which input(s) has to make a transition in order to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes.

Solution

The worst case t_{pHL} happens when the internal node capacitances (*Cx2* and *Cx3*) are charged before the high to low transition. The initial states that can cause this are: ABCD=[1010, 1110, 0110]. The final state is one of: ABCD=[1011, 0111].

The worst case t_{pLH} happens when *Cx1* is charged before the low to high transition. The input pattern that can cause this is: ABCD=[0111] =>[0011].

c. Verify part (b) with SPICE. Assume all transistors have minimum gate length (0.25μm).

Solution

The two cases are shown below.

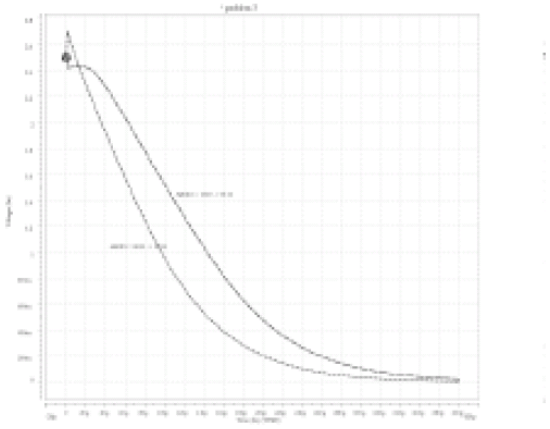

Figure 6.2 Best and worst t_{pHL}.

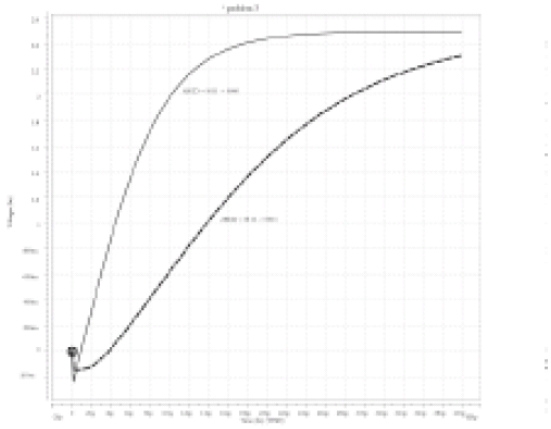

Figure 6.3 Best and worst t_{pLH}.

d. If P(A=1)=0.5, P(B=1)=0.2, P(C=1)=0.3 and P(D=1)=1, determine the power dissipation in the logic gate. Assume V_{DD}=2.5V, C_{out}=30fF and f_{clk}=250MHz.

Solution

Since D is always 1, the circuit implements the following function $Y = \overline{(A+B)C}$.

$P_{(A+B)=1} = P_{A=0}.P_B = 0 = 0.5*(1-0.2) = 0.4$,

$P_{(A+B)=0} = 1 - 0.4 = 0.6$,

$P_{Y=0} = P_{(A+B)=1}.P_C = 1 = 0.6*0.3 = 0.18$

$P_{Y=1} = 1 - 0.18 = 0.82$

$P_{Y=0=>1} = 0.18*0.82 = 0.1476$

So $Pdyn = P_{Y=0=>1} C_{out} V_{DD}^2 f_{clk} = (0.1476)(30.10^{-15})(2.5^2)(250.10^6) = 6.92\,\mu$ W.

7. [E, None, 4.2] Compute the following for the pseudo-NMOS inverter shown in Figure 6.6:

a. V_{OL} and V_{OH}

Solution

To find V_{OH}, set V_{in} to 0, because V_{OL} is likely to be below V_{T0} for the NMOS. If V_{in}=0, then M_1 is off, so the PMOS pulls the output all the way to the rail. So, V_{OH}=V_{DD}=2.5V.

To find V_{OL}, set V_{in} = V_{OH} = 2.5V. The NMOS is all the way on, but so is the PMOS. To find V_{OL}, we can write a current balancing equation at the output node: I_{DP}+I_{DN}=0. First, we must determine the region of operation for each device. We can assume that V_{DS} = V_{OL} for the NMOS is less than V_{DSAT}, so the NMOS is in the linear region. V_{DS} for the PMOS will be more negative than V_{DSAT}, and V_{GTp} = -2.1, so the PMOS is velocity saturated. The equation is therefore:

$$k'_p \cdot \frac{W}{L} \cdot V_{DSAT} \cdot (V_{GT} - 0.5V_{DSAT}) \cdot (1 + \lambda V_{DS}) + k'_n \cdot \frac{W}{L} \cdot V_o \cdot (V_{GT} - 0.5V_o) \cdot (1 + \lambda V_o) = 0$$

Plugging in numbers (process parameters such as V_{DSAT} appear in tables in previous chapters) gives:

$$-30 \cdot 2 \cdot -1 \cdot (-1.6) \cdot (1 - 0.1(V_o - 2.5)) + 115(16) \cdot V_o \cdot (2.07 - 0.5V_o) \cdot (1 + 0.06V_o) = 0$$

Solving for V_o gives VOL = 31.6mV.

b. NM_L and NM_H

Solution

Rather than calculating the derivative of the current, we will estimate V_{IL} and V_{IH} from the simulated VTC. This approach estimates that the noise margin low is about 0.47Vand the noise margin high is about 1.67V.

c. The power dissipation: (1) for V_{in} low, and (2) for V_{in} high

Solution

For Vin low, the NMOS is off, so the power dissipation is 0W. For Vin high, P=VI=2.5*I_{DP}. We saw in part a) the equation for I_{DP}. Plugging in the value for V_{OL}, we get P=VI=2.5*120 μ A=300 μ W.

d. For an output load of 1 pF, calculate t_{pLH}, t_{pHL}, and t_p. Are the rising and falling delays equal? Why or why not?

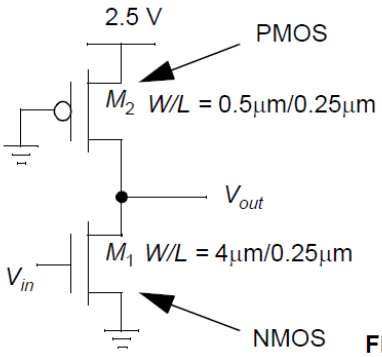

Figure 6.6 Pseudo-NMOS inverter.

Solution

We cannot use the estimate of resistance from the I-V curve for the HL transition because the PMOS is still on. Therefore, we will use the average current method for estimating delay. The average current for the HL transition through the PMOS is 0.5($I_{VDD=2.5}$ + $I_{VDD=1.25}$). $I_{VDD=2.5}$ = 0. $I_{VDD=1.25}$ = -30(2)(-1)(-2.1+0.5) *(1+0.1(1.25)) = 108uA. Thus, Iavg for the PMOS is 54uA.

For the NMOS, $I_{VDD=2.5}$ = 115(16)(0.63)(2.07-.63/2)(1+0.06*2.5)=2.4mA and $I_{VDD=1.25}$ = 115 (16) (0.63) *(2.07-.63/2)(1+0.06*1.25) = 2.2mA. So, Iavg for the NMOS is 2.3mA. The average current discharging the capacitor is then 2.3mA-54uA = 2.25mA. Then t_{pHL} = C*delV/I_{avg} = 556ps.

For t_{pLH}, the NMOS is off, so we can use equivalent resistance to find the transistion time. From the table of resistances in the text, we can calculate R_{EQ} = 31kΩ /(W/Lp) = 15.5kΩ . Then t_{pLH} = 0.69*C*R_{EQ}. So t_{pLH} = 10.7ns.

t_p = (t_{pLH} + t_{pHL})/2 = 5.6ns. The rising delay is much longer because the PMOS is very weak relative to the NMOS.

8. [M, SPICE, 4.2] Consider the circuit of Figure 6.7.

a. What is the output voltage if only one input is high? If all four inputs are high?

Solution

$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GT} \cdot V_{min} - \frac{V_{min}^2}{2} \right) \cdot (1 + \lambda \cdot V_{DS})$$

Consider a case when one input is high: A = V_{DD} and B = C = D = 0 V. Assume that V_{out} is small enough that $V_{min} = V_{DSAT}$ for the PMOS device, and $V_{min} = V_{DS} = V_{out}$ for the NMOS devices. Solve for V_{out} by setting the drain currents in the PMOS and NMOS equal to each other, $|I_{DP}| = |I_{DN}|$, where the drain currents are functions of V_{out}, V_{DD}, and the device parameters.

V_{out} = 102 mV, and I_D = 35.7 μA.

Now verify that the assumptions for V_{min} are correct. For the PMOS: V_{DS} = -2.34 V, V_{DSAT} = -1 V, V_{GT} = -2.1 V, therefore $V_{min} = V_{DSAT}$. For the NMOS: V_{DS} = 102mV, V_{DSAT} = 630mV, V_{GT} = 2.07 V, therefore $V_{min} = V_{DS}$.

Consider the case when all inputs are high: A = B = C = D = V_{DD}. For these hand calculations, this is numerically equivalent to a circuit with a single NMOS device with W/L = 4*1.5 and its gate tied to V_{DD}. Now, the analysis used above for the case when one device is on can be reused, replacing W/L of the NMOS with 6, and using the same assumptions for V_{min}. V_{out} = 25 mV, and I_D = 35.9 μA. The assumptions for V_{min} are correct.

b. What is the average static power consumption if, at any time, each input turns on with an (independent) probability of 0.5? 0.1?

Solution

Notice in part a) that the drain current in the PMOS is 35.7 μA with one NMOS on and 35.9 μA with four NMOS devices on. The current in the PMOS can be approximated as 35.8 μA when any number of NMOS devices are on and 0 μA when all four are off. The probability that all four NMOS devices are off is $(1-\rho)^4$ where ρ is the probability an input is high. Therefore,

$$P_{AVG} = P_{OFF} \cdot (1-\rho)^4 + P_{ON} \cdot \left[1 - (1-\rho)^4 \right]$$

where P_{OFF} = 0 W, and P_{ON} = 89.5 μW. P_{AVG} = 83.9 μW when ρ = 0.5 and P_{AVG} = 30.7 μW when ρ = 0.5.

c. Compare your analytically obtained results to a SPICE simulation.

Solution

From SPICE: V_{out} = 98.7 mV, and I_D = 38.2 μA with one NMOS device on and V_{out} = 23.5 mV, and I_D = 38.3 μA with all NMOS devices on.

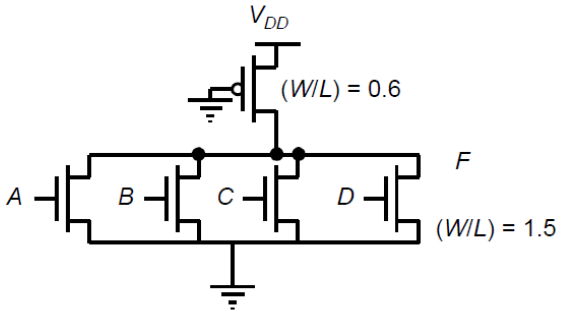

Figure 6.7 Pseudo-NMOS gate.

16. [M, None. 4.2] Figure 6.12 contains a pass-gate logic network.

a. Determine the truth table for the circuit. What logic function does it implement?

Solution

The truth table is shown below

AB	Out
00	1
01	0
10	0
11	1

The circuit implements an XNOR.

b. Assuming 0 and 2.5 V inputs, size the PMOS transistor to achieve a V_{OL} = 0.3 V.

Solution

The PMOS device will be velocity saturated and the NMOS passgate will be in the linear region. $I_{DN}+I_{DP}=0$, so

$$k'_p \cdot \frac{W}{L} \cdot V_{DSAT} \cdot (V_{GT} - 0.5V_{DSAT}) \cdot (1 + \lambda V_{DS}) + k'_n \cdot \frac{W}{L} \cdot V_o \cdot (V_{GT} - 0.5V_o) \cdot (1 + \lambda V_o) = 0$$

We know that V_o=0.3V, so we can plug in numbers and solve for W/L for the PMOS is 7. Let the PMOS be 1.75/0.25.

c. If the PMOS were removed, would the circuit still function correctly? Does the PMOS transistor serve any useful purpose?

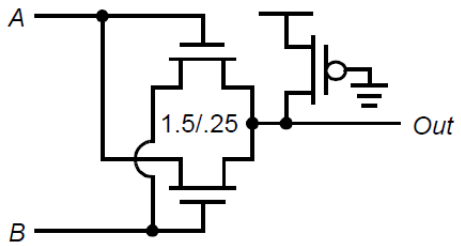

Figure 6.12 Pass-gate network.

Solution

No. If the PMOS were removed, the output node could remain low when AB=00 because it would be floating. The PMOS device pulls the output node high when it would otherwise be in a high impedence state.