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EHB322E Digital Electronic Circuits
Quiz 2

Duration: 30 Minutes
Grading: 1) 50%, 2) 50%,
Quiz is in closed-notes and closed-books format; calculators are allowed
For your answers please use the space provided in the exam sheet
GOOD LUCK!

Consider a Boolean function $f = x_1\overline{x_2} + \overline{x_1}x_2 + x_3$ to be implemented by gates.

- Suppose that all NMOS/PMOS transistors are identical in a gate.
  Equivalent resistor for an NMOS transistor: $\boldsymbol{R_N}$**= (12kΩ) / (W/L)$_N$**
  Equivalent resistor for a PMOS transistor: $\boldsymbol{R_P}$**= (24kΩ) / (W/L)$_P$**
- Suppose that a load capacitor of **10pF** is connected to the output of gates. Neglect all internal MOS capacitors.
- Worst case propagation delays $\mathbf{t_{PLH} = t_{PHL} = 41{,}4ns}$ should be achieved for every gate.

1) Find the values of **(W/L)$_P$** and **(W/L)$_N$** if f is implemented with "a CMOS Pass Transistor Gate".

2) Find the values of **(W/L)$_P$** and **(W/L)$_N$** if f is implemented with "a CMOS Dynamic Logic Gate".