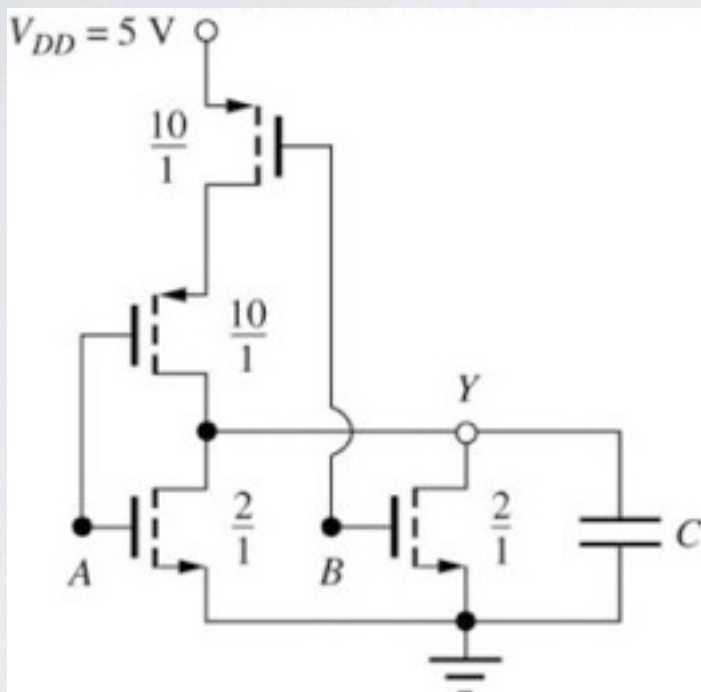# COMPLEX CMOS LOGIC DESIGN
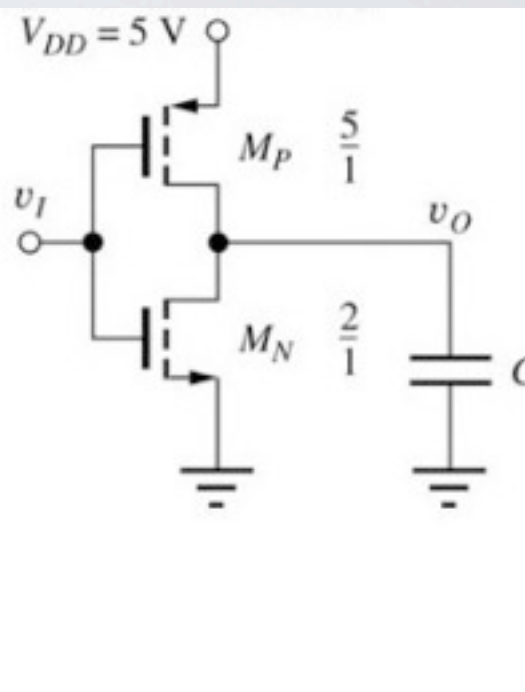
INEL 4207 Digital Electronics

M. Toledo - Spring 2012

CMOS NOR GATE

CMOS NOR gate implementation
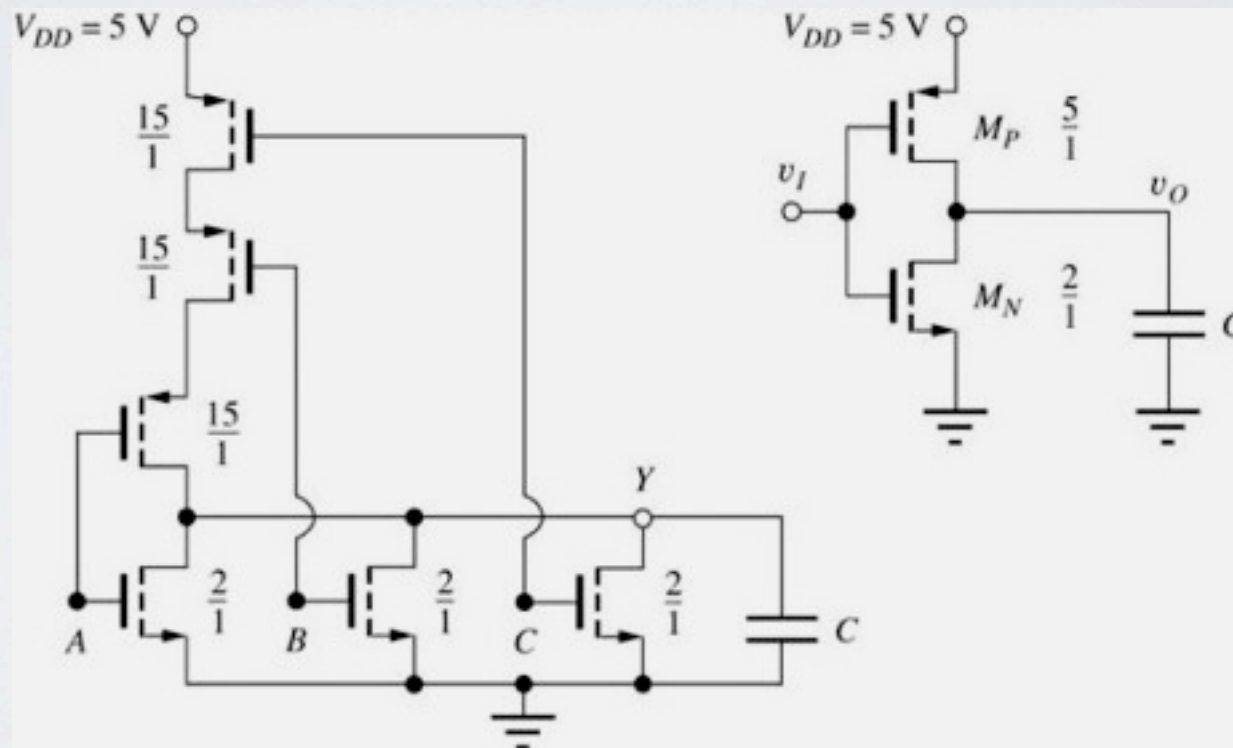
Reference Inverter

2

CMOS NOR GATE SIZING

- Size transistors to keep delay times the same as the reference inverter.

  - the on-resistance on the PMOS branch of the NOR gate must be the same as the reference inverter

  - For a two-input NOR gate, the $(W/L)_p$ must be made twice as large
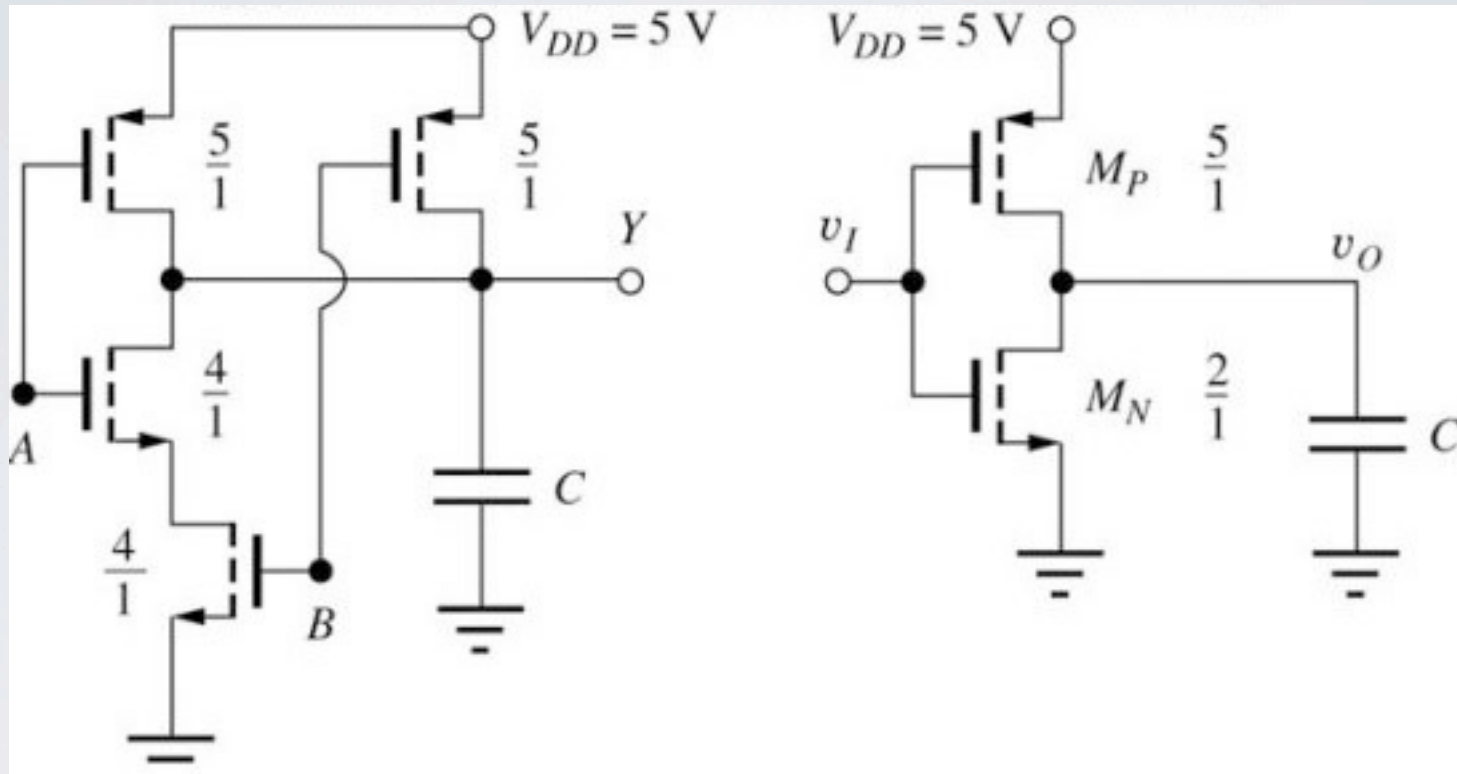
3

THREE-INPUT NOR GATE LAYOUT

- It is possible to extend this same design technique to create multiple input NOR gates

SHORTHAND NOTATION FOR NMOS AND PMOS

NMOS transistors   PMOS transistors
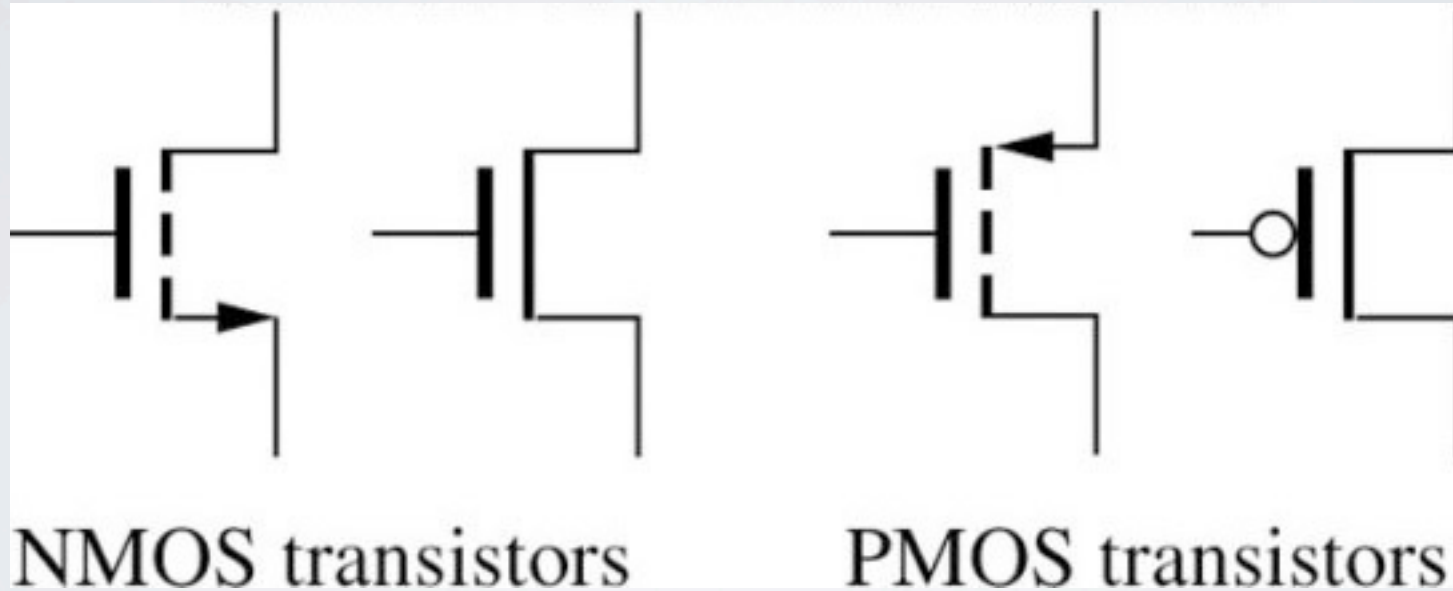
CMOS NAND GATES

CMOS NAND gate implementation

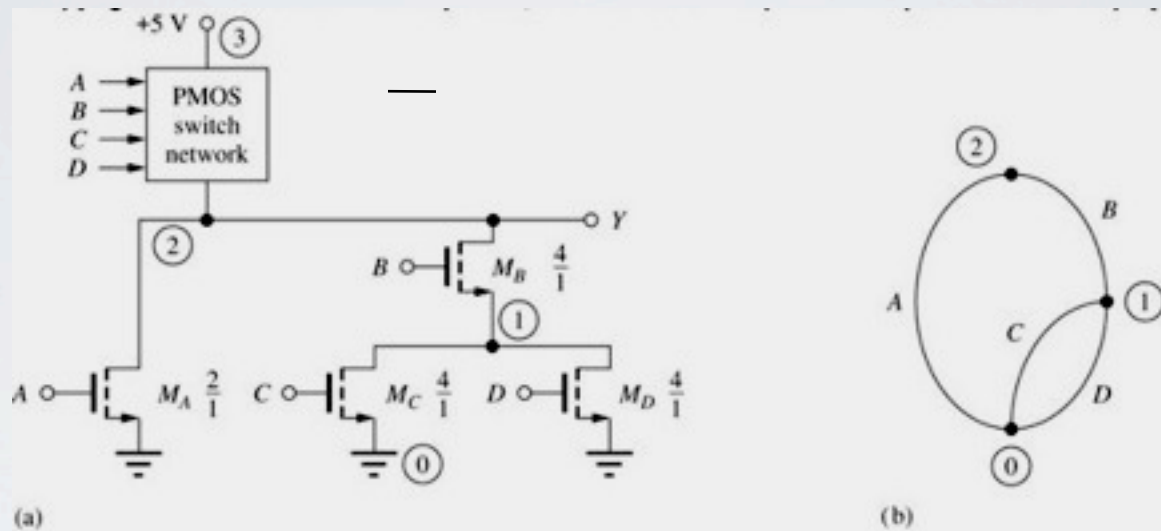Reference Inverter

CMOS NAND GATES SIZING

- The same rules apply for sizing the NAND gate as the did for the NOR gate, except for now the NMOS transistors are in series

- The $(W/L)_N$ will be twice the size of the reference inverter's NMOS

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MULTI-INPUT CMOS NAND GATES

COMPLEX CMOS LOGIC GATE DESIGN EXAMPLE

(a)   (b)
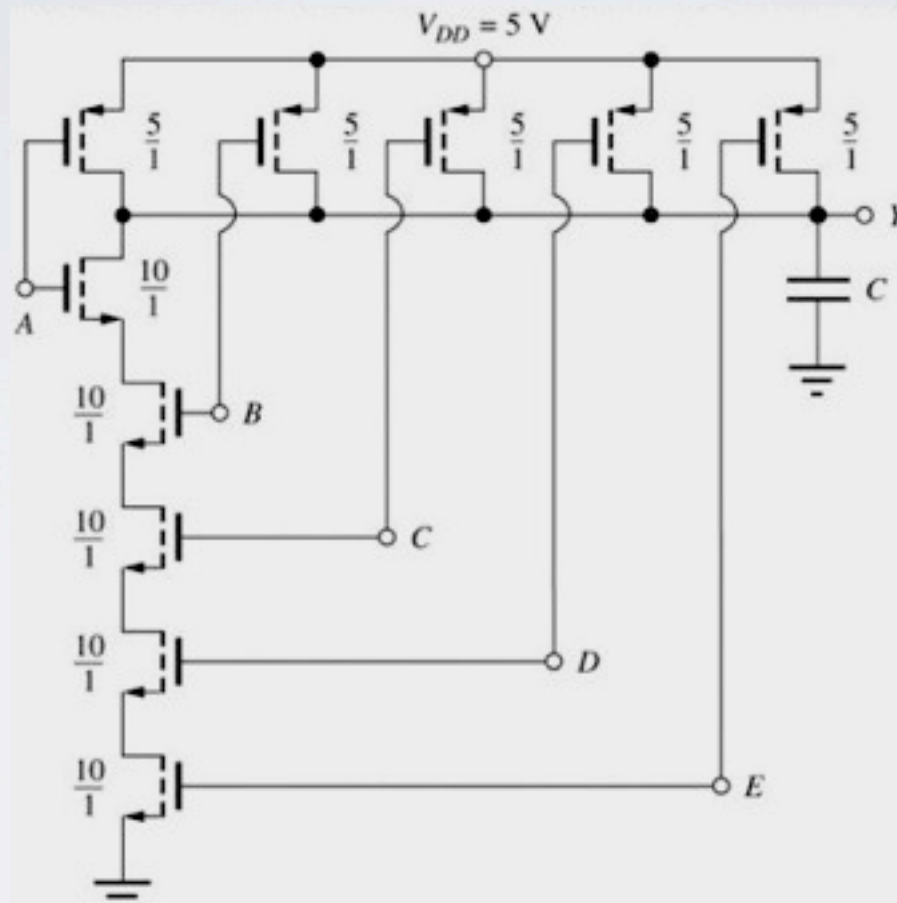
- Design a CMOS logic gate for $(W/L)_{p,ref}=5/1$ and for $(W/L)_{n,ref}=2/1$ that exhibits the function: $Y' = A + BC + BD$

- By inspection (knowing Y), the NMOS branch of the gate can drawn as the following with the corresponding graph, while considering the longest path for sizing purposes:

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COMPLEX CMOS LOGIC GATE DESIGN EXAMPLE

(c)   (d)
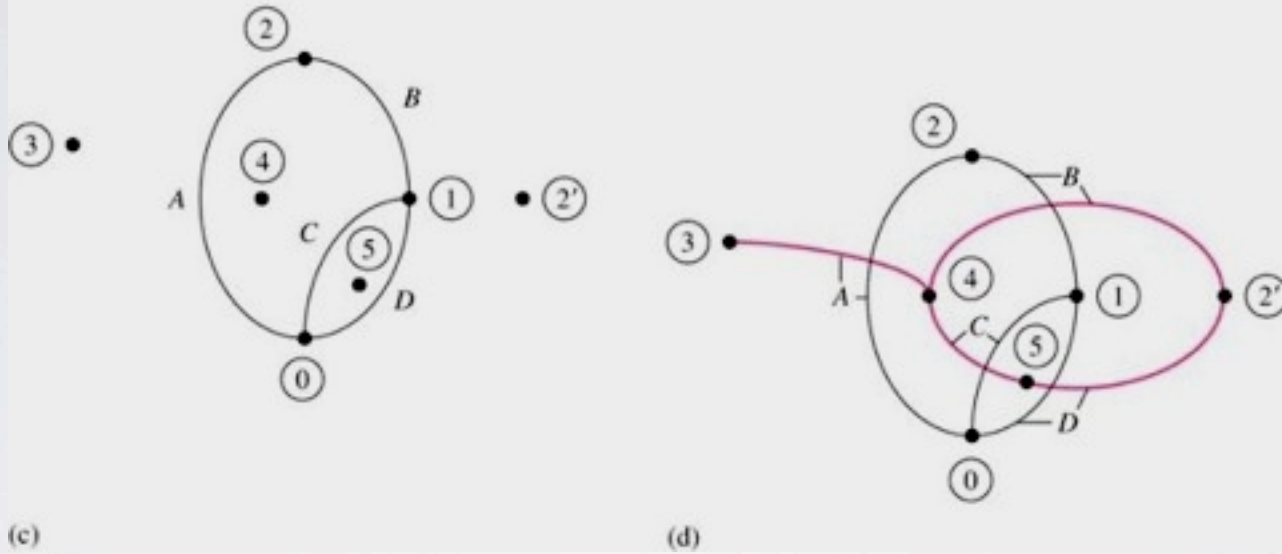
- By placing nodes in the interior of each arc, plus two more outside the graph for V_{DD} (3) and the complementary output (2'), the PMOS branch can be realized as shown on the left figure

- Connect all of the nodes in the manner shown in the right figure, and the NMOS arc that PMOS arc intersects have the same inputs

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COMPLEX CMOS LOGIC GATE DESIGN EXAMPLE


Final CMOS circuit
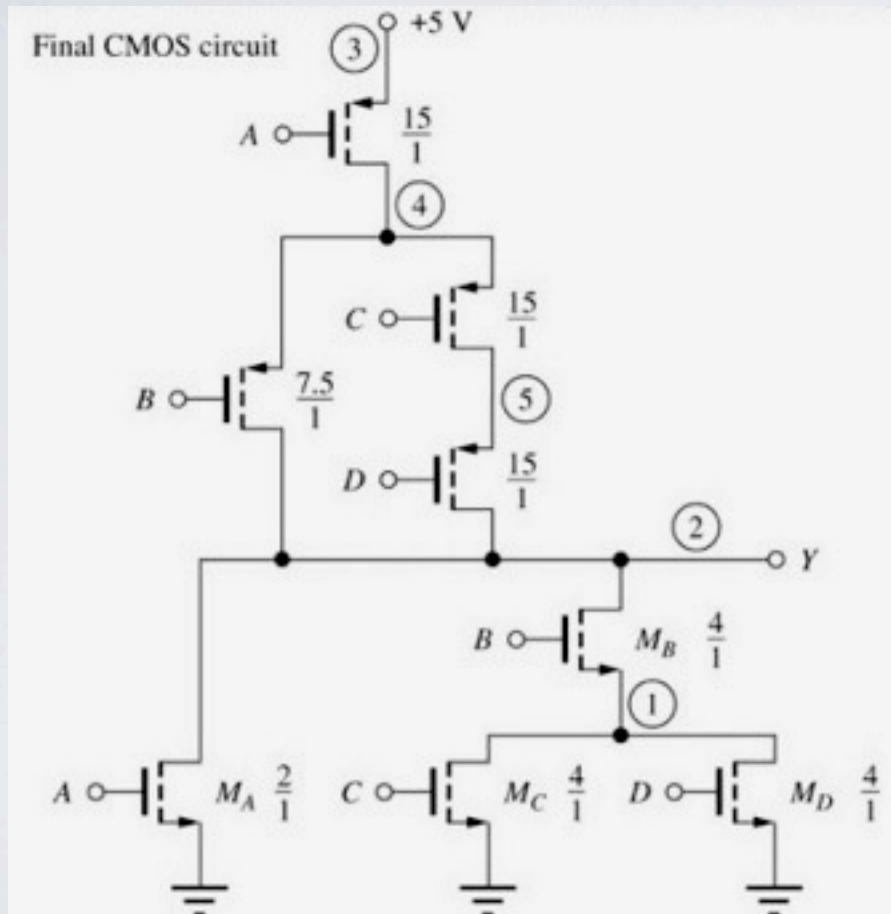
- From the PMOS graph, the PMOS branch can now be drawn for the final CMOS logic gate while once again considering the longest PMOS path for sizing

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COMPLEX CMOS GATE WITH A BRIDGING

- Design a CMOS gate that implements the following logic function using the same reference inverter sizes as the previous example:

  - $Y = AB + CE + ADE + CDB$

- The NMOS branch can be realized in the following manner using bridging NMOS D to implement Y. The corresponding NMOS graph is shown to the right.

Thursday, February 2, 12
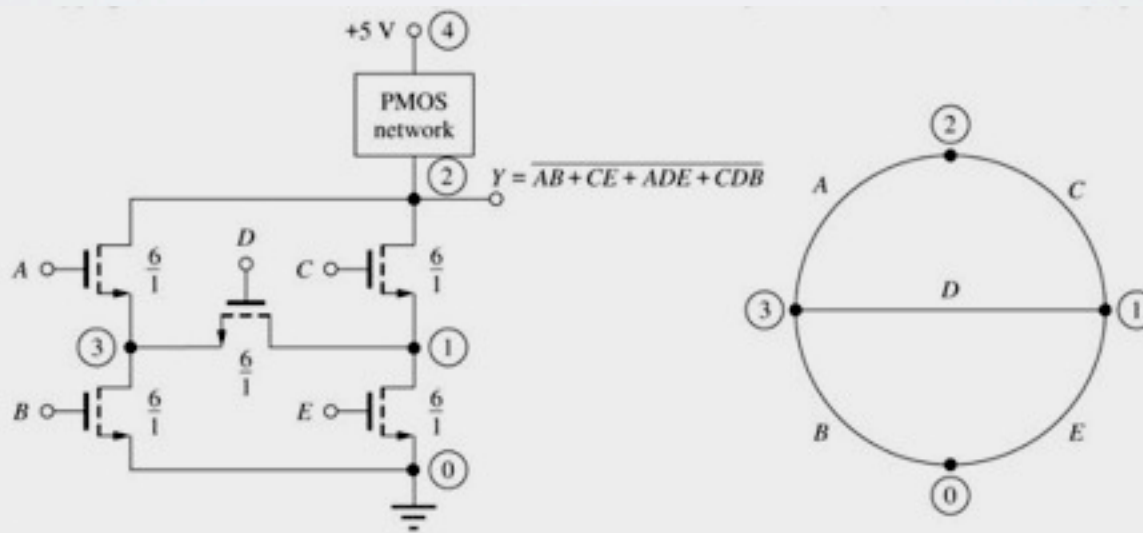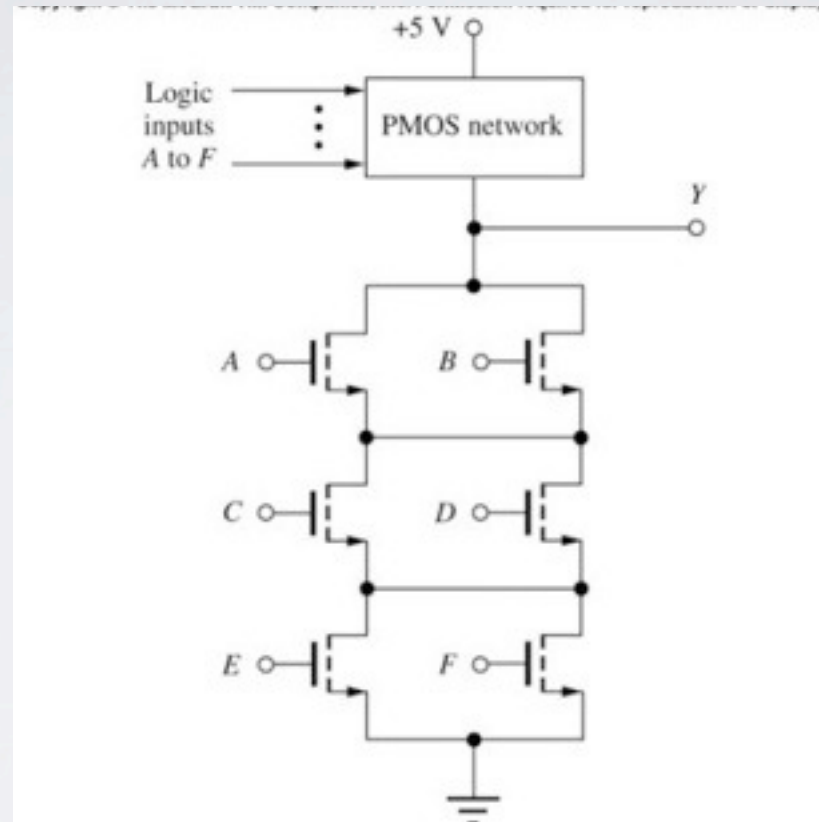
COMPLEX CMOS GATE WITH A BRIDGING
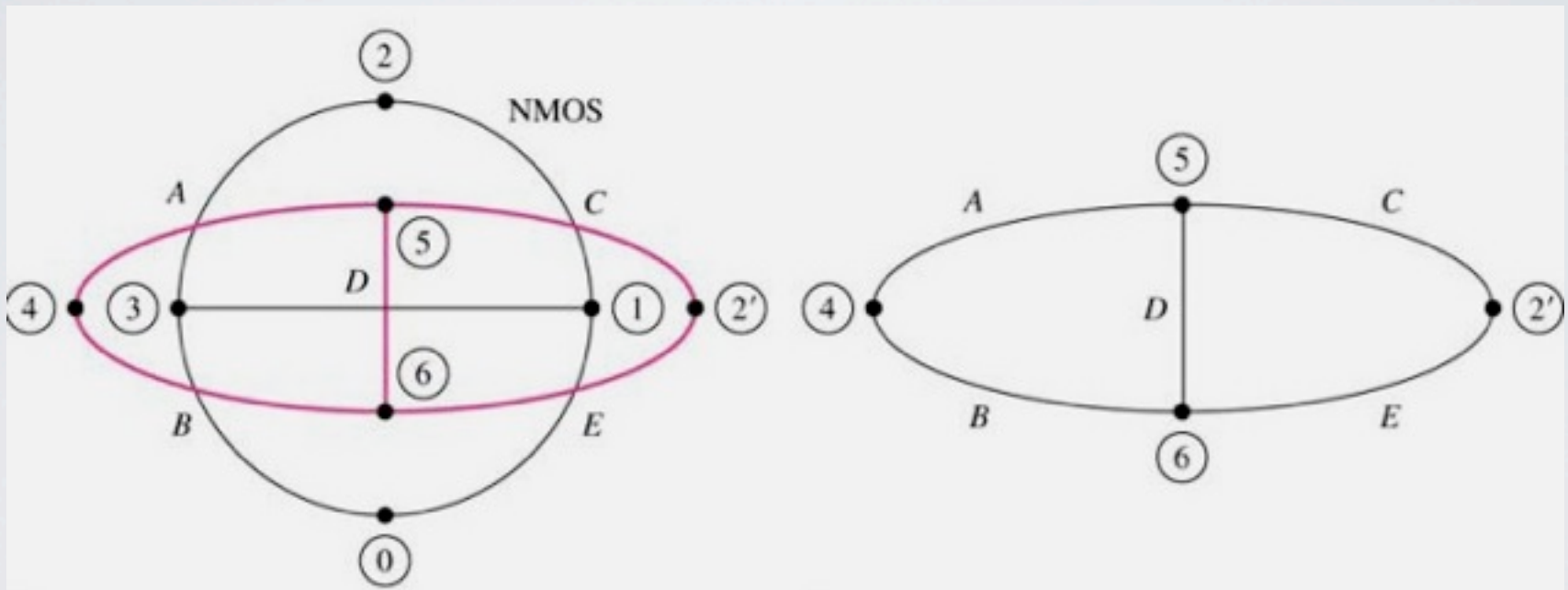
COMPLEX CMOS GATE WITH A BRIDGING
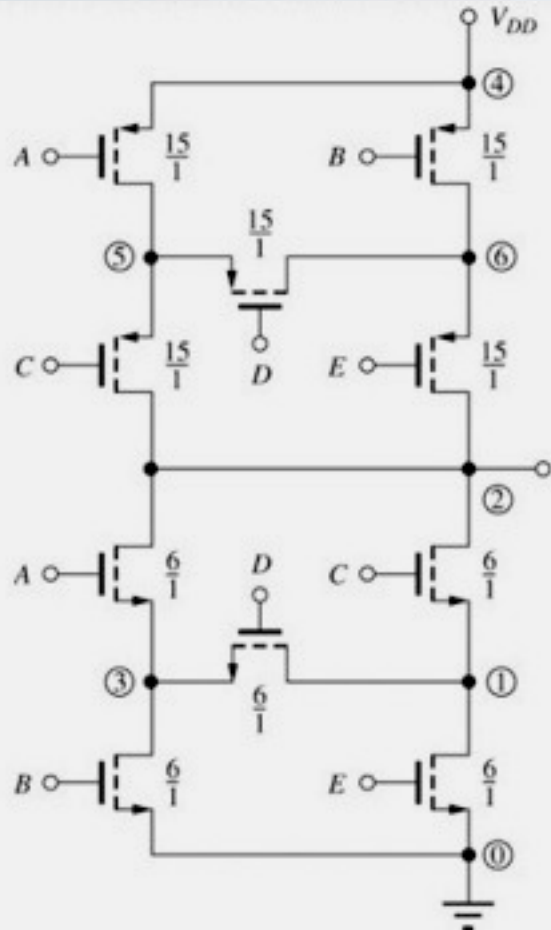
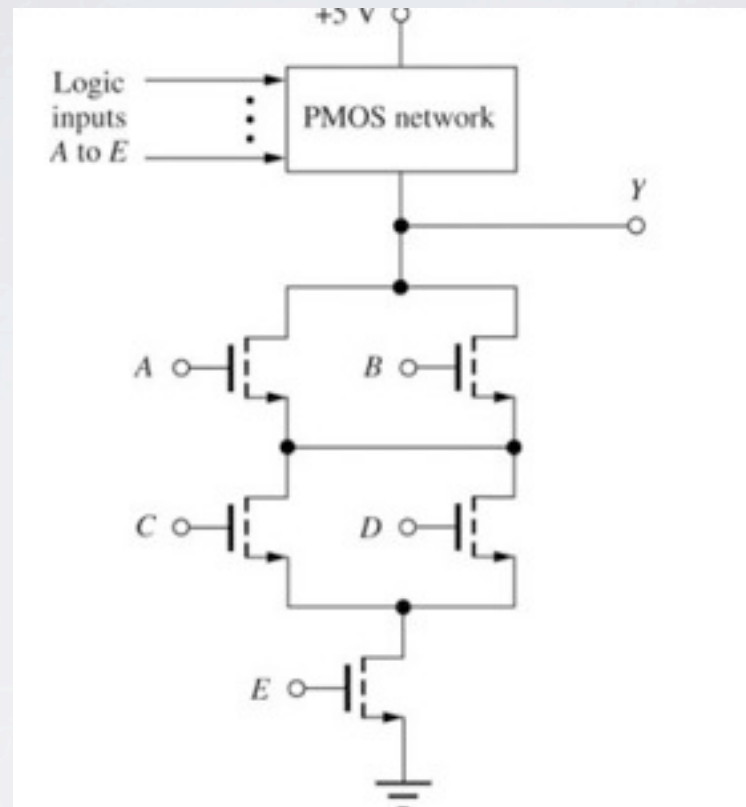By using the PMOS graph the PMOS branch can now be realized as the one shown on the left.

The longest path was used to select sizing.

Find Pull-up Network (PUN)

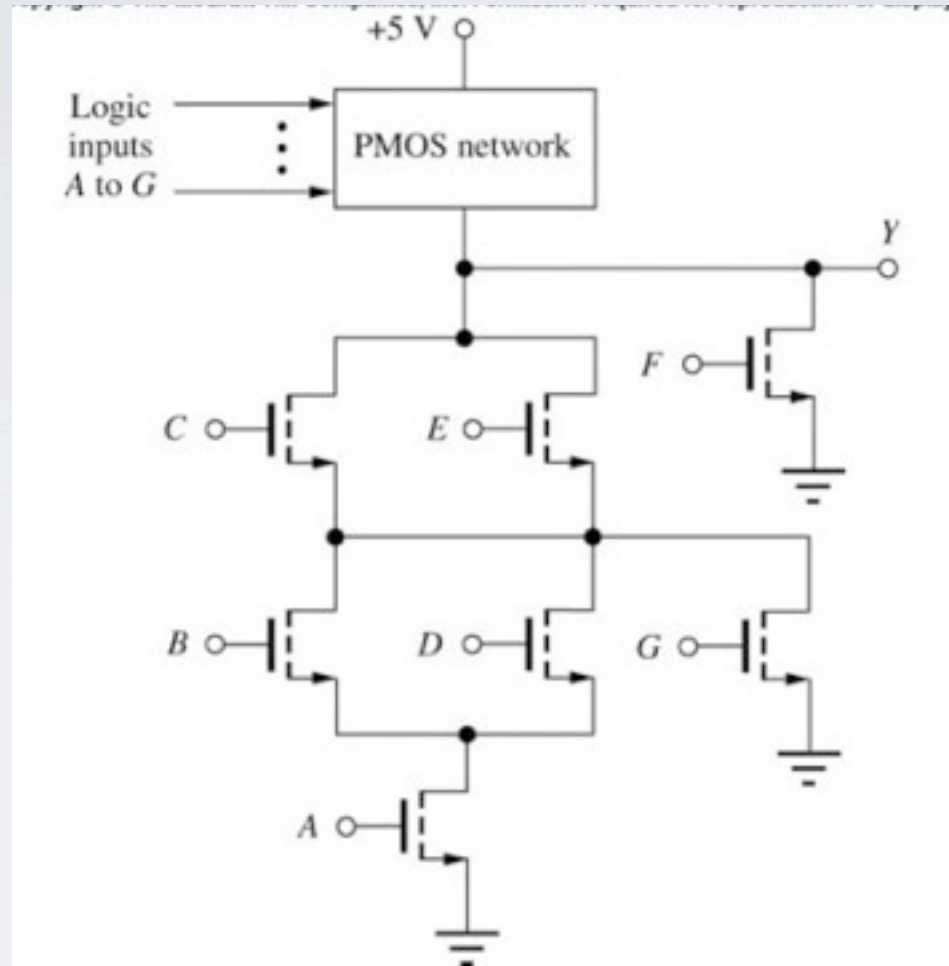

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PUN?

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PUN?

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- Design a CMOS logic gate based on the reference inverter to implement the following function:

$$Y=(ABC+DE)'$$

Select transistor sizes to obtain propagation times simllar to those of the reference inverter.

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- Design CMOS L.G. to implement

$$Y=[A(B+C(D+E))]'$$

  Select sizes to obtain same t_p as in reference inverter.

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CMOS NOR GATE BODY EFFECT

- Since the bottom PMOS body contact is not connected to its source, its threshold voltage changes as V_{SB} changes during switching

- Once $v_O = V_H$ is reached, the bottom PMOS is not affected by body effect, thus the total on-resistance of the PMOS branch is the same

- However, the rise time is slowed down due to $|V_{TP}|$ being a function of time

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TWO-INPUT NOR GATE LAYOUT
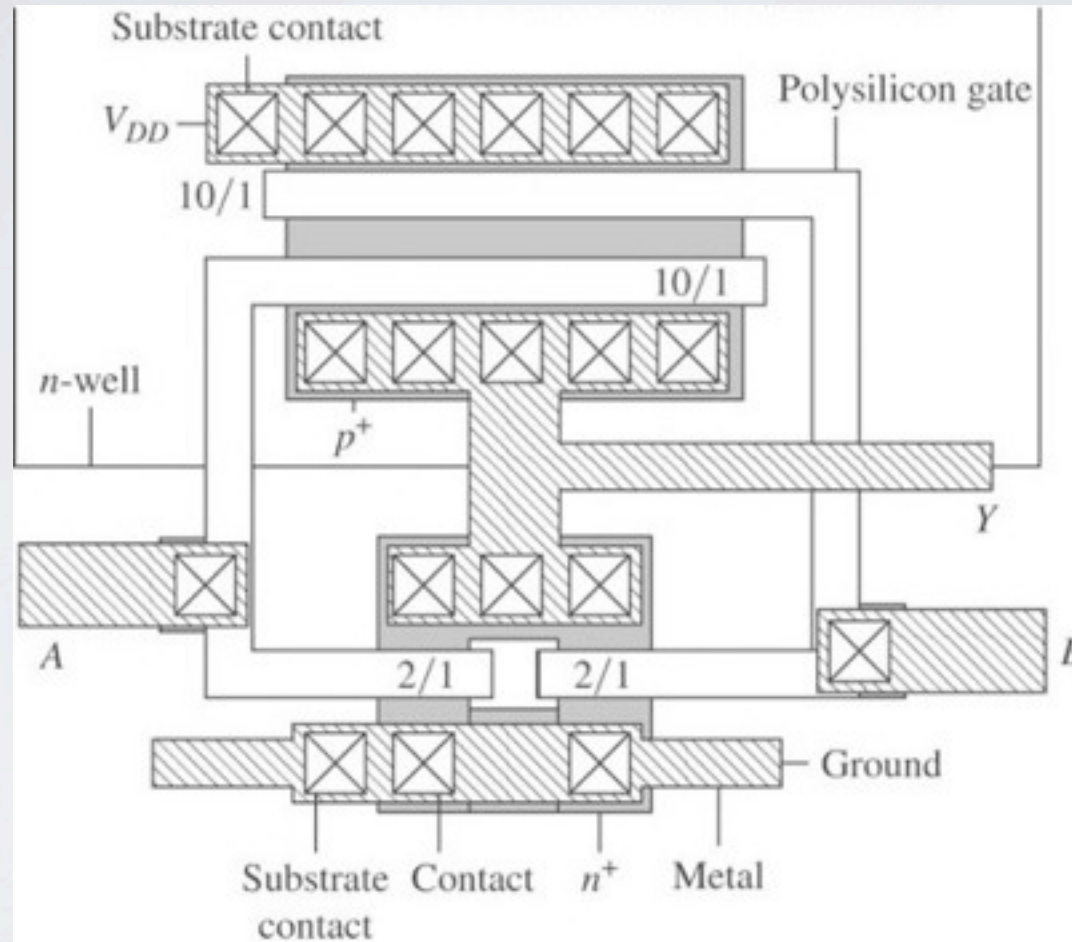
MINIMUM SIZE GATE DESIGN AND PERFORMANCE

- With CMOS technology, there is a area/delay tradeoff that needs to be considered

- If minimum feature sized are used for both devices, then the τ_{PLH} will be decreased compared to the symmetrical reference inverter

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MINIMUM SIZE COMPLEX GATE AND LAYOUT

- a

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