Istanbul Technical University

Faculty of Computer and Informatics
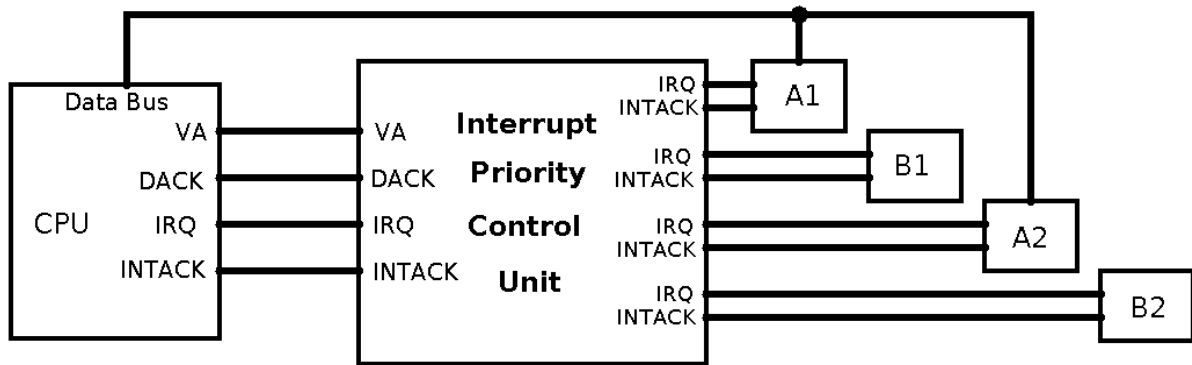

BLG322E Computer Architecture

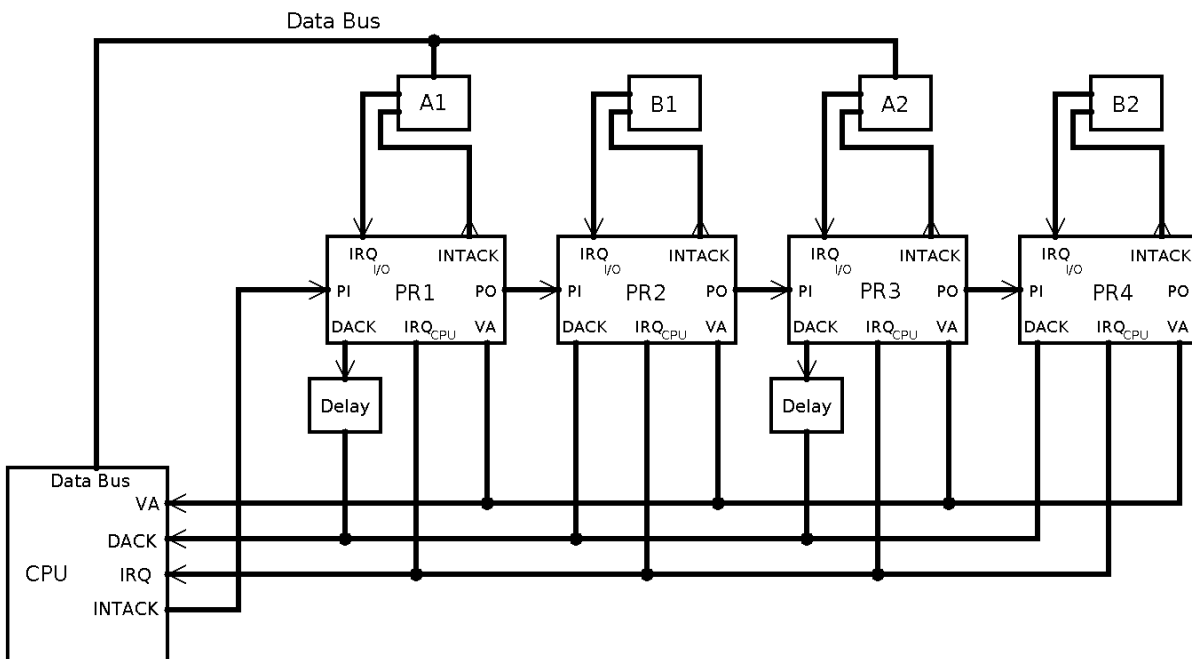# Homework 2

Cem Yusuf Aydoğdu

150120251
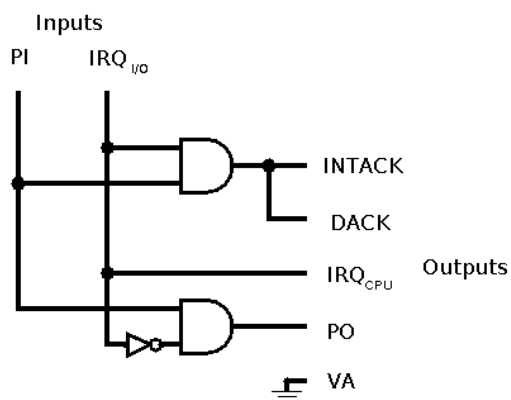
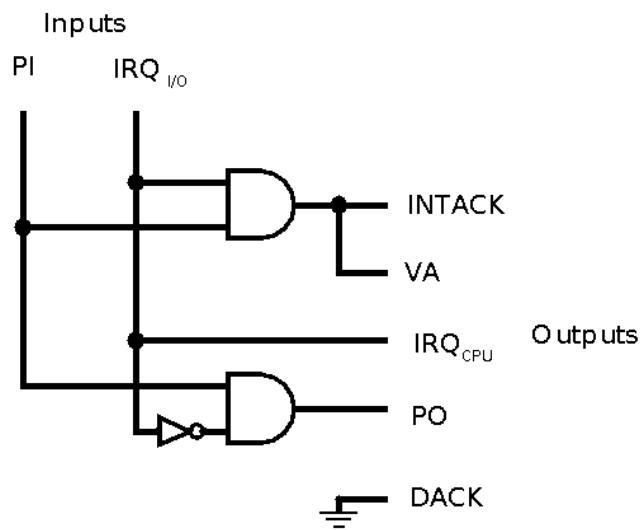**Date of Submission : 7.4.2015**

1) a. Representation of the system

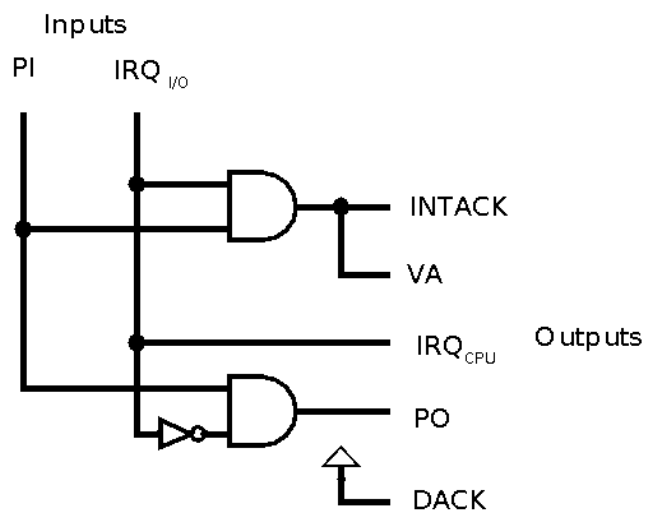## 1) b. Serial priority circuit and connections

Inside priority chains for A:

Inside priority chain for B_1:

Inputs

PI   IRQ $_{I/O}$

INTACK

VA

IRQ$_{CPU}$ Outputs

PO

DACK

Inside priority chain for B_2:

Inputs

PI   IRQ $_{I/O}$

INTACK

VA

IRQ$_{CPU}$ Outputs

PO

DACK

1) c. Parallel circuit

IRQ$_{B2}$
IRQ$_{A2}$
IRQ$_{B1}$
IRQ$_{A1}$

0
Pri
MSB
1
0 LSB

INTACK$_{CPU}$

VA

DACK

IRQ$_{CPU}$

INTACK INTACK INTACK INTACK
A1   B1   A2   B2
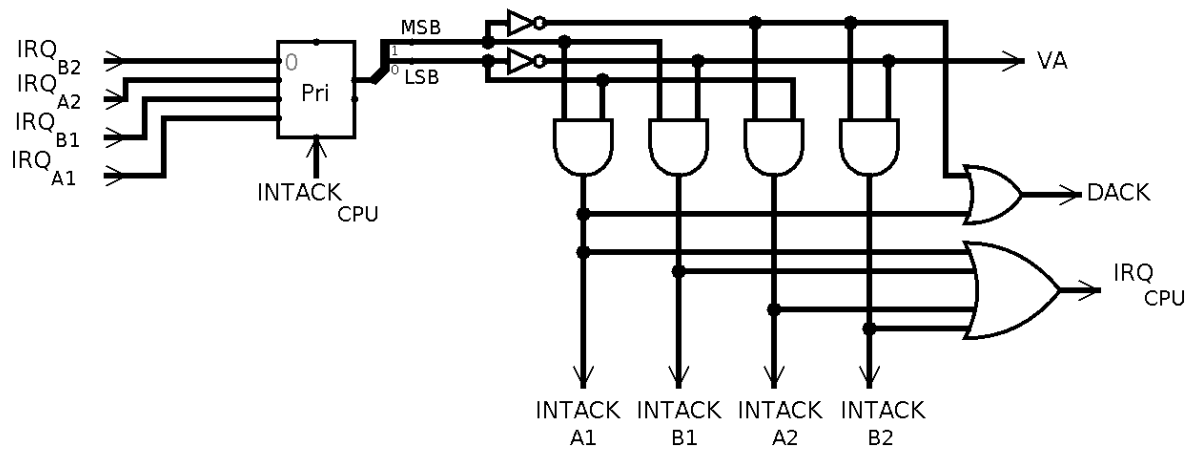
2) In both connection types, if the request comes from one of the A devices, chain circuit outputs VA=0 and DACK=1, and the relevant device puts its interrupt address to the data bus.
If the B_1 device requests an interrupt, chain circuit outputs VA=1 and DACK=0. If the B_2 device requests an interrupt, its chain circuit outputs VA=1 and DACK=1.