08.11.2013

Istanbul Technical University
Department of Computer Engineering

BLG 231E - Digital Circuits
Assignment 4

Due Date: 14.11.2013, **Thursday,** 17.00.

- Please **write <u>neatly</u>**.
- If you are not preparing your homework in a computer, please show complement of a symbol by putting a **dash** over the symbol (e.g. do not use ~~x'~~ use $\bar{x}$).
- Plagiarized assignments will be given a negative mark.
- **No late submissions** will be accepted.

Submissions: Please submit your solutions to the Digital Circuits Course Assignment Box at the department secretary's office.

1. A combinational logic circuit has three 4-bit inputs (A, B and C) and three 1-bit outputs (f1, f2 and f3). Unsigned integers are applied to the inputs. Outputs should be set to 1 only in the following conditions.

- **f1:** The number applied to A is greater than the numbers at other inputs
- **f2:** The number applied to A is the median of three numbers at the inputs.
- **f3:** The number applied to A is smaller than the numbers at other inputs

Design this circuit using only two 4-bit parallel full adders, one decoder with appropriate size and necessary logic gates.

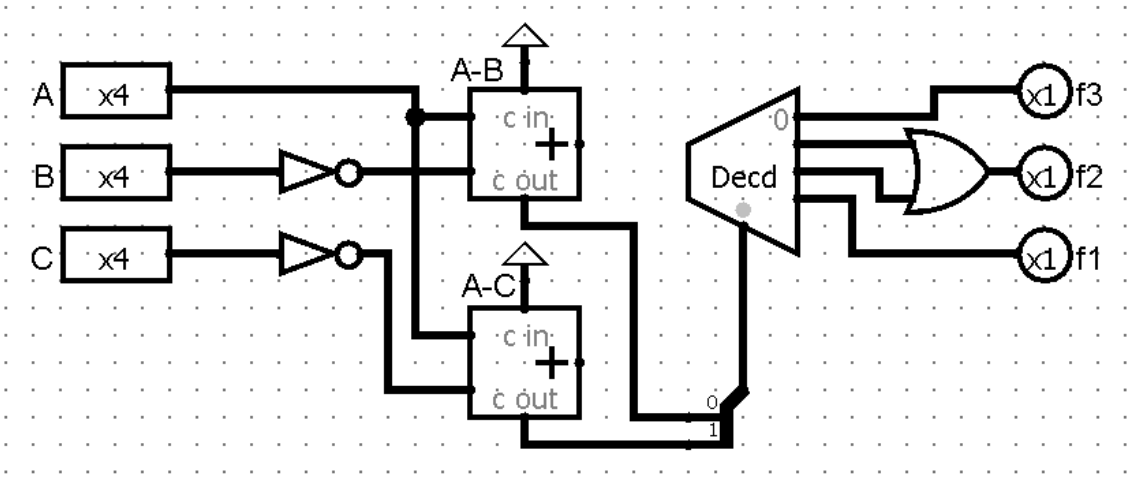
2. Definition of a function with four inputs (a, b, c and d) is given below.

$$f(a,b,c,d) = \bigcup_1(2,3,5,6,8,10,11,15)$$

Implement this function using only necessary number of 4:1 multiplexers and a NOT gate.

Solutions:

1. Carry outputs of the adders can be used to compare numbers. In subtraction of unsigned integers, if carry output is set then there is no borrow and the first operand is greater than or equal to the second one. If carry output is not set then there is borrow and the first operand is less than the second one.



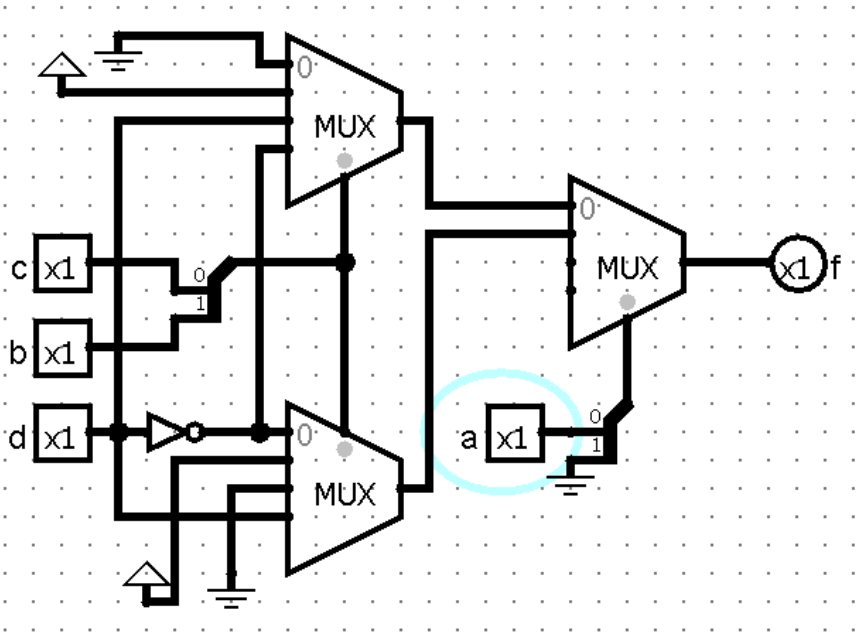
In the circuit above 2 subtractions are made using Two's complement. If both subtractions result in no borrow (c out = 1) then A is greater than or equal to both B and C so f1 is set. If both subtractions result in borrow (c out = 0) then A is less than both B and C so f3 is set. In other two cases A is greater than or equal to either A or B and less than the other so it is the median and f2 is set.

Please note that the NOT gates in the above circuit have 4 data bits and carry inputs of both adders are set to logic 1. Another common mistake is to interpret "carry out = 1" as borrow, while it means no borrow.

2. One possible solution can be obtained by redefining the output in terms of input d. Related truth table is given below.

	a	**b**	**c**	**d**	**f**	
0	0	0	0	0	0	**0**
1	0	0	0	1	0	
2	0	0	1	0	1	**1**
3	0	0	1	1	1	
4	0	1	0	0	0	**d**
5	0	1	0	1	1	
6	0	1	1	0	1	**d'**
7	0	1	1	1	0	
8	1	0	0	0	1	**d'**
9	1	0	0	1	0	
10	1	0	1	0	1	**1**
11	1	0	1	1	1	
12	1	1	0	0	0	**0**
13	1	1	0	1	0	
14	1	1	1	0	0	**d**
15	1	1	1	1	1	

Given truth table can be realized using a single 8:1 multiplexer and a NOT gate. Since we can only use 4:1 multiplexers, we should use 3 of them in order to obtain an 8:1 multiplexer. One of the 4:1 multiplexers is used as a 2:1 multiplexer by connecting logic 0 to its significant select bit.



A common mistake in this question is to use the method introduced in slide 5.12. Such an approach requires a 16:1 multiplexer which can be obtained using five 4:1 multiplexers. However, the question allows to use only necessary number of multiplexers.