

DENEY RAPORU

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| **Deney Adı** | Logic Gates and Multivibrators |
| **Deneyi Yaptıran Ar. Gör.** | Latif Akçay |
| **Raporu Hazırlayan**  **(İsim / Numara / Bölüm)** | Cem Yusuf Aydoğdu / 150120251 / BLGE |
| **Grup Numarası ve**  **Deney Tarihi** | D27 / 07.11.2014 |

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| **Rapor Notu** | **Teslim Edildiği Tarih** | **Teslim Alındığı Tarih** |
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**Logic Gates and Multivibrators**

In this experiment basic operation principles of logic gates, monostable and bistable circuits are studied.

Two main types of technologies are used in logic circuits: TTL and CMOS. In this

experiment, CMOS circuits are used. While CMOS instruments are generally more costly than TTL circuits, they consume less energy. Also they are faster and more stable. A CMOS circuit is produced by NMOS and PMOS components which are slightly different due to semiconductor properties of source and drain regions.

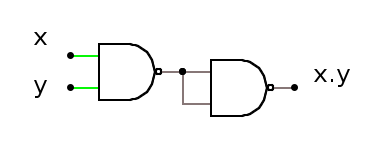
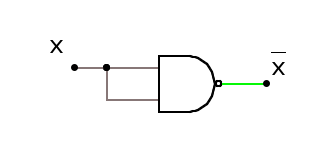
**Exp 6.1, 6.2**

NAND gate in Fig. 6.9 is constructed on CADET without additional transistor and resistors. Output is connected directly to a led on CADET. Truth table of NAND gate is obtained.

|  |  |  |
| --- | --- | --- |
| x | y | (x.y)’ |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Exp 6.3**

NOT and AND gates are builded with only NAND gates.



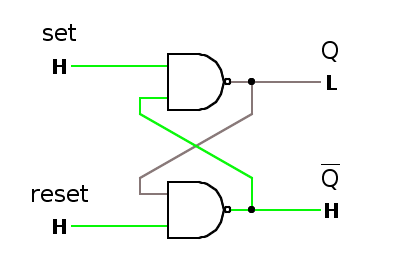
|  |  |  |
| --- | --- | --- |
| x | y | (x.y) |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

|  |  |
| --- | --- |
| x | x’ |
| 0 | 1 |
| 1 | 0 |

**Exp 6.4, 6.5**

SR flip-flop is implemented with NAND gates as shown below. S=0 and R=0 is unvanted state since both Q and Q’ are 1.

|  |  |  |  |
| --- | --- | --- | --- |
| S | R | Q | Q’ |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | Qprev | Q’prev |



**Exp 6.6**

Circuit in Fig 6.16 is constructed. Transistor is in cut-off while Vin=0, and in saturation with square wave. Vc voltage drops with raising edge of the square wave. Graphs are plotted in the protocol sheet.

