**Mapping a Performance-Portable Global Shallow Water Model onto**

**Field Programmable Gate Arrays Using Advanced Compiler Tools**

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**Abstract**

1. **Introduction**
2. **Background**

**2.1 Related/Previous Work**

**2.2 Shallow Water Equations**

The following formulation of the SWE are described in [5]. The SWE in a 3D Cartesian coordinate system for a rotating fluid are given by

∂u/∂t=-(u∙∇u)-f (x × u)-g∇h (2.1.1),

∂h/∂t=-∇∙(hu) (2.1.2),

where f is the Coriolis force, u=〖[u,v,w]〗^T is the velocity vector, h is the geopotential height and x=〖[x,y,z]〗^T is the position vector

The shallow water model test case on the sphere is the zonal flow over an isolated mountain (test case 5) proposed by (Drake, et al., 1991). This is the same validation test that was used to validate in [Elliott, 2017].

The specifics of this test are as follows: zonal flow.The initial wind and height fields are given by

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the mean height, *h0* = 5400 m, the radius of the Earth, a = 6.37122x106, and the angular frequency of rotation of the earth, 7.292 e-5 sec-1, and the gravity g = 9.80616 m/s.

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**2.3 RBF Discretization**

Then the discretization of the *RHS* defined in equation 2.1.4, denoted by *RHSD*, is given by

(2.3.3)

where ∘ is element by element multiplication and *x, y, z, u, v, w, and h* are simply the vectors containing the values of x, y, z, u, v, w and h at each of the node points {x\_i }\_(i=1)^N. Let H={▁u,▁v,▁w,▁h}. Using this our discretization of equations 2.1.4-7 becomes

Let H\_t be H at a time t and ∆t be our time step. This system is then advanced in time using 4th order Runge Kutta by

(2.3.5)

where

**2.4 Performance-Portable implementation**

1. **FPGA Software Toolchain**

**3.1 QCC**

**3.2 Performance Simulation** - do you nail the time observed?

1. **Results and Analysis**

**4.1 Methodology**

**CPU -** Intel Skylake/OpenMP - look into HPC Futures Lab power sensing.

Intel Xeon Gold 6140

Date chip GA:

Fab:

**GPU - NVIDIA** Tesla V100/GPU -

power:SMI toolchain

Date chip GA:

Fab:

**FPGA -** Xilinx Alveo U250 -

Power: overclocking?

Date chip GA:

Fab:

The Alveo U250 offers 1.728M LUTs, 12,288 DSP slices, 3,456K registers, 64GB of DDR4 memory with 77 GB/sec, dual 100Gbps network interfaces. The internal SRAM bandwidth is 47 TB/s. Power and thermal specs are: 225W, with typical draw of 110W

**4.2 Performance Comparison**

**4.3 Power Efficiency** Power reported by toolchain; actual power observed on device.

**4.4 Discussion**

1. **Conclusion**

**Multi-FPGA test - MPI.** Not bloody likely.

**Acknowledgement**

1. **References**

[1] Drake, et al. 1991

[2] Elliott, et al., 2017