

Chisel Bootcamp

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```
ssh xxx@yyy  
password: bootcamp
```

to prevent lossage of state if disconnected ... when you first log in, type

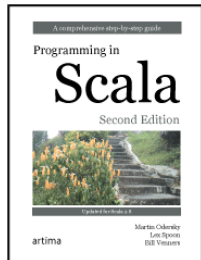
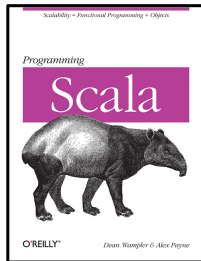
```
screen
```

when you log back into the instance, type

```
screen -r
```

```
cd chisel  
git pull
```

- Compiled to JVM
 - Good performance
 - Great Java interoperability
 - Mature debugging, execution environments
- Object Oriented
 - Factory Objects, Classes
 - Traits, overloading etc
- Functional
 - Higher order functions
 - Anonymous functions
 - Currying etc
- Extensible
 - Domain Specific Languages (DSLs)



```
def f (x: Int) = 2 * x
```

```
def g (xs: List[Int]) = xs.map(f)
```

```
object Blimp {  
  var numBlimps = 0  
  def apply(r: Double) = {  
    numBlimps += 1  
    new Blimp(r)  
  }  
}
```

```
Blimp.numBlimps  
Blimp(10.0)
```

```
class Blimp(r: Double) {  
  val rad = r  
  println("Another Blimp")  
}
```

```
class Zep(r: Double) extends Blimp(r)
```

```
// Array's
val tbl = new Array[Int](256)
tbl(0) = 32
val y = tbl(0)
val n = tbl.length

// ArrayBuffer's
val buf = new ArrayBuffer[Int]()
buf += 12
val z = buf(0)
val l = buf.length

// List's
val els = List(1, 2, 3)
val a :: b :: c :: Nil = els
val m = els.length
```



```
val tbl = new Array[Int](256)

// loop over all indices
for (i <- 0 until tbl.length)
  tbl(i) = i

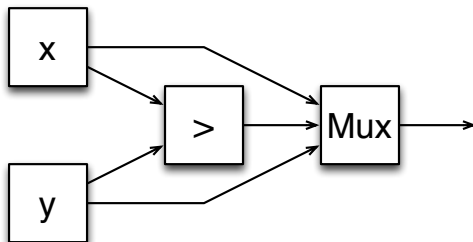
// loop of each sequence element
for (e <- tbl)
  tbl(i) += e

// nested loop
for (i <- 0 until 16; j <- 0 until 16)
  tbl(j*16 + i) = i

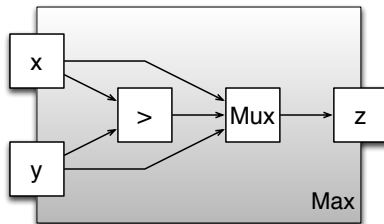
// create second table with doubled elements
val tbl2 = for (i <- 0 until 16) yield tbl(i)*2
```

```
scala  
1 + 2  
def f (x: Int) = 2 * x  
f(4)
```

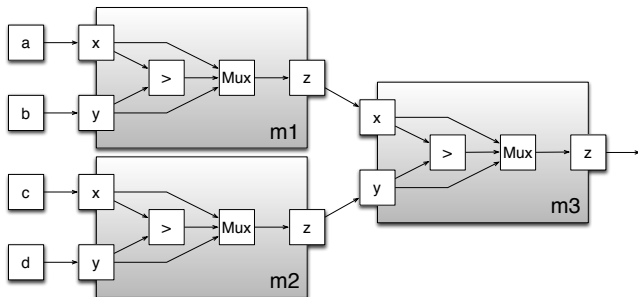
$\text{Mux}(x > y, x, y)$



```
class Max2 extends Module {  
  val io = new Bundle {  
    val x = UInt(width = 8).asInput  
    val y = UInt(width = 8).asInput  
    val z = UInt(width = 8).asOutput }  
  io.z := Mux(io.x > io.y, io.x, io.y)  
}
```

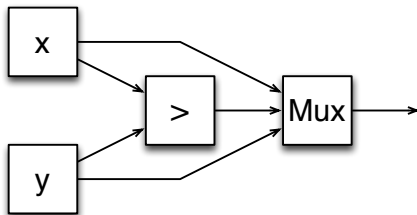


```
val m1 =  
  Module(new  
    Max2()  
  m1.io.x := a  
  m1.io.y := b  
val m2 =  
  Module(new  
    Max2()  
  m2.io.x := c  
  m2.io.y := d  
val m3 =  
  Module(new  
    Max2()  
  m3.io.x := m1.io.z  
  m3.io.y := m2.io.z
```

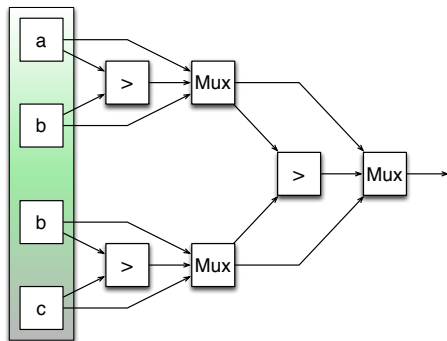


```
def Max2 = Mux(x > y, x, y)
```

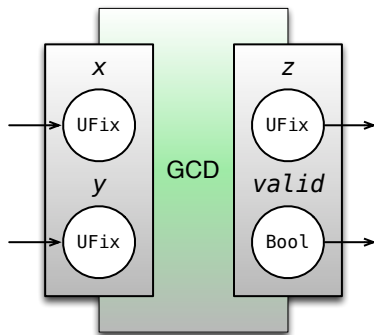
```
Max2(x, y)
```



Reduce(Array(a, b, c, d), Max2)

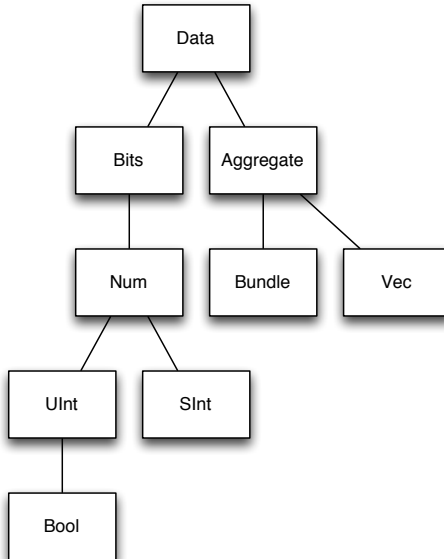


```
class GCD extends Module {  
  val io = new Bundle {  
    val a      = UInt(INPUT, 16)  
    val b      = UInt(INPUT, 16)  
    val z      = UInt(OUTPUT, 16)  
    val valid  = Bool(OUTPUT) }  
  val x = Reg(reset = io.a)  
  val y = Reg(reset = io.b)  
  when (x > y) {  
    x := x - y  
  } .otherwise {  
    y := y - x  
  }  
  io.z      := x  
  io.valid  := y === UInt(0)  
}
```



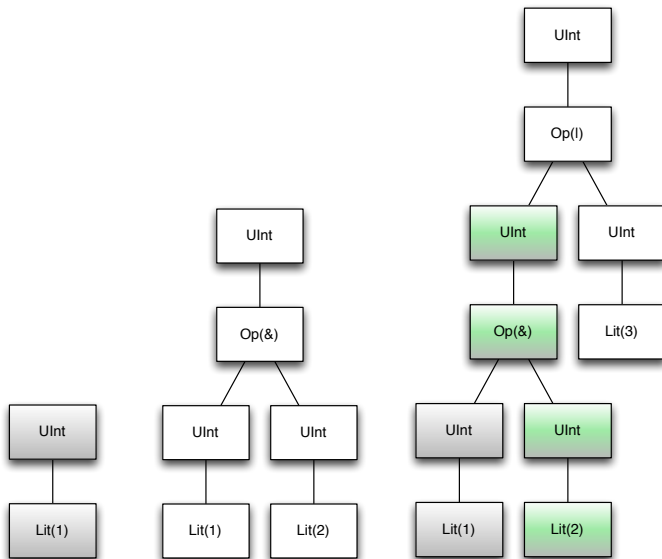

```
UInt(1)           // decimal 1-bit literal from Scala Int.  
UInt("ha")        // hexadecimal 4-bit literal from string.  
UInt("o12")       // octal 4-bit literal from string.  
UInt("b1010")     // binary 4-bit literal from string.  
  
SInt(5)           // signed decimal 4-bit literal from Scala Int.  
SInt(-8)          // negative decimal 4-bit literal from Scala Int.  
UInt(5)           // unsigned decimal 3-bit literal from Scala Int.  
  
Bool(true)        // Bool literals from Scala literals.  
Bool(false)
```

```
UInt("h_dead_beef") // 32-bit literal of type UInt.  
UInt(1)              // decimal 1-bit literal from Scala Int.  
UInt("ha", 8)        // hexadecimal 8-bit literal of type UInt.  
UInt("o12", 6)        // octal 6-bit literal of type UInt.  
UInt("b1010", 12)    // binary 12-bit literal of type UInt.  
  
SInt(5, 7)           // signed decimal 7-bit literal of type SInt.  
UInt(5, 8)           // unsigned decimal 8-bit literal of type UInt.
```



```
(a & b) | (~c & d)
```

```
val sel = a | b  
val out = (sel & in1) | (~sel & in0)
```



`a = UInt(1)`

`b = a & UInt(2)`

`b | UInt(3)`

Valid on UInt, SInt, Bool.

```
// Bitwise-NOT
val invertedX = ~x
// Bitwise-AND
val hiBits    = x & UInt("h_ffff_0000")
// Bitwise-OR
val flagsOut  = flagsIn | overflow
// Bitwise-XOR
val flagsOut  = flagsIn ^ toggle
```

Valid on SInt and UInt. Returns Bool.

```
// AND-reduction
val allSet = andR(x)
// OR-reduction
val anySet = orR(x)
// XOR-reduction
val parity = xorR(x)
```

Valid on SInt, UInt, and Bool. Returns Bool.

```
// Equality
val equ = x === y
// Inequality
val neq = x != y
```


Valid on SInt, and UInt.

```
// Logical left shift.  
val twoToTheX = SInt(1) << x  
// Right shift (logical on UInt & UInt, arithmetic on SInt).  
val hiBits    = x >> UInt(16)
```

Valid on SInt, UInt, and Bool.

```
// Extract single bit, LSB has index 0.  
val xLSB      = x(0)  
// Extract bit field from end to start bit pos.  
val xTopNibble = x(15,12)  
// Replicate a bit string multiple times.  
val usDebt     = Fill(3, UInt("hA"))  
// Concatenates bit fields, w/ first arg on left  
val float      = Cat(sgn,exp,man)
```

Valid on Bools.

```
// Logical NOT.  
val sleep = !busy  
// Logical AND.  
val hit    = tagMatch && valid  
// Logical OR.  
val stall  = src1busy || src2busy  
// Two-input mux where sel is a Bool.  
val out    = Mux(sel, inTrue, inFalse)
```

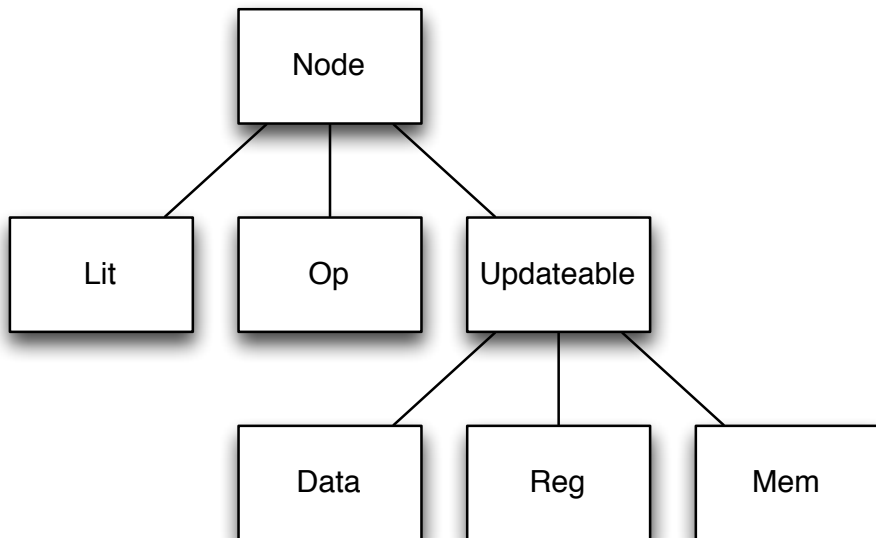
Valid on Nums: SInt and UInt.

```
// Addition.  
val sum = a + b  
// Subtraction.  
val diff = a - b  
// Multiplication.  
val prod = a * b  
// Division.  
val div = a / b  
// Modulus  
val mod = a % b
```

Valid on Nums: SInt and UInt. Returns Bool.

```
// Greater than.  
val gt = a > b  
// Greater than or equal.  
val gte = a >= b  
// Less than.  
val lt = a < b  
// Less than or equal.  
val lte = a <= b
```

operation**bit width** $z = x + y$ $wz = \max(wx, wy)$ $z = x - y$ $wz = \max(wx, wy)$ $z = x \& y$ $wz = \max(wx, wy)$ $z = \text{Mux}(c, x, y)$ $wz = \max(wx, wy)$ $z = w * y$ $wz = wx + wy$ $z = x \ll n$ $wz = wx + \text{maxNum}(n)$ $z = x \gg n$ $wz = wx - \text{minNum}(n)$ $z = \text{Cat}(x, y)$ $wz = wx + wy$ $z = \text{Fill}(n, x)$ $wz = wx * \text{maxNum}(n)$



src	<i># chisel scala source code</i>
csrc	<i># chisel emulator source code</i>
doc	<i># documentation</i>
www	<i># web sources</i>
tutorial	<i># tutorial project</i>
tutorial/src	<i># tutorial source code</i>
tutorial/sbt	<i># tutorial sbt files</i>
tutorial/emulator	<i># tutorial emulator build products</i>
tutorial/emulator/Makefile	<i># Makefile for emulator products</i>
tutorial/verilog	<i># tutorial verilog build products</i>
tutorial/verilog/Makefile	<i># Makefile for verilog products</i>


```
package Tutorial

import Chisel._

class Combinational extends Module {
  val io = new Bundle {
    val x = UInt(INPUT, 16)
    val y = UInt(INPUT, 16)
    val z = UInt(OUTPUT, 16)
  }
  io.z := io.x + io.y
}
```

```
package Tutorial

import Chisel._

object Tutorial {
  def main(args: Array[String]) = {
    val args = args.slice(1, args.length)
    args(0) match {
      case "combinational" =>
        chiselMain(args, () => new Combinational())
      ...
    }
  }
}
```

```
def main(args: Array[String]) = {  
  val args = args.slice(1, args.length)  
  args(0) match {  
    case "combinational" => chiselMain(args, () => new Combinational())  
  }  
}
```

get into sbt directory:

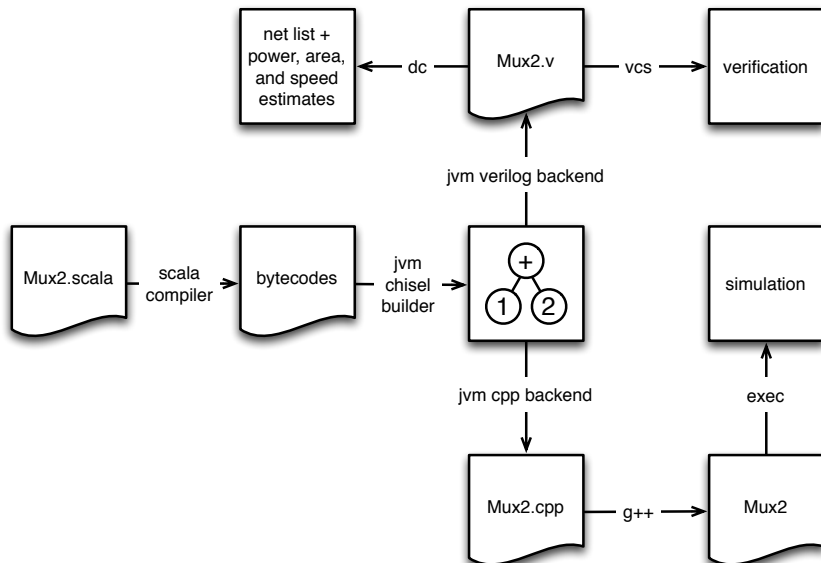
```
cd $CHISEL/tutorial/sbt
```

emit C++ and compile tutorial/emulator/Combination-* to produce combinational circuit app named tutorial/emulator/Combination:

```
bash> sbt  
sbt> project tutorial  
sbt> compile  
sbt> run Combinational --backend c --targetDir ../emulator --compile --genHarness  
sbt> exit
```

or on one line

```
sbt "project tutorial" "run Combinational --backend c --targetDir ../emulator --compile --genHarness"
```



```
package Tutorial
import Chisel._
import scala.collection.mutable.HashMap
import scala.util.Random

class Combinational extends Module {
  val io = new Bundle {
    val x = UInt(INPUT, 16)
    val y = UInt(INPUT, 16)
    val z = UInt(OUTPUT, 16) }
  io.z := io.x + io.y
}

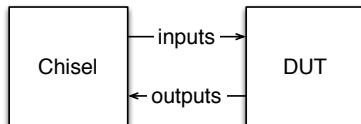
class CombinationalTests(c: Combinational)
  extends Tester(c, Array(c.io)) {
  defTests {
    var allGood = true
    val vars = new HashMap[Node, Node]()
    val rnd = new Random()
    val maxInt = 1 << 16
    for (i <- 0 until 10) {
      vars.clear()
      val x = rnd.nextInt(maxInt)
      val y = rnd.nextInt(maxInt)
      vars(c.io.x) = UInt(x)
      vars(c.io.y) = UInt(y)
      vars(c.io.z) = UInt((x + y) & (maxInt - 1))
      allGood = step(vars) && allGood
    }
    allGood
  } }
}
```

```
class Tester[T <: Module]
  (val c: T, val testNodes: Array[Node])

def defTests(body: => Boolean)

def step(vars: HashMap[Node, Node]): Boolean
```

- user subclasses **Tester** defining DUT and **testNodes** and tests in **defTests** body
- **vars** is mapping from **testNodes** to literals, called bindings
- **step** runs test with given bindings, where var values for input ports are sent to DUT, DUT computes next outputs, and DUT sends next outputs to Chisel
- finally **step** compares received values against var values for and returns false if any comparisons fail output ports



```
object chiselMainTest {  
  def apply[T <: Module]  
    (args: Array[String], comp: () => T)(tester: T => Tester[T]): T  
}
```

and used as follows:

```
chiselMainTest(args + "--test", () => new Combinational()){  
  c => new CombinationalTests(c)  
}
```

```
cd $CHISEL/tutorial/sbt  
sbt "project tutorial" "run Combinational ... --compile --test"  
...  
PASSED
```

or through makefile

```
cd $CHISEL/tutorial/emulator  
make combinational  
...  
PASSED
```

```
def clb(a: UInt, b: UInt, c: UInt, d: UInt) =  
  (a & b) | (~c & d)  
  
val out = clb(a,b,c,d)
```



```
class Functional extends Module {  
  def clb(a: UInt, b: UInt, c: UInt, d: UInt) =  
    (a & b) | (~c & d)  
  val io = new Bundle {  
    val x = UInt(INPUT, 16)  
    val y = UInt(INPUT, 16)  
    val z = UInt(OUTPUT, 16)  
  }  
  io.z := clb(io.x, io.y, io.x, io.y)  
}
```

```
class MyFloat extends Bundle {  
  val sign      = Bool()  
  val exponent  = UInt(width = 8)  
  val significand = UInt(width = 23)  
}  
  
val x = new MyFloat()  
val xs = x.sign
```

```
// Vector of 5 23-bit signed integers.
val myVec = Vec.fill(5) { SInt(width = 23) }

// Connect to one static element of vector.
val reg3 = myVec(3)
reg3      := data3
myVec(4)  := data4

// Connect to one dynamic element of vector.
val reg    = myVec(addr)
reg        := data1
myVec(addr2) := data2
```

Data object with directions assigned to its members

```
class Decoupled extends Bundle {  
  val ready = Bool(OUTPUT)  
  val bits  = UInt(INPUT, 32)  
  val valid = Bool(INPUT)  
}
```

Direction assigned at instantiation time

```
class ScaleIO extends Bundle {  
  val in    = new MyFloat().asInput  
  val scale = new MyFloat().asInput  
  val out   = new MyFloat().asOutput  
}
```

- inherits from Module,
- contains an interface stored in a port field named `io`, and
- wires together subcircuits in its constructor.

```
class Mux2 extends Module {  
  val io = new Bundle{  
    val sel = UInt(INPUT, 1)  
    val in0 = UInt(INPUT, 1)  
    val in1 = UInt(INPUT, 1)  
    val out = UInt(OUTPUT, 1)  
  }  
  io.out := (io.sel & io.in1) | (~io.sel & io.in0)  
}
```

```
sbt
sbt> project tutorial
sbt> compile                // compiles Chisel Scala code
sbt> run Combinational      // produces C++ files
sbt> run Combinational --compile // produces C++ files and compiles
sbt> run Combinational --test  // produces C++ files, compiles, tests
sbt> exit
```

with a complete set of command line arguments being:

--targetDir	target pathname prefix
--genHarness	generate harness file for C++
--debug	put all wires in C++ class file
--compile	compiles generated C++
--test	runs tests using C++ app
--backend v	generate verilog
--backend c	generate C++ (default)
--vcd	enable vcd dumping

```
cd $CHISEL/tutorial/sbt; sbt "project tutorial" "run Mux2 --backend v ..."
```

or through makefile:

```
cd $CHISEL/tutorial/verilog; make Mux2.v
```

producing Mux2.v:

```
module Mux2(  
    input  io_sel,  
    input  io_in0,  
    input  io_in1,  
    output io_out);  
  
    wire T0;  
    wire T1;  
    wire T2;  
    wire T3;  
  
    assign io_out = T0;  
    assign T0 = T3 | T1;  
    assign T1 = T2 & io_in0;  
    assign T2 = ~ io_sel;  
    assign T3 = io_sel & io_in1;  
endmodule
```

```
cd $CHISEL/tutorial/sbt  
sbt "project tutorial" "run Mux2 --backend c ... --vcd --compile --test"
```

which then produces

```
$CHISEL/tutorial/emulator/Mux2.vcd
```

which you can view with a vcd viewer

- child modules stored in fields of parent
- now write 4-to-1 mux out of 3 2-to-1 mux's

```
class Mux4 extends Module {  
  val io = new Bundle {  
    val in0 = UInt(INPUT, 1)  
    val in1 = UInt(INPUT, 1)  
    val in2 = UInt(INPUT, 1)  
    val in3 = UInt(INPUT, 1)  
    val sel = UInt(INPUT, 2)  
    val out = UInt(OUTPUT, 1)  
  }  
  val m0 = new Mux2()  
  m0.io.sel := io.sel(0); m0.io.in0 := io.in0; m0.io.in1 := io.in1  
  
  // flush this out ...  
  
  io.out := io.in0 & io.in1 & io.in2 & io.in3 & io.sel  
}
```

- loop
 - edit and flush out Mux4.scala
 - make Mux4
- until PASSES

```
cd $CHISEL/tutorial/emulator
make Mux4
...
PASSED
```

```
Reg(data = in)
```

```
def risingEdge(x: Bool) = x && !Reg(data = x)
```

```
def wrapAround(n: UInt, max: UInt) =  
  Mux(n > max, UInt(0), n)  
  
def counter(max: UInt) = {  
  val x = Reg(reset = UInt(0, max.getWidth))  
  x := wrapAround(x + UInt(1), max)  
  x  
}
```

```
// Produce pulse every n cycles.  
def pulse(n: UInt) = counter(n - UInt(1)) === UInt(0)
```

```
// Flip internal state when input true.  
def toggle(p: Bool) = {  
  val x = Reg(reset = Bool(false))  
  x := Mux(p, !x, x)  
  x  
}
```

```
// Square wave where each half cycle has given period.  
def squareWave(period: UInt) = toggle(pulse(period))
```

- write sequential circuit that sums `in` values

```
class Accumulator extends Module {  
  val io = new Bundle {  
    val in  = UInt(INPUT, 1)  
    val out = UInt(OUTPUT, 8)  
  }  
  
  // flush this out ...  
  
  io.out := UInt(0)  
}
```

```
val pcPlus4      = UInt()  
val branchTarget = UInt()  
val pcNext       = Mux(io.ct1.pcSel, branchTarget, pcPlus4)  
val pcReg        = Reg(data = pcNext, reset = UInt(0, 32))  
pcPlus4          := pcReg + UInt(4)  
...  
branchTarget     := addOut
```

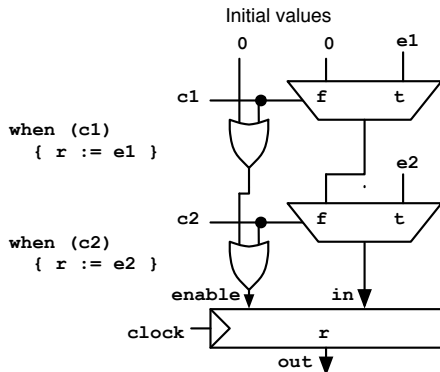
```
val r = Reg( UInt(16) )  
when (c === UInt(0) ) {  
    r := r + UInt(1)  
}
```



```
when (c1) { r := UInt(1) }  
when (c2) { r := UInt(2) }
```

Conditional Update Order:

c1	c2	r	
0	0	r	r unchanged
0	1	2	
1	0	1	
1	1	2	c2 takes precedence over c1



- Each `when` statement adds another level of data mux and ORs the predicate into the enable chain and
- the compiler effectively adds the termination values to the end of the chain automatically.

```
r := SInt(3)
s := SInt(3)
when (c1) { r := SInt(1); s := SInt(1) }
when (c2) { r := SInt(2) }
```

leads to r and s being updated according to the following truth table:

c1	c2	r	s	
0	0	3	3	r updated in c2 block, s updated using default
0	1	2	3	
1	0	1	1	
1	1	2	1	

```
when (a) { when (b) { body } }
```

which is the same as:

```
when (a && b) { body }
```

```
when (c1) { u1 }  
.elsewhen (c2) { u2 }  
.otherwise { ud }
```

which is the same as:

```
when (c1) { u1 }  
when (!c1 && c2) { u2 }  
when (!(c1 || c2)) { ud }
```

```
switch(idx) {  
  is(v1) { u1 }  
  is(v2) { u2 }  
}
```

which is the same as:

```
when (idx === v1) { u1 }  
when (idx === v2) { u2 }
```

```
class Parity extends Module {  
  val io = new Bundle {  
    val in  = Bool(INPUT)  
    val out = Bool(OUTPUT) }  
  val s_even :: s_odd :: Nil = Enum(2, UInt())  
  val state = Reg(reset = s_even)  
  when (io.in) {  
    when (state === s_even) { state := s_odd }  
    .otherwise             { state := s_even }  
  }  
  io.out := (state === s_odd)  
}
```

- write vending machine which needs accepts 20 cents or more before raising valid high

```
class VendingMachine extends Module {  
  val io = new Bundle {  
    val nickel = Bool(INPUT)  
    val dime   = Bool(INPUT)  
    val valid   = Bool(OUTPUT) }  
  val sIdle :: s5 :: s10 :: s15 :: s0k :: Nil = Enum(5, UInt())  
  val state = Reg(reset = sIdle)  
  
  // flush this out ...  
  
  io.valid := (state === s0k)  
}
```



```
def Vec[T <: Data](elts: Seq[T])(data: => T): Vec[T]  
def Vec[T <: Data](elts: T*)(data: => T): Vec[T]
```

```
val i = Array(UInt(1), UInt(2), UInt(4), UInt(8))  
val m = Vec.fill(i){ UInt(width = 32) }  
val r = m(counter(UInt(3)))
```

- write 16x16 multiplication table using Vec

```
class Mul extends Module {  
  val io = new Bundle {  
    val x    = UInt(INPUT, 4)  
    val y    = UInt(INPUT, 4)  
    val z    = UInt(OUTPUT, 8)  
  }  
  val muls = new Array[UInt](256)  
  
  // flush this out ...  
  
  io.z := UInt(0)  
}
```

```
def object Mem {  
  def apply[T <: Data](n: Int, reset: T = null)(type: => T): Mem  
}  
  
class Mem[T <: Data]  
  (val n: Int, val reset: T, val inits: Seq[T], type: () => T)  
  extends Updateable {  
    def apply(addr: UInt): T  
  }
```

```
val regs = Mem(32, UInt(width = 32) )
when (wr_en) {
  regs(wr_addr) := wr_data
}
val idat = regs(iaddr)
val mdat = regs(maddr)
```

- write read/write table using Mem

```
class Memo extends Module {  
  val io = new Bundle {  
    val isWr    = Bool(INPUT)  
    val wrAddr  = UInt(INPUT, 8)  
    val wrData  = UInt(INPUT, 8)  
    val isRd    = Bool(INPUT)  
    val rdAddr  = UInt(INPUT, 8)  
    val rdData  = UInt(OUTPUT, 8)  
  }  
  val mem = Mem(256, UInt(width = 8) )  
  
  // flush this out ...  
  
  io.rdData := UInt(0)  
}
```

```
class LinkIO extends Bundle {  
  val data = UInt(16, OUTPUT)  
  val valid = Bool(OUTPUT)  
}
```

We can then extend SimpleLink by adding parity bits using bundle inheritance:

```
class PLinkIO extends LinkIO {  
  val parity = UInt(5, OUTPUT)  
}
```

In general, users can organize their interfaces into hierarchies using inheritance.

From there we can define a filter interface by nesting two `LinkIO`s into a new `FilterIO` bundle:

```
class FilterIO extends Bundle {  
  val in  = new LinkIO().flip  
  val out = new LinkIO()  
}
```

where `flip` recursively changes the “gender” of a bundle, changing input to output and output to input.

We can now define a filter by defining a filter class extending module:

```
class Filter extends Module {  
  val io = new FilterIO()  
  io.out.valid := io.in.valid  
  io.out.data  := io.in.data  
}
```

where the `io` field contains `FilterIO`.

- write filter that filters out even numbers

```
class Filter extends Module {  
  val io = new FilterIO()  
  
  // flush this out ...  
  
  io.out.valid := Bool(true)  
  io.out.data  := UInt(0)  
}
```



```
class GCDTests(c: GCD) extends Tester(c, Array(c.io)) {  
  defTests {  
    val (a, b, z) = (64, 48, 16)  
    val svars = new HashMap[Node, Node]()  
    val ovars = new HashMap[Node, Node]()  
    var t = 0  
    do {  
      svars(c.io.a) = UInt(a)  
      svars(c.io.b) = UInt(b)  
      step(svars, ovars)  
      t += 1  
    } while (t <= 1 || ovars(c.io.v).litValue() == 0)  
    ovars(c.io.z).litValue() == z  
  }  
}
```

```
class CrossbarIO extends Bundle {  
  val in  = Vec.fill(2){ new LinkIO() }  
  val sel = UInt(INPUT, 2)  
  val out = Vec.fill(2){ new LinkIO() }  
}
```

where `Vec` takes a size as the first argument and a block returning a port as the second argument.

```
class CrossbarIO(n: Int) extends Bundle {  
  val in  = Vec.fill(n){ new LinkIO() }  
  val sel = UInt(INPUT, log2Up(n))  
  val out = Vec.fill(n){ new LinkIO() }  
  override def clone() = new CrossbarIO(n).asInstanceOf[this.type]  
}
```

where `clone` definition fixes cloning, by incorporating the crossbar construction argument `n` in cloning.

We can now compose two filters into a filter block as follows:

```
class Block extends Module {  
  val io = new FilterIO()  
  val f1 = Module(new Filter())  
  val f2 = Module(new Filter())  
  
  f1.io.in  <> io.in  
  f1.io.out <> f2.io.in  
  f2.io.out <> io.out  
}
```

where `Module` is the module constructor function and `<>` bulk connects interfaces:

- Bulk connections connect leaf ports of the same name to each other.
- After all connections are made and the circuit is being elaborated, Chisel warns users if ports have other than exactly one connection to them.

```
def Mux[T <: UInt](c: Bool, con: T, alt: T): T  
  
Mux(c, UInt(10), UInt(11))
```

yields a `UInt` wire because the `con` and `alt` arguments are each of type `UInt`.

$$y[t] = \sum_j w_j * x_j[t - j] \quad (1)$$

```
def delays[T <: Data](x: T, n: Int): List[T] =  
  if (n <= 1) List(x) else x :: delays(Reg(data = x), n-1)  
  
def FIR[T <: Num](w: Seq[T], x: T): T =  
  (w, delays(x, hs.length)).zipped.map( _ * _ ).reduceRight( _ + _ )
```

```
class FilterIO[T <: Data]() (data: => T) extends Bundle {  
  val in  = data.asInput.flip  
  val out = data.asOutput  
}  
  
class Filter[T <: Data]() (data: => T) extends Module {  
  val io = new FilterIO() { data }  
  ...  
}
```

```
class Decoupled[T <: Data](type: T) extends Bundle {  
  val ready = Bool(INPUT)  
  val valid = Bool(OUTPUT)  
  val bits  = type.asOutput  
}  
  
class Valid[+T <: Data](type: T) extends Bundle {  
  val valid = Bool(OUTPUT)  
  val bits  = type.asOutput  
}
```



```
class RealGCDInput extends Bundle {  
  val a = UInt(width = 16)  
  val b = UInt(width = 16)  
}  
  
class RealGCD extends Module {  
  val io = new Bundle {  
    val in = new Decoupled( new RealGCDInput() ).flip()  
    val out = new Valid( UInt(width = 16) )  
  }  
  
  // flush this out ...  
}
```

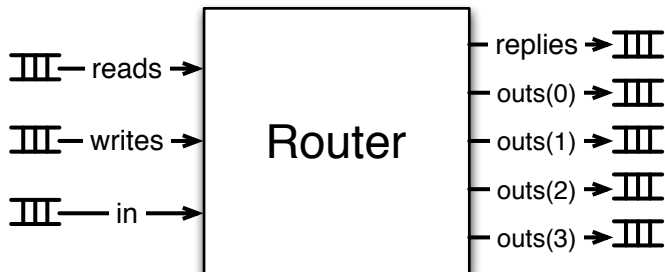
```
class EnqIO[T <: Data]() (data: T) extends FIFOIO()(data) {
  def enq(dat: T): T = { valid := Bool(true); data := dat; dat }
  valid := Bool(false);
  for (io <- data.flatten.map(x => x._2))
    io := UInt(0, io.getWidth());
}

class DeqIO[T <: Data](type: T) extends FIFOIO()(data) {
  flip()
  ready := Bool(false);
  def deq(b: Boolean = false): T = { ready := Bool(true); data }
}

class Filter[T <: Data](type: T) extends Module {
  val io = new Bundle {
    val in  = new DeqIO( data )
    val out = new EnqIO( data )
  }
  when (io.in.valid && io.out.ready) {
    io.out.enq(io.in.deq())
  }
}
```

```
class ReadCmd extends Bundle {  
  val addr = UInt(width = 32)  
}  
  
class WriteCmd extends ReadCmd {  
  val data = UInt(width = 32)  
}  
  
class Packet extends Bundle {  
  val header = UInt(width = 8)  
  val body   = UInt(width = 64)  
}  
  
class RouterIO(n: Int) extends Bundle {  
  override def clone = new RouterIO(n).asInstanceOf[this.type]  
  val reads  = new DeqIO( new ReadCmd() )  
  val replies = new EnqIO( UInt(width = 8) )  
  val writes = new DeqIO( new WriteCmd() )  
  val in     = new DeqIO( new Packet() )  
  val outs   = Vec.fill(n){ new EnqIO(){ new Packet() } }  
}
```

```
class Router extends Module {  
  val depth = 32;  
  val n      = 4;  
  val io     = new RouterIO(n);  
  val tbl    = Mem(depth, UInt(width = sizeof(n)) );  
  
  // flush it out ...  
}
```



- git
- sbt
- project directory structure
- project file
- installation

```
cd ${HOME}
git clone git@github.com:ucb-bar/chisel.git
export CHISEL=${HOME}/chisel
git pull
git status
git log
git add filename
git commit -m "comment"
git push
```

```
cd ${CHISEL}/tutorial/sbt  
sbt  
project tutorial  
compile  
run  
console
```

```
chisel/  
  tutorial/  
  src/  
gpu/  
  sbt/  
    project/build.scala # edit this as shown below  
  src/                  # your source files go here  
    gpu.scala  
  emulator/             # your C++ target can go here
```



```
import sbt._
import Keys._

object BuildSettings {
  val buildOrganization = "edu.berkeley.cs"
  val buildVersion = "1.1"
  val buildScalaVersion = "2.9.2"

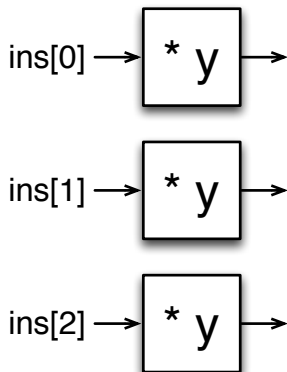
  def apply(projectdir: String) = {
    Defaults.defaultSettings ++ Seq (
      organization := buildOrganization,
      version      := buildVersion,
      scalaVersion := buildScalaVersion,
      scalaSource in Compile := Path.absolute(file(projectdir + "/src"))
    )
  }
}

object ChiselBuild extends Build {
  import BuildSettings._
  val chiselDir = System.getProperty("CHISEL")
  lazy val chisel =
    Project("chisel", file("chisel"),
      settings = BuildSettings(chiselDir))
  lazy val gpu =
    Project("gpu", file("gpu"),
      settings = BuildSettings("."))
    dependsOn(chisel)
}
```

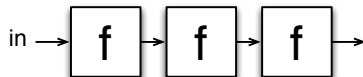
- on mac install:
 - XCODE console tools
 - <http://www.macports.org>
- on windows install:
 - cygwin
- everywhere install:
 - git
 - g++
 - java
- everywhere
 - `export $CHISEL=...`
 - `git clone https://github.com/ucb-bar/chisel.git`

audio processing	Echo.scala
image processing	Darken.scala
risc processor	Risc.scala
game of life	Life.scala
router	Router.scala
map/reduce	<i>see next slide</i>
network	
fft	
cryptography	
serial multiplier	
pong	

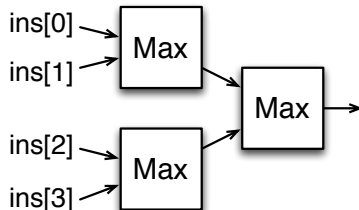
Map($ins, x \Rightarrow x * y$)



Chain($n, in, x \Rightarrow f(x)$)



Reduce(ins, Max)



website	<code>chisel.eecs.berkeley.edu</code>
mailing list	<code>groups.google.com/group/chisel-users</code>
github	<code>https://github.com/ucb-bar/chisel/</code>
me	<code>jrb@pobox.com</code>

- **Arrangements** – Roxana and Tammy
- **EC2 configuration** – Henry Cook and Michael Armbrust
- **Bootcamp Materials** – Huy Vo and Andrew Waterman
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