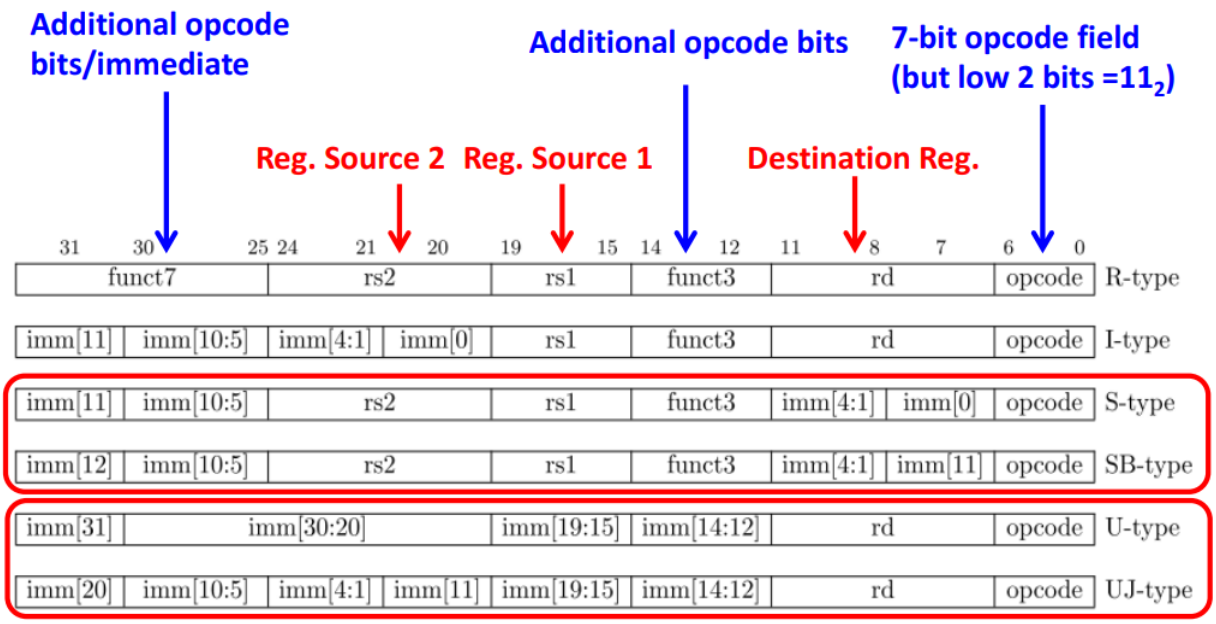
CO502 - Computer Architecture
Lab 01 - part 1
Group 04

01.Describe the instructions.
We have chosen 32 bits RISC-V Pipeline Implementation

Instruction	Type	Description
ADD	R-Type	Addition
SUB	R-Type	Substitution
SLL	R-Type	Shift Left Logic
SLT	R-Type	Set Less Than
SLTU	R-Type	Set Less Than Unsigned
XOR	R-Type	Bitwise XOR
SRL	R-Type	Shift Right Left
SRA	R-Type	Shift Right Arithmetic
OR	R-Type	Bitwise OR
AND	R-Type	Bitwise AND
MUL	R-Type	Multiplication
MULH	R-Type	Multiplication signed x signed and return upper half (32 bits)
MULHSU	R-Type	Multiplication signed x unsigned and return upper half (32 bits)
MULHU	R-Type	Multiplication unsigned x unsigned and return upper half (32 bits)
DIV	R-Type	Integer Division
REM	R-Type	Remainder of signed integer division
REMU	R-Type	Remainder of unsigned integer division
LB	I-Type	Load Byte
LH	I-Type	Load Half word (2 Bytes)
LW	I-Type	Load Word (4 Bytes)
LBU	I-Type	Load Byte Unsigned
LHU	I-Type	Load Half Byte Unsigned
ADDI	I-Type	Addition Immediate
SLLI	I-Type	Shift Left Logic By Immediate
SLTI	I-Type	Set Less Than By Immediate
SLTIU	I-Type	Set Less Than Unsigned By Immediate
XORI	I-Type	Bitwise XOR with Immediate
SRLI	I-Type	Shift Right Logic By Immediate (Shifting by logic val of immediate)
SRAI	I-Type	Shift Right Arithmetic By Immediate (Shifting by arithmetic val of immediate)

ORI	I-Type	Bitwise OR with Immediate value
ANDI	I-Type	Bitwise AND with immediate value
JALR	I-Type	Jump and Link Register
FENCE		Fence - This to ensure all the operation before FENCE observed before operation after the Fence
FENCE.I		Fence Instruction
SB	S-Type	Store Byte
SH	S-Type	Store Half Word
SW	S-Type	Store word
SBU	S-Type	Store unsigned Byte
SHU	S-Type	Store unsigned half word
BLT	B-Type	Branch Less Than
BGE	B-Type	Branch Greater Than or equal
BLTU	B-Type	Branch Less Than Unsigned
BGEU	B-Type	Branch Greater Than or Equal Unsigned
AUIPC	U-type	Add Upper Immediate to PC
LUI	U-type	Load Upper Immediate
JAL	J-Type	Jump and Link (Unconditional Jumps)

02.Clearly identify instruction encoding formats.



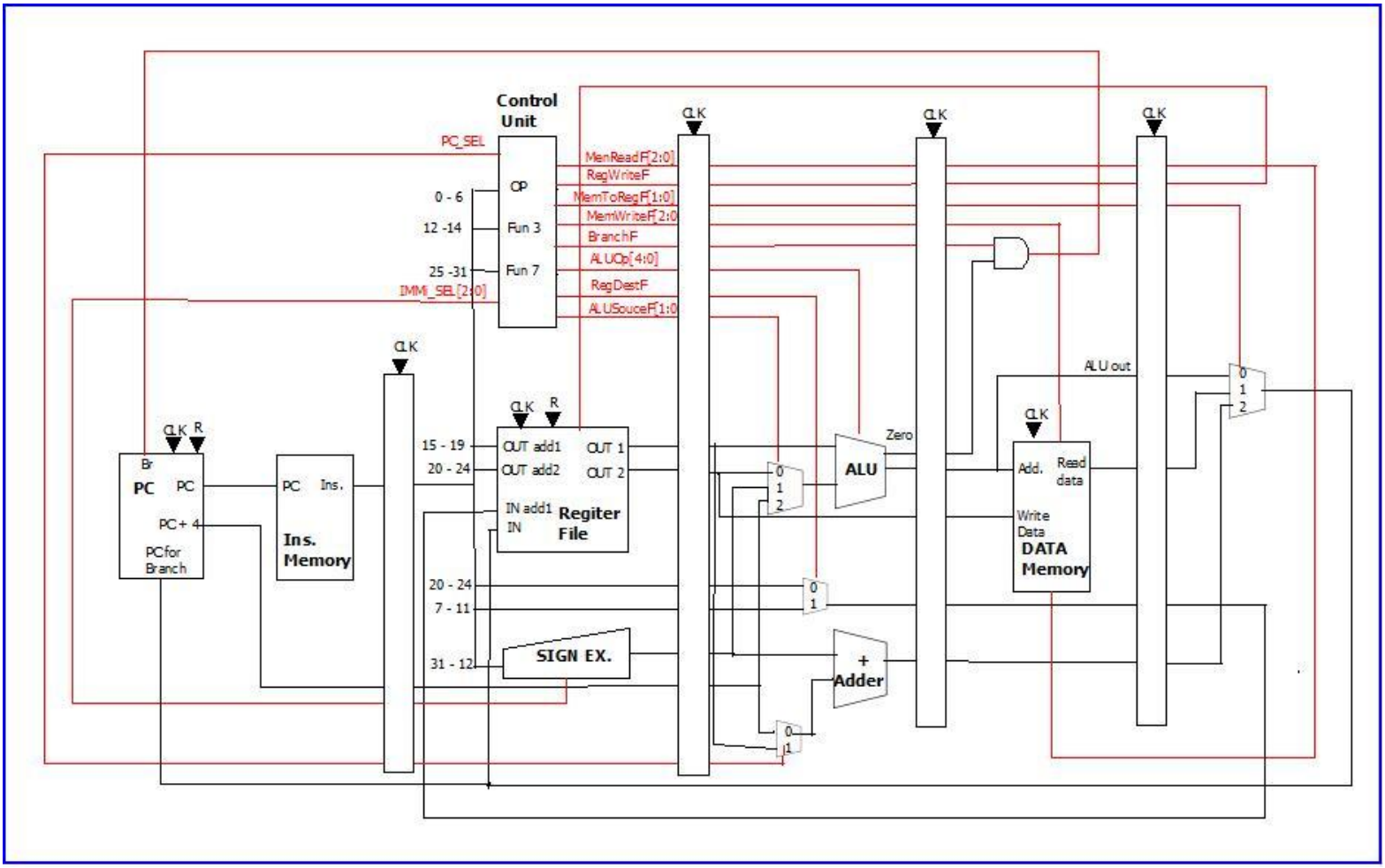
03.Clearly identify opcodes.

Instruction	Type	op-code	function 3	function 7
LB	I-Type	**0000011**	000	
LH	I-Type	**0000011**	001	
LW	I-Type	**0000011**	010	
LBU	I-Type	**0000011**	100	
LHU	I-Type	**0000011**	101	
FENCE		**0001111**	000	
FENCE.I		**0001111**	001	
ADDI	I-Type	**0010011**	000	
SLLI	I-Type	**0010011**	001	
SLTI	I-Type	**0010011**	010	
SLTIU	I-Type	**0010011**	011	
XORI	I-Type	**0010011**	100	
SRLI	I-Type	**0010011**	101	
SRAI	I-Type	**0010011**	101	
ORI	I-Type	**0010011**	110	
ANDI	I-Type	**0010011**	111	
AUIPC	U-type	**0010011**		
SB	S-Type	**0100011**	000	
SH	S-Type	**0100011**	001	
SW	S-Type	**0100011**	010	
SBU	S-Type	**0100011**	100	
SHU	S-Type	**0100011**	101	
ADD	R-Type	**0110011**	000	0000000
SUB	R-Type	**0110011**	000	0100000
SLL	R-Type	**0110011**	001	0000000
SLT	R-Type	**0110011**	010	0000000
SLTU	R-Type	**0110011**	011	0000000
XOR	R-Type	**0110011**	100	0000000
SRL	R-Type	**0110011**	101	0000000
SRA	R-Type	**0110011**	101	0100000
OR	R-Type	**0110011**	110	0000000
AND	R-Type	**0110011**	111	0000000
MUL	R-Type	**0110011**	000	0111011
MULH	R-Type	**0110011**	001	0111011

MULHSU	R-Type	**0110011**	010	0111011
MULHU	R-Type	**0110011**	011	0111011
DIV	R-Type	**0110011**	100	0111011
REM	R-Type	**0110011**	101	0111011
REMU	R-Type	**0110011**	111	0111011
LUI	U-type	**0110111**		
JALR	I-Type	**1100111**		
JAL	J-Type	**1101111**		
BEQ	B-Type	**1101111**	000	
BNE	B-Type	**1101111**	001	
BLT	B-Type	**1101111**	100	
BGE	B-Type	**1101111**	101	
BLTU	B-Type	**1101111**	110	
BGEU	B-Type	**1101111**	111	

Activity 2

Draw a pipeline diagram with datapath and control , identify the hardware and control signals



Control signals

1. **Memory Read Flag**
2. **Register write Flag**
3. **Memory to register Flag**
4. **Memory write Flag**
5. **Branch Flag**
6. **ALU opcode**
7. **Register destination Flag**
8. **ALU source Flag**
9. **IMMediate value selector**
10. **PC selector**