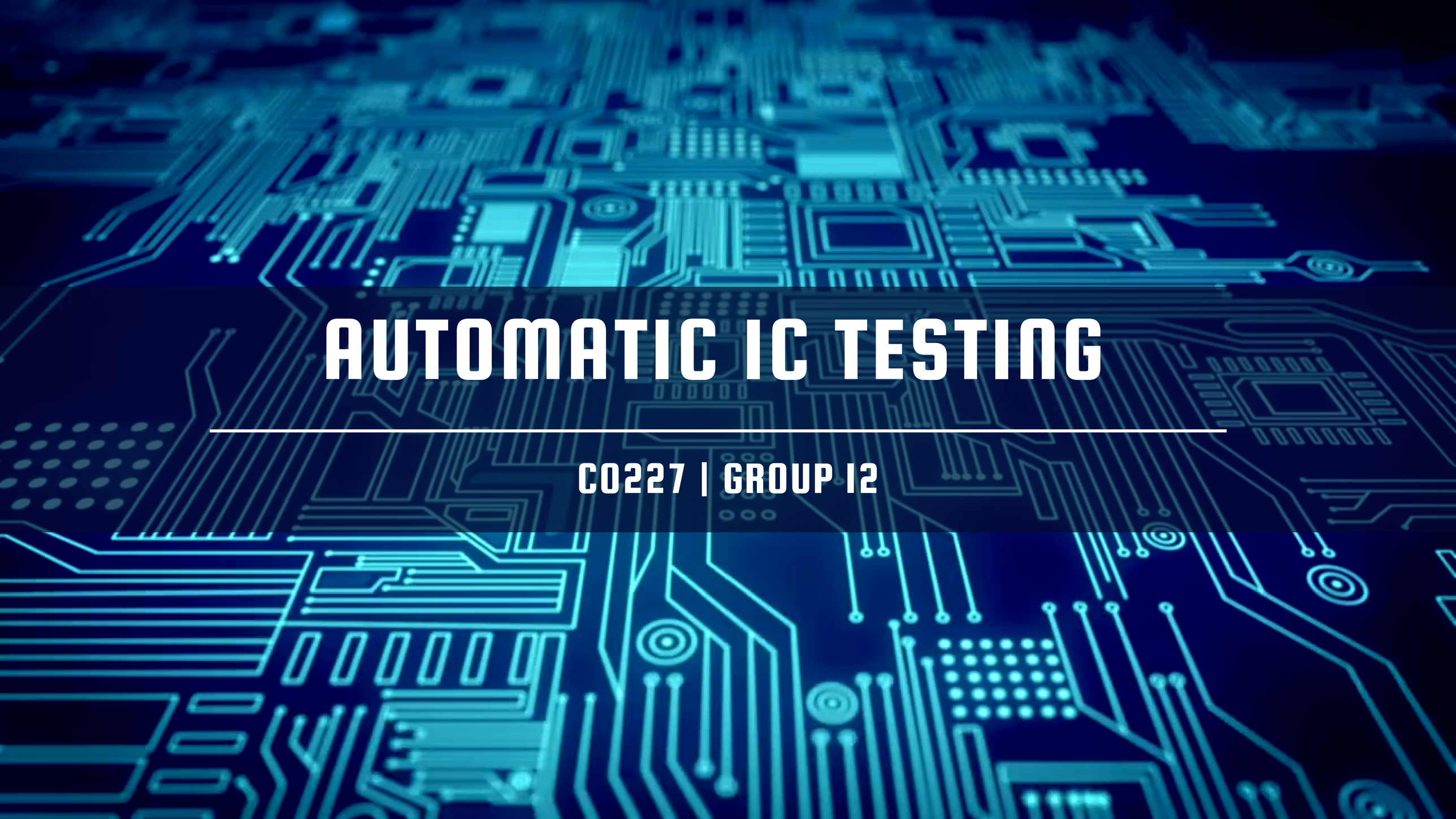


AUTOMATIC IC TESTING

C0227 | GROUP 12

Meet Our Team

Asela

Janitha

Nuwantha

Ashan

Table Of Content

Understanding The Problem

The Problem with modern IC testers

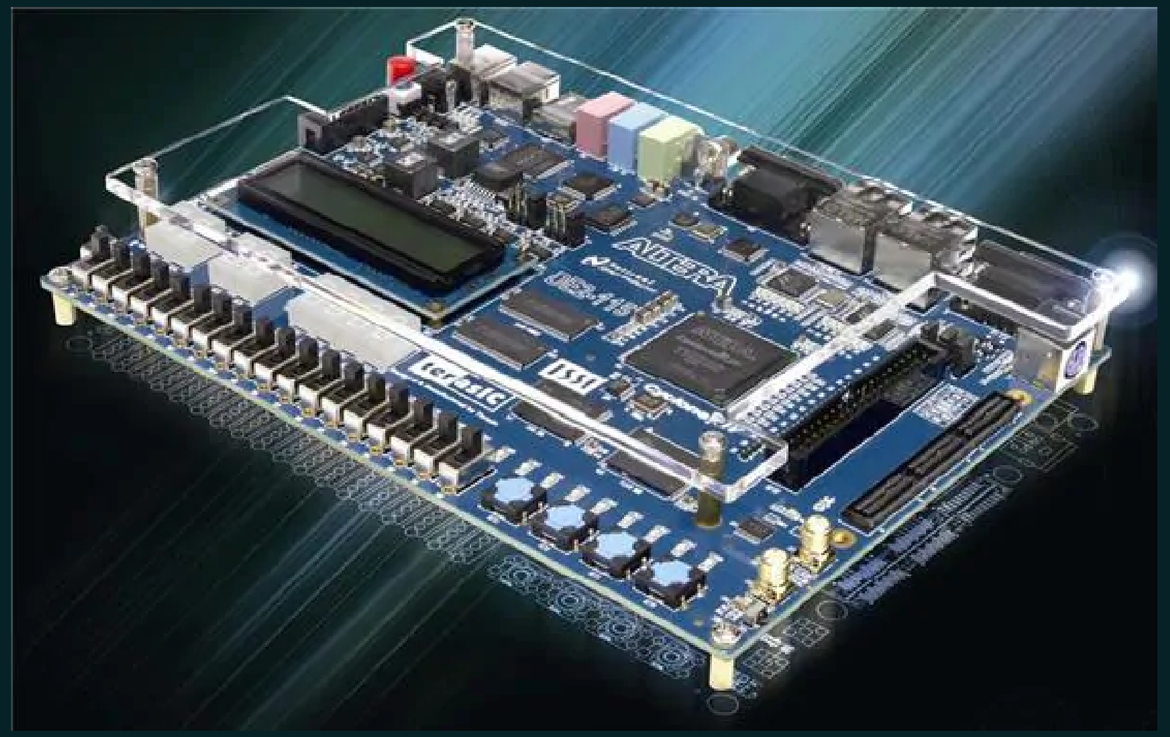
- Costly and Inefficient Testing Tools
- Limited Range of ICs
- Lack of Reprogrammability
- Need for User-Friendly Solutions
- Focus on Cost-Effectiveness
- Versatility Requirement

Understanding The Solution

- Check each gate of IC individually for the expected result
- Display the result on the 7-segment display and LCD displat

Components

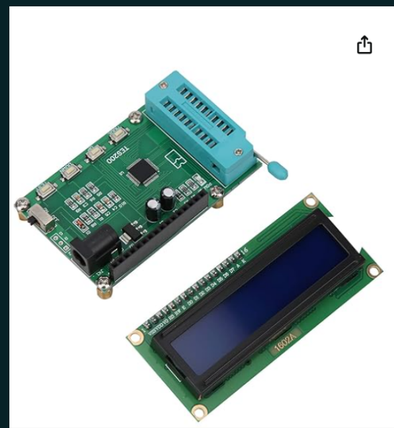
- FPGA Development Board
- Testing ICs
- ZIF Socket
- Jumper Wires



Bill Of Material (BOM)

Component Name	Quantity	Unit Cost(LKR)	Cost(LKR)
FPGA Board EP1C3T144	1	16 000	16 000
Jumper Wires	30	8	240
ZIF Socket	1	120	120
Testing ICs	5	100	500
Total Cost			16 860

Bill Of Material (BOM)



IC Tester Digital Meter, Corrosion-resistant IC Tester Anti-oxidation Simple for General Purpose for Professional Use for Electronic Component for Factory

Brand: HUADM

-50% ₹7,155

M.R.P.: ~~₹14,310~~

Inclusive of all taxes

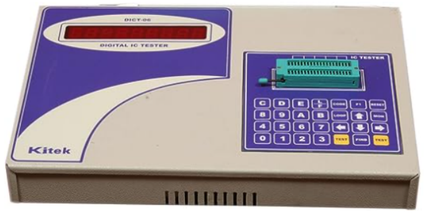
EMI starts at ₹347. No Cost EMI available EMI options

Offers

Bank Offer	No Cost EMI	Partner Offers
Upto ₹715.50 discount on SBI Credit Cards	Upto ₹322.18 EMI interest savings on Amazon Pay ICICI…	Get GST invoice and save up to 28% on business purchases.
2 offers ›	1 offer ›	1 offer ›

Cost for a IC Tester in the market

22000 - 88 000 LKR



ASICO Digital IC Tester

Brand: ASICO

₹22,000

Inclusive of all taxes

EMI starts at ₹1,067. No Cost EMI available EMI options

Offers

Bank Offer	No Cost EMI	Partner Offers
Upto ₹1,500.00 discount on SBI Credit Cards	Upto ₹990.61 EMI interest savings on Amazon Pay ICICI…	Get GST invoice and save up to 28% on business purchases.
2 offers ›	1 offer ›	1 offer ›

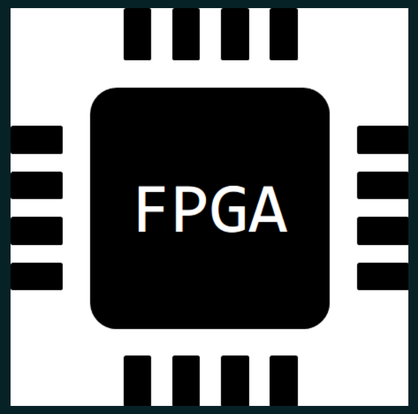
But in out solution

It’s only **17 000 LKR**

Technology Stack

What Technologies we are going to use ?

- FPGA Development Board - Altera DE2-115
- HDL (Hardware Description Language) - Verilog
- FPGA Synthesis Tool: Quartus II
- Simulation Tool: MultiSim
- Version Control: Git



Solution Architecture
High-Level Overview

1. There is a Zero Insertion Force (ZIF) Socket to configure the IC.

2. The IC number is taken by the board as the user input through the IR sensor module.

3. Then, the related data associated with the particular IC is fetched which includes testing patterns, pin configurations, and all required other data.

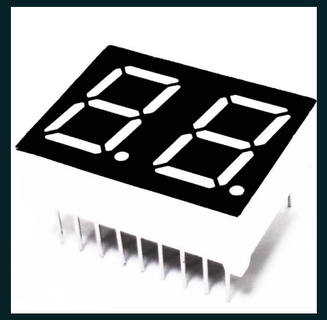
4. Then the IC is tested testing patterns and compared the result with the expected output.

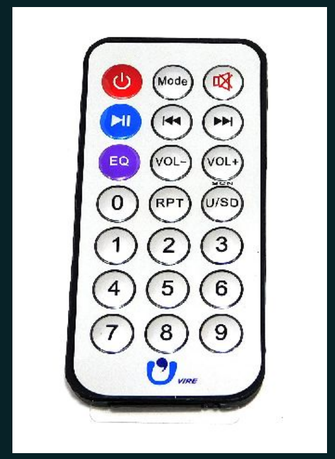
5. Finally, the result is displayed whether it is fully functional or not.If there is an error in a gate ,it is indicated in the LCD board and in the seven segment display.

Solution Architecture
High-Level Overview

The system consist of these modules for above functionalities

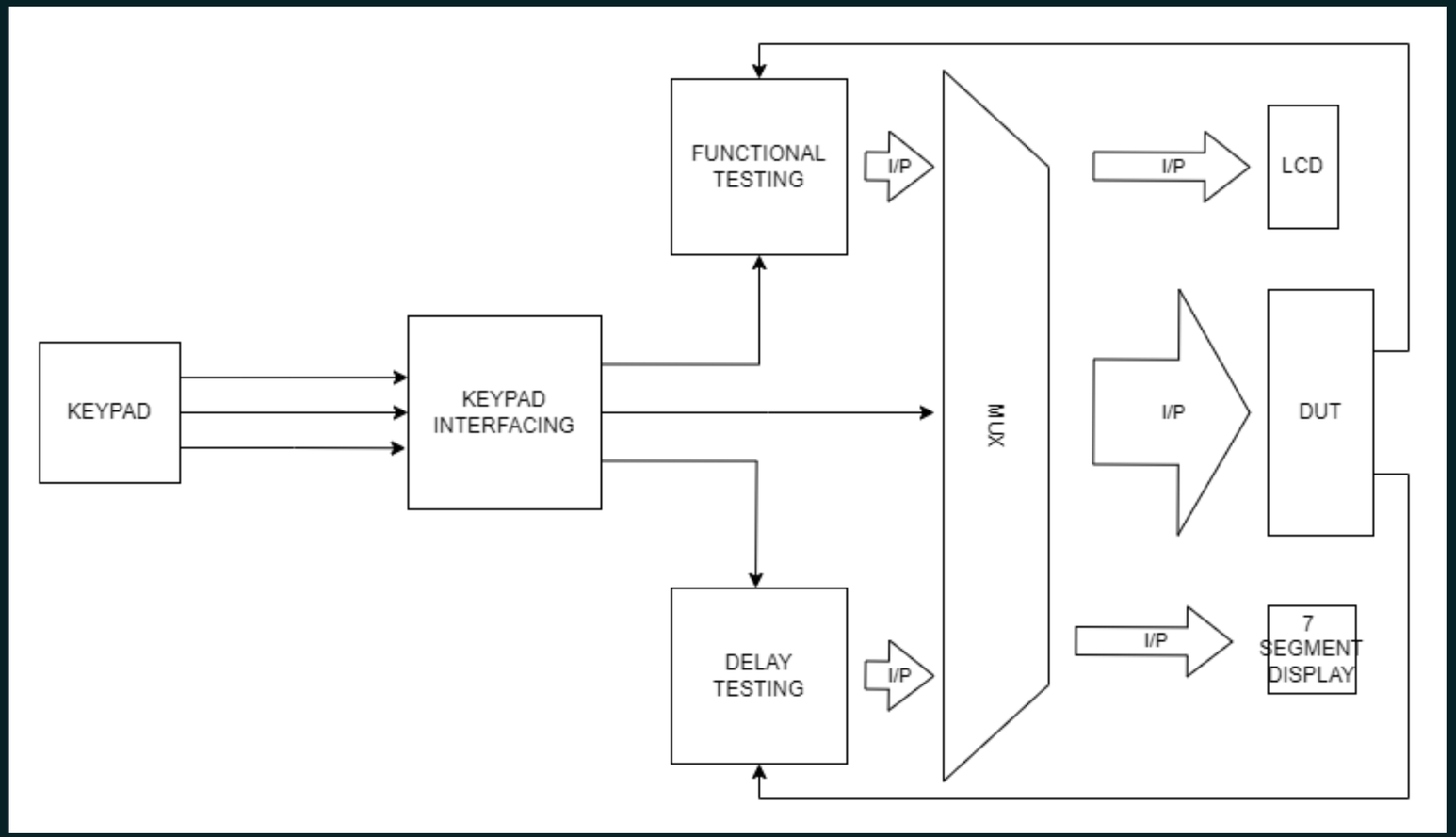
- IR Reciver interface Module - To Get the IC Number
- 7 Segmet Display Module - Display the Entered IC Number
- Logical IC Tester Module - Test the IC
- LCD Display Module - Show the IC State





Solution Architecture
Data Flow

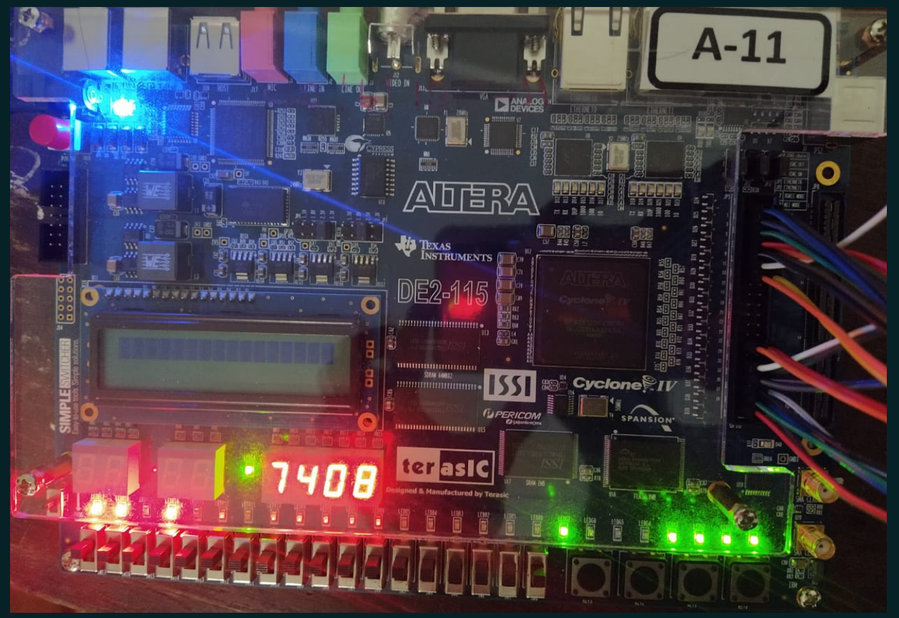
Primary Data Flow of our Solution



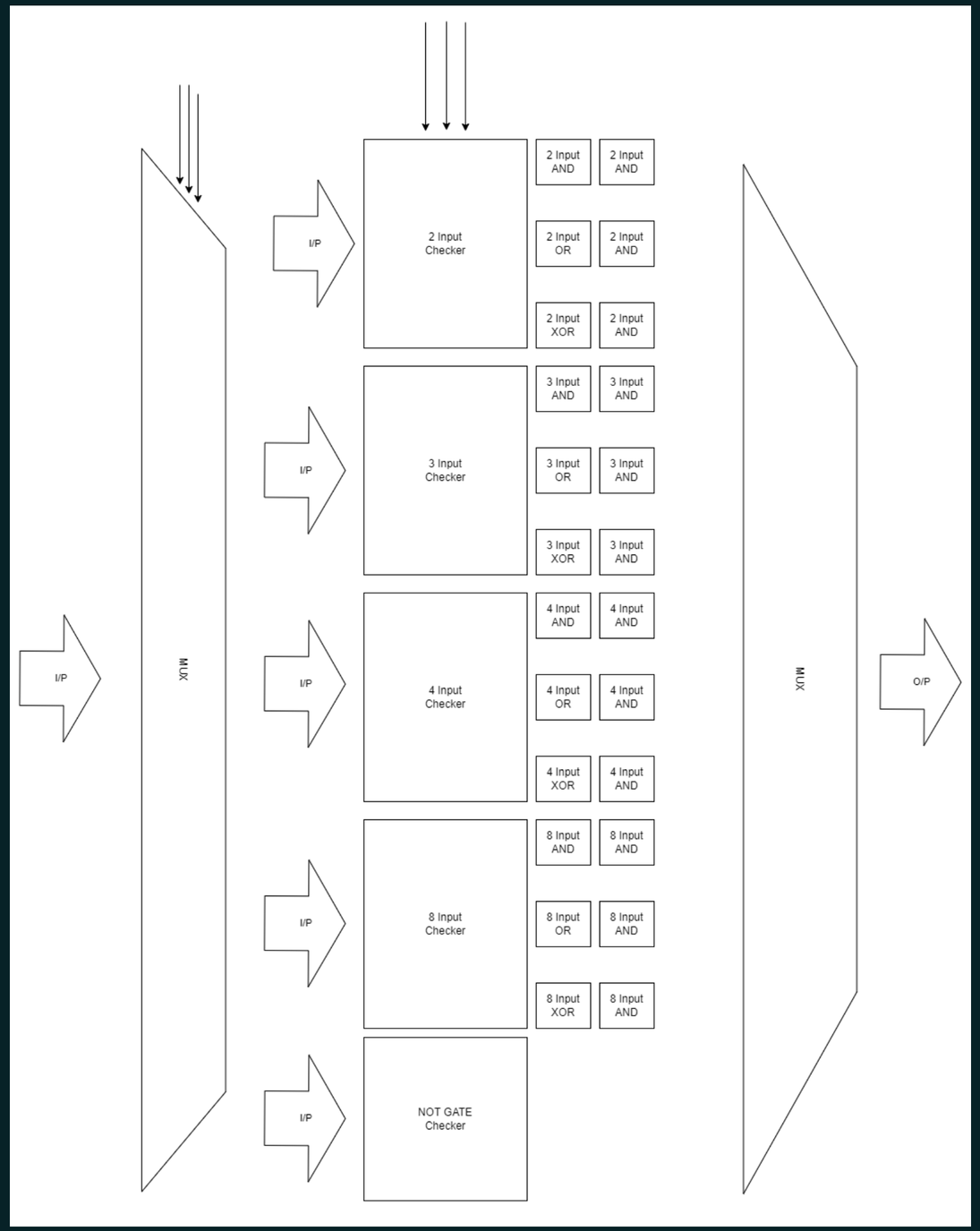
Solution Architecture
Data Flow

The Logical Tester Module consist of these sub modules to perform its functionality.

- Not Gate Checker
- Two Input Checker
- Three Input Checker
- Four Input Checker
- Eight Input Checker



Data Flow in the Logical Tester Module



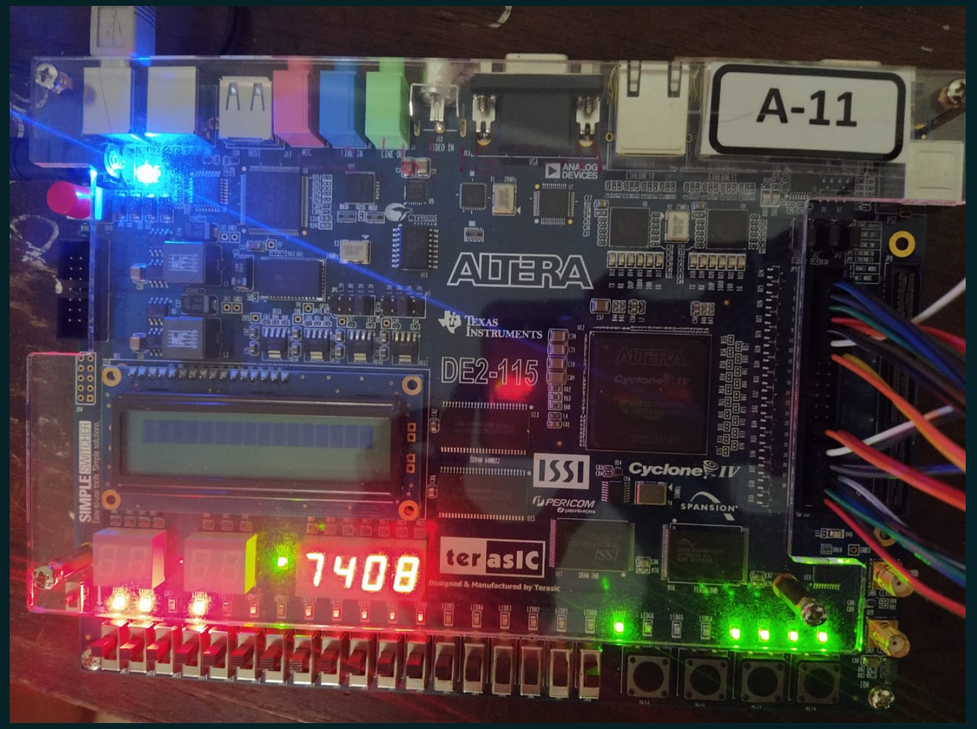
Current Process

Successfully Implemented and Integrated

- Logical Tester Module
- IR Module (To Get the IC Number)
- Seven Segment Module

Still in the Development Stage

- LCD Display Module



Version Controlling & Documentation

GitHub Repository

Project Page

https://cepdnaclk.github.io/e19-co227-Automatic-IC-Testing-Application-Using-FPGA/

DEMOSTRATION

Q & A ?

THANK YOU!