

Universidad de las Ame´ricas Puebla

Escuela de ingenier´ıa

Departamento de computacio´n,

y mecatro´nica

electro´nica

**Lab report #1**

**Course:**

**Digital design LRT2022-secci´on**

**Equipo: Mesa 1**

Id del estudiante 1

Id del estudiante 2

Nombre 1

Nombre 2

April 1st, 2022, San Andr´es Cholula, Puebla

UDLAP

CEM

**1**

[[1](#_bookmark0)]

**Secci´on**

*x* >0

e Item 1

e Item 2

e Item 3

e Item 4

**1.1**

[[2](#_bookmark1)]

**Subseccio´n**

**1.1.1**

**Sub-subsecci´on**

1

Digital design

C´odigo 1: C´odigo desde archivo

== *Simple AND gate design*

**l ibrary** IEEE ;

**use** IEEE . s t d l o g i c 1 1 6 4 . **a l l** ;

**entity** and gate **i s port** (

a **in** s t d l o g i c ;

b **in** s t d l o g i c ;

q **out** s t d l o g i c ) ;

**end** and gate ;

**architecture** r t l **of** and gate **i s begin**

q = a **and** b ;

**end** r t l ;

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2

Digital design

C´odigo 2: C´odigo en VHDL

**l ibrary** IEEE ;

**use** IEEE . STD LOGIC 1164 .**ALL**;

**use** IEEE . s t d l o g i c u n s i g n e d . **a l l** ;

**entity** Contador 0 9 **i s**

**Port** ( clock 100 Mhz : **in** STD LOGIC; r e s e t : **in** STD LOGIC;

Anode Activate : **out** STD LOGIC VECTOR ( 3 **downto** 0 ) ; LED out : **out** STD LOGIC VECTOR ( 6 **downto** 0 ) ;

Led0 : **out** STD LOGIC: = ’ 0 ’ ;

Led1 : **out** s t d l o g i c : = ’ 0 ’ ) ; *COMMENT*

**end** Contador 0 9 ;

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**A**

**C´odigos**

**completos**

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**References**

[1]

gh. (2020) Ctan. [En l´ınea]. Disponible: <https://www.ctan.org/>

[2]

V. Agarwal and Instructables, “Minimalistic word clock,” Jul 2019. [En l´ınea]. Disponible:

<https://www.instructables.com/id/Minimalistic-Word-Clock/>

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Digital design