STT-RAM Memory Hierarchy Designs Aimed to Performance, Reliability and Energy Consumption

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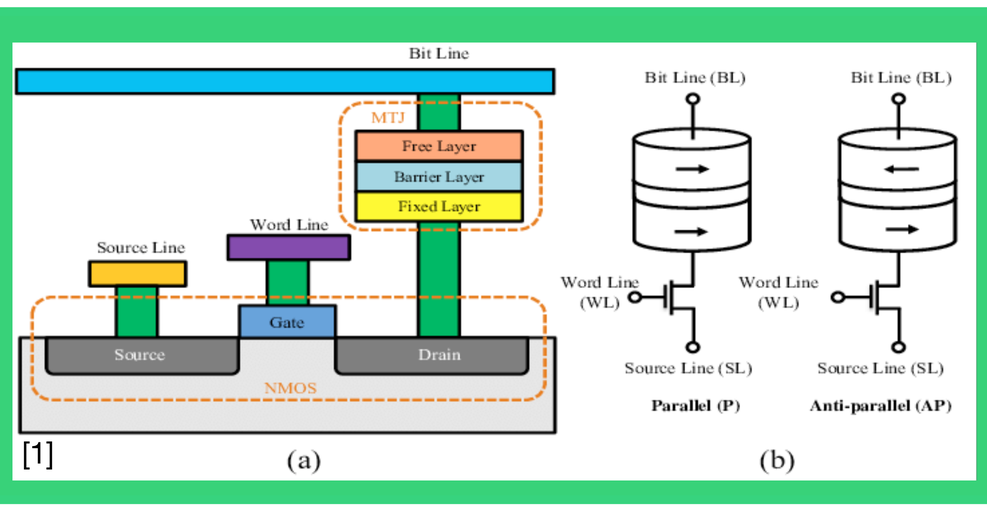
Background

- Current applications demand **larger on-chip memory capacity** since off-chip memory accesses become a problem.
- STT-RAM technology has come to be a real alternative to build LLC due to SRAM area and energy expenses.



STT-RAM cell **MTJ** with two magnetic layers:

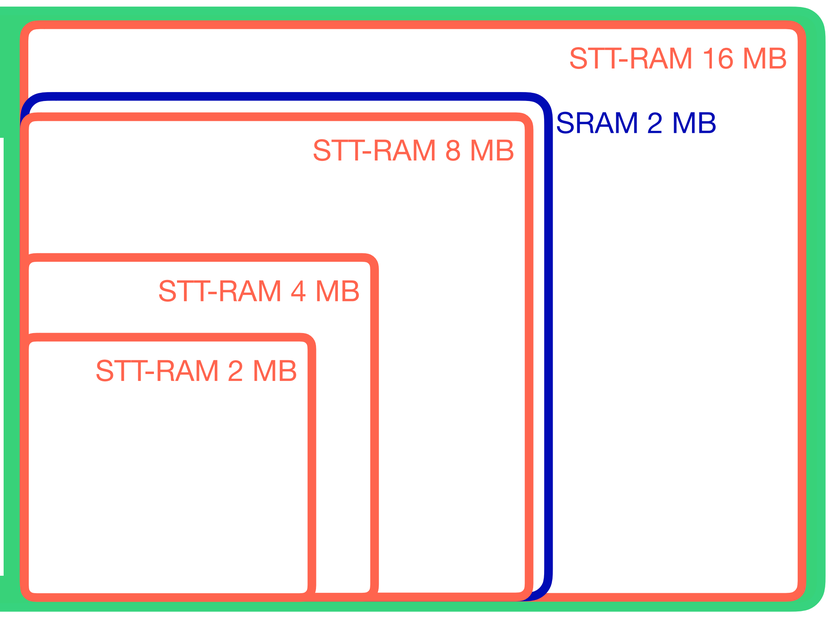
- **Fixed** layer. Reference magnetic field.
- **Free** layer. The magnetic field orientation determines the stored logical value ('0' / '1').

STT-RAM vs. SRAM

vs. SRAM 2MB	2 MB	4 MB	8 MB	16 MB
Area	0,29	0,45	0,92	1,70
Read latency	1,16	1,13	1,32	1,57
Write latency	3,58	3,61	3,65	3,78
Read energy	0,58	0,94	1,20	1,88
Write energy	1,96	2,18	2,44	2,92
Static power	0,41	0,90	1,62	3,44

STT-RAM (NVSim)
SRAM (CACTI-P)

- 45 nm
- Sequential access
- Write EDP optimization
- Vdd = 0,9 v
- 320 K (47 ºC)

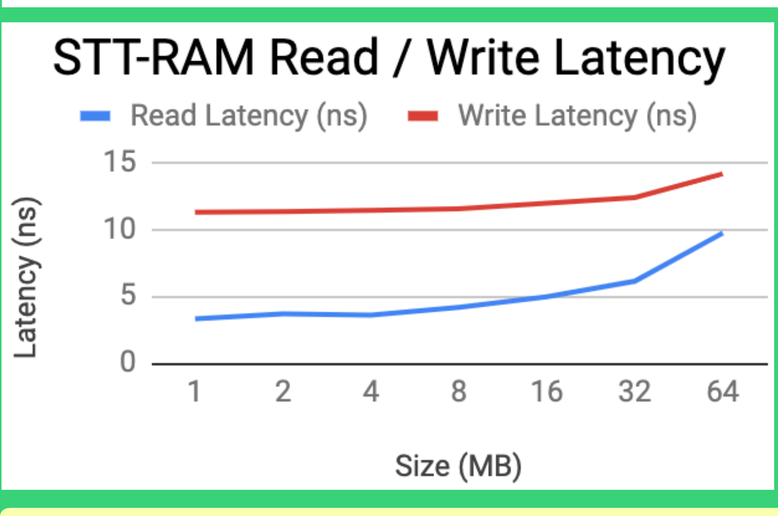


New Challenges in the STT-RAM Memory Hierarchy Designs

Big bitcell (≥ 32 nm)

Read and write operations are asymmetric:

- **Write operations** are more **expensive** in terms of **latency** and **energy** consumption than read operations.
- Even more expensive than SRAM write operations.



STT-RAM (NVSim)

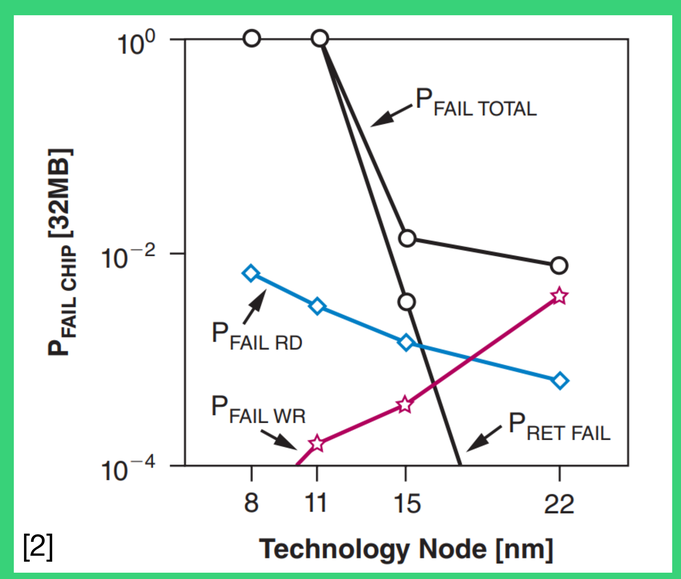
- 45 nm
- Sequential access
- Write EDP optimization
- Vdd = 0,9 v
- 320 K (47 ºC)

Goals: Performance and energy consumption

- **Minimize** the **number** of write operations on STT-RAM cells.
- STT-RAM and SRAM **hybrid** cache designs.
- Specific replacement algorithms and content management policies in order to **reduce** the write operations **drawbacks**.

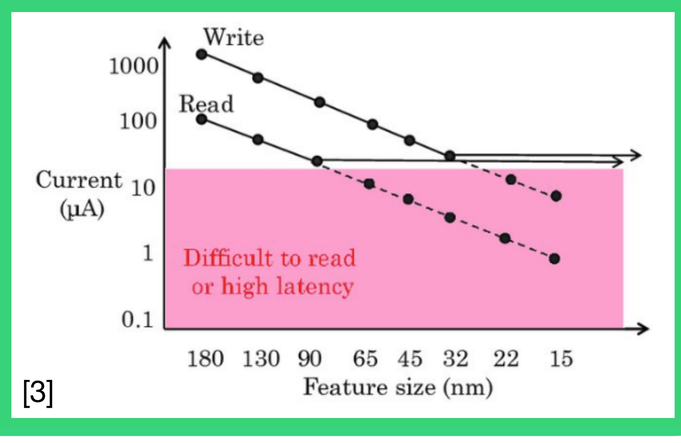
Small bitcell (< 32 nm)

- **Write errors**. The write operation ends up with the opposite value.
- **Read Disturbance Errors** (RDE). The read operation accidentally flips the cell content.
- **Retention errors.** Even idle cells randomly experience loss of information.



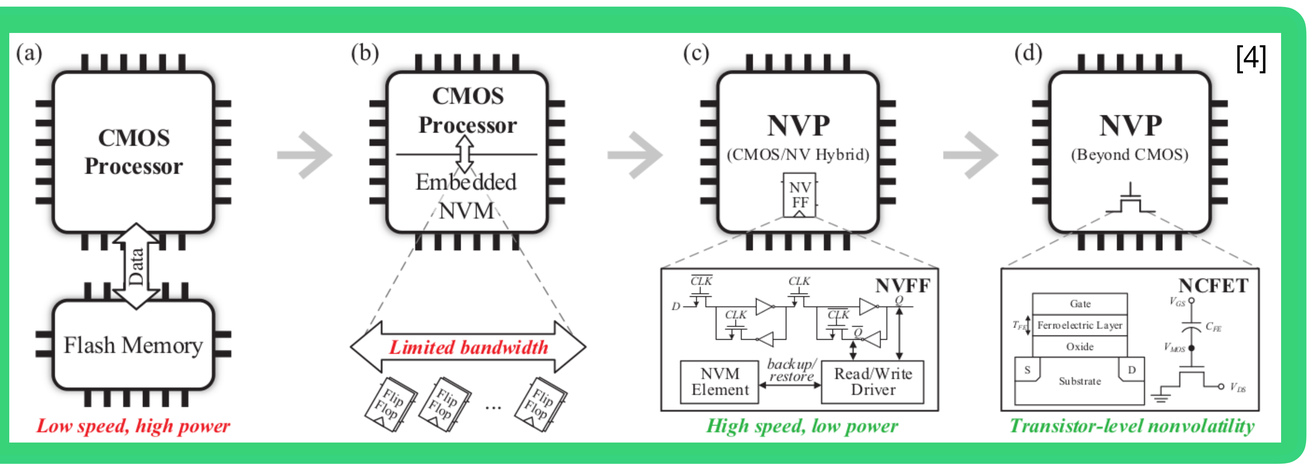
Goals: Reliability

New techniques to manage **redundant information** that allows **error detection** and **information recovery**.



Non-Volatile Processors (NVP)

- Fed by **intermittent power sources**.
- Frequent shutdowns.
- Backup / recovery.
- STT-RAM cells aimed to low level caches (L1). **New trade-offs**.



References

[1] S. M. Seyedzadeh et al., "Leveraging ECC to Mitigate Read Disturbance, False Reads and Write Faults in STT-RAM," *DSN* 2016

[2] H. Naeimi et al., "STT-RAM Scaling and Retention Failure," *Intel Technology Journal* 2013.

[3] S. Mittal, "A Survey of Soft-Error Mitigation Techniques for Non-Volatile Memories." *Computers* 2017

[4] F. Su et al., "Nonvolatile processors: Why is it trending?." *DATE* 2017.