

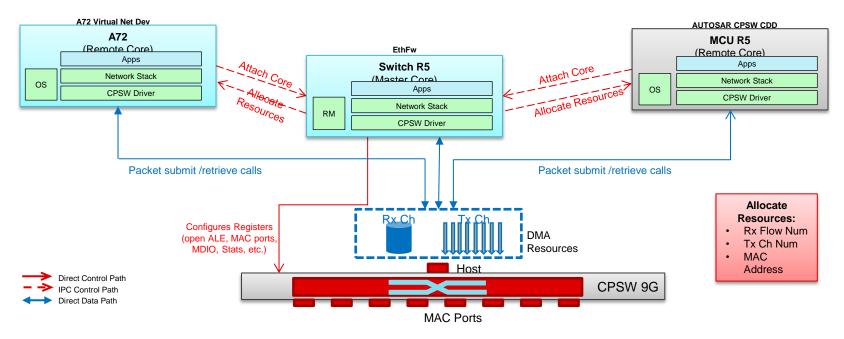
Agenda

- Why Multi-core time synchronization?
- Multi-core Ethernet architecture
- Multi-core Time-synchronization design
 - Time Sync Router Configuration
 - Coupling remote core timer with CPTS
 - Multi core Time Synchronization sequence
- Example

Why Multi-core time synchronization?

- In Multi-core Ethernet architecture of Jacinto 7 family of devices, the control path of CPSW9G IP is solely controlled by the Main domain R5 core(EthFw), preventing other cores in the SoC to change CPSW9G configurations.
- Common Platform Time Sync (CPTS), one of the IP sub-module of CPSW9G used for packet time-stamping is also controlled solely by the EthFw.
- EthFw uses this CPTS timer and synchronizes itself with a master in the network using PTP stack.
- So, a mechanism to provide time synchronization support to time-sensitive applications on remote cores is necessary in Ethernet firmware.

Multi-core Ethernet architecture

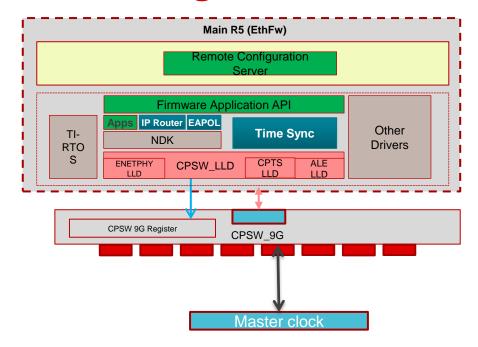


- Once the switch is configured via the firmware on Main R5, other CPUs on the SoC can perform network IO simultaneously without involving the Main R5 core.
- Subsequent packet IO can happen directly between the CPU specific network stack and switch HW via UDMA.

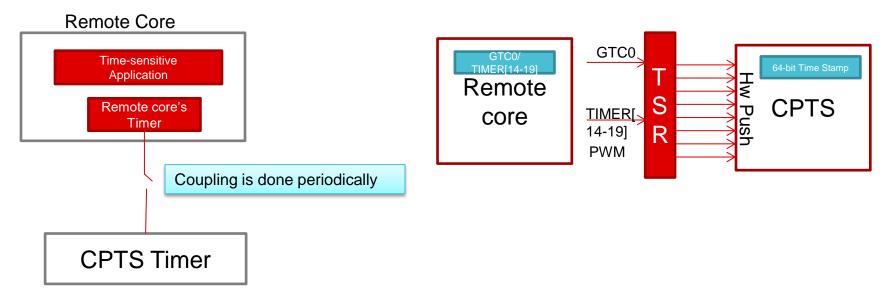


Multi-core Time-synchronization design

- Ethernet firmware running on Main R5 core configures Time Sync PTP stack and enables it.
- Time Sync PTP stack synchronizes CPSW's CPTS timer with the Master clock in network.
- Using Ethernet remote configuration framework, EthFw provides timer coupling support to remote cores, and let them subscribe for callback notifications.
- Ethfw uses Time Sync Router to route remote core timer's event to hardware push of CPTS timer.
- CPTS timer timestamps every hardware push event from remote core and returns the timestamps.

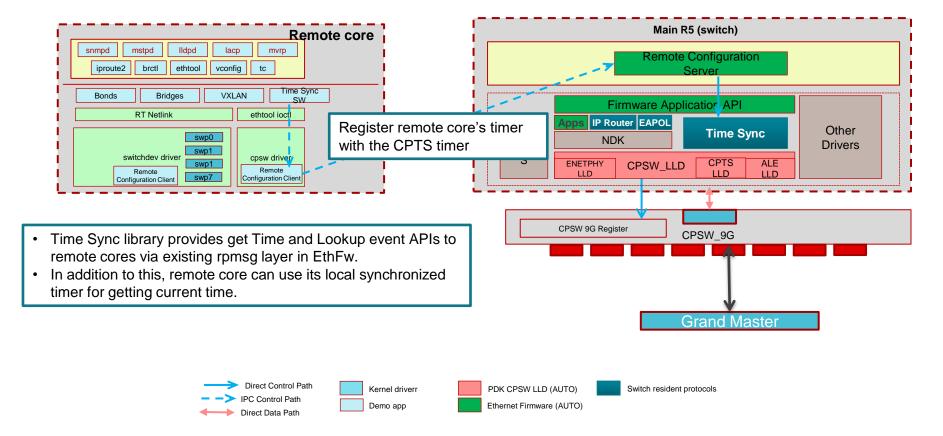


Time Sync Router Configuration



- Coupling between remote core's timer and CPTS timer is done through Hardware push events of CPTS and Time Sync Router(TSR).
- With this a linear relation is established between CPTS & remote timer.
- Once the relation is established, remote core can independently use this coupled timer locally.

Coupling remote core timer with CPTS



Multi – core Time Synchronization sequence



- 2. Sets up DM TIMER[14-19] / GTC0 and enable periodic PWM output/ HW push output
- Call CpswProxy_registerRemoteTimer with timer Information & call back function.

 With two consecutive Hw push Time stamp values, the DMTIMER/GTC to CPTS clock rate ratio and linear relationship are established.

$$T = r * t + C$$

T – Synchronized Time (CPTS time)

- r Rate ratio
- t Local Timer Value
- C Constant value

IPC

Register HW Push

Call back with Event Info

Hw Push Time stamp value N

Call back with Event Info

Hw Push Time stamp value N+1



- R5 runs PTP and synchronizes with the external master clock
- 4. Allocates a Hardware Push Instance.
 - Configures TSR to map the DM Timer's PWM to the HW Push Instance
 - Save the callback for the Hardware Push Instance

5. When hardware push event occurs, remote core's registered callback is called with CPTS timer value.

Next Hw Push event



Example

- EthFw RTOS Server(MCU2_0) and EthFw RTOS Client (MCU2_1) demonstrates Multicore time synchronization.
- EthFw RTOS Server enables Time Sync PTP stack on MAC port 2 in slave mode and synchronizes with available master clock in the network.
- EthFw RTOS Client registers GTC timer used by it for coupling using TSR.
- Using registered hardware push callback, client establishes a linear relation and stores it locally.
- Whenever Client calls CpswRemoteApp_getSynchronizedTime(), the API computes synchronized time using current GTC time and the established linear relationship with CPTS timer.

$$T = r * t + C$$

T – Synchronized Time

r - Rate ratio

t - GTC Timer Value

C - Constant value



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