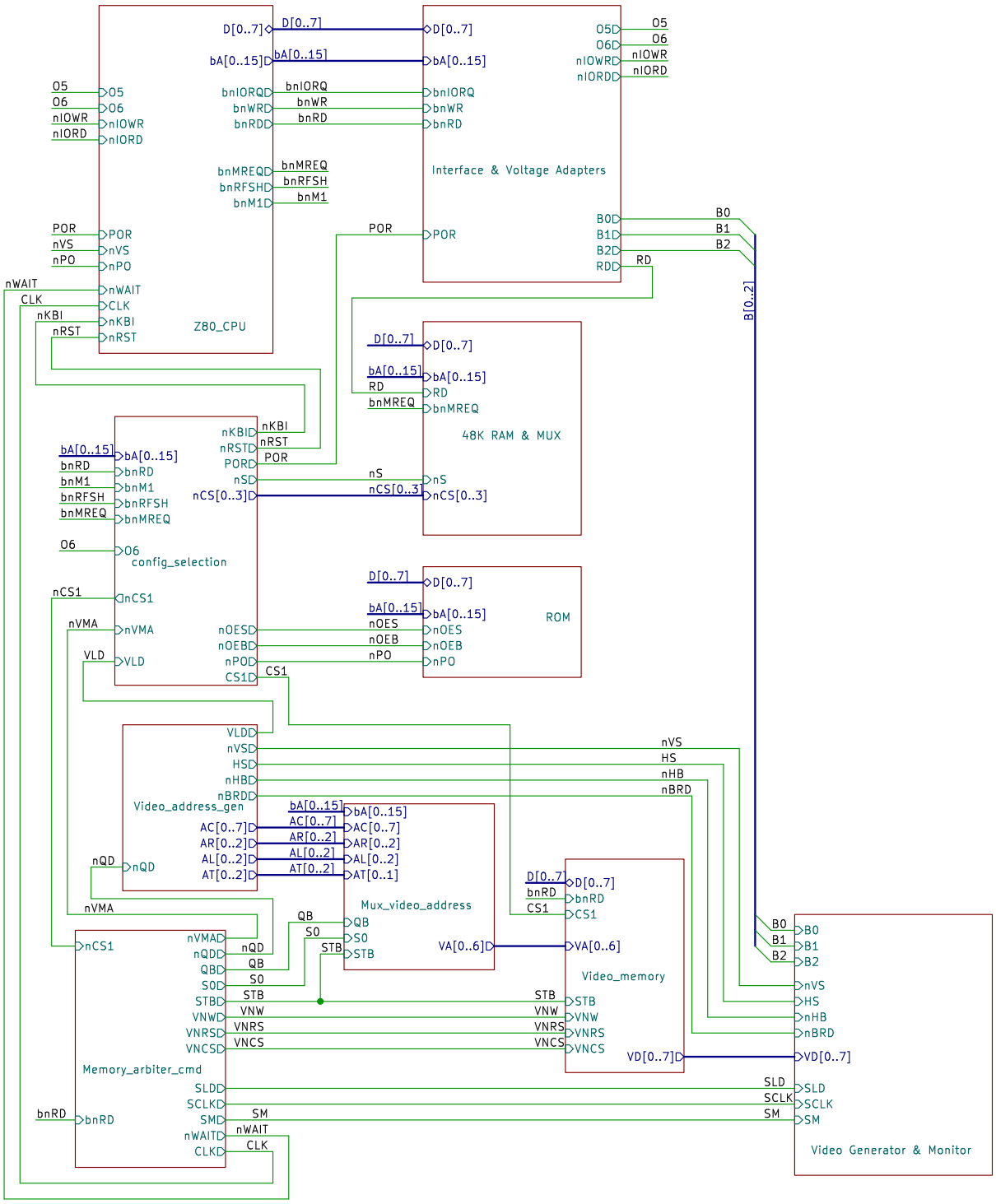
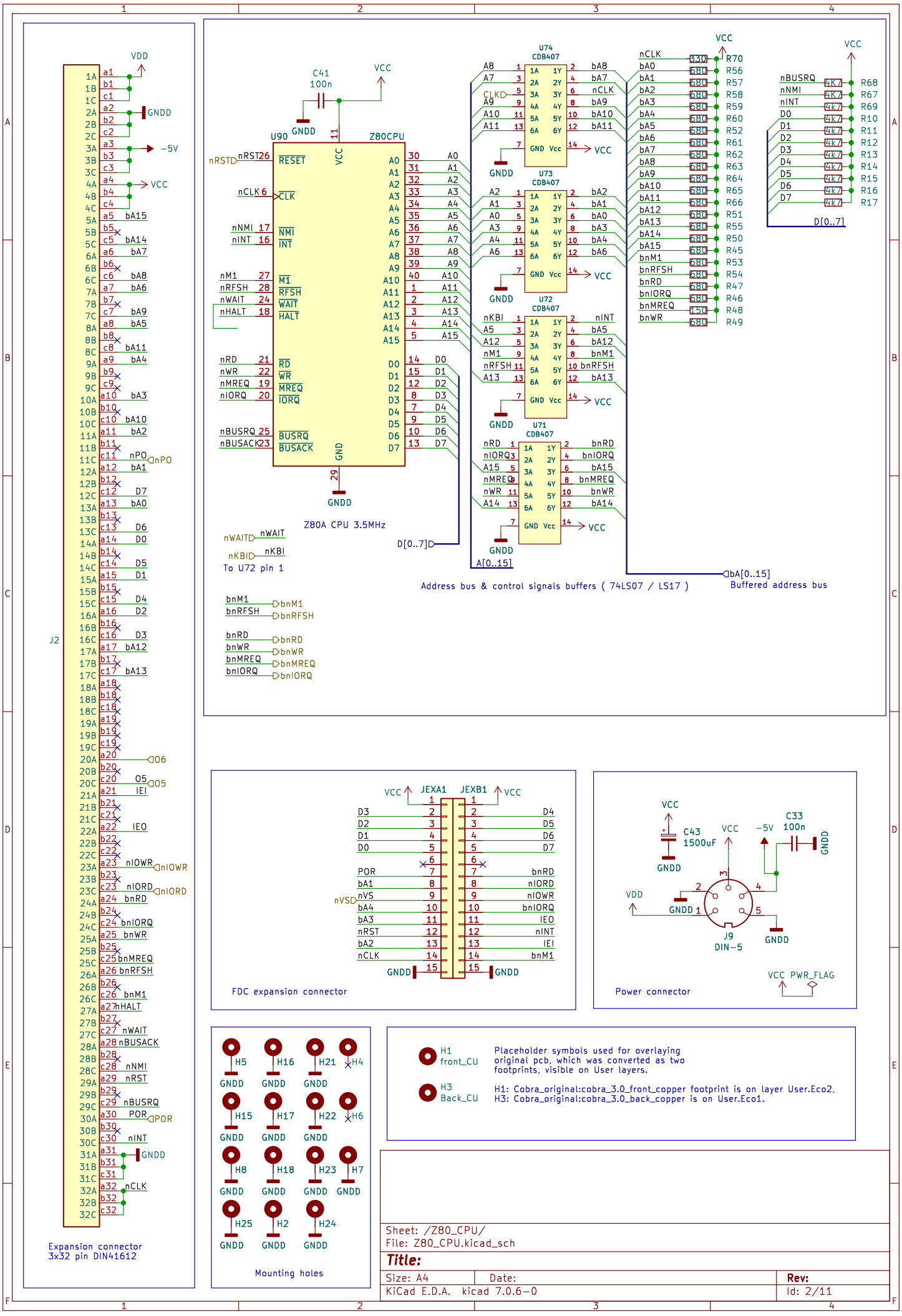
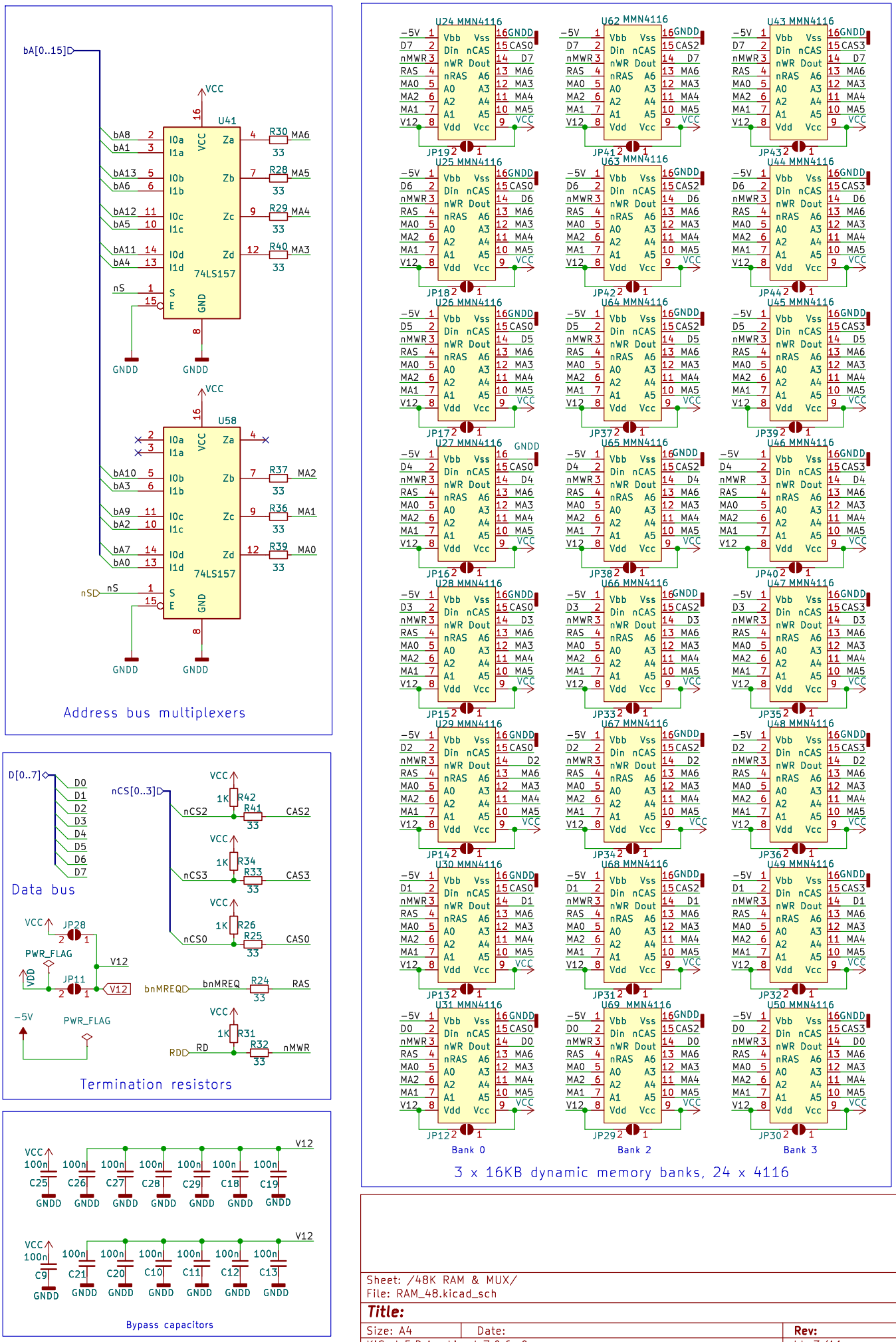



Sheet: /
File: main.kicad_sch

**Title:**

| Size: A4 | Date: | Rev: |
|---|---|---|
| KiCad E.D.A. kicad 7.0.6-0 | | Id: 1/11 |


Z80A CPU 3.5MHz
Address bus & control signals buffers ( 74LS07 / LS17 )
Buffered address bus
Expansion connector
3x32 pin DIN41612
FDC expansion connector
Power connector
Mounting holes
H1 front_CU
H3 Back_CU
Placeholder symbols used for overlaying original pcb, which was converted as two footprints, visible on User layers.
H1: Cobra_original:cobra_3.0_front_copper footprint is on layer User.Eco2,
H3: Cobra_original:cobra_3.0_back_copper is on User.Eco1.
Sheet: /Z80_CPU/
File: Z80_CPU.kicad_sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 7.0.6-0
Id: 2/11




Sheet: /48K RAM & MUX/
File: RAM_48.kicad_sch

**Title:**

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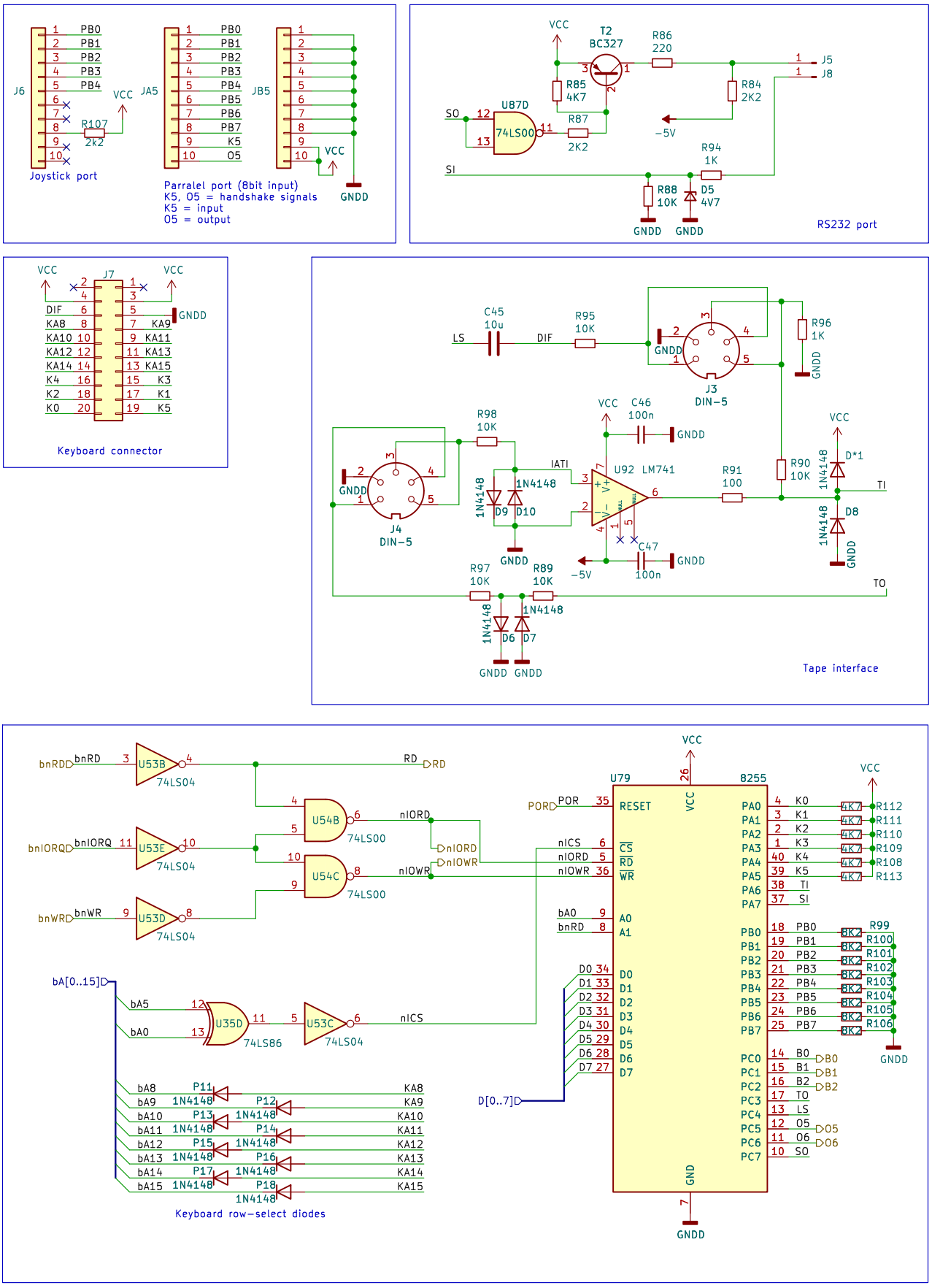
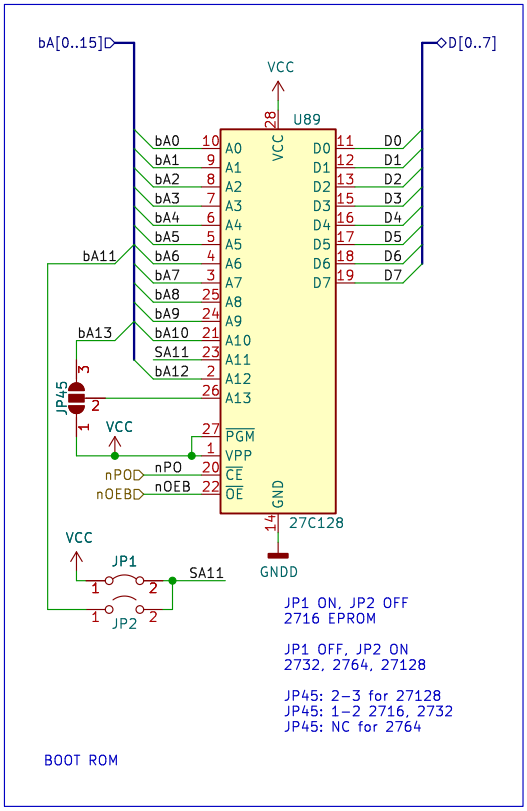
|---|---|---|
| KiCad E.D.A. kicad 7.0.6-0 | | Id: 3/11 |

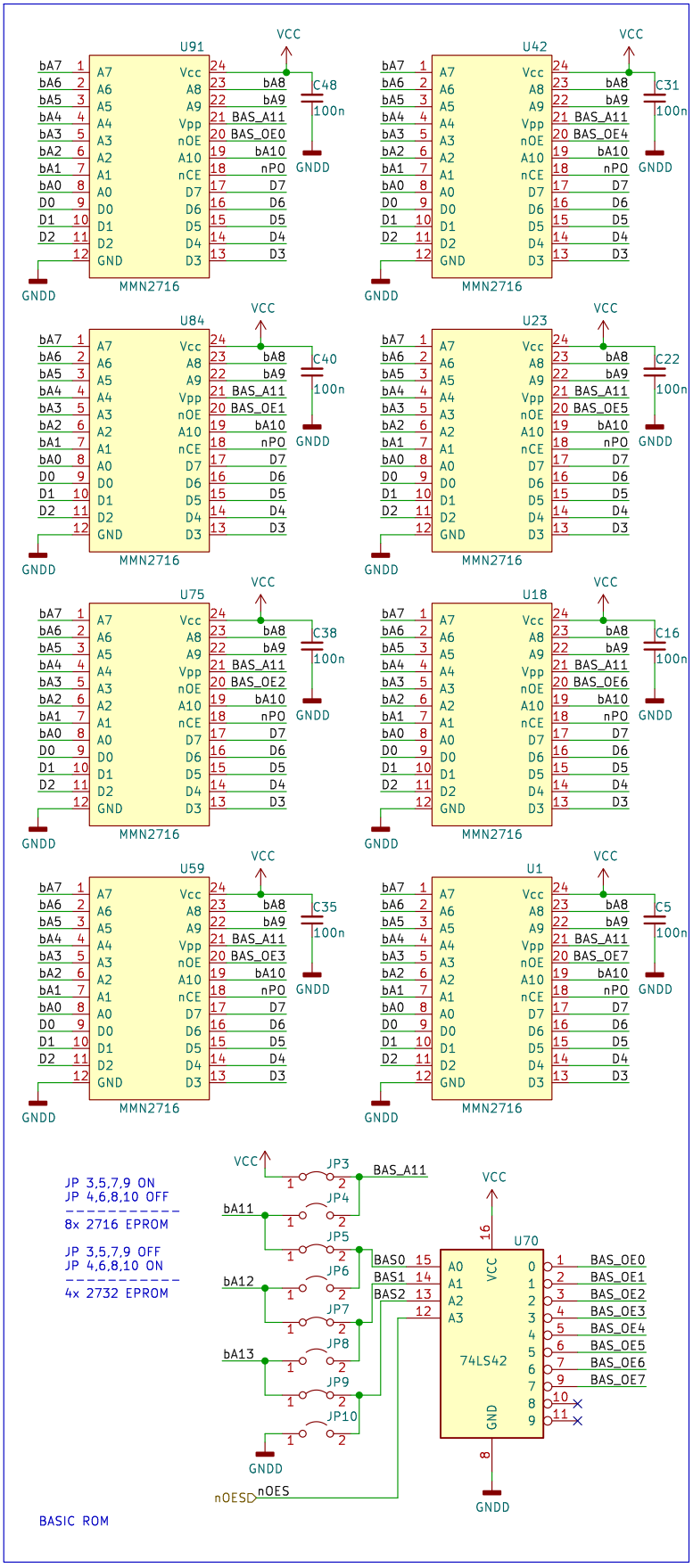



Sheet: /Interface & Voltage Adapters/
File: Interface.kicad_sch

**Title:**

| Size: A4 | Date: | Rev: |
|---|---|---|
| KiCad E.D.A. kicad 7.0.6-0 | | Id: 5/11 |

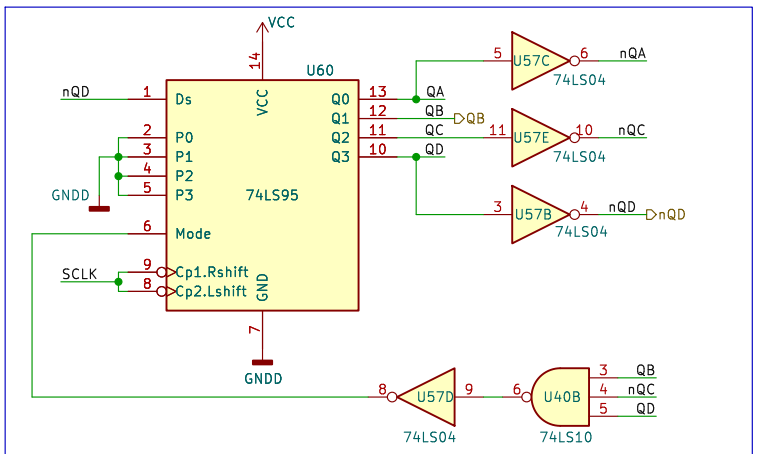


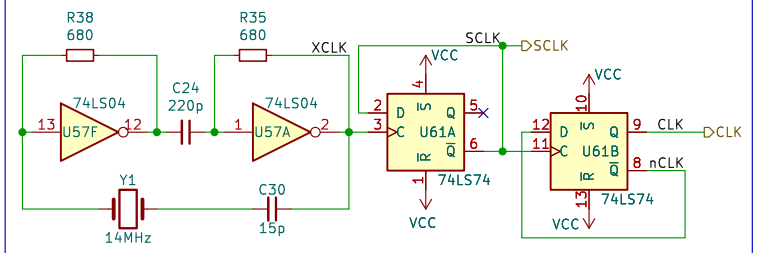

Sheet: /ROM/
File: ROM.kicad_sch

**Title:**

| Size: A4 | Date: | Rev: |
|---|---|---|
| KiCad E.D.A. kicad 7.0.6-0 | | Id: 6/11 |

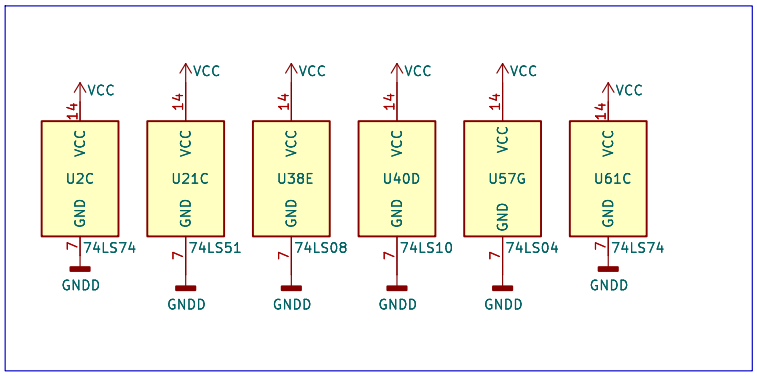


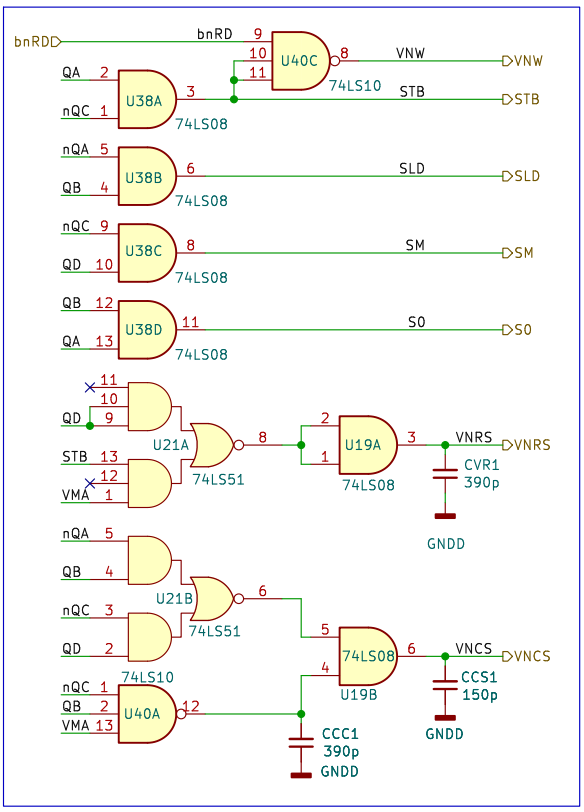

Finite State Machine using a twisted-ring Johnson counter.
Q[A..D] go through 8 states, and only one bit changes from one state to the next.
Gate U40B (3 input NAND) and the U57D inverter form a 3 input AND gate.
It resets the shift register when an invalid value is present after power on: Q[A..D] = X101 .




Clock generator

XCLK = 14MHZ
SCLK = 7MHZ
CLK = 3.5MHZ (CPU clock)




VNW – Video Not Write, active-low signal, video DRAM bank WR pins

STB – Strobe, loads P8212 video register with data from video memory, for CPU to read it
Also, it controls the video memory address multiplexer MSB, when STB = 1, cpu address bus is selected

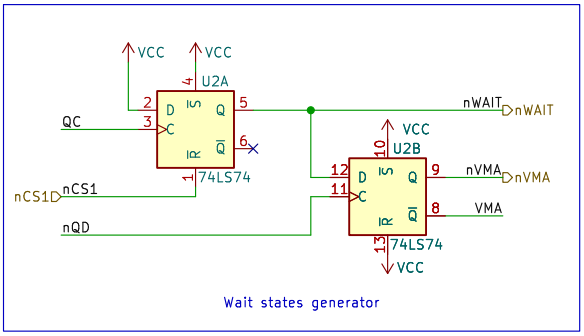
SLD – Serializer Load, controls loading data from the video memory bus into the pixel shift registers

SM – Serial Mode (?) – loads color attributes in shift registers used as 2x4bit D registers

SO – Select Zero (not SO which is Serial OUT)
controls the video memory address multiplexer LSB
performs the switching between ROW and COLUMN address for video dram

VNRS – Video Not RAS is the RAS signal for the video memory DRAM

VNCS – Video Not CAS is the CAS signal for the video memory DRAM

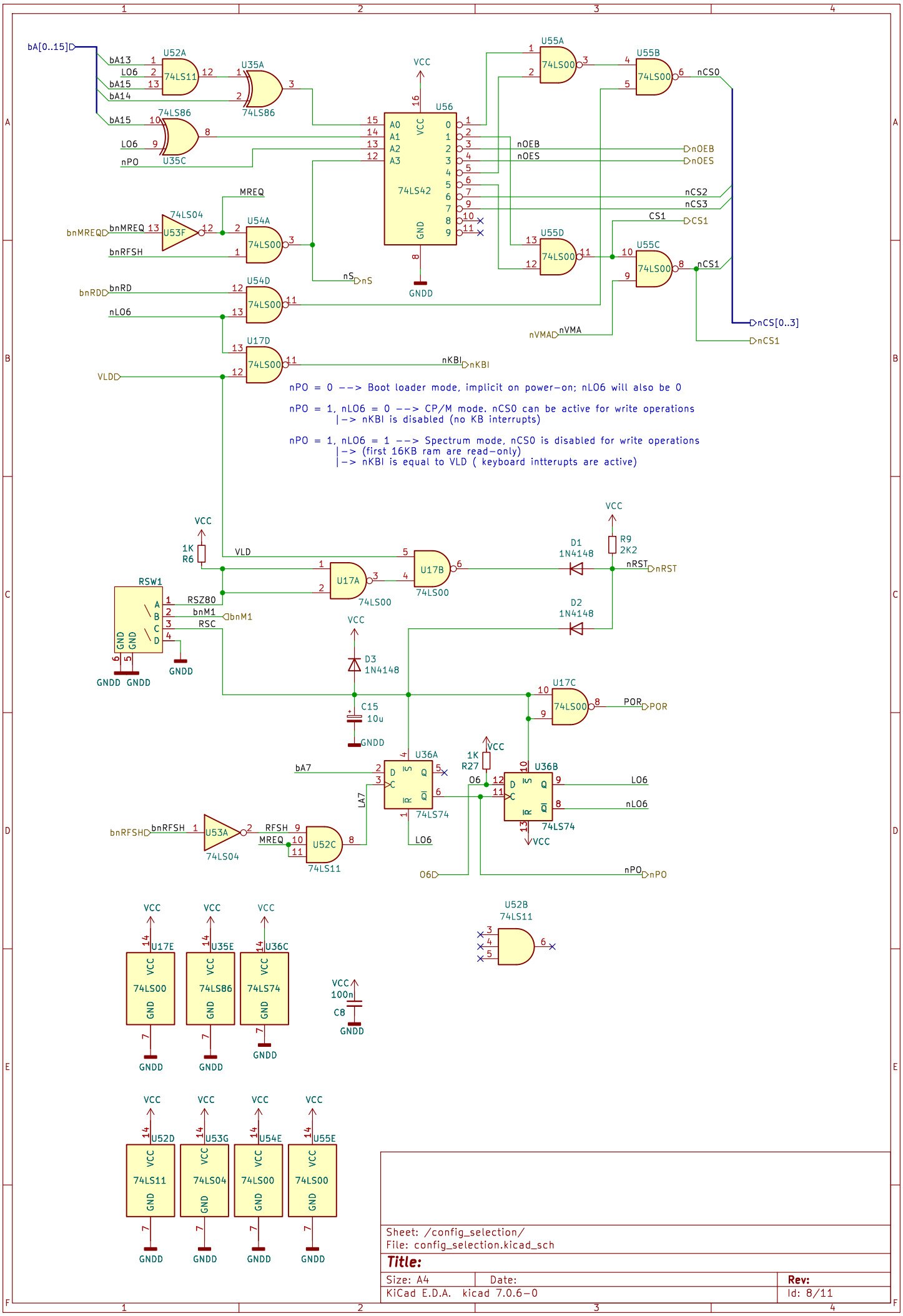



Wait states generator

Sheet: /Memory_arbiter_cmd/
File: Memory_arbiter_cmd.kicad_sch

**Title:**

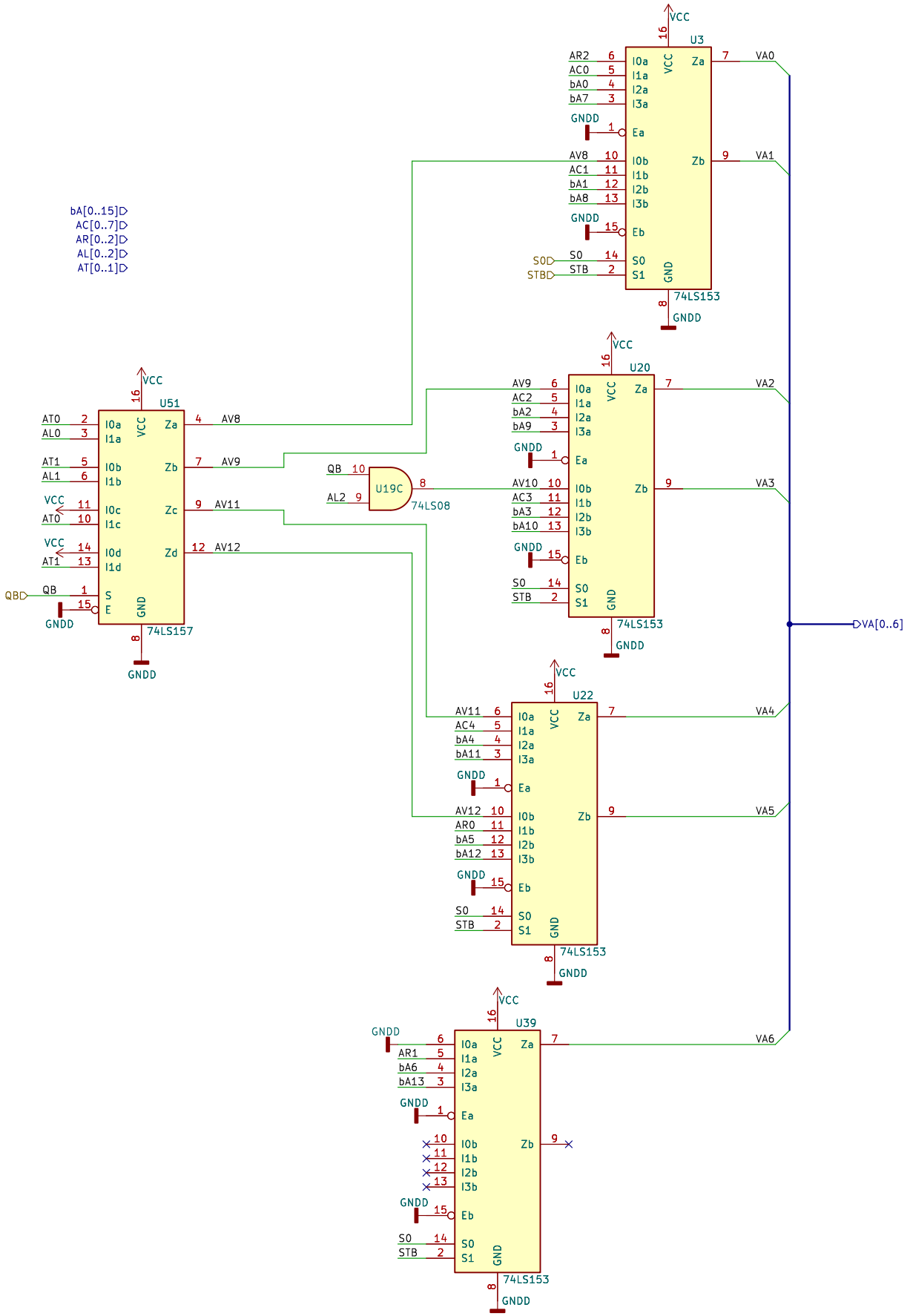
| Size: A4 | Date: | Rev: |
|---|---|---|
| KiCad E.D.A. kicad 7.0.6-0 | | Id: 7/11 |




Sheet: /config_selection/
File: config_selection.kicad_sch

**Title:**

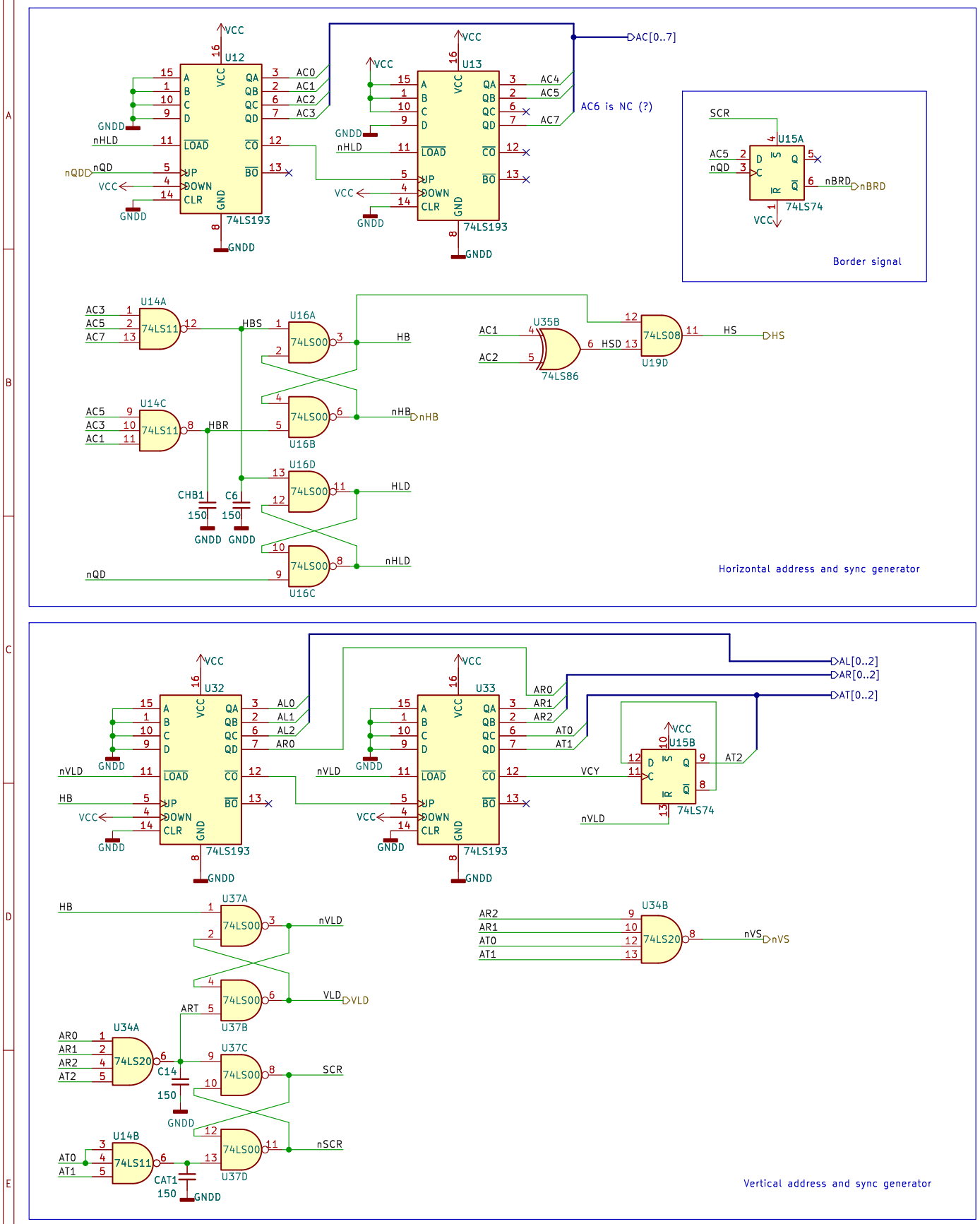
| Size: A4 | Date: | Rev: |
|---|---|---|
| KiCad E.D.A. kicad 7.0.6-0 | | Id: 8/11 |




Sheet: /Mux_video_address/
File: Mux_video_address.kicad_sch

**Title:**

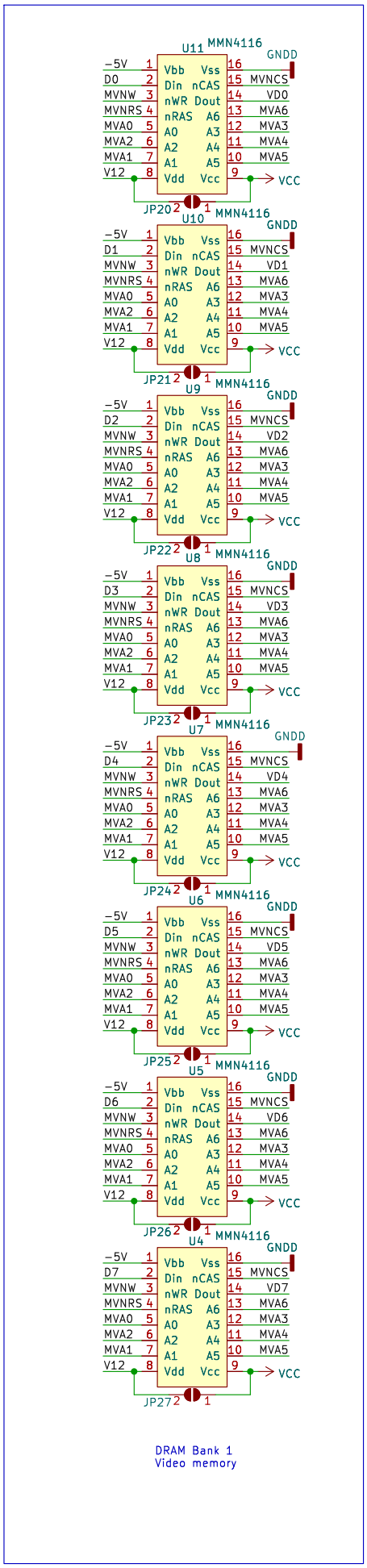
| Size: A4 | Date: | Rev: |
|---|---|---|
| KiCad E.D.A. kicad 7.0.6-0 | | Id: 10/11 |

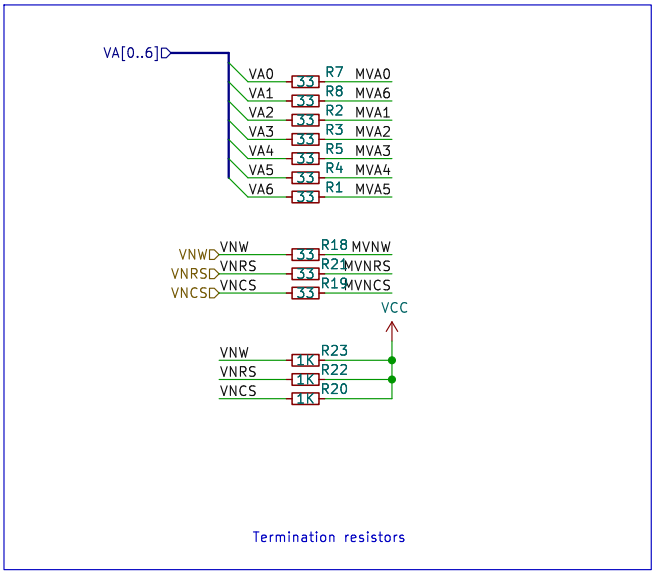


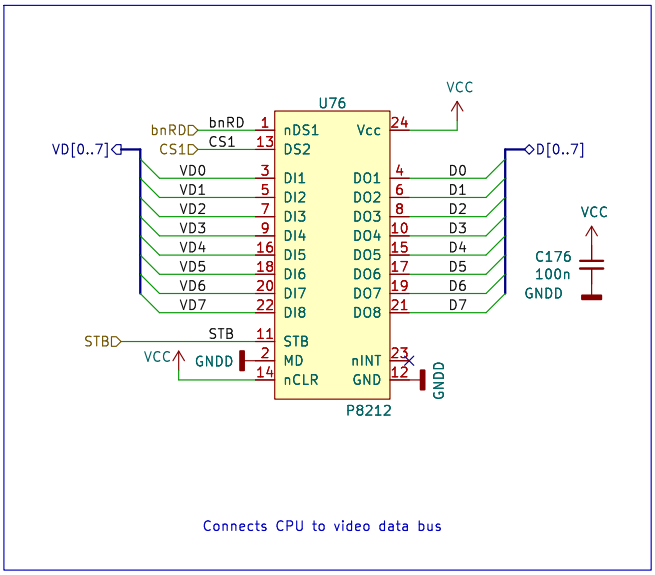

Sheet: /Video_address_gen/
File: Video_address_gen.kicad_sch

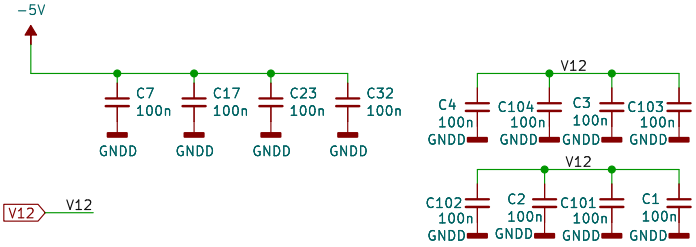
**Title:**

| Size: A4 | Date: | Rev: |
|---|---|---|
| KiCad E.D.A. kicad 7.0.6-0 | | Id: 11/11 |




Sheet: /Video_memory/
File: Video_memory.kicad_sch

**Title:**

| Size: A4 | Date: | Rev: |
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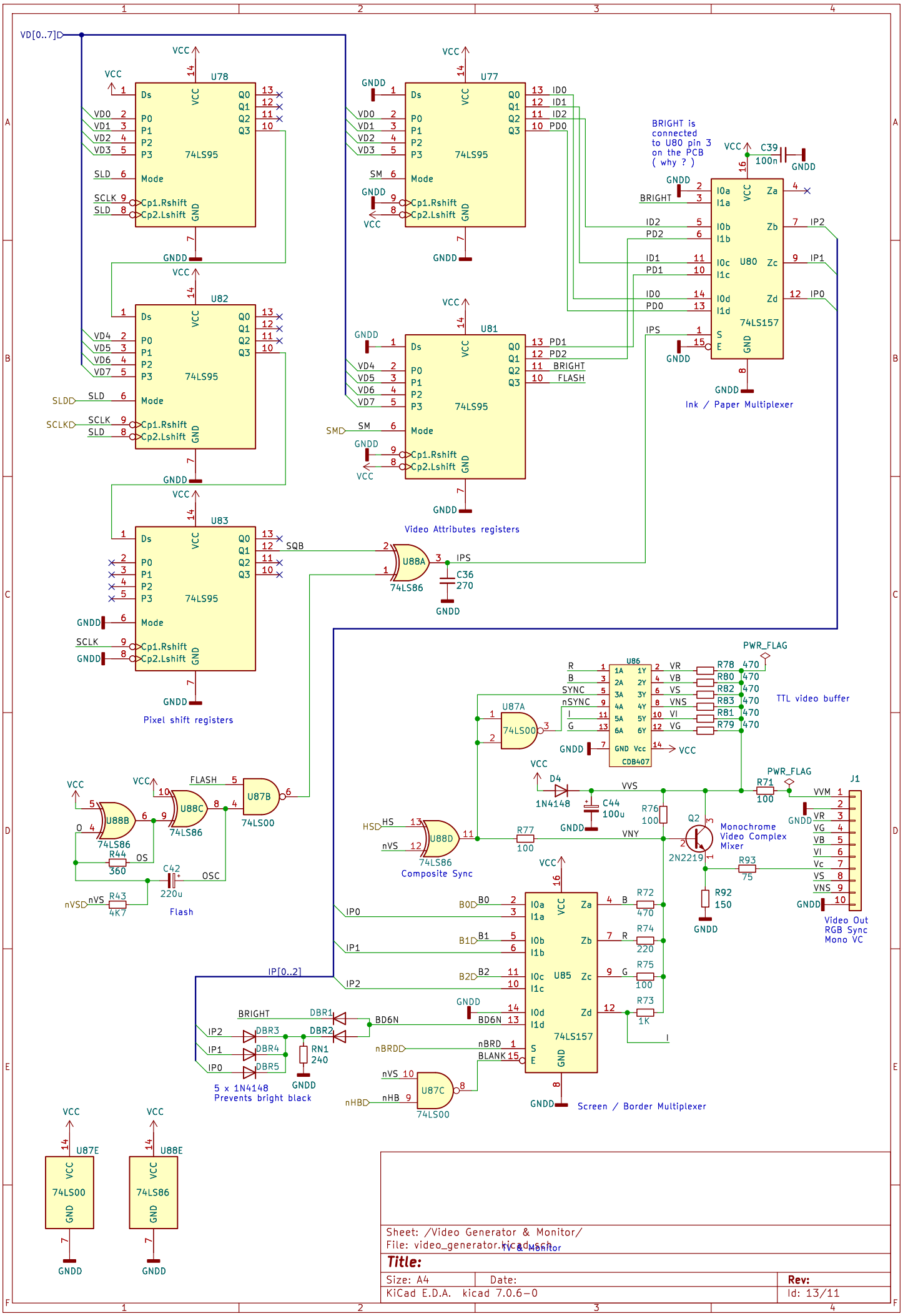
VD[0..7]
U78
U77
U82
U81
U83
74LS95
Video Attributes registers
Pixel shift registers
BRIGHT is connected to U80 pin 3 on the PCB ( why ? )
U80
74LS157
Ink / Paper Multiplexer
U88A
74LS86
U88B
U88C
U87B
74LS00
Flash
U87A
U86
CDB407
TTL video buffer
U88D
Composite Sync
Monochrome Video Complex Mixer
2N2219
J1
Video Out RGB Sync Mono VC
U85
Screen / Border Multiplexer
U87C
5 x 1N4148 Prevents bright black
U87E
U88E
PWR_FLAG
Sheet: /Video Generator & Monitor/
File: video_generator.kicad_sch
TV & Monitor
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 7.0.6-0
Id: 13/11