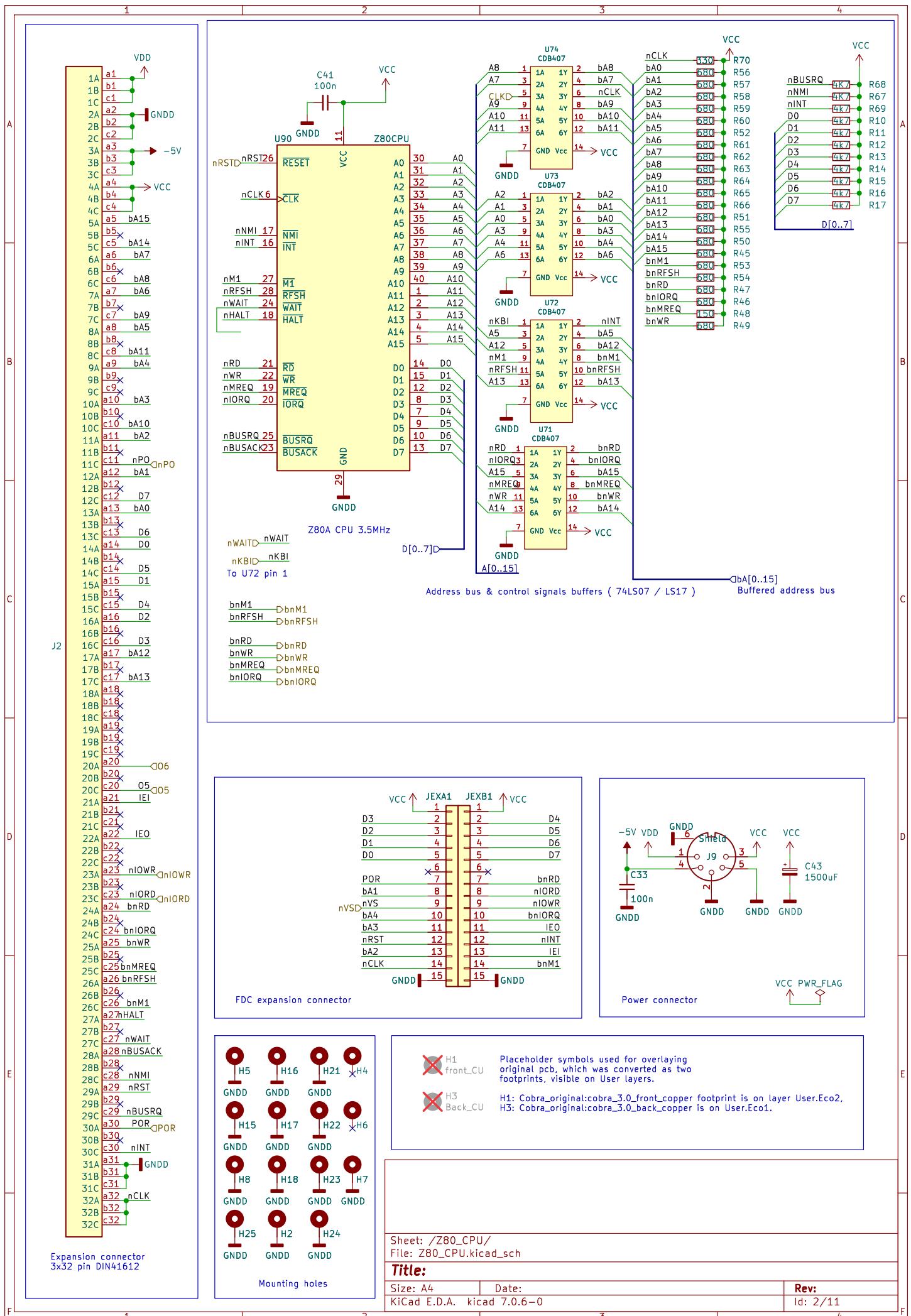
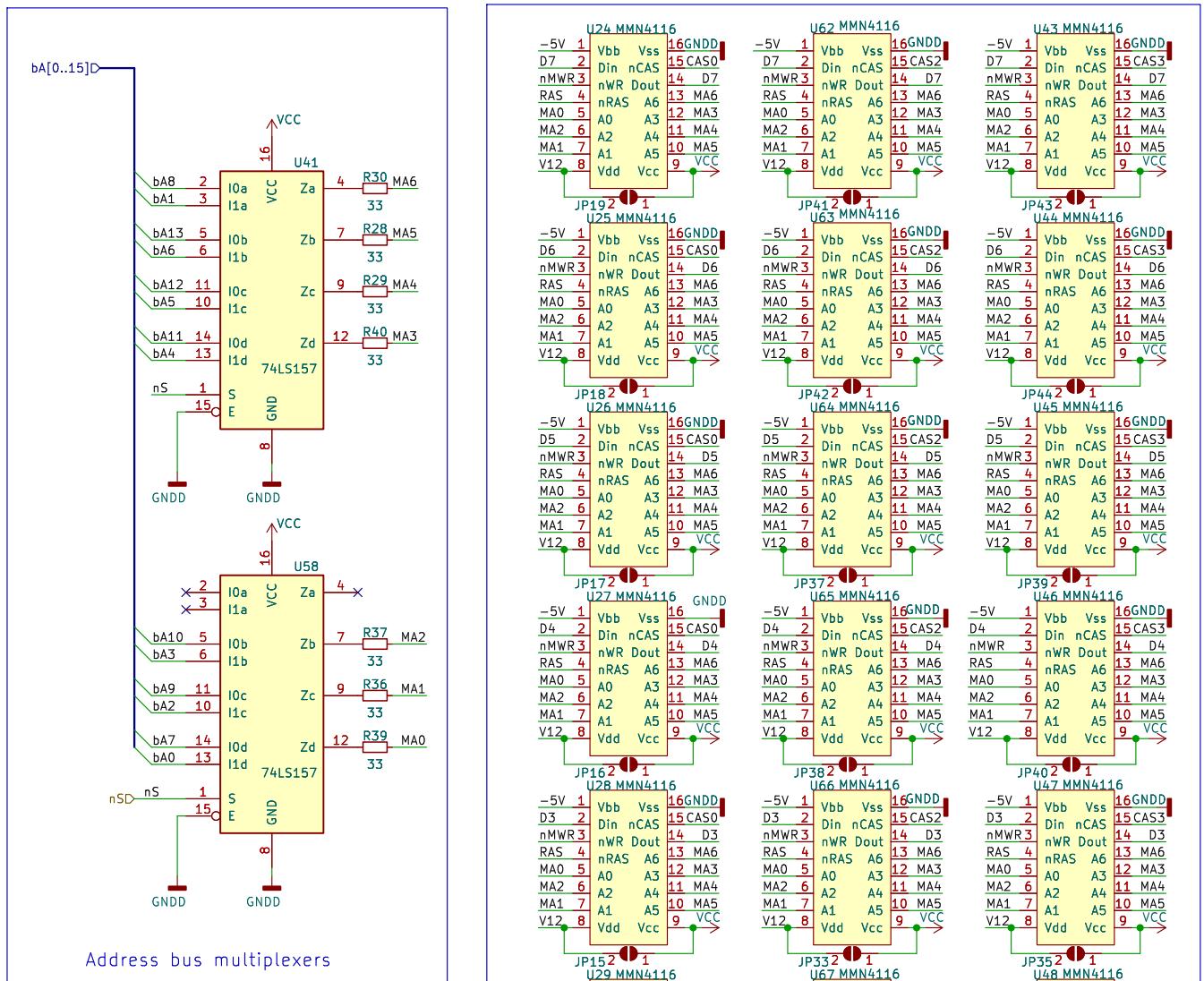


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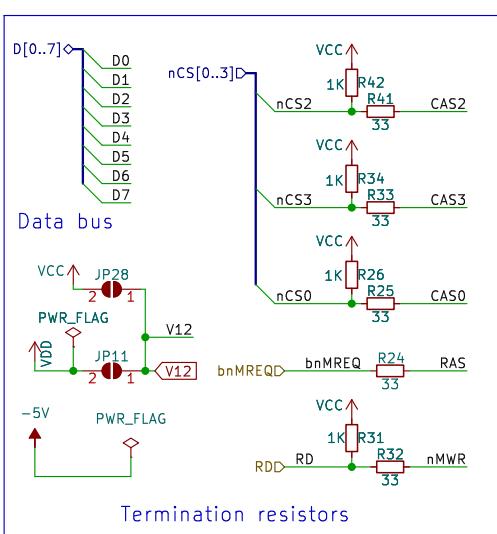
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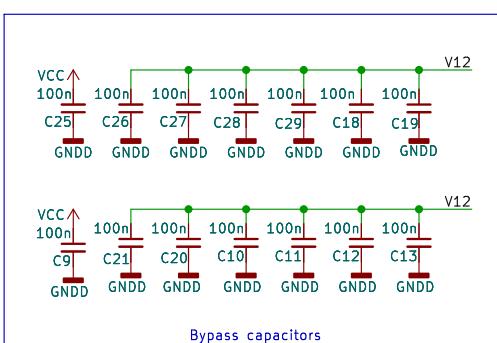




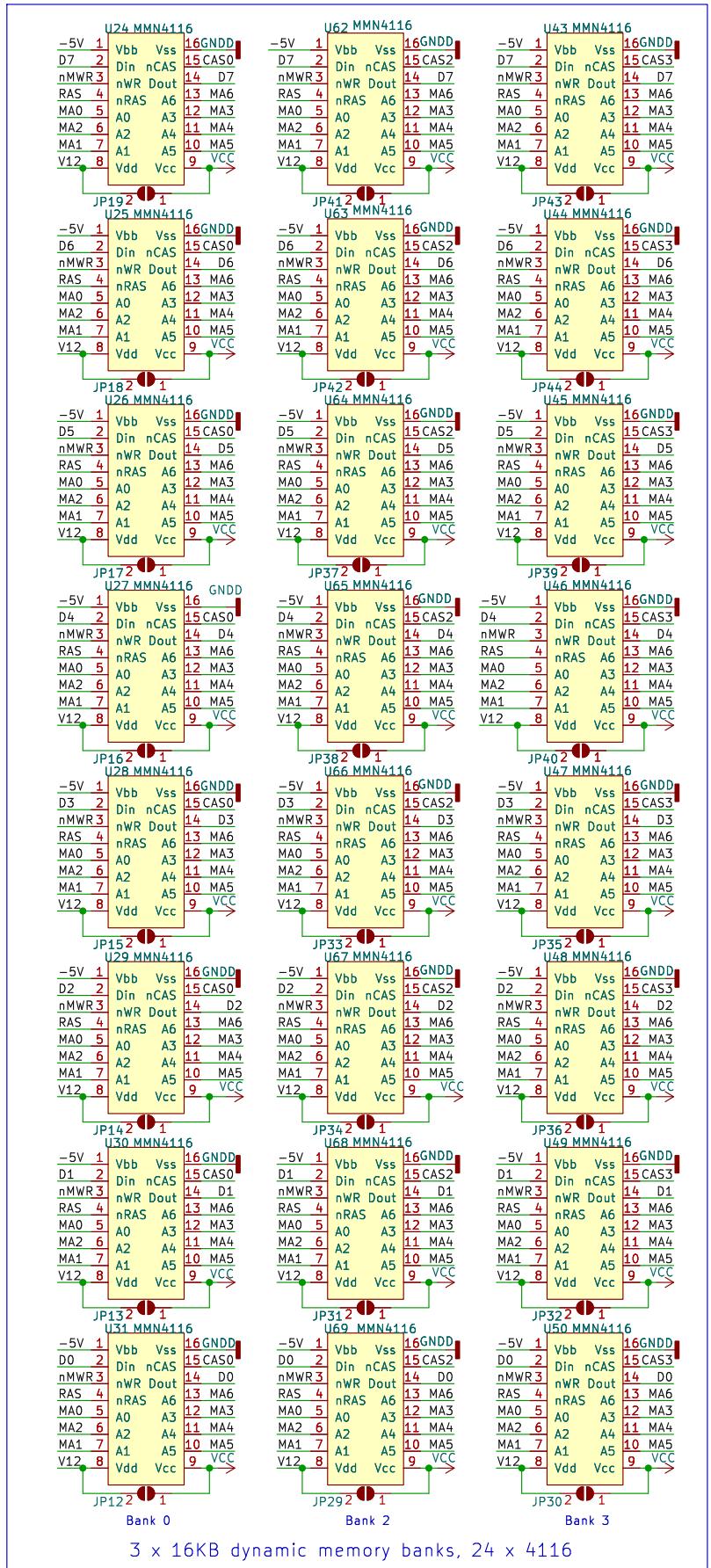
### Address bus multiplexers



## Termination resistors



### Bypass capacitors



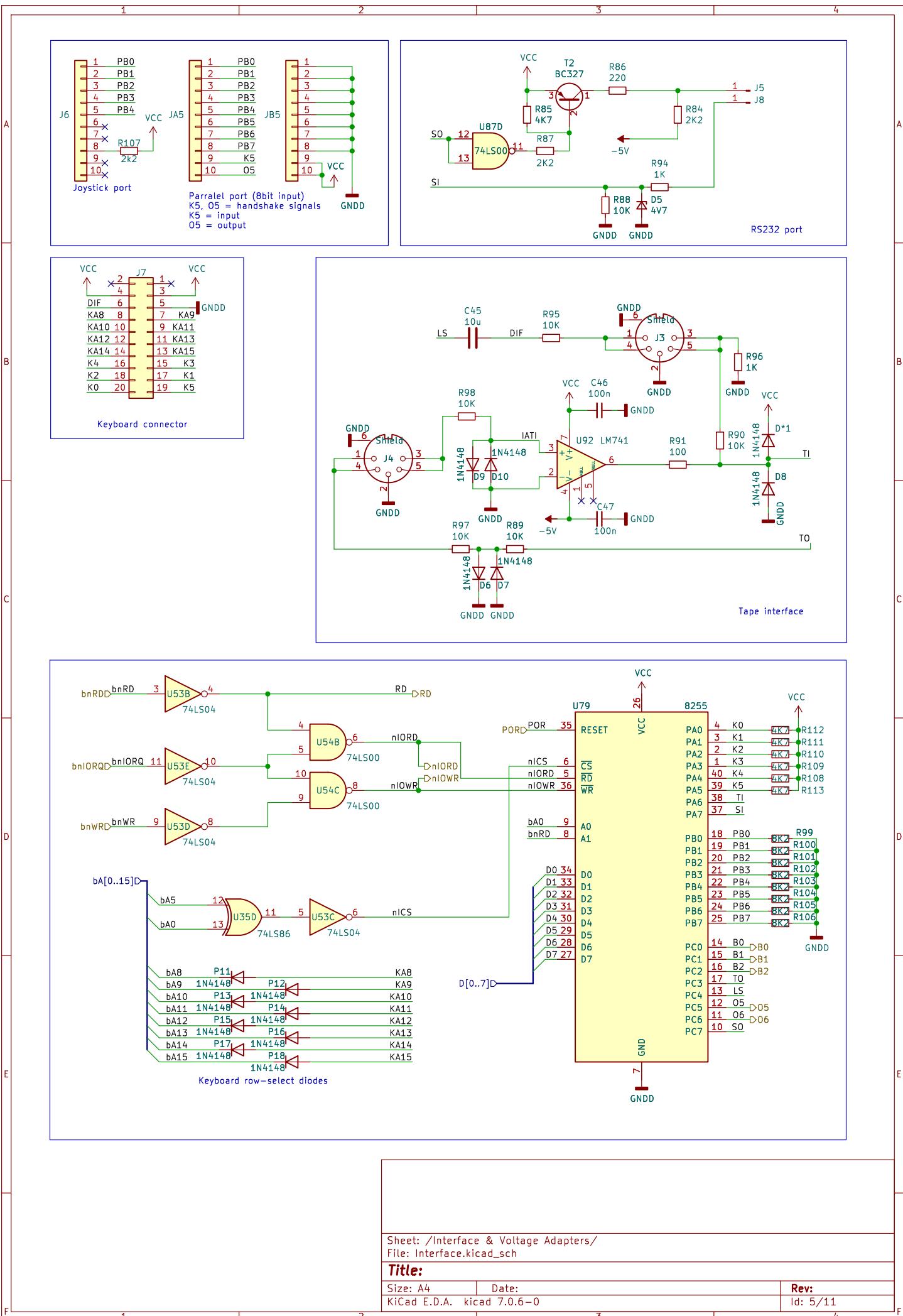
3 x 16KB dynamic memory banks, 24 x 4116

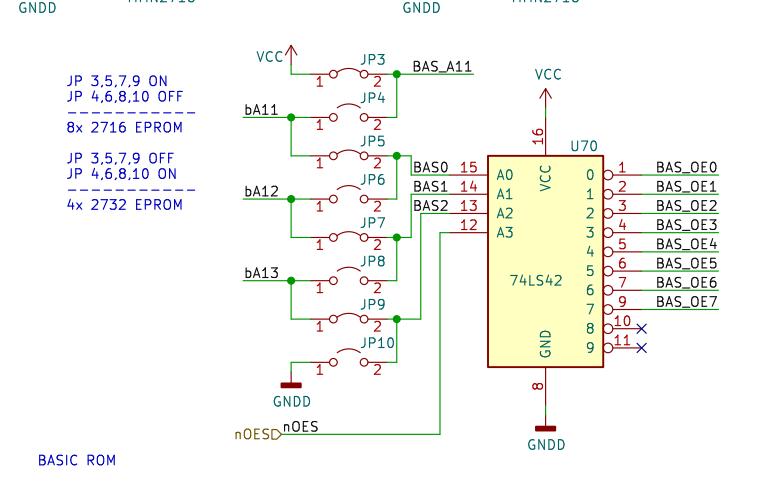
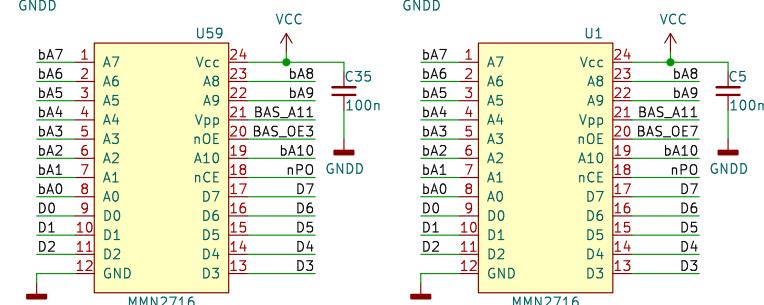
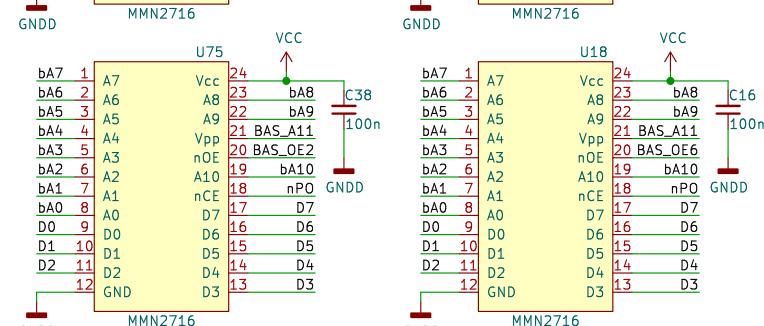
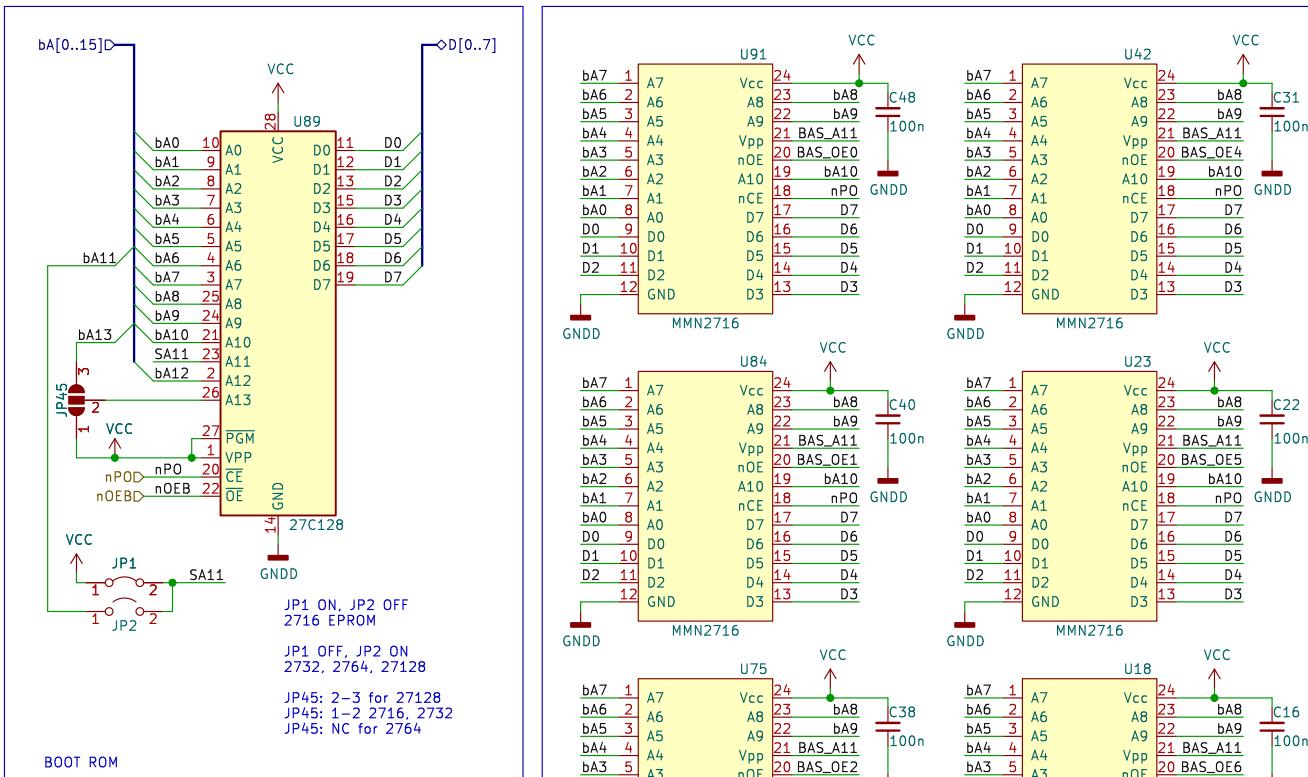
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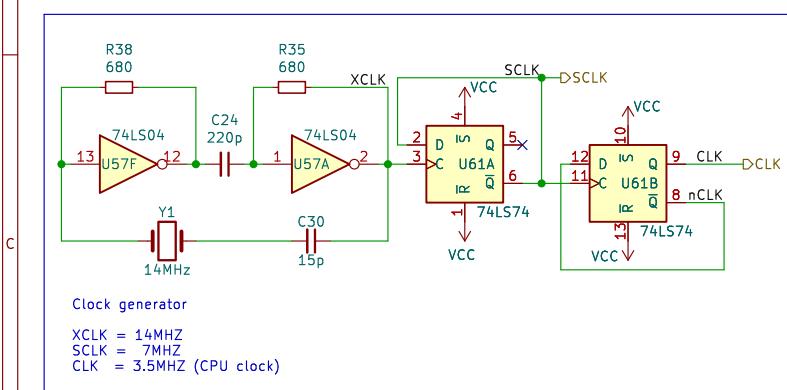
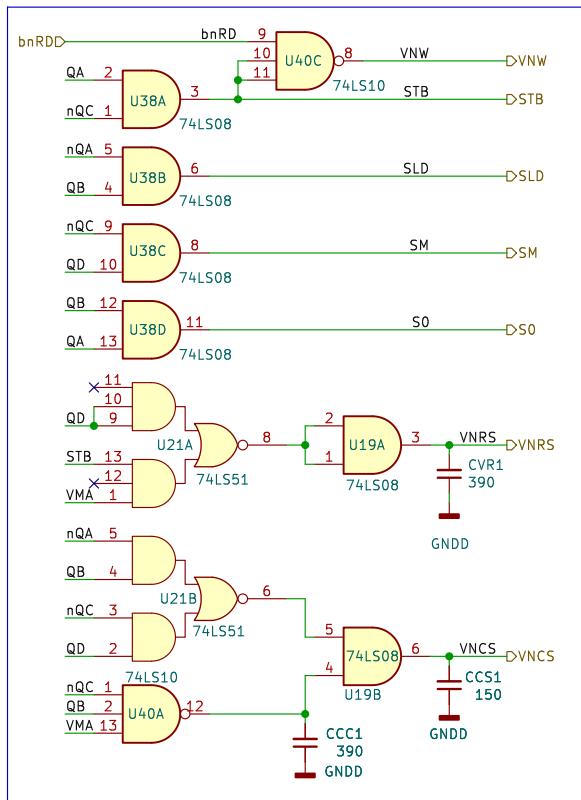
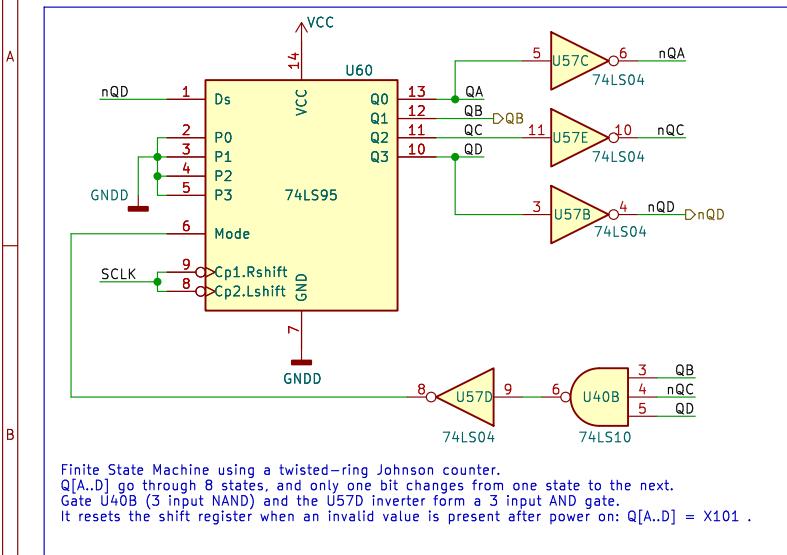




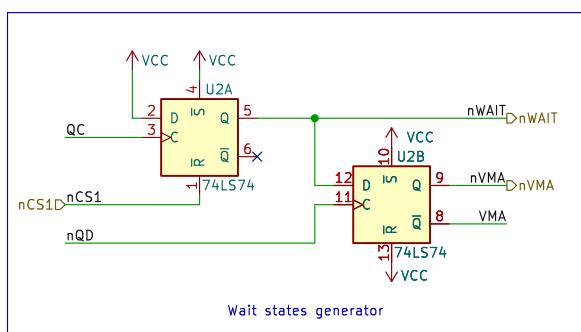
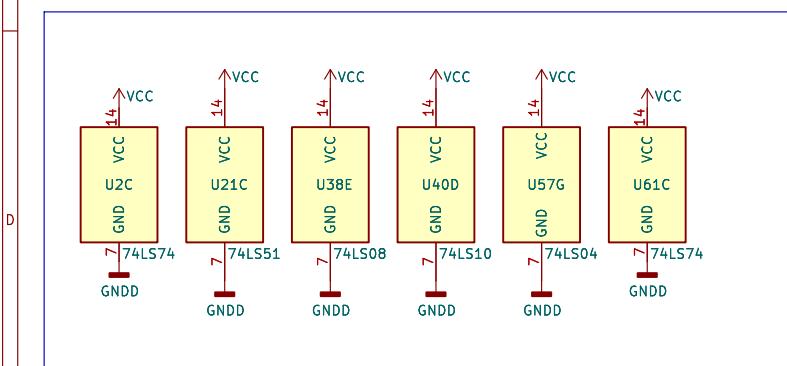
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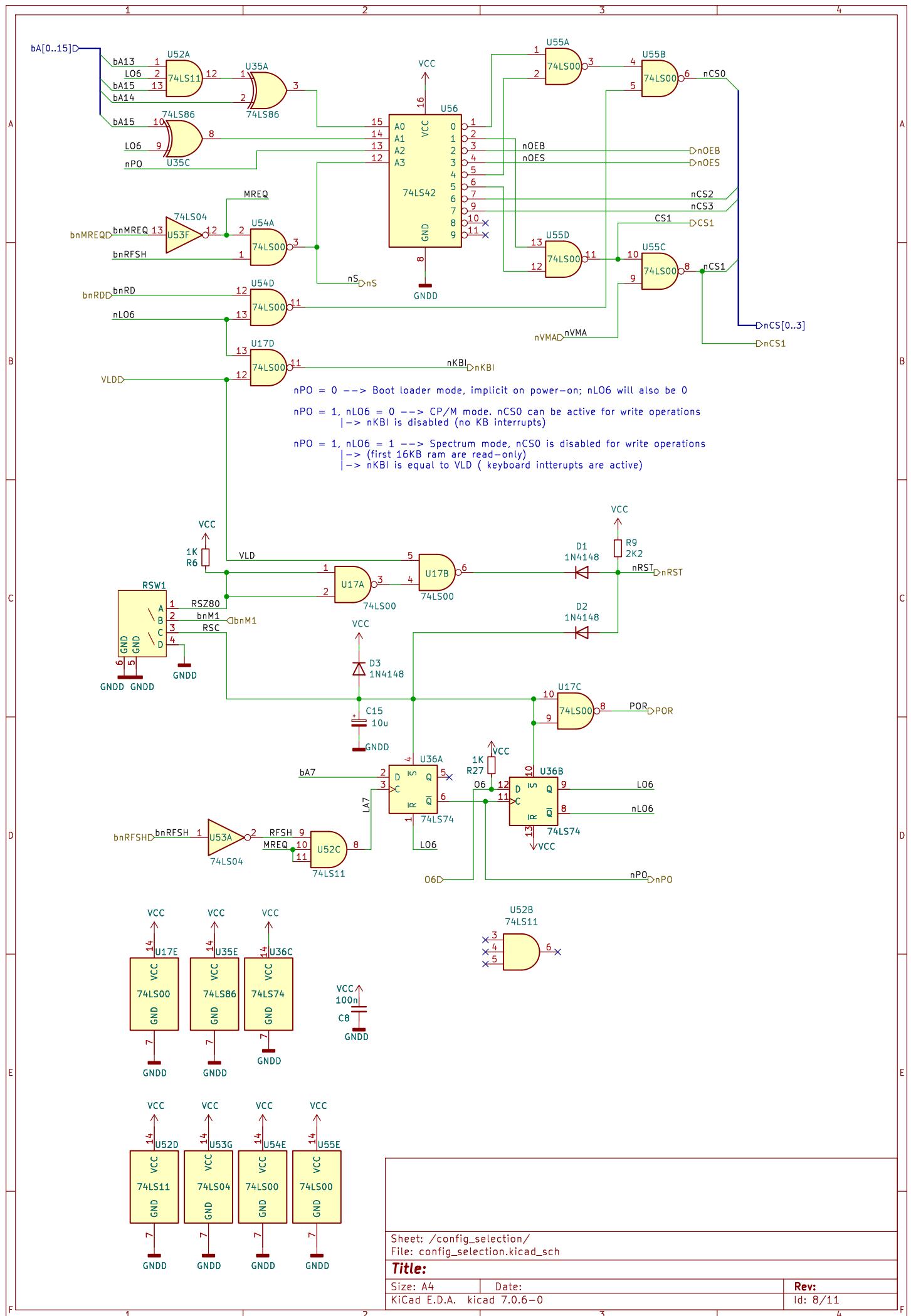
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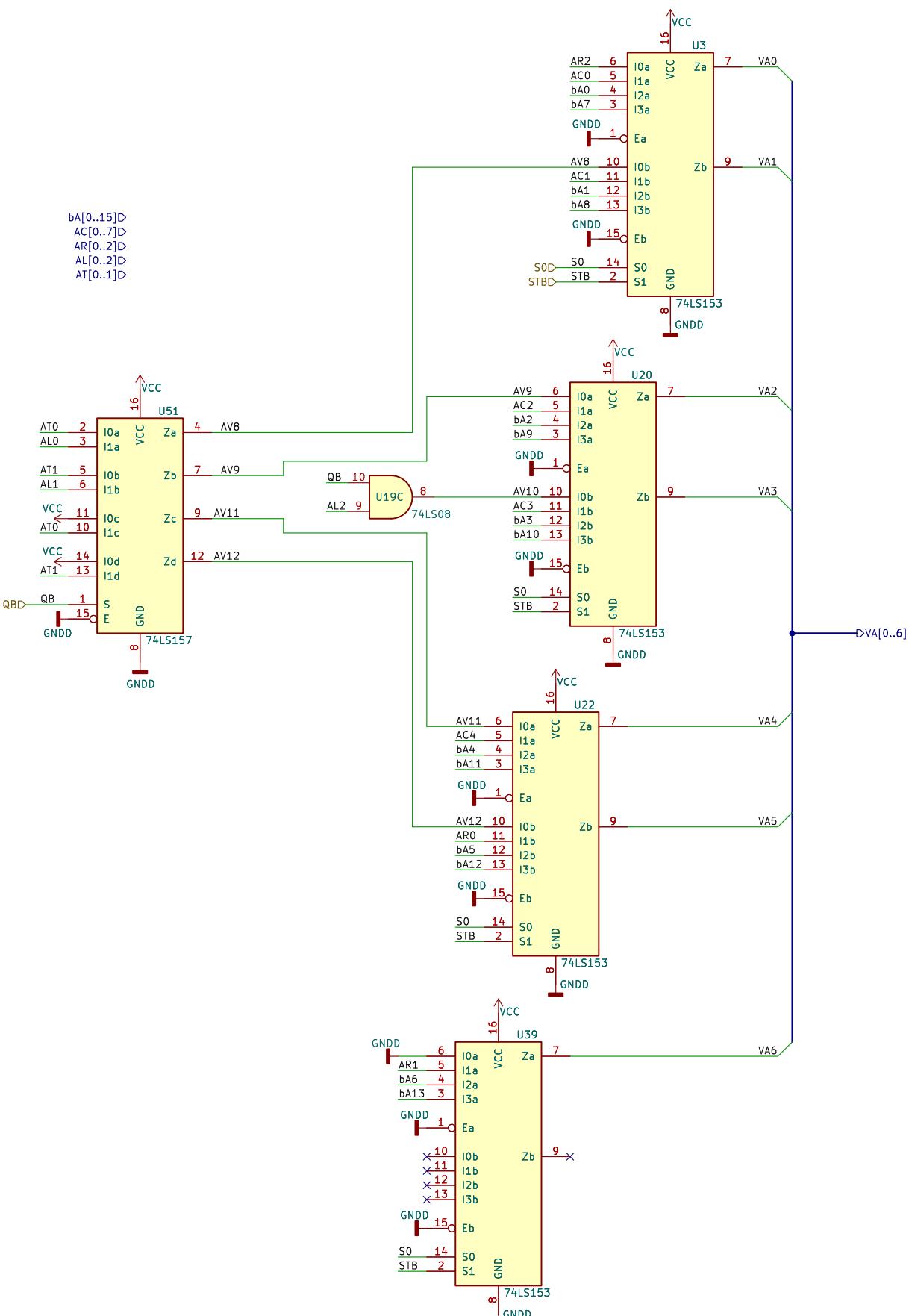


VNW – Video Not Write, active-low signal, video DRAM bank WR pins  
STB – Strobe, loads P8212 video register with data from video memory, for CPU to read it  
Also, it controls the video memory address multiplexer MSB, when SIB = 1, cpu address bus is selected  
SLD – Serializer Load, controls loading data from the video memory bus into the pixel shift registers  
SM – Serial Mode (?) – loads color attributes in shift registers used as 2x4bit D registers  
SO – Select Zero (not SO which is Serial OUT)  
controls the video memory address multiplexer LSB  
performs the switching between ROW and COLUMN address for video dram  
VNRS – Video Not RAS is the RAS signal for the video memory DRAM  
VNCS – Video Not CAS is the CAS signal for the video memory DRAM





bA[0..15] D  
AC[0..7] D  
AR[0..2] D  
AL[0..2] D  
AT[0..1] D

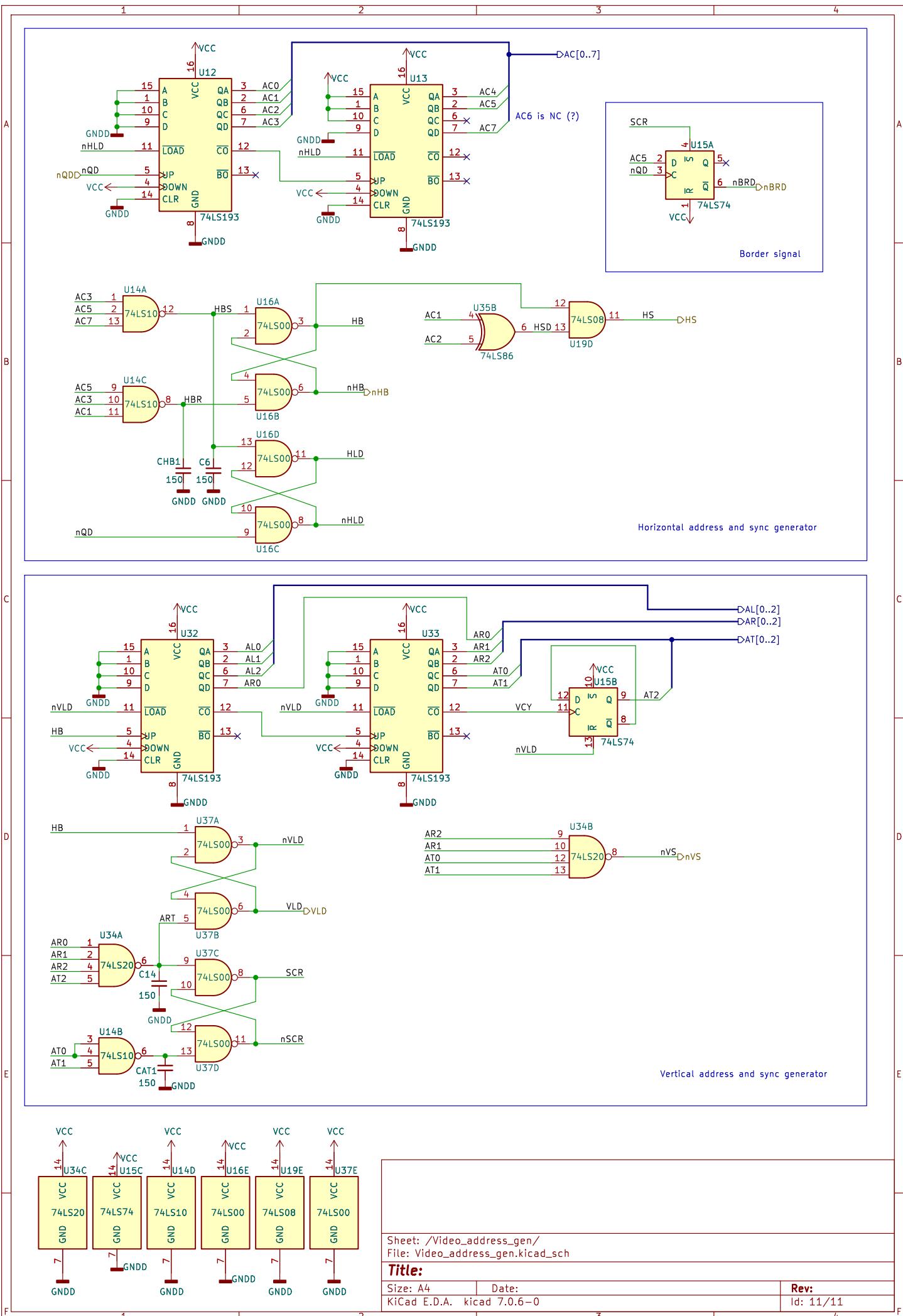


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File: Mux\_video\_address.kicad\_sch

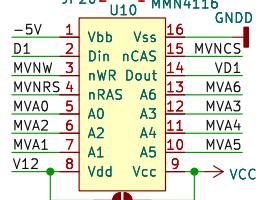
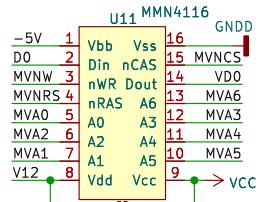
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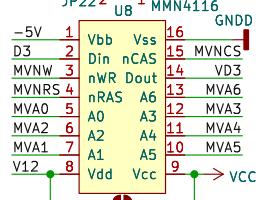
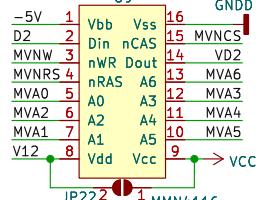
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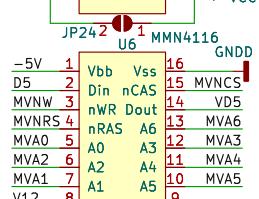
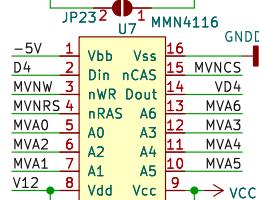
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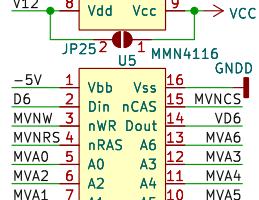
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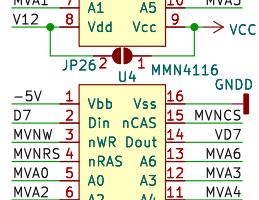
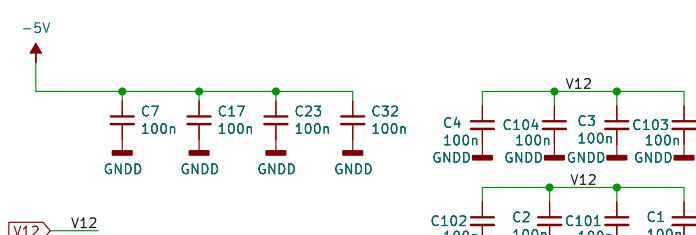
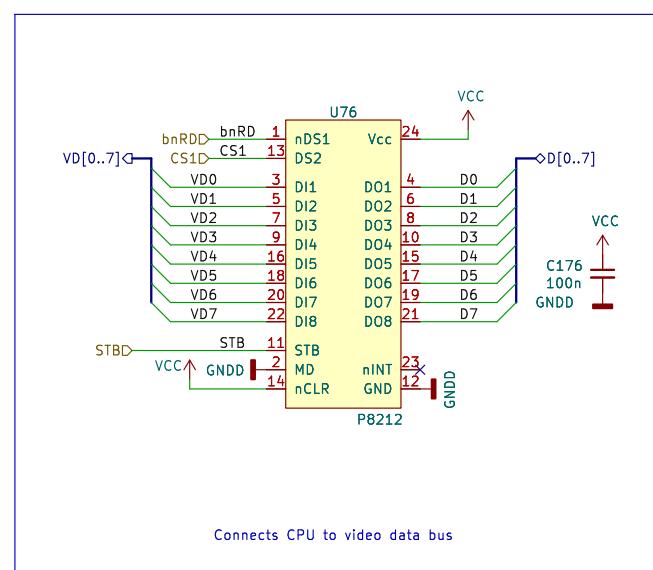
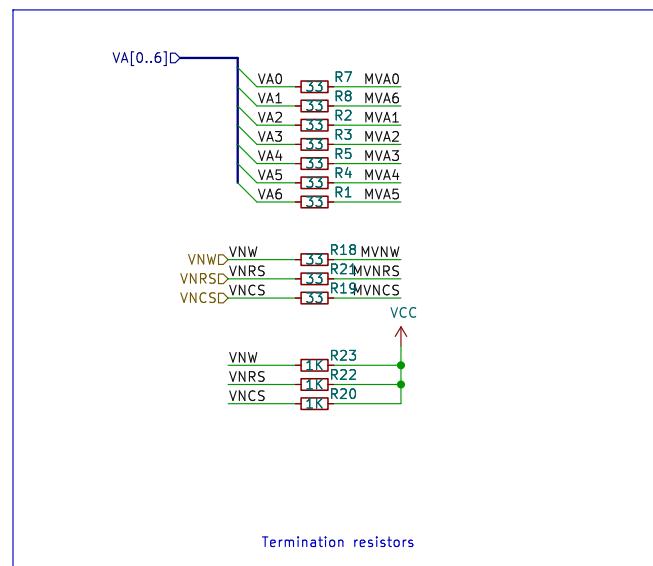
C



D



E

DRAM Bank 1  
Video memory

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