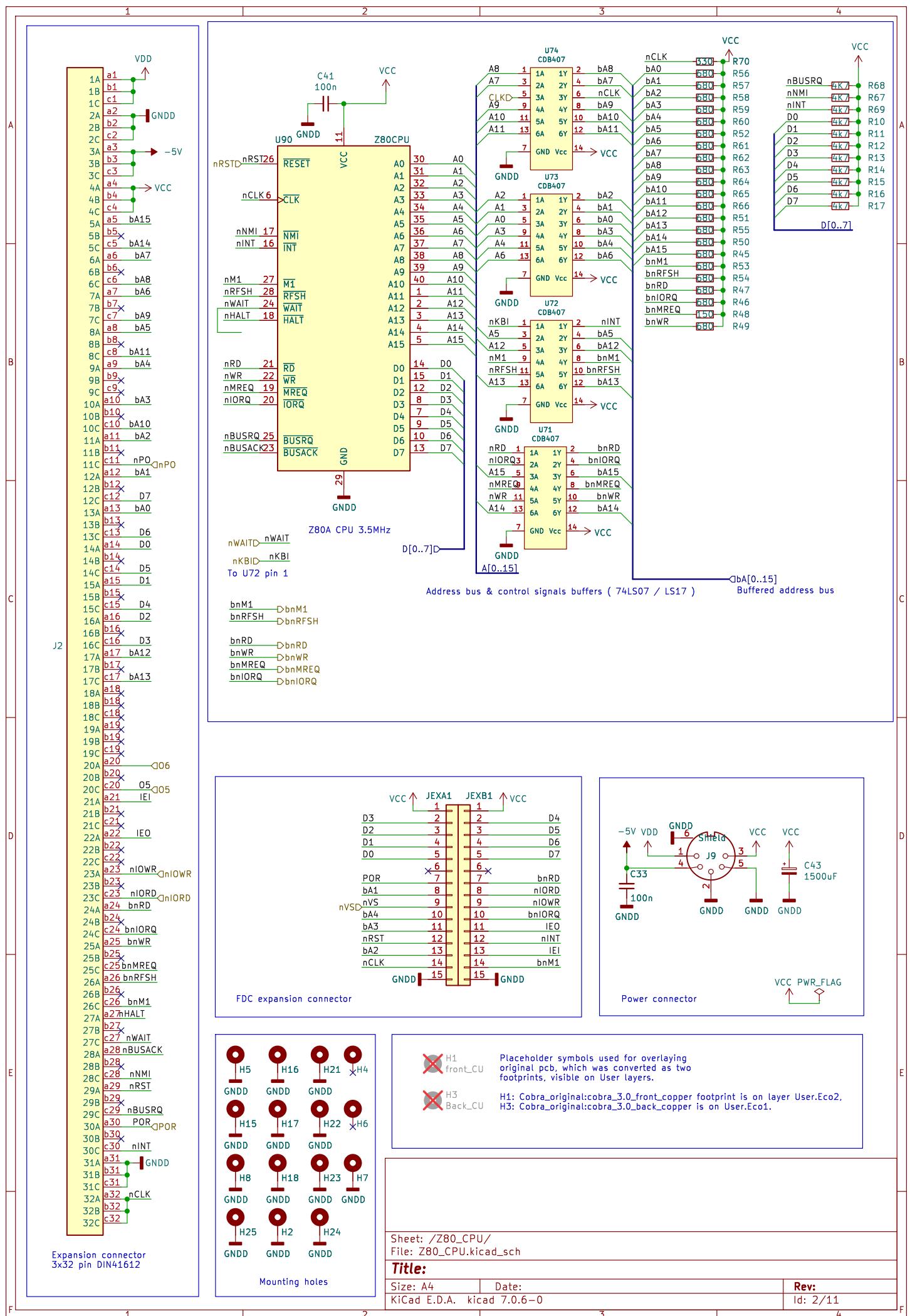


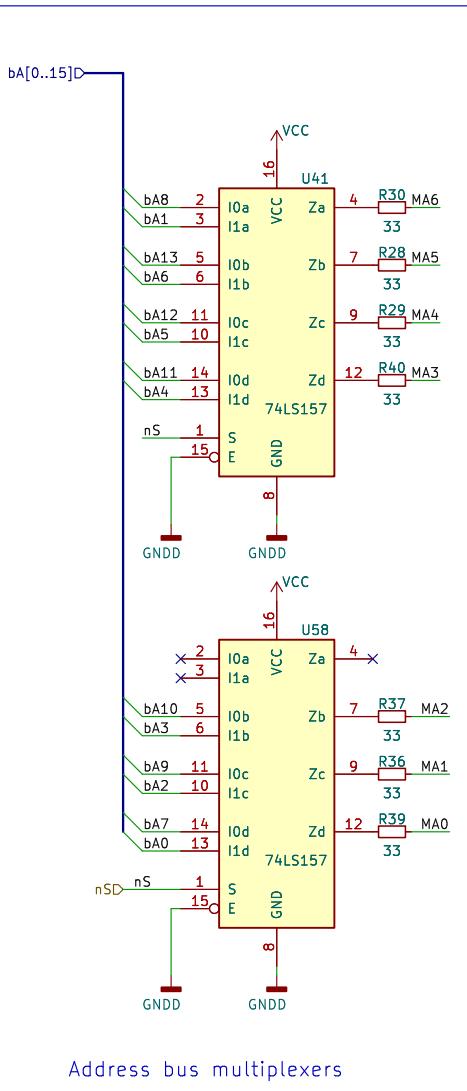
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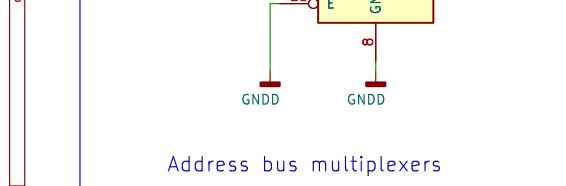


A



Address bus multiplexers

B



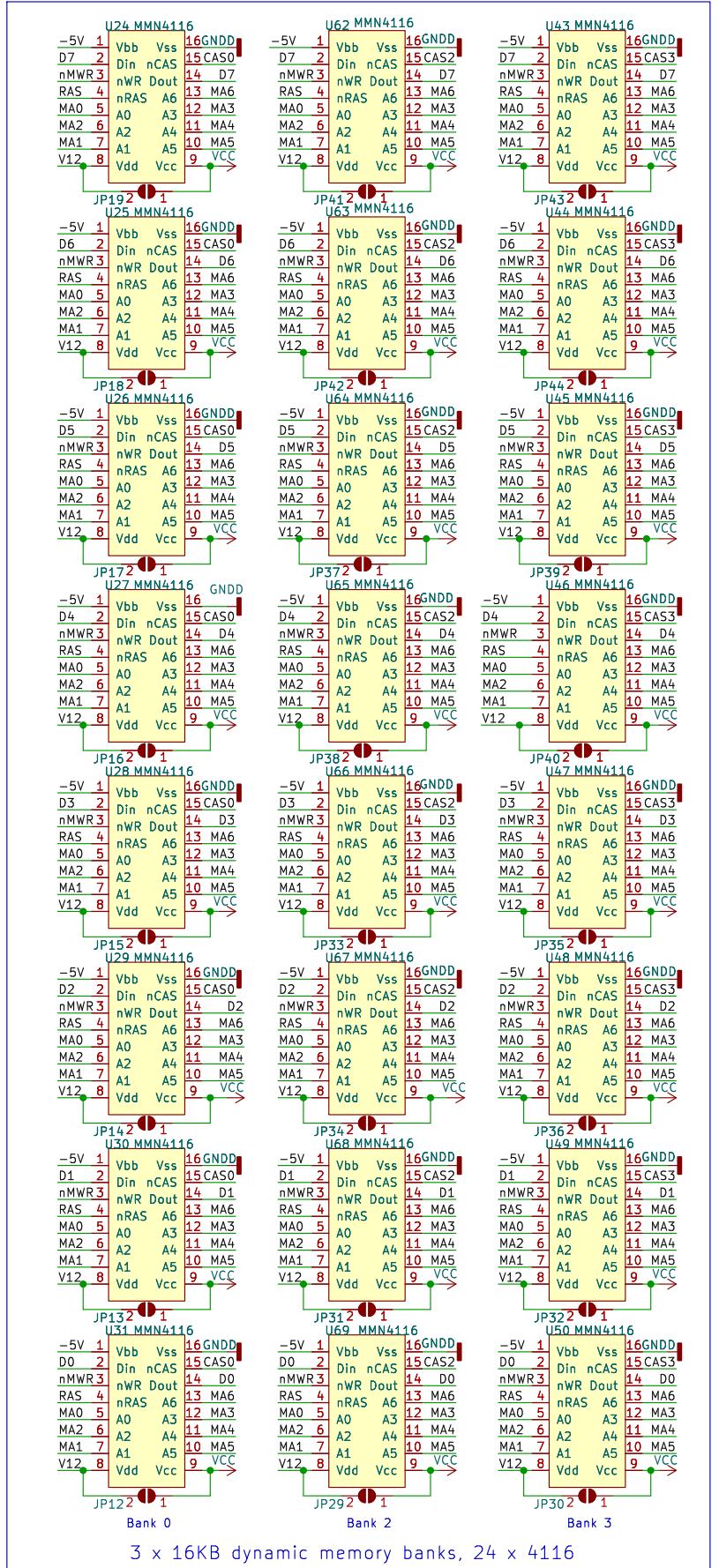
C



E



F



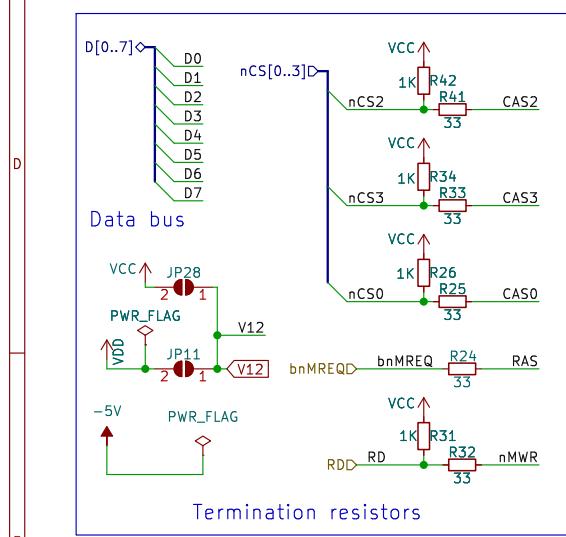
3 x 16KB dynamic memory banks, 24 x 4116

Sheet: /48K RAM & MUX/  
File: RAM\_48.kicad\_sch

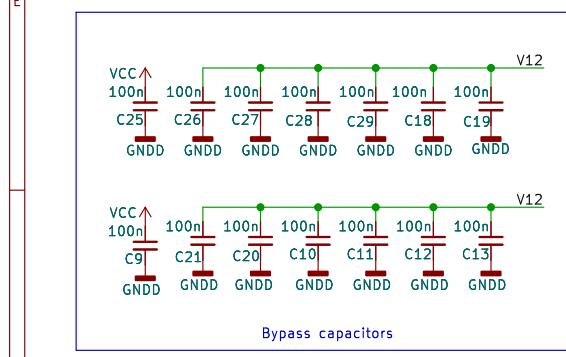
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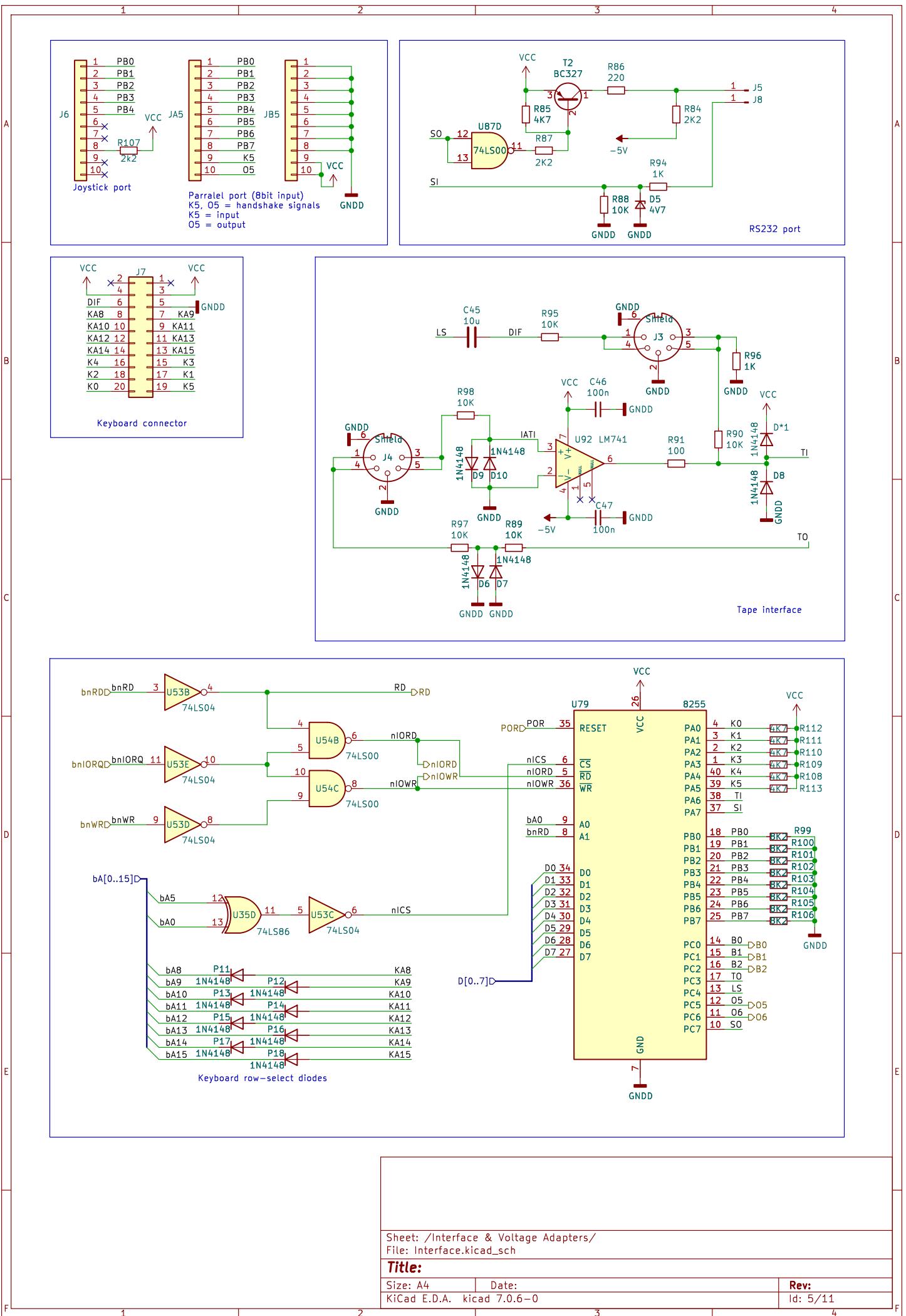
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| Rev: | Id: 3/11 |
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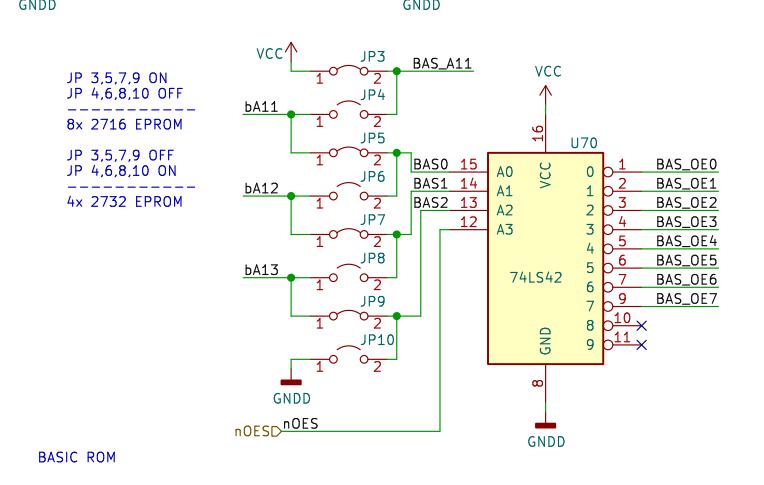
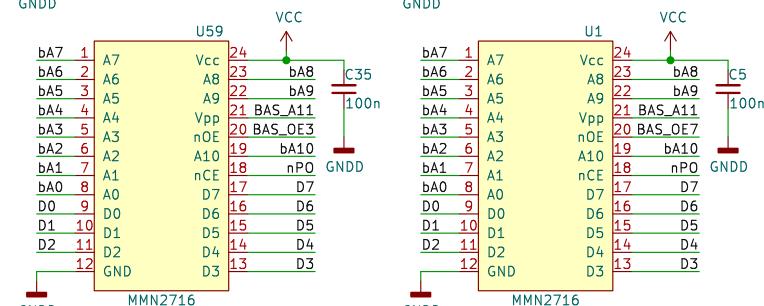
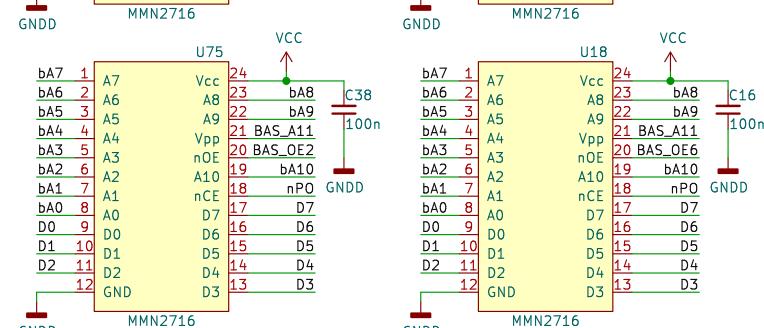
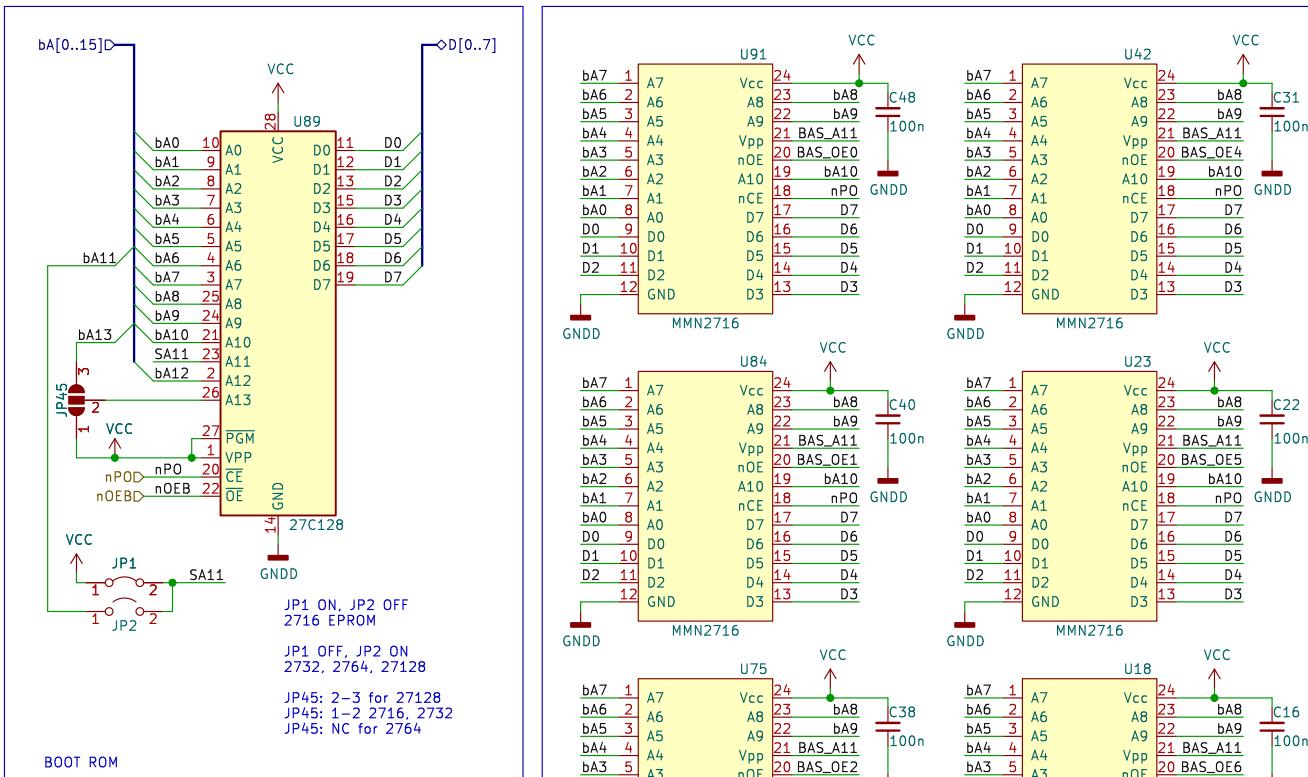


Termination resistors



Bypass capacitors

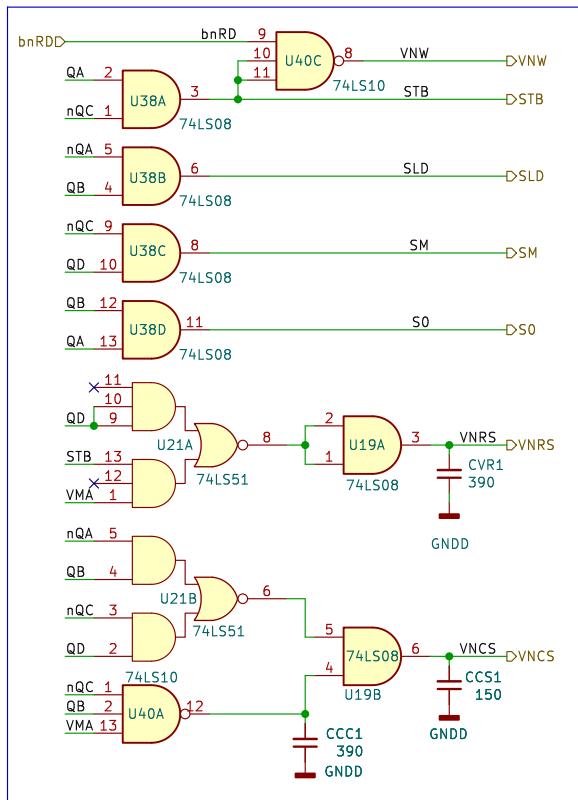
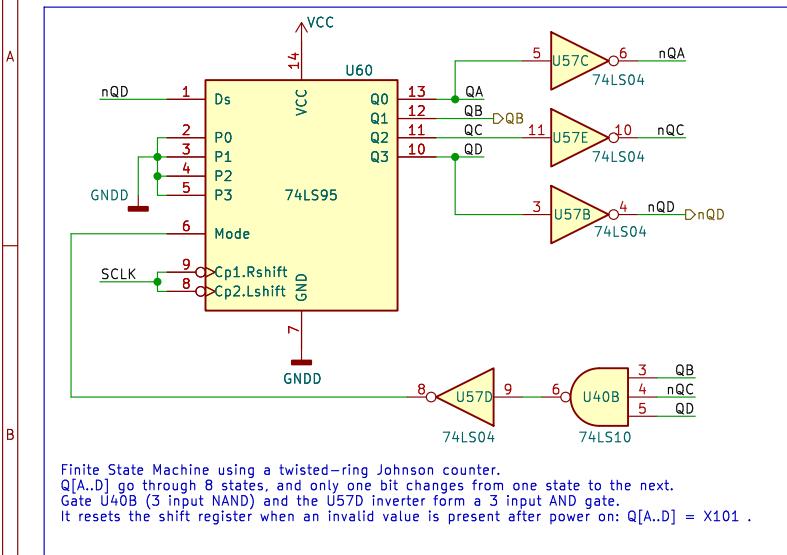




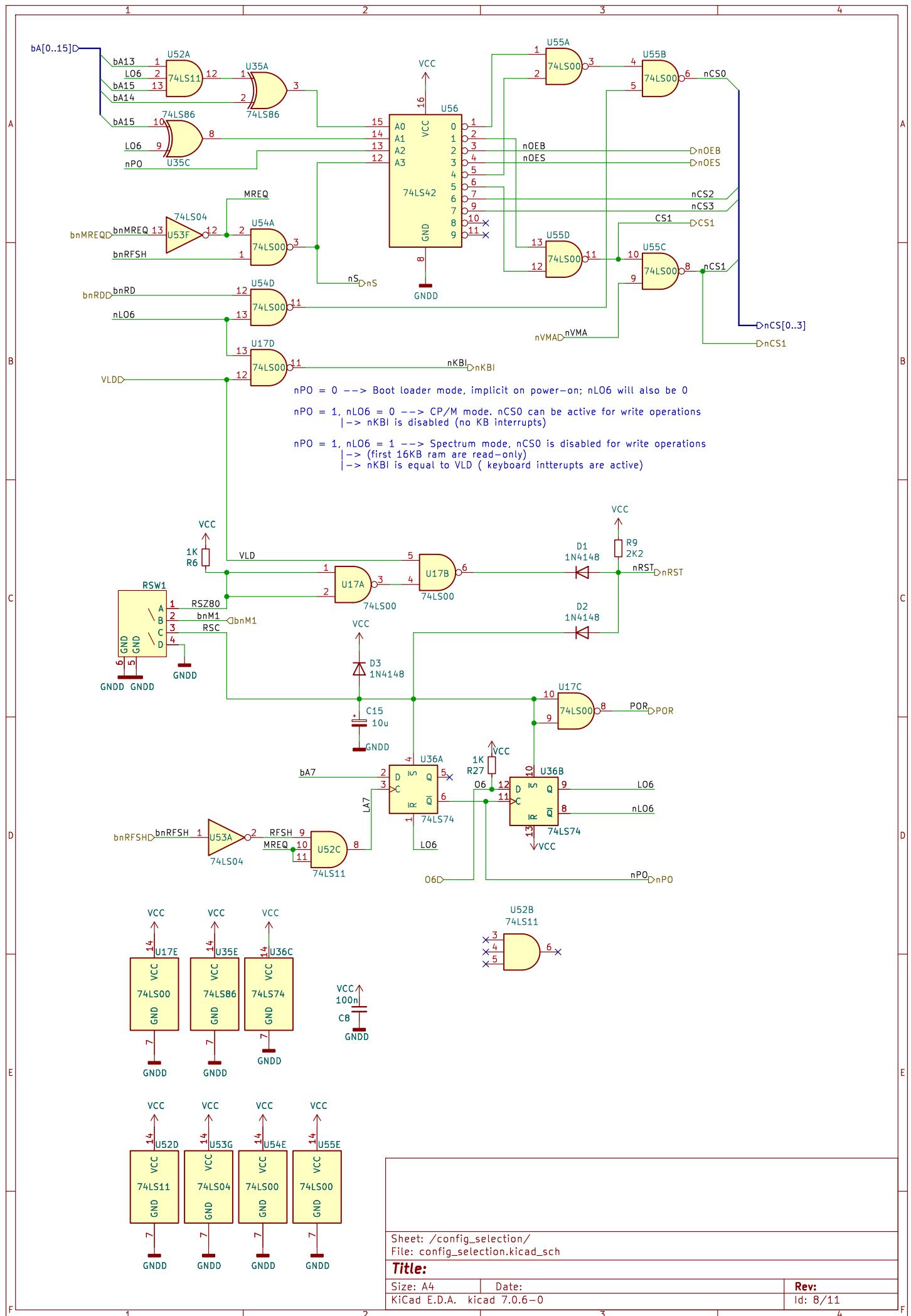
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File: ROM.kicad\_sch

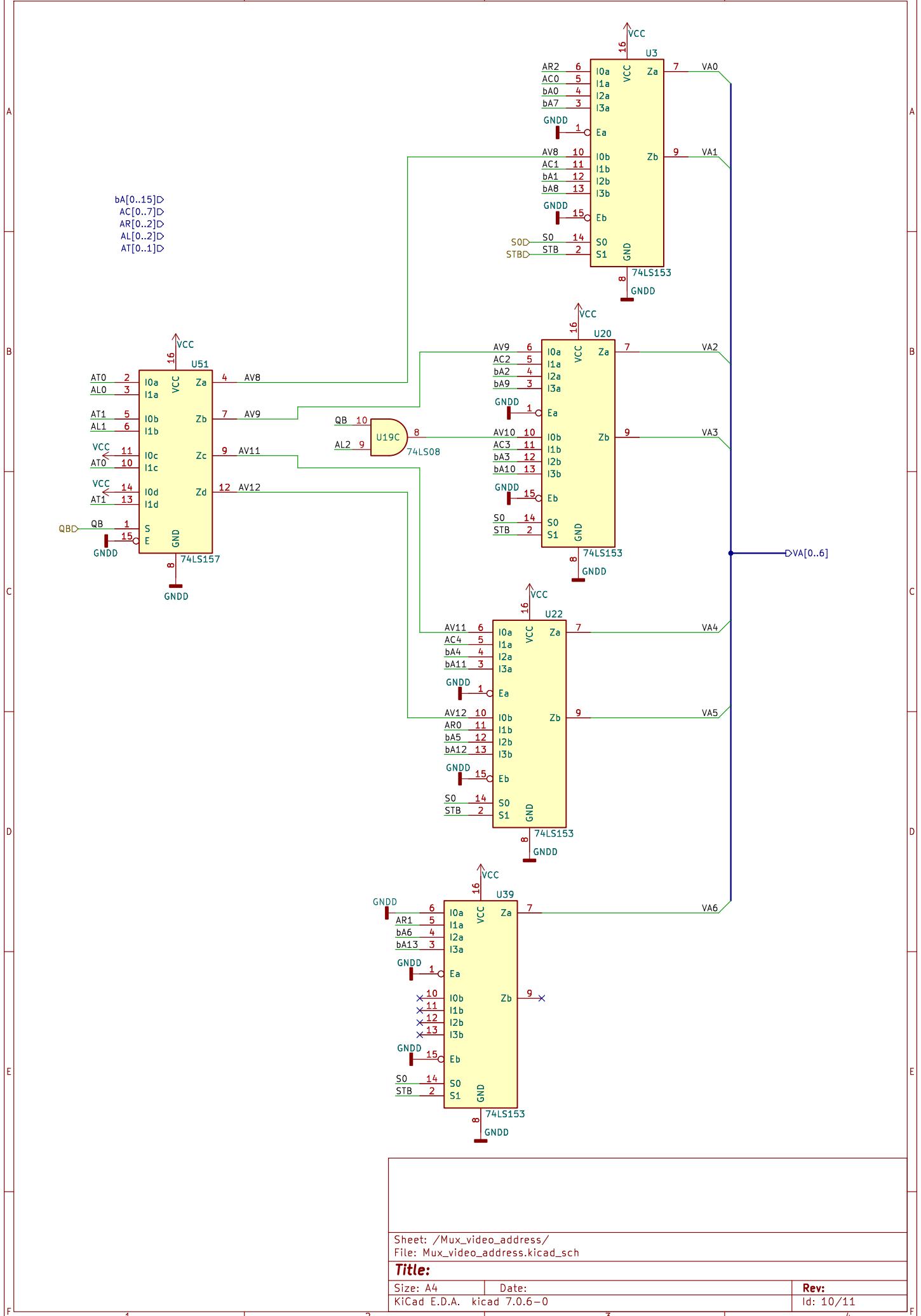
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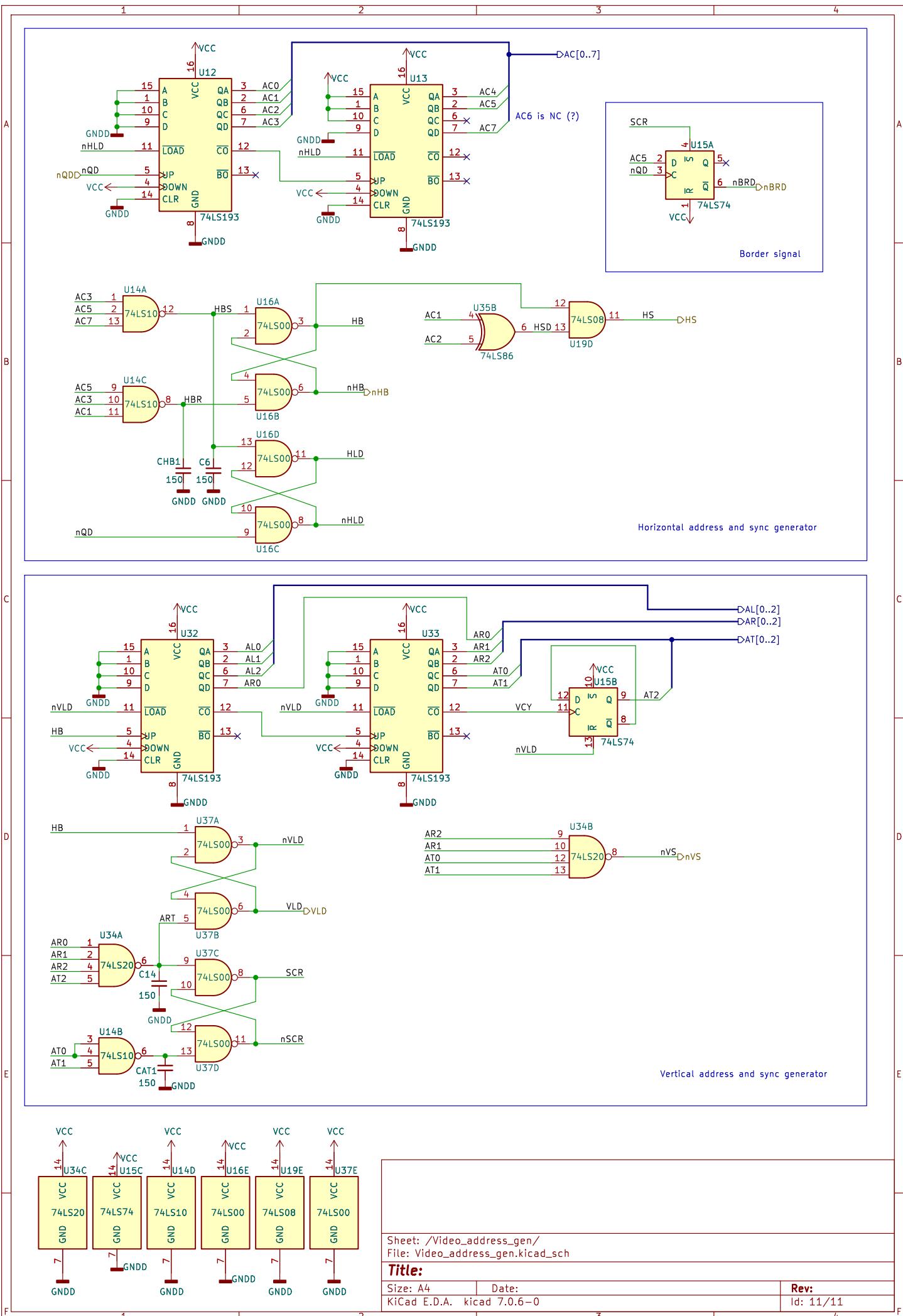
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KiCad E.D.A. kicad 7.0.6-0 Id: 6/11



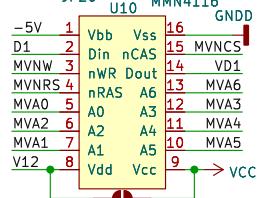
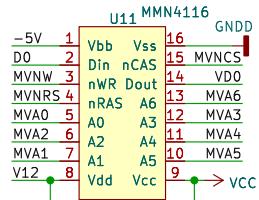
**VNW** – Video Not Write, active-low signal, video DRAM bank WR pins  
**STB** – Strobe, loads P8212 video register with data from video memory, for CPU to read it  
 Also, it controls the video memory address multiplexer MSB, when SIB = 1, cpu address bus is selected  
**SLD** – Serializer Load, controls loading data from the video memory bus into the pixel shift registers  
**SM** – Serial Mode (?) – loads color attributes in shift registers used as 2x4bit D registers  
**S0** – Select Zero (not S0 which is Serial OUT) controls the video memory address multiplexer LSB performs the switching between ROW and COLUMN address for video dram  
**VNRS** – Video Not RAS is the RAS signal for the video memory DRAM  
**VNCS** – Video Not CAS is the CAS signal for the video memory DRAM



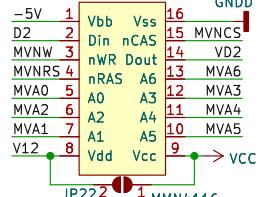




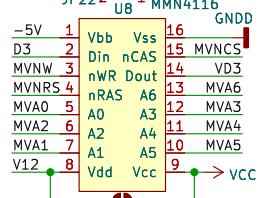
A



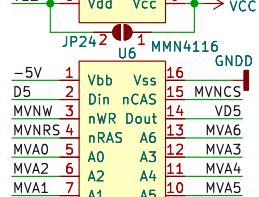
B



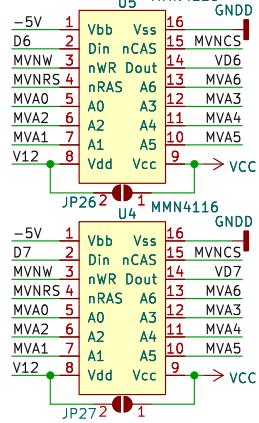
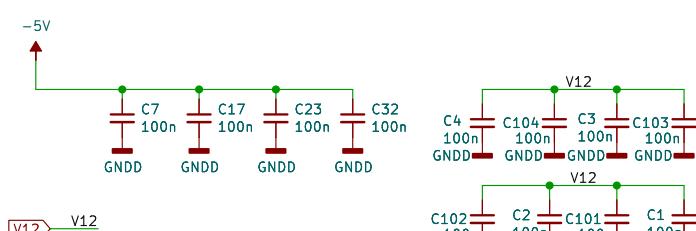
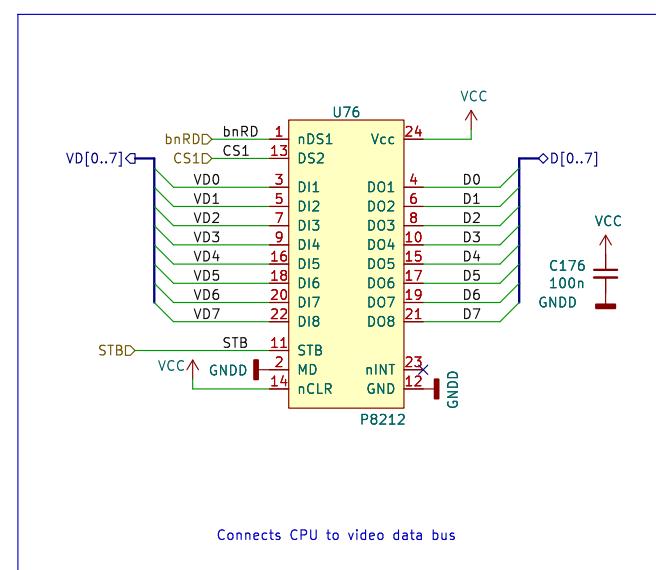
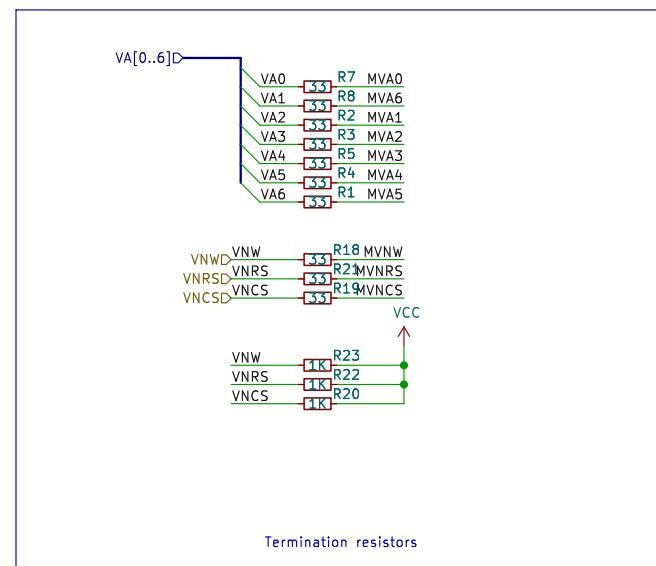
C



D



E

DRAM Bank 1  
Video memorySheet: /Video\_memory/  
File: Video\_memory.kicad\_sch**Title:**

Size: A4 Date:

KiCad E.D.A. kicad 7.0.6-0

Rev:

Id: 12/11

