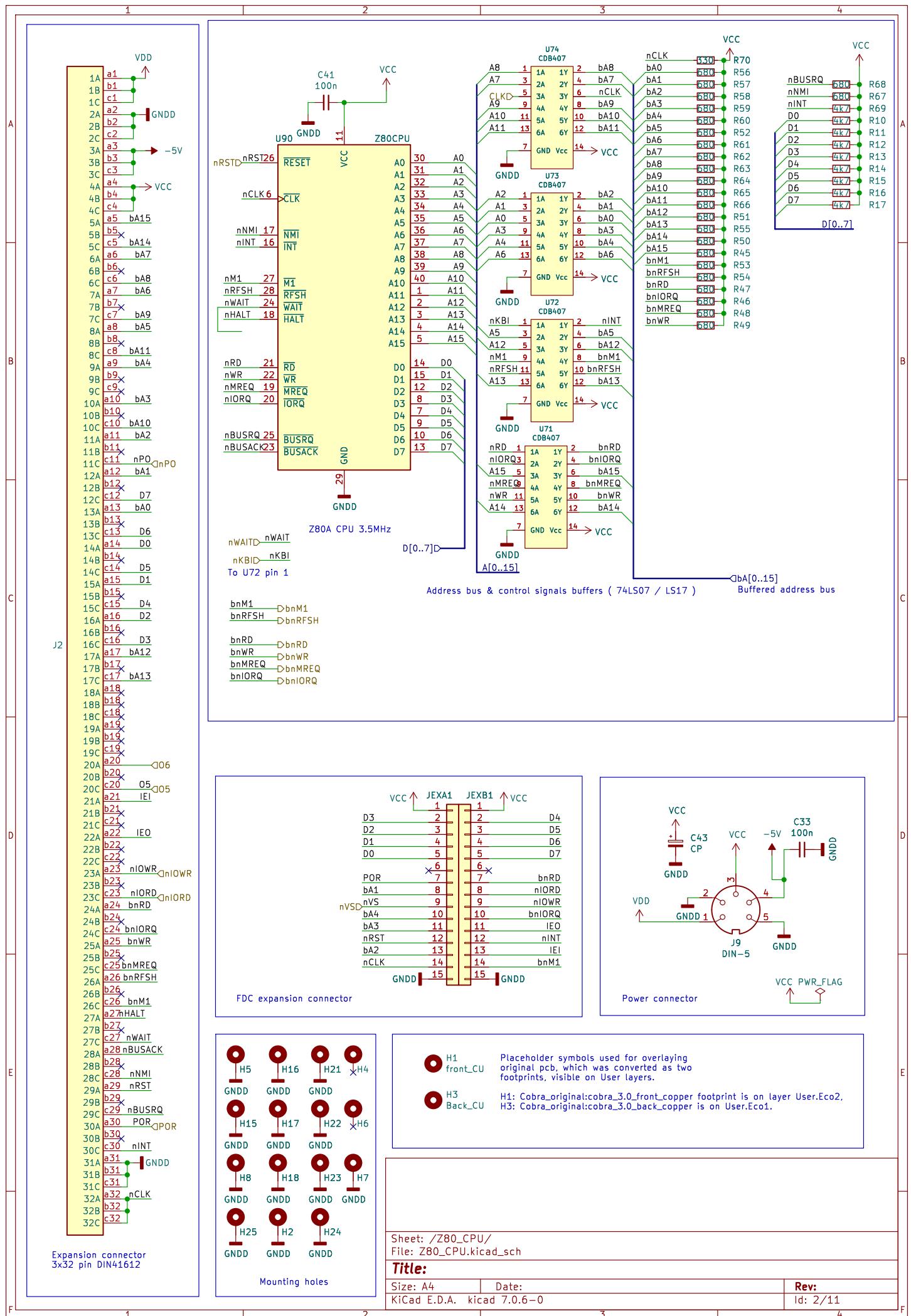
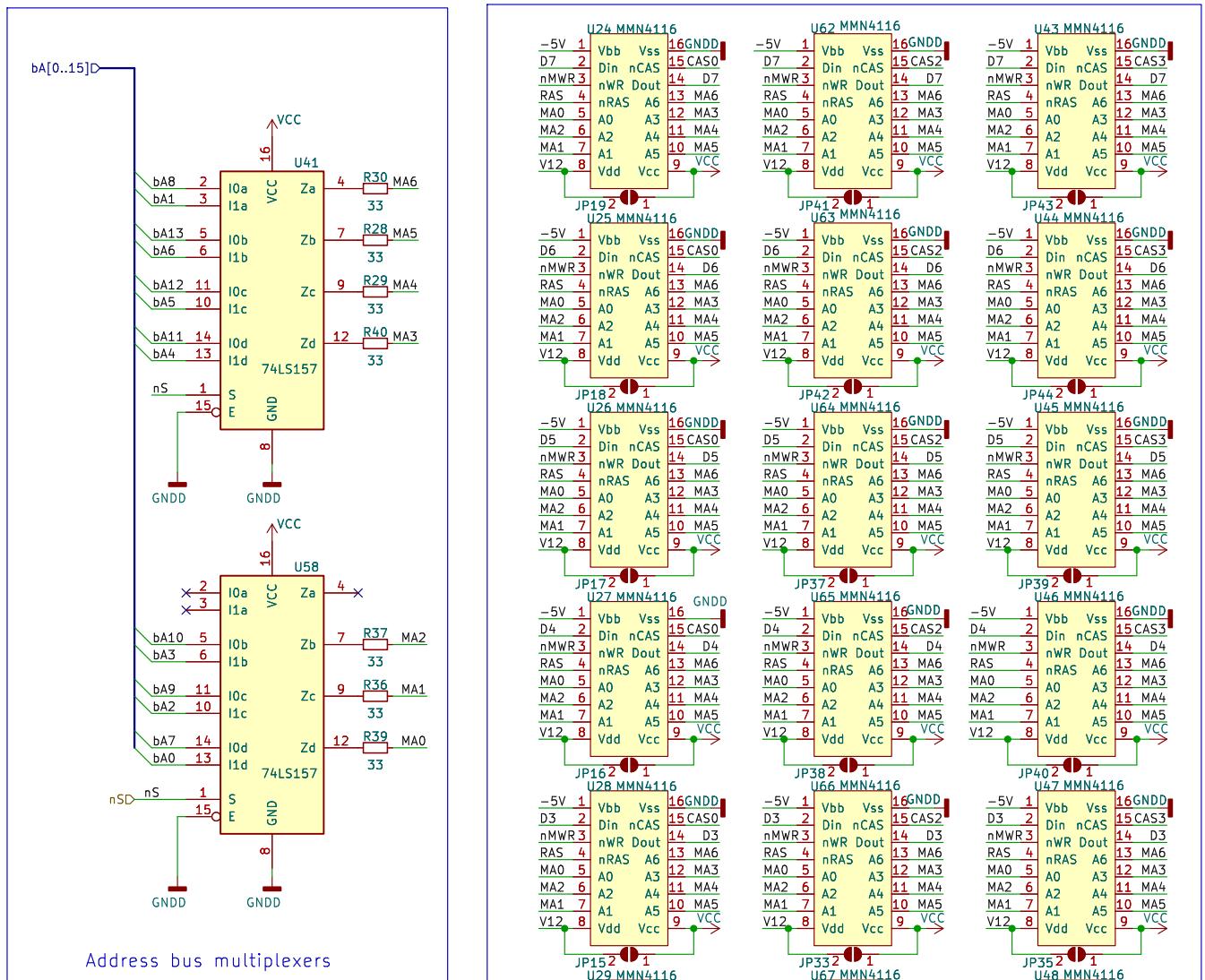


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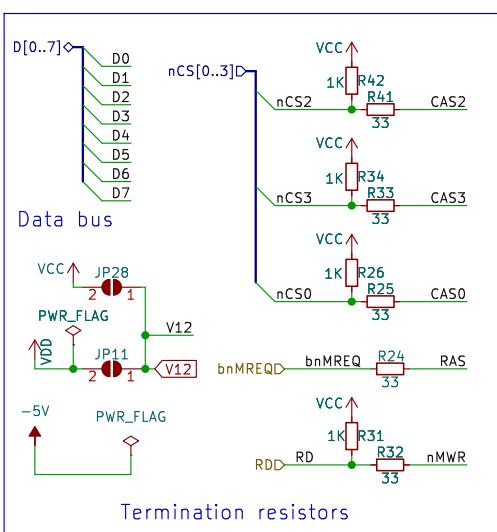
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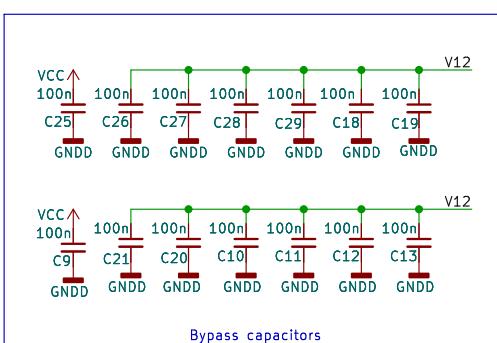




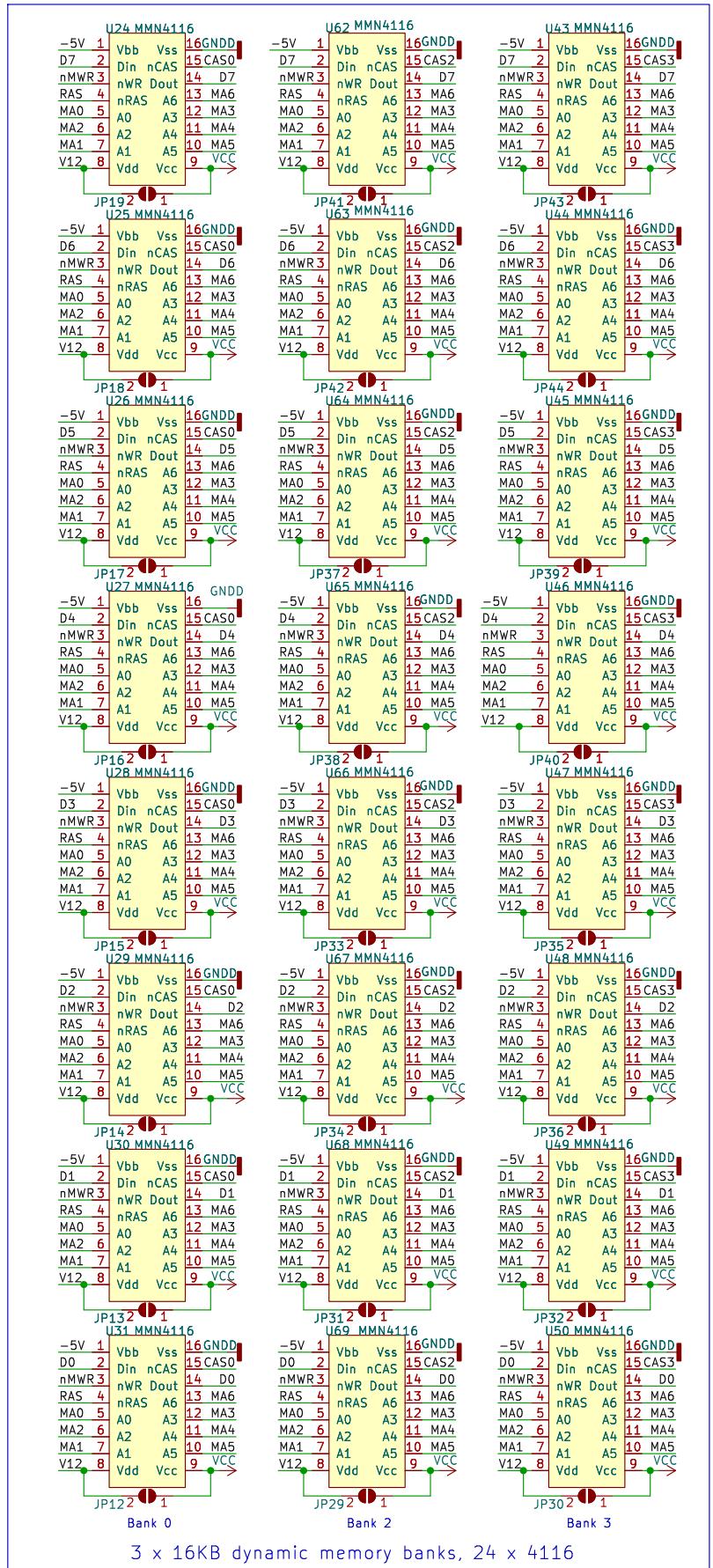
Address bus multiplexers



Termination resistors



Bypass capacitors



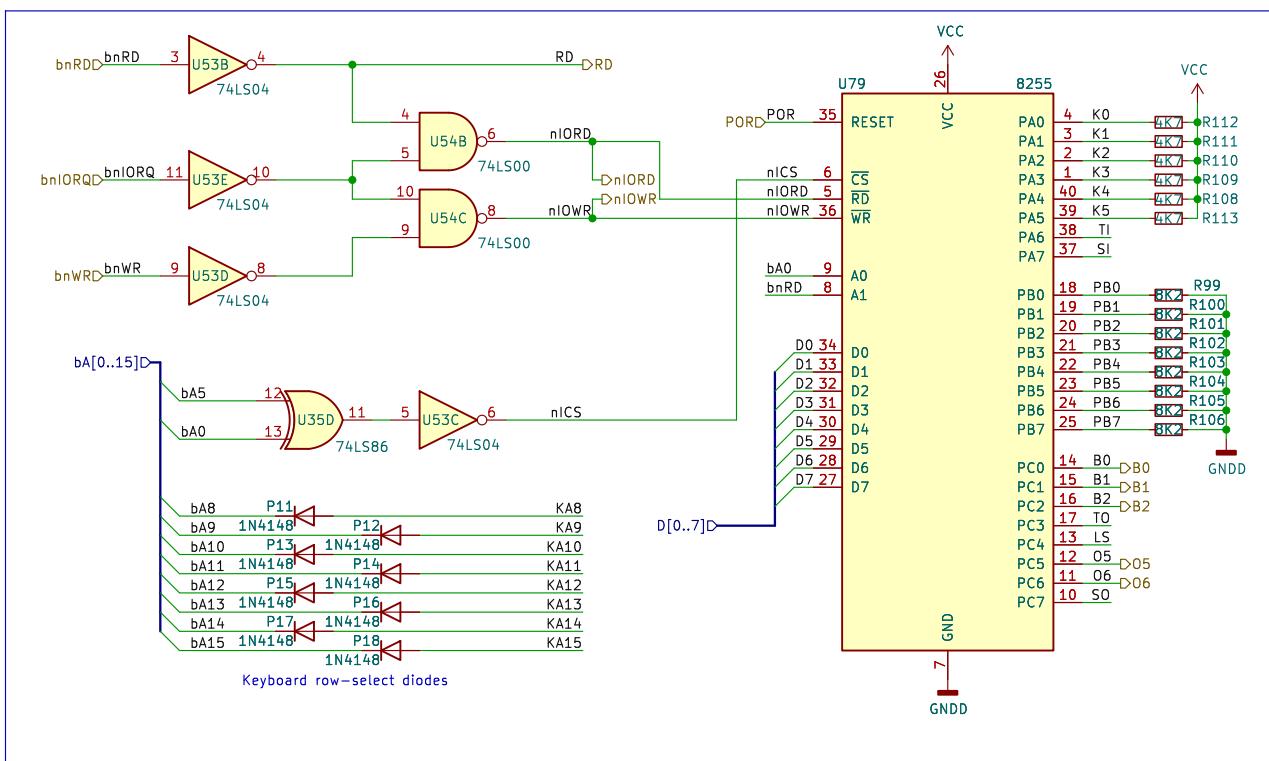
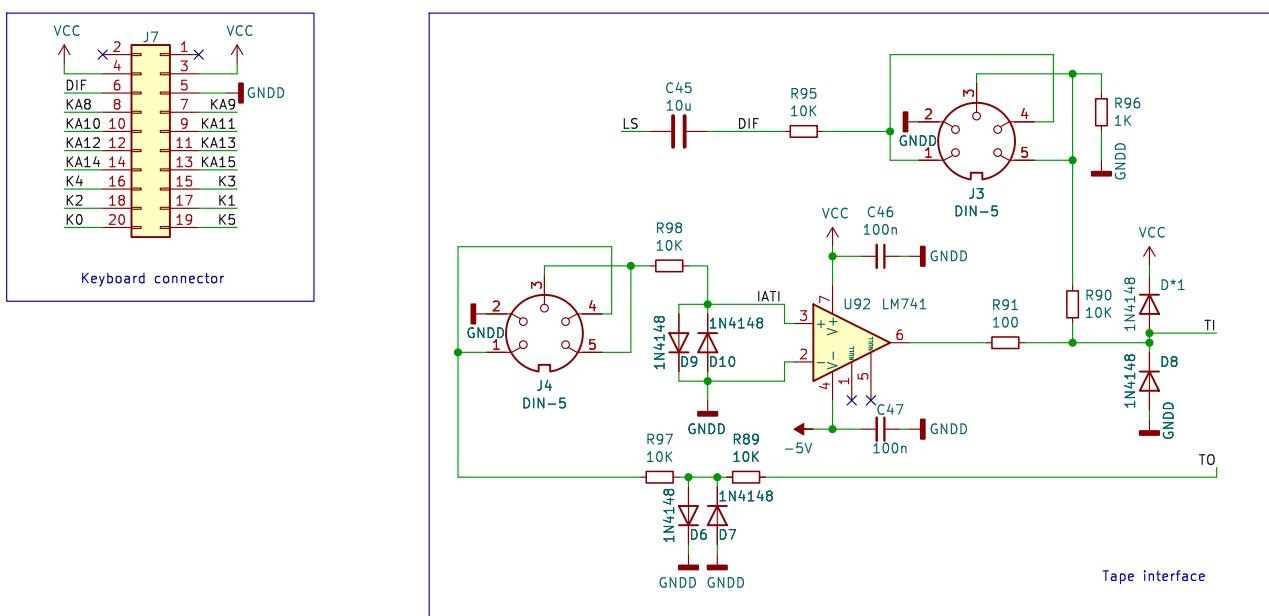
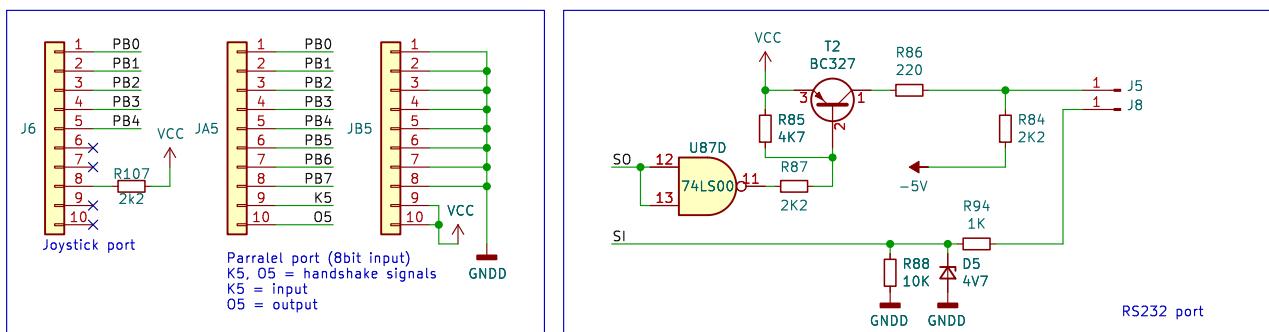
3 x 16KB dynamic memory banks, 24 x 4116

Sheet: /48K RAM & MUX/
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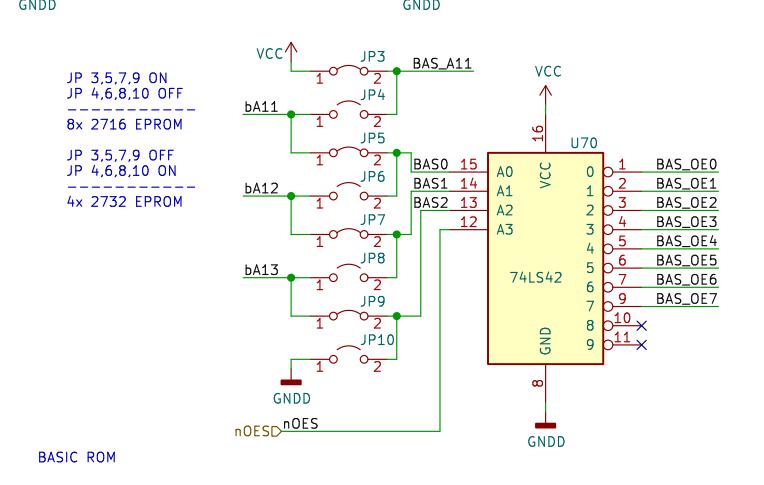
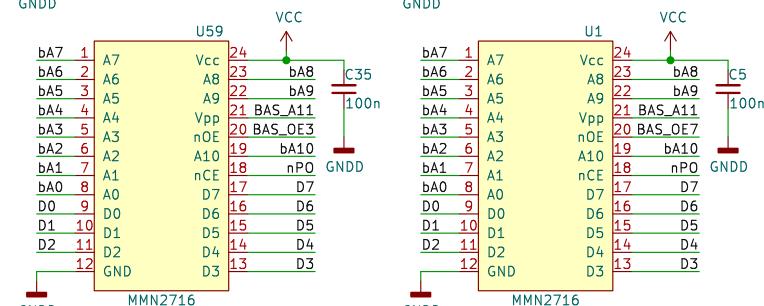
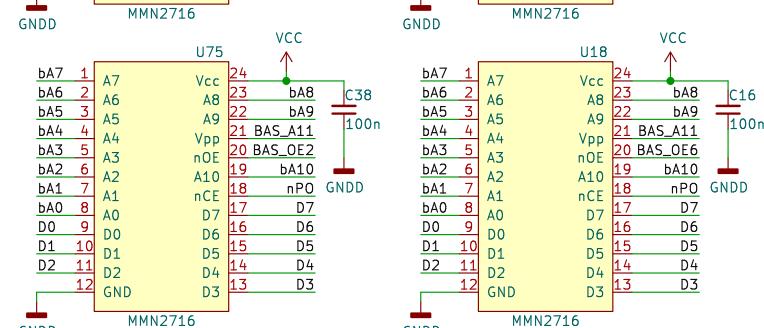
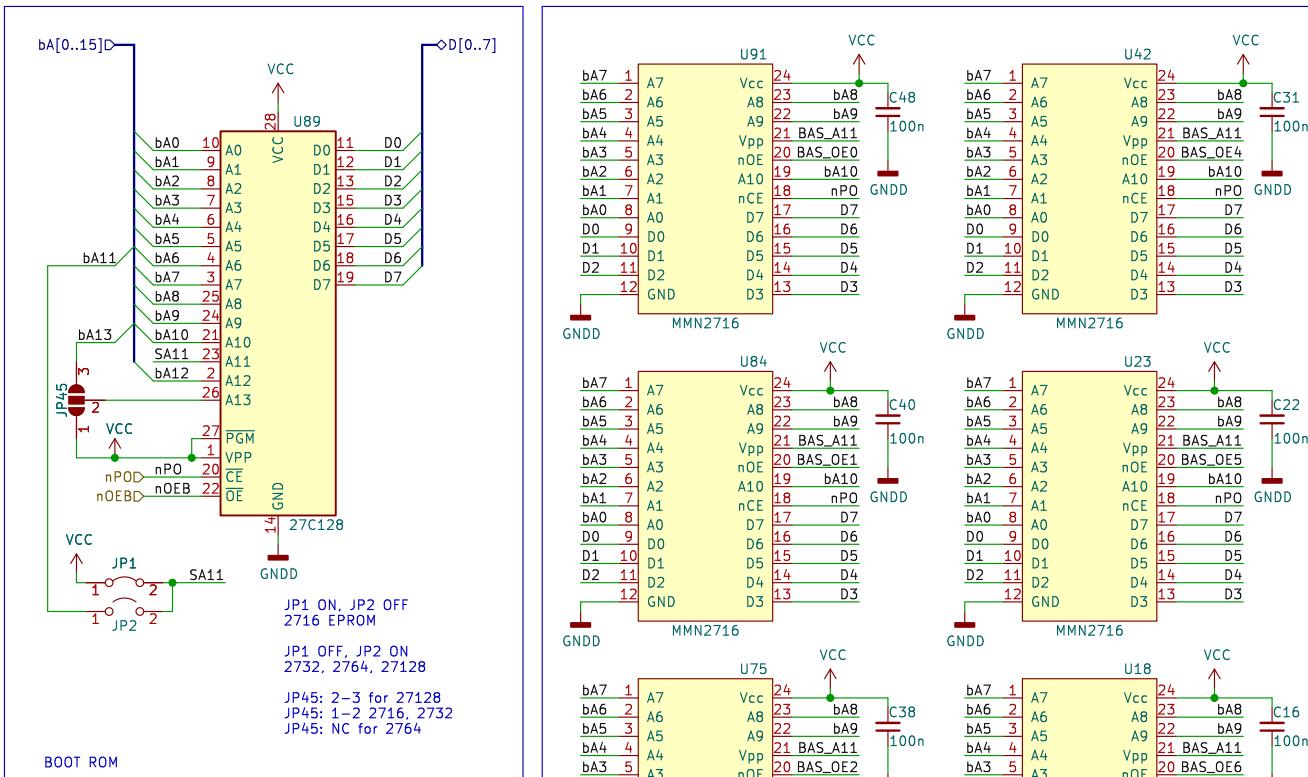


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Size: A4 Date:
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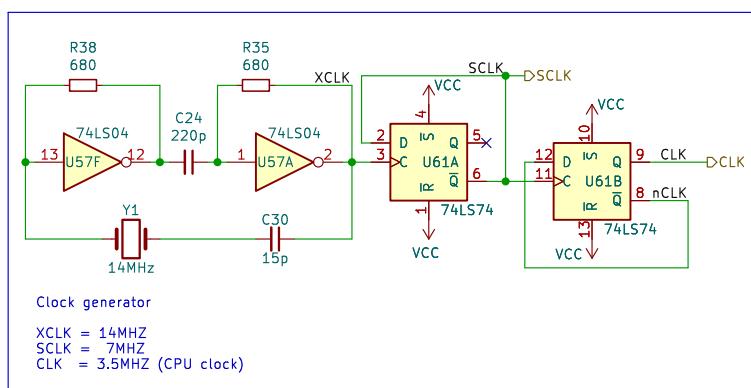
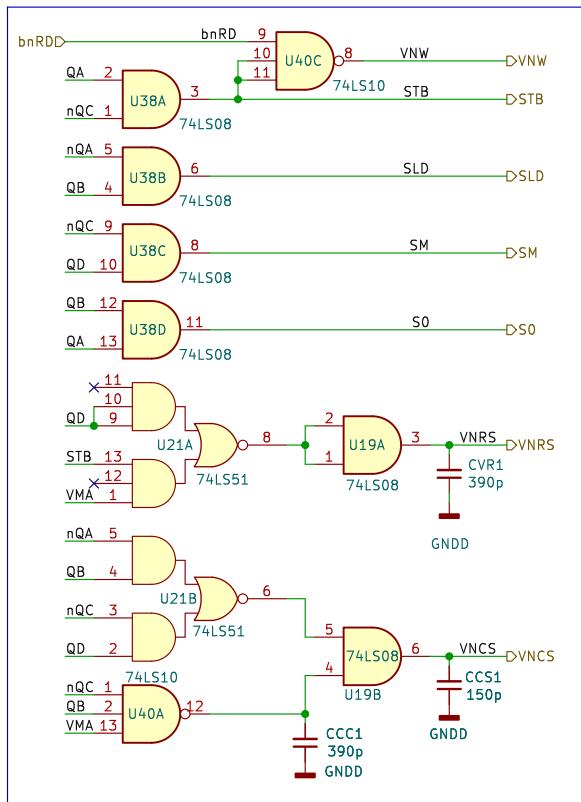
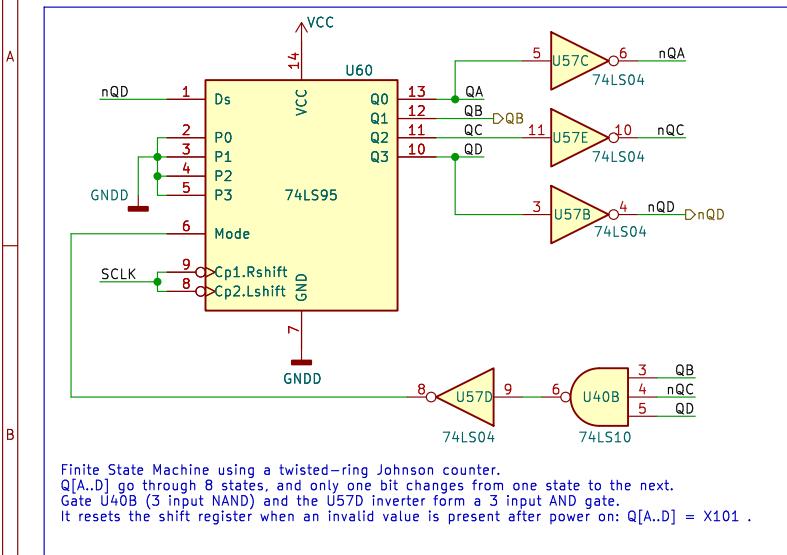
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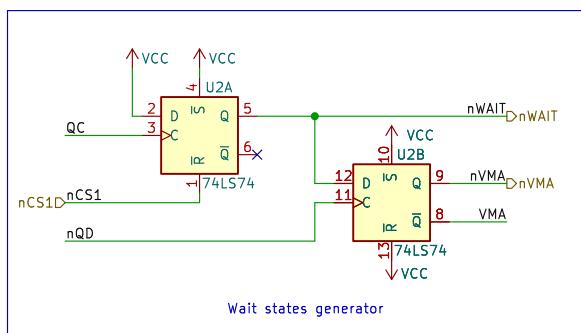
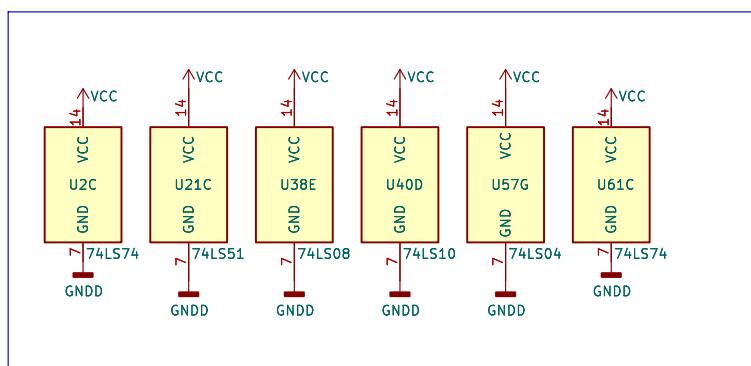
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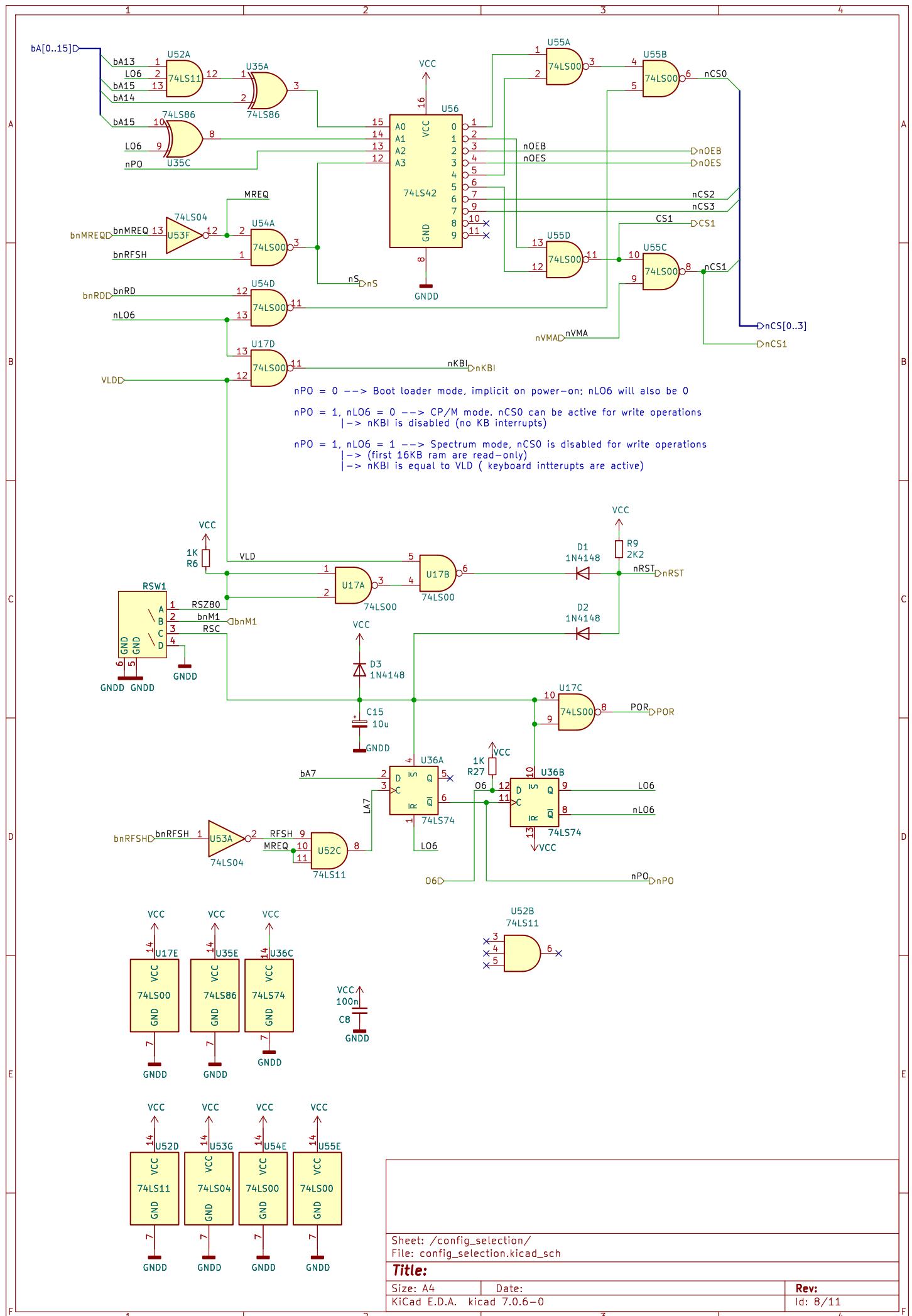
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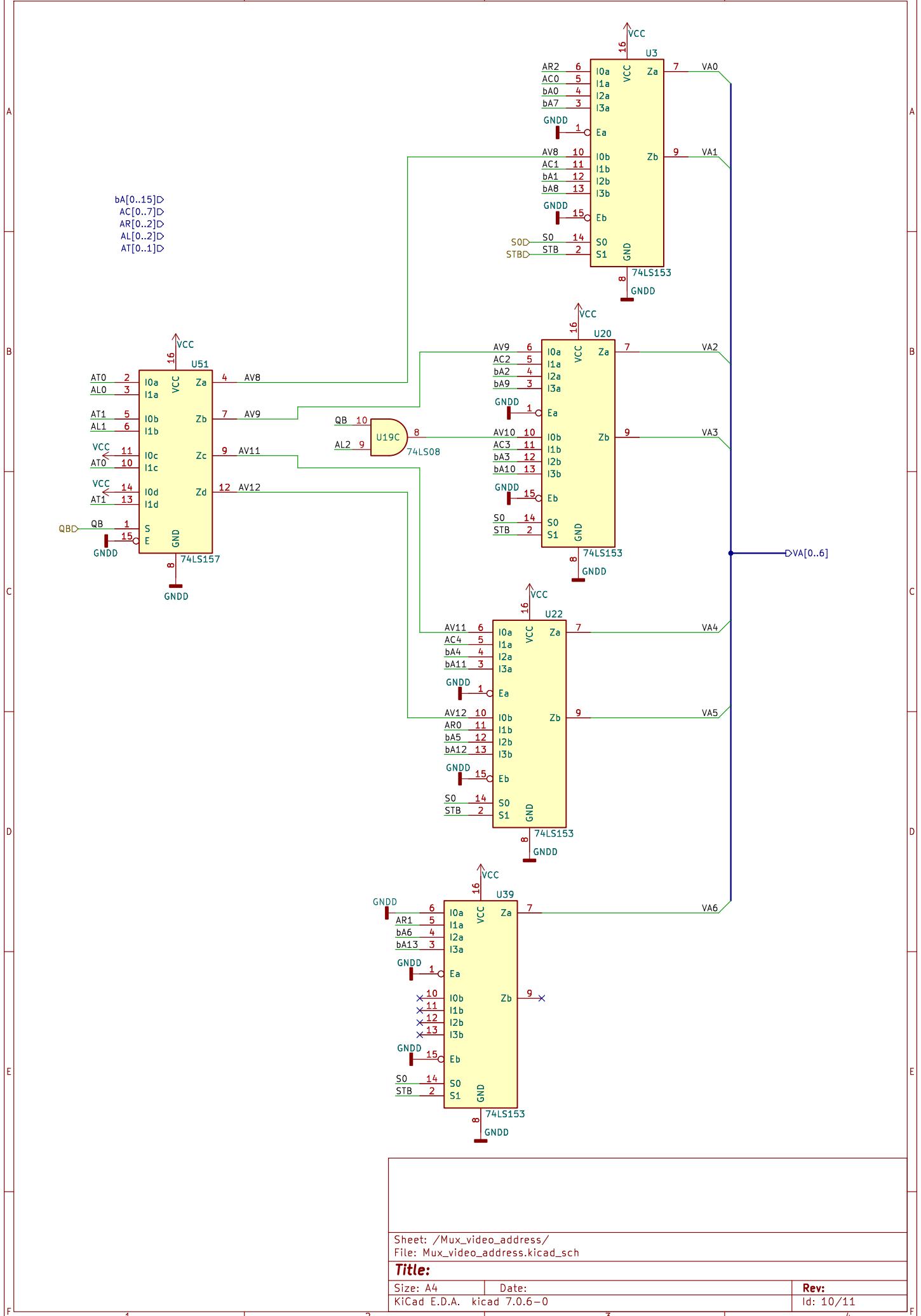
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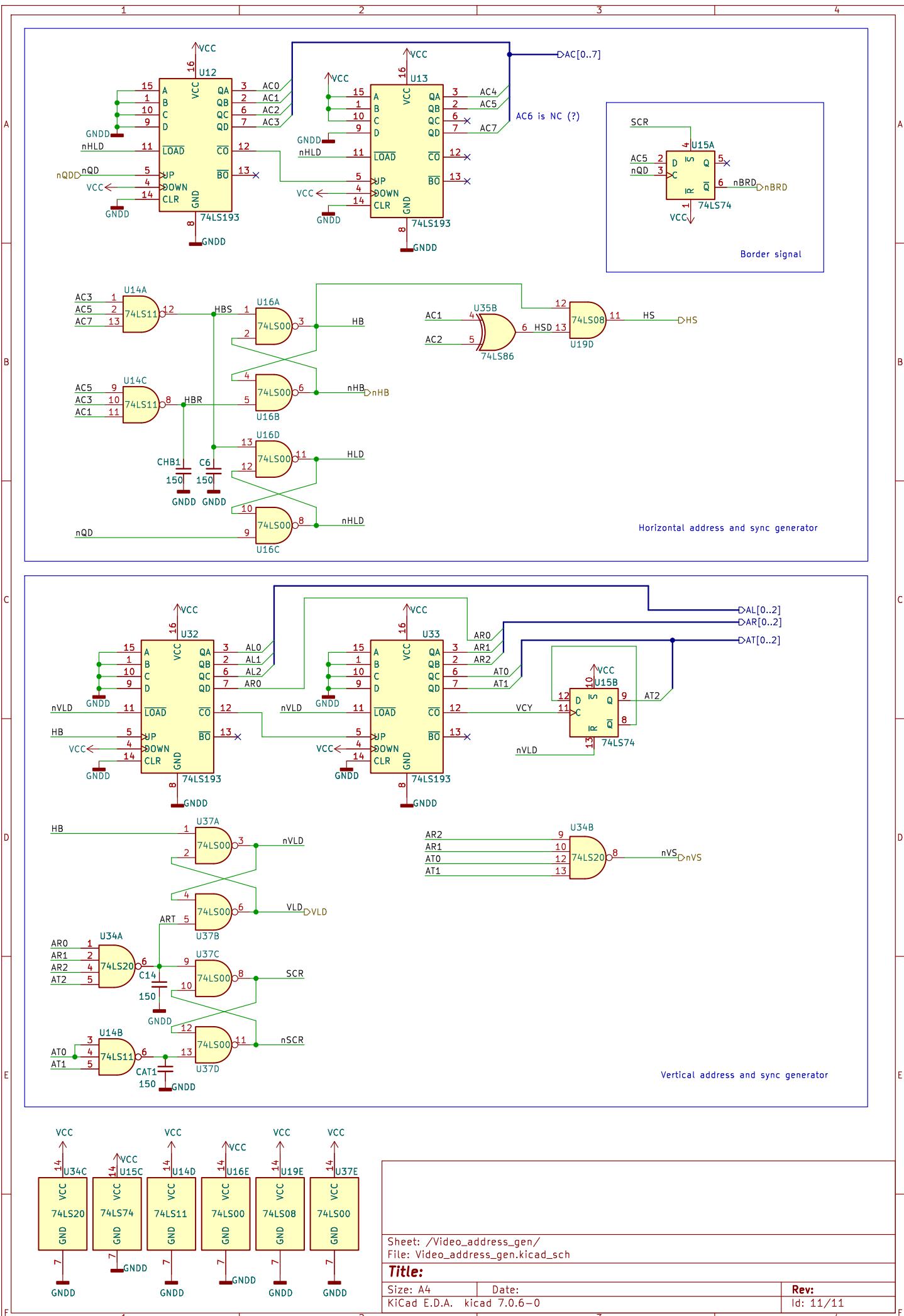


VNW – Video Not Write, active-low signal, video DRAM bank WR pins
STB – Strobe, loads P8212 video register with data from video memory, for CPU to read it
Also, it controls the video memory address multiplexer MSB, when SIB = 1, cpu address bus is selected
SLD – Serializer Load, controls loading data from the video memory bus into the pixel shift registers
SM – Serial Mode (?) – loads color attributes in shift registers used as 2x4bit D registers
SO – Select Zero (not SO which is Serial OUT)
controls the video memory address multiplexer LSB
performs the switching between ROW and COLUMN address for video dram
VNRS – Video Not RAS is the RAS signal for the video memory DRAM
VNCS – Video Not CAS is the CAS signal for the video memory DRAM

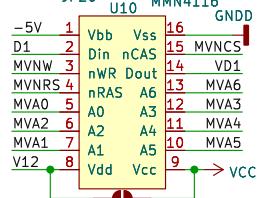
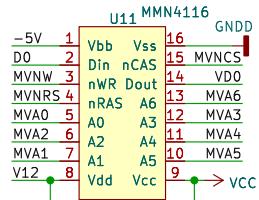




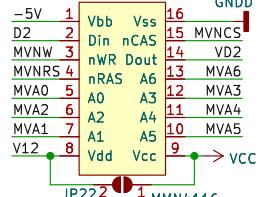




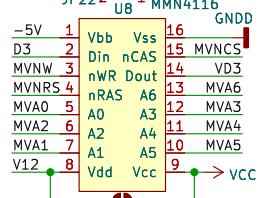
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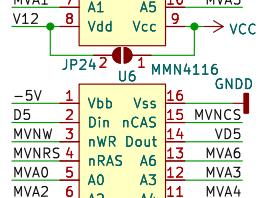
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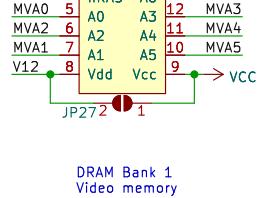
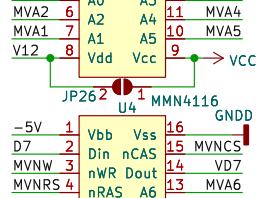
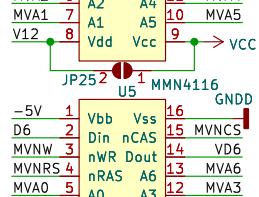
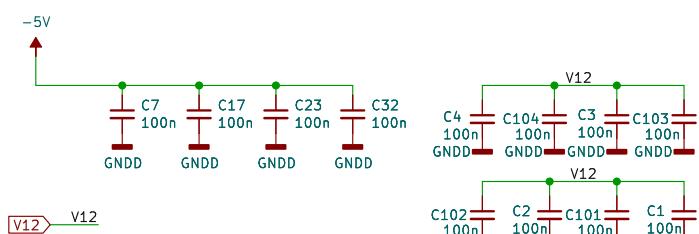
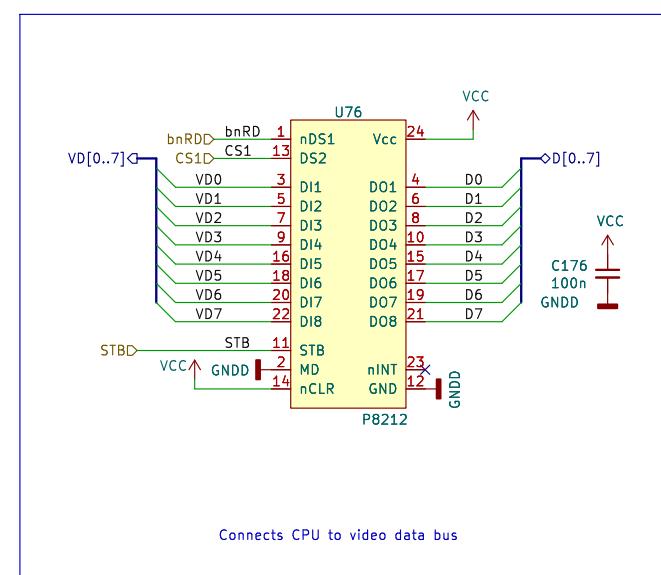
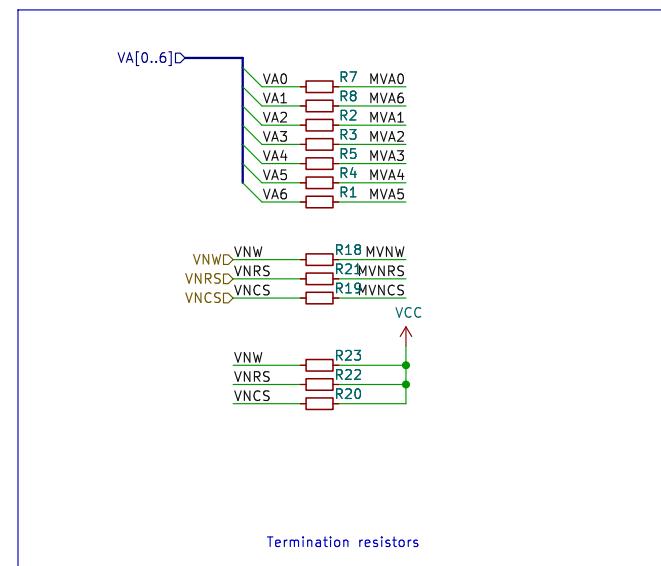
C



D



E

DRAM Bank 1
Video memory

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