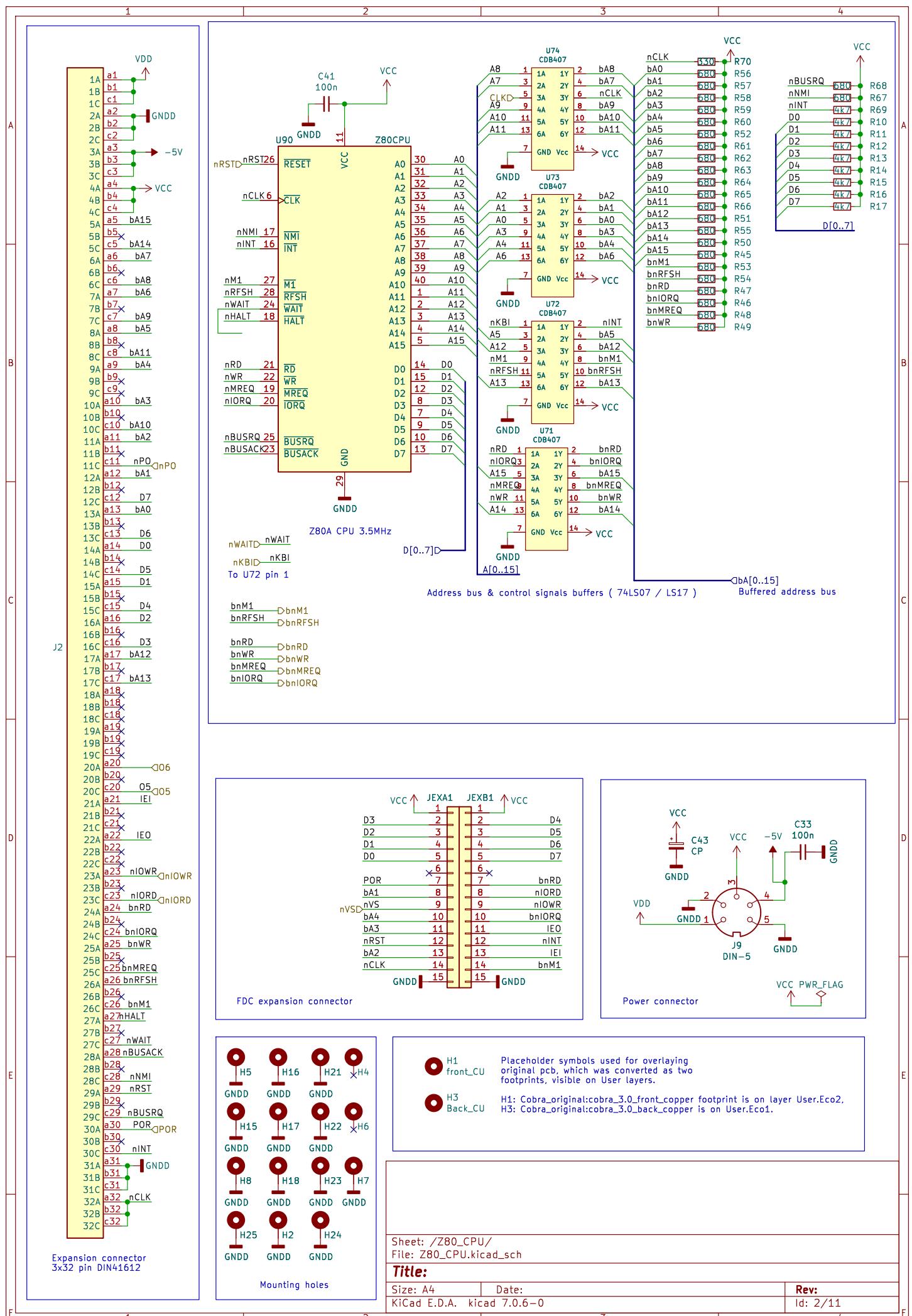


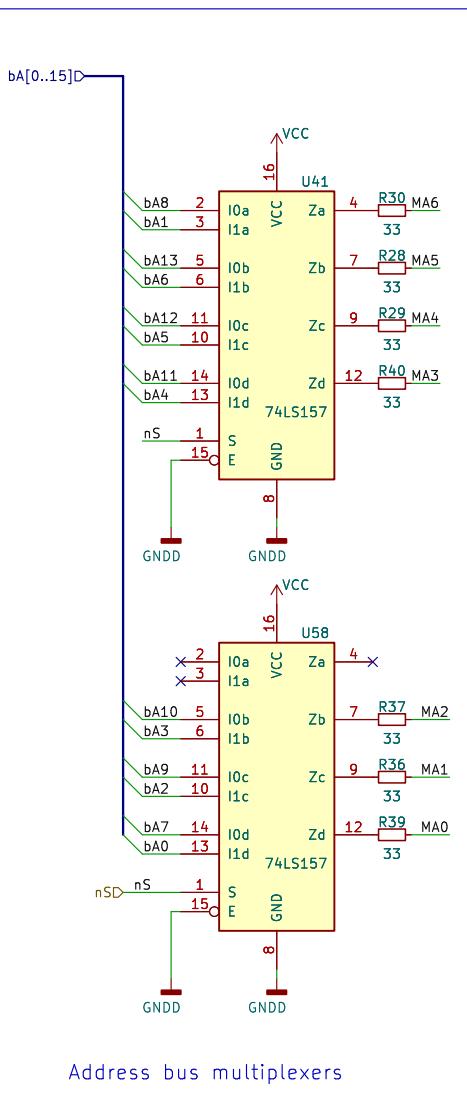
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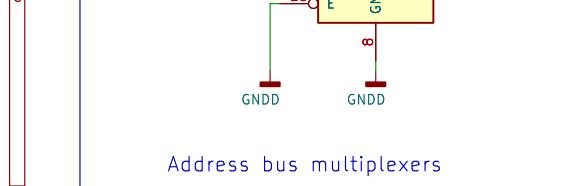


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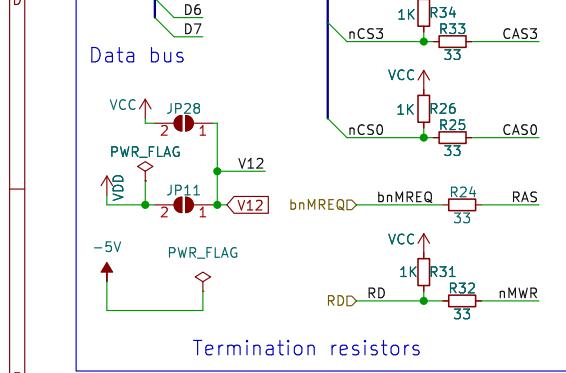


Address bus multiplexers

B

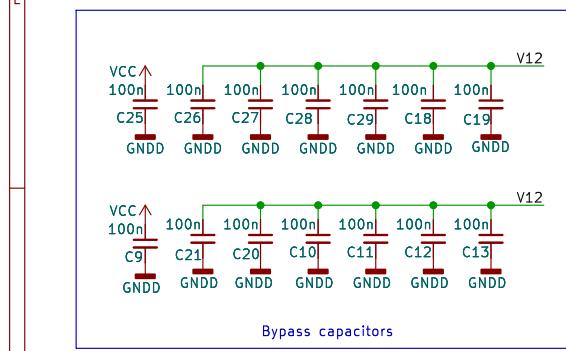


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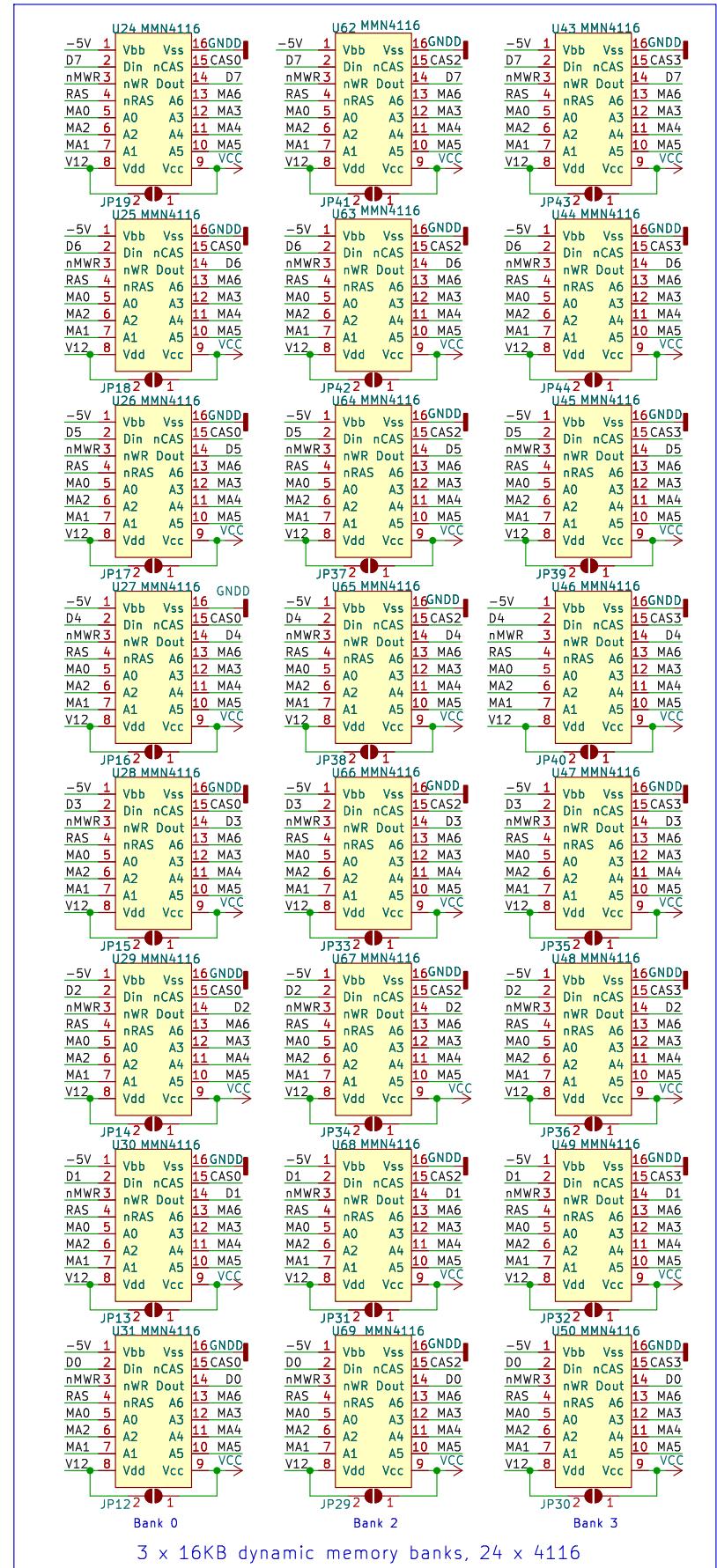


Termination resistors

E



Bypass capacitors



3 x 16KB dynamic memory banks, 24 x 4116

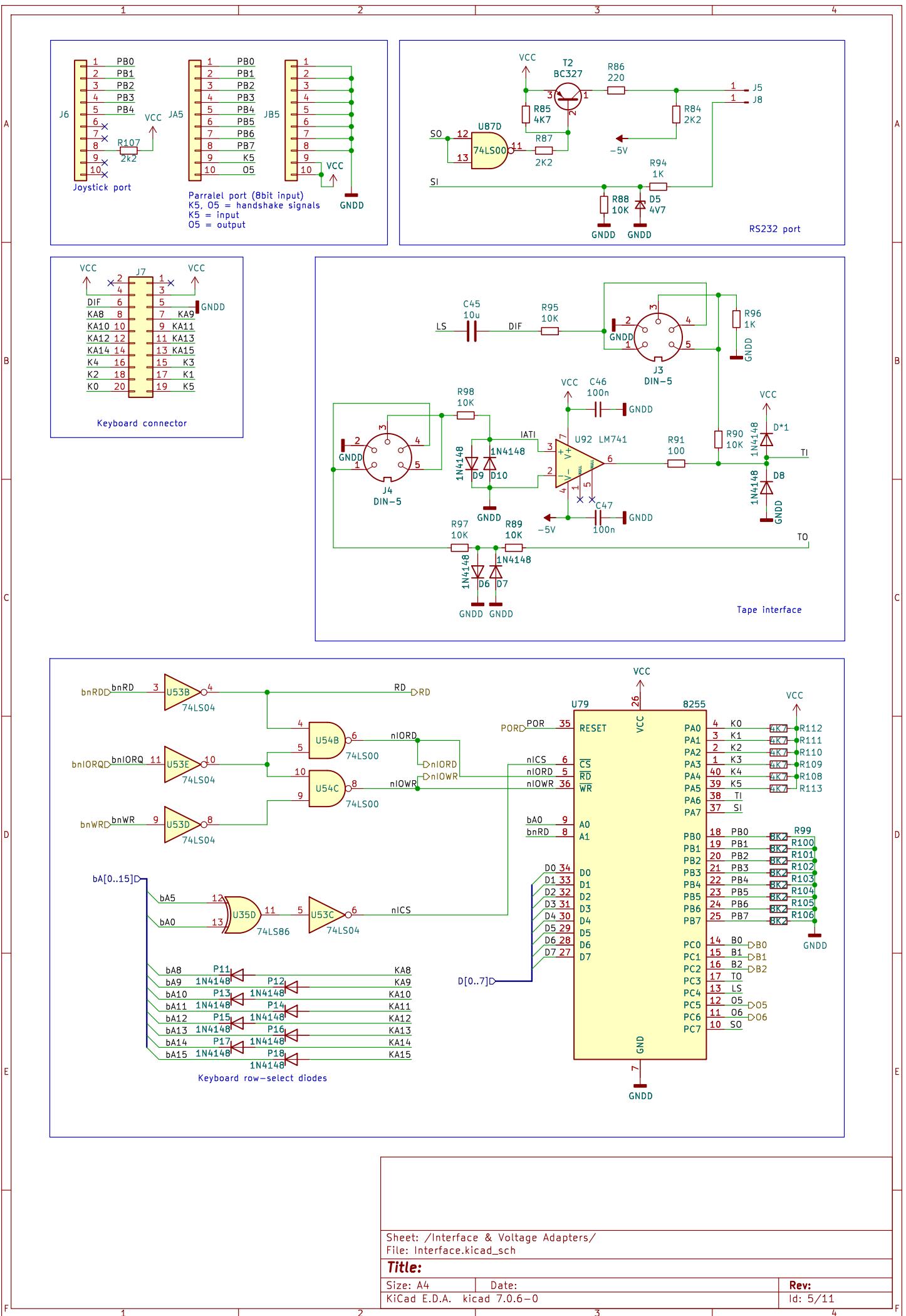
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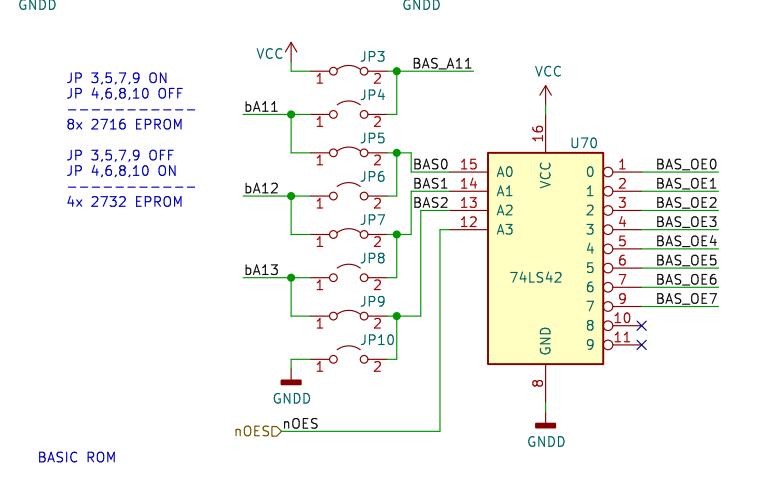
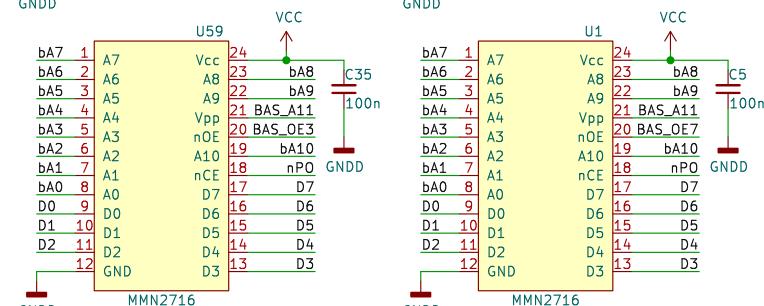
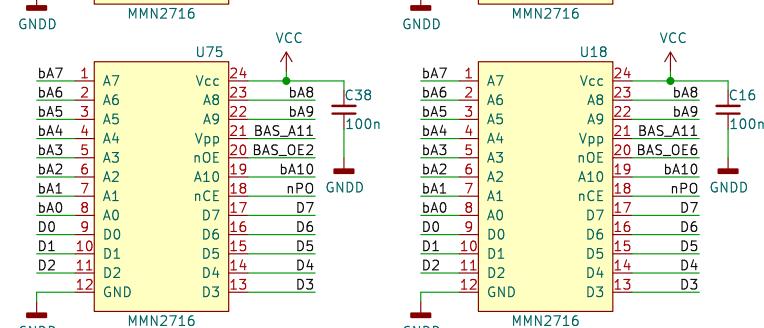
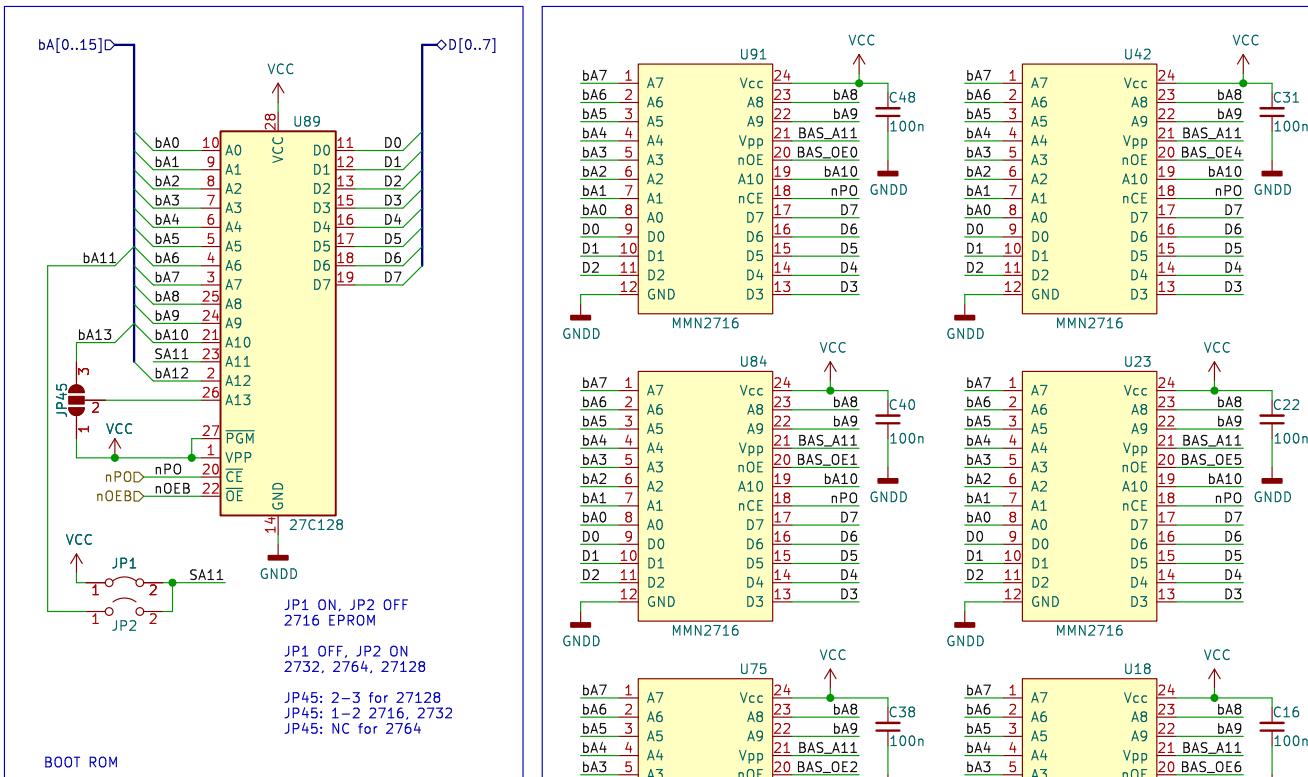
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F

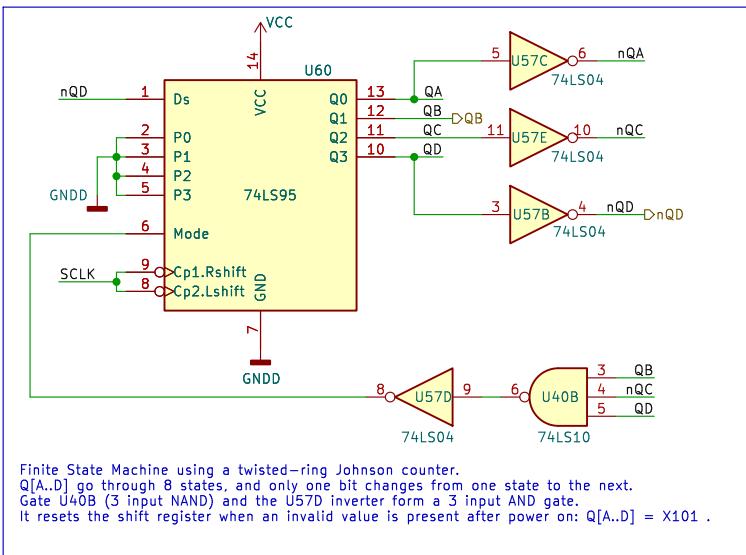




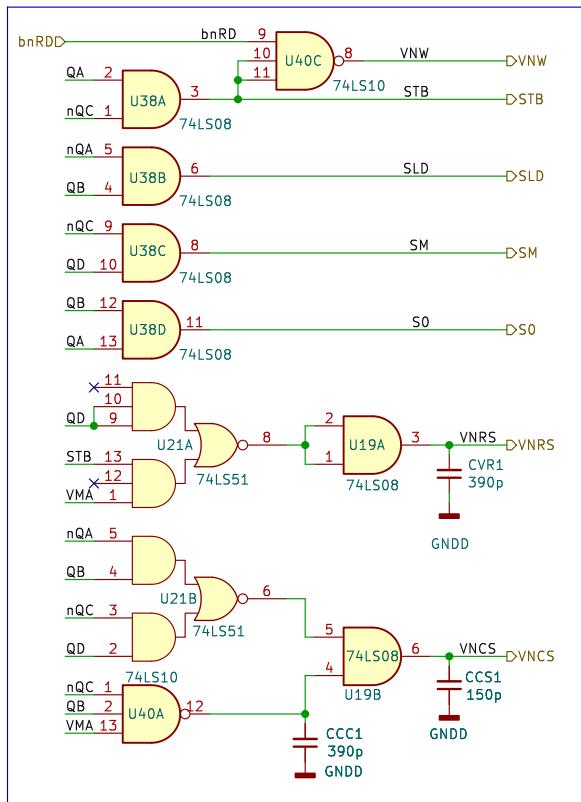
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Finite State Machine using a twisted-ring Johnson counter.
 Q[A..D] go through 8 states, and only one bit changes from one state to the next.
 Gate U408 (3 input NAND) and the U507 inverter form a 3 input AND gate.
 It resets the shift register when an invalid value is present after power on: Q[A..D] = X101 .



VNW – Video Not Write, active-low signal, video DRAM bank WR pins

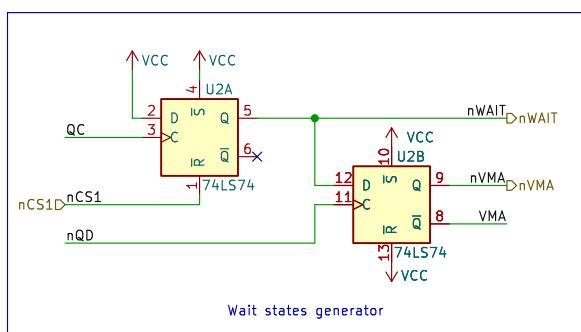
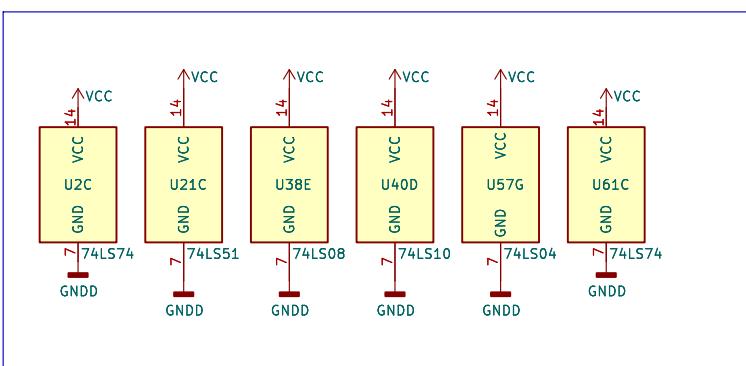
STB – Strobe, loads P8212 video register with data from video memory, for CPU to read it.
Also, it controls the video memory address multiplexer MSB, to GTR = 1, so address bus is selected.

SLD – Serializer Load, controls loading data from the video memory bus into the pixel shift registers

SM – Serial Mode (?) – loads color attributes in shift registers used as 2x4bit D registers

S0 – Select Zero (not SO which is Serial OUT)
controls the video memory address multiplexer LSB
performs the switching between ROW and COLUMN
address for video dram

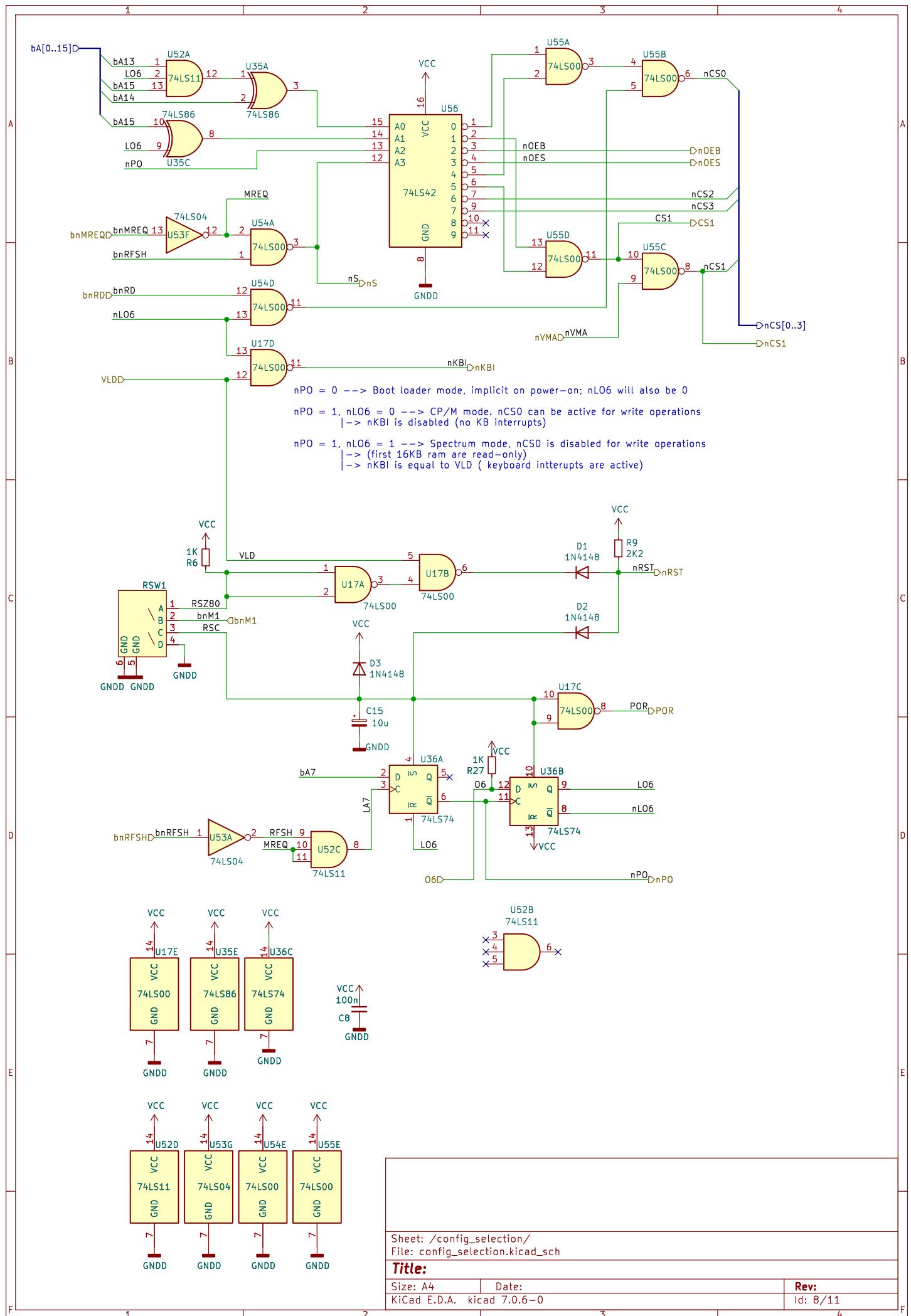
VNRS – Video Not RAS is the RAS signal for the video memory DRAM

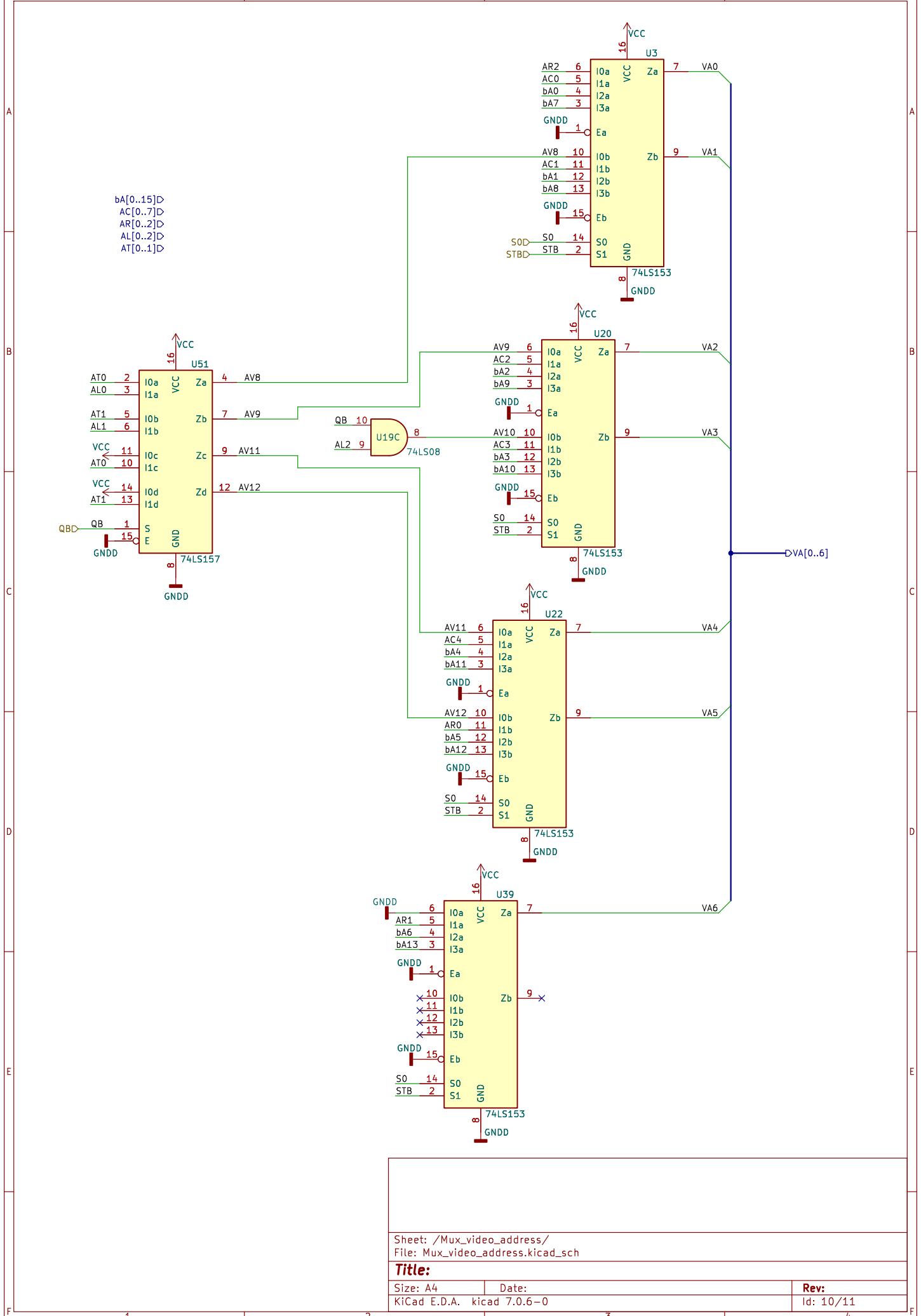


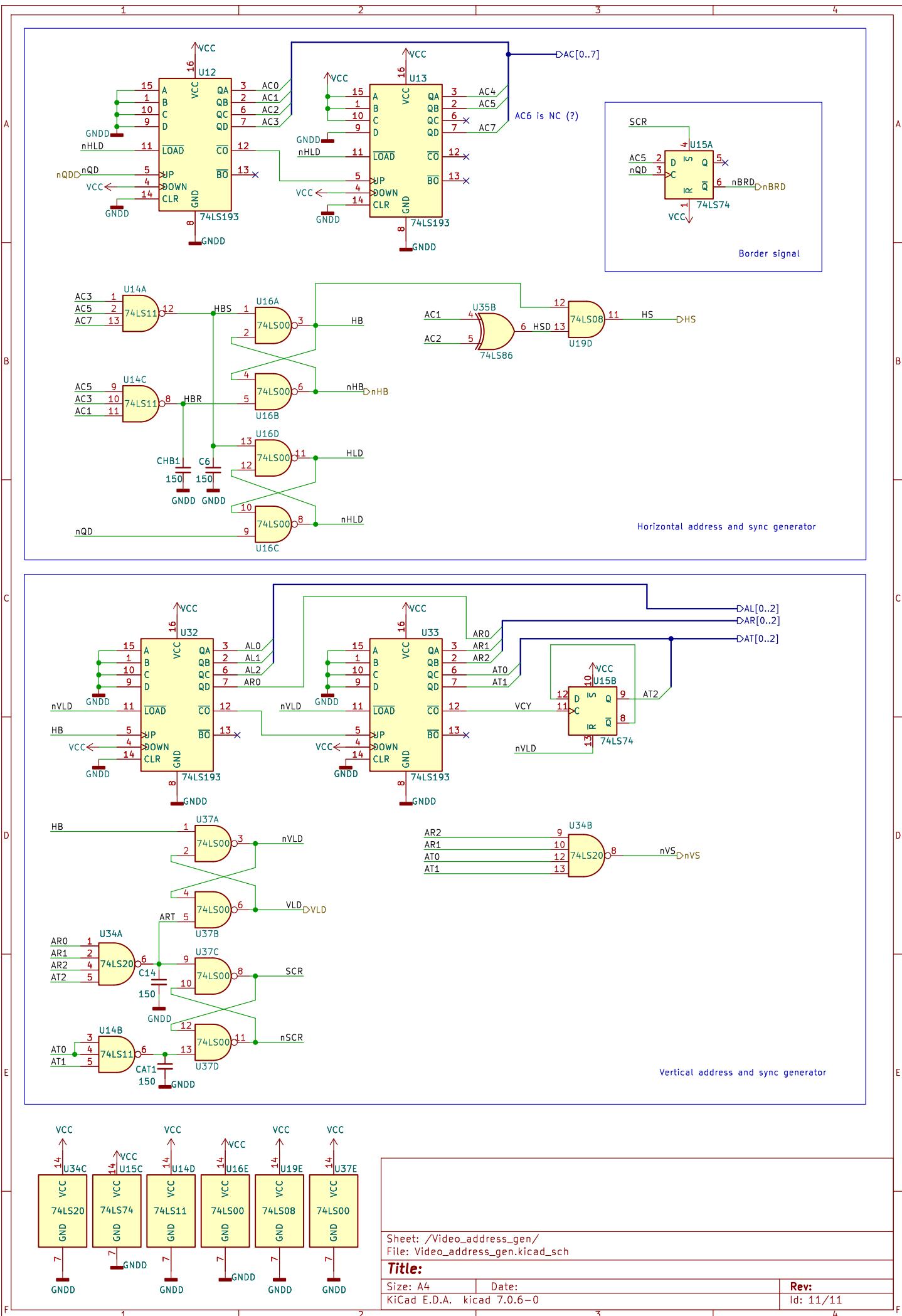
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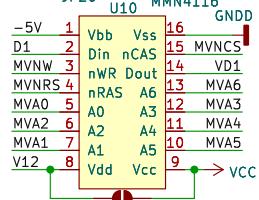
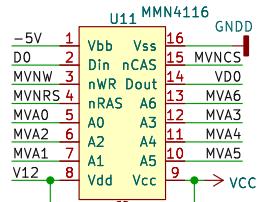
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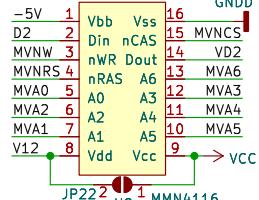




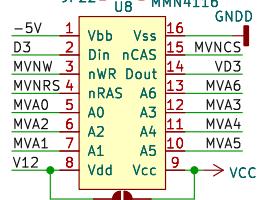
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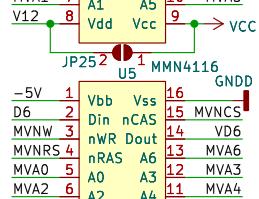
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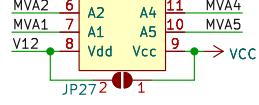
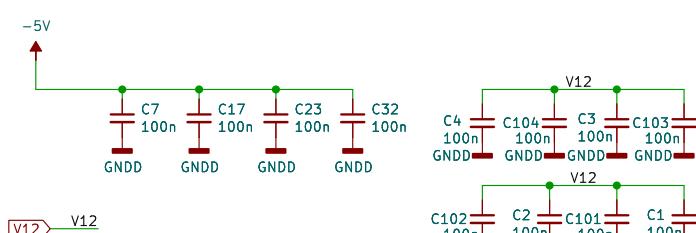
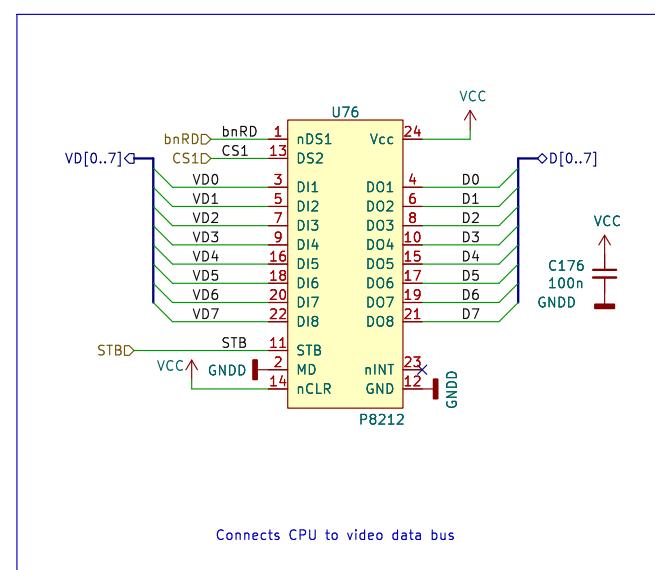
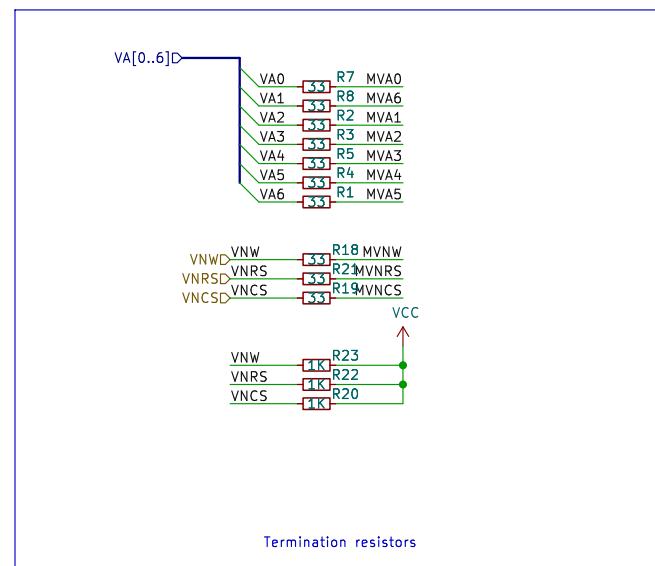
C



D



E

DRAM Bank 1
Video memory

Sheet: /Video_memory/
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